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A High Performance Operational Amplifier Using Coplanar Dual Gate a-IGZO TFTs

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ABSTRACT We fabricate an operational amplifier (op-amp) composed with the coplanar amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs). The circuit consisted of 19-TFTs and designed on a glass substrate in both dual gate (DG) and single gate (SG) structure for performance evaluation. Having the yield of a total voltage gain (A_v) of 23.5 dB, a cutoff frequency (f_c) of 500 kHz, a unit gain frequency (f_{ug}) of 2.37 MHz, gain-bandwidth product (GBWP) of 7500 kHz, a slew rate (up/down) of (2.1/1.2) V/μs, and a phase margin (PM) of 102° at a supply voltage of ±10 V, the fabricated DG TFT op-amp demonstrates good performance among all a-IGZO-based literature.

INDEX TERMS Coplanar *a*-IGZO TFTs, dual gate, single gate, operational amplifier (op-amp).

I. INTRODUCTION

Amorphous–indium-gallium-zinc-oxide (a-IGZO) TFTs and related circuits are becoming a potential player in the vast analog and digital electronics industry. Not only limited its applications to active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light emitting diode (AMOLED) displays or numerous digital circuits but also diverse analog circuits [l]. Compared to low-temperature poly-Si (LTPS) TFTs, many advantages such as high device performance, room temperature process, and low production cost is guaranteed [2]–[5]. The self-aligned coplanar a-IGZO process shows it's suitability for high speed, high frequency, and high gain operations [7]–[9].

Since op-amp was first conceived to use in analog computers, still dominates the single most important integrated circuit (IC) element for analog design. Zysset *et al.* [10] reported a 16-TFT op-amp in the flexible substrate with the A_v of 18.7 dB and f_c of 108 kHz. Cantarella *et al.* [11] reported another 13-TFT op-amp in the flexible substrate with the A_v of 19.4 dB and f_c of 6.9 kHz. Recently, Kim *et al.* [12] demonstrated a solution processed op-amp on the glass substrate with 19-TFTs and using direct light pattering (DLP) method with the A_v of 24.6 dB and f_c of 0.47 kHz. Although some other reports using a-Si [13] and poly-Si [14] shows a higher gain but lacks in very limited f_c and lower slew rate. a-IGZO TFT op-amp reports are handful [6], [10]–[12], [15] in comparing to CMOS counterpart. Hopefully, a-IGZO technology is continuously spreading its footprints in the analog domain like different amplifiers [l] (common source, transimpedance, differential, cascode, operational, and Cherry–Hooper), X-ray readout circuits, and antenna channel select circuits. In more complex circuit and technologies like [16] Internet of Things (IoT) sensor node, radio-frequency identification (RFID), near field communication (NFC) tag and hybrid combination with Si CMOS, signal processing and operation are part and parcel. Therefore, the op-amp research considers wider scopes and still in high demand for a-IGZO based electronics.

In this study, we fabricate the op-amp using coplanar SG and DG TFTs while all other reports [10]–[13], [15] used SG inverted staggered structure. The DG structure is emphasized as it is boasted bulk accumulation, higher drain current [17], performance improvement under negative bias illumination stress (NBIS) [18], [19], which further enhances circuit speed

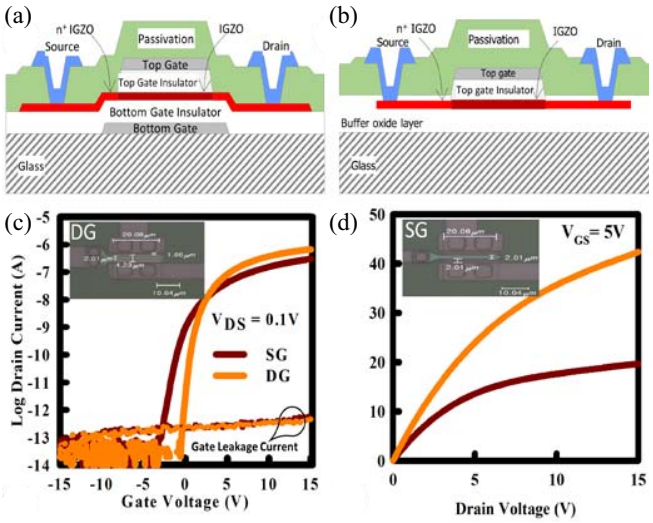

FIGURE 1. TFT schematics for dual gate (a), and single gate (b) structure . DG TFT shows superiority by the transfer (c), and output curve (d) over the SG TFT. In (d) the drain current of DG TFT is almost 2.5 times higher in comparison with the SG TFT. Inset shows the optical image of the fabricated (W/L=20 μm /2 μm) TFT of both structures.

in inverters [20], and ring oscillator [21]. By considering all of these advantages [22], it is expected that the op-amp with DG TFTs will outclass the SG one. The 2-μm a-IGZO process is applied to all TFTs. The op-amp stable linear gain response starts from 100 kHz, and it achieves an A_v of 23.5 dB, an f_c of 500 kHz, a f_{ug} of 2.37 MHz. With a broad bandwidth (BW) of 400 kHz, in contrast with other previous reports [10]–[15], the fabricated DG TFT op-amp poses the potentiality to use in low frequency (LF) band. The LF band frequency ranges from (30-300) kHz which is applicable for RFID, navigation, time signals, AM longwave broadcast and amateur radios [23].

From here, the whole article can be subdivided into broad three sections. At first, in the experiment section, details of the coplanar TFT fabrication process (A), and how the op-amp circuit designed (B) was discussed. Then, the performance was analyzed in the results and discussion section. Finally, this fabricated op-amp is studied with state-of-the-art technologies in TABLE 2.

II. EXPERIMENT

A. COPLANAR TFT FABRICATION

The schematic cross-sectional view of the DG and SG TFTs investigated in this work is depicted in Fig. 1(a), and 1(b) respectively. At first, Mo is deposited by sputtering on the glass substrate and patterned to form the bottom gate (BG). A 250-nm thick SiOx is deposited through plasma- enhanced chemical vapor deposition (PECVD) at 350 °C as the BG-insulator (BGI). Then, a 20-nm-thick *a*-IGZO layer was deposited by dc sputtering at a substrate temperature of 200 °C using a polycrystalline IGZO target ($In_2O_3 : Ga_2O_3 : Z_nO = 1 : 1 : 1$ mol %). The a-IGZO layer

TABLE 1. Geometry of the TFTS used for the op-amp.

TFT	W/L[μm]	TFT	W/L[μm]	TFT	W/L[μm]
T1	20/2	T8	20/2	T14	20/2
T2	20/2	T9	1200/2	T15	1000/2
T3	20/2	T10	1200/2	T16	40/2
T4	1200/2	T11	1200/2	T17	1200/2
T5	20/2	T12	20/2	T18	200/2
T6	200/2	T13	200/2	T19	40/2
T7	20/2				

was patterned by conventional photolithography. A 200-nm-thick SiO_X was deposited on the top of the *a*-IGZO by PECVD as a top gate insulator (TGI) without breaking the vacuum. The deposition temperature (200 °C) of TGI is not same as that (350 °C) of BGI. As deposition temperature is different, gate insulator thickness asymmetry can be possible to achieve the optimized performance. We have optimized thickness as $t_{BGI} = 250$ nm and $t_{TGI} = 200$ nm for the DG coplanar process. During the optimization process, TGI thickness was varied from 100 nm, 150 nm, 200 nm, 250nm, to 300 nm. The best results for TFT performance was obtained at 200 nm. The GI thickness asymmetry (here in this case 50 nm) is not surprising and multiple reports having asymmetric GI thickness of the DG structured BCE TFTs [17], [21], [22], [27], [29], and coplanar TFTs [30] are reported.

A 120-nm Mo was then deposited by sputtering and patterned as the top gate electrode. GI layer was etched by a self-aligned process with the gate pattern. Then, F plasma treatment was performed up to 100 s at room temperature with a flow rate, pressure, and RF power of 25 sccm, 48 mTorr and 250 W, respectively. A 400-nm-thick SiO_X layer was deposited as the interlayer (IL) by PECVD followed by the formation of via holes, and a 200-nm-thick Mo layer was deposited and patterned for the S/D electrodes.

Finally, the devices were annealed at 300 °C in vacuum for 1 h. In the DG TFT, the BG is connected to the TG through via holes. The TG does not overlap the source/drain (S/D) electrodes [Fig. 1(a)], as this would introduce additional parasitic capacitance, which impedes to circuit speed. To ensure this, 2 μm offsets are allowed between the TG and S/D electrodes. The fabrication of SG coplanar TFT is similar and just without forming the BG electrode. The detailed process of SG coplanar TFT fabrication appears in elsewhere [8].

B. DESIGNING THE OP-AMP CIRCUIT

Fig. 2(a) shows the schematic of the proposed op-amp constitutes with a total of 19 coplanar TFTs. All TFTs width varies from the lowest 20 μm to highest 1200 μm, and a channel length of all 19 TFTs is 2 μm. TABLE 1 enlists the geometry of all TFTs. Fig. 2(b) shows the layout design of the circuits.

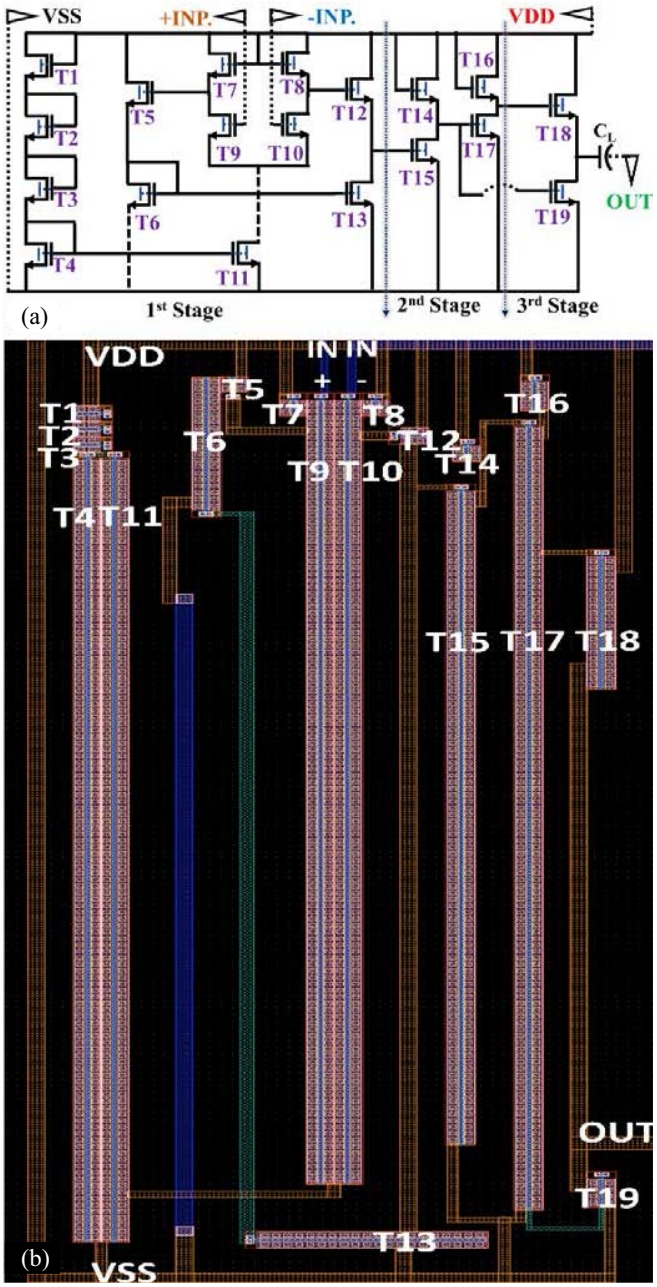

FIGURE 2. **(a) The op-amp circuit schematic, which can be subdivided in three stage. The 1st stage comprises of input terminal, current mirror and single ended converter stage. The 2nd stage ensures proper amplification and 3rd stage works as output buffer. In (b) layout has been added to depict the respective TFT position in the proposed circuit. The contact points like VDD, VSS, OUT and differential inputs (IN+ and IN-) are also marked.**

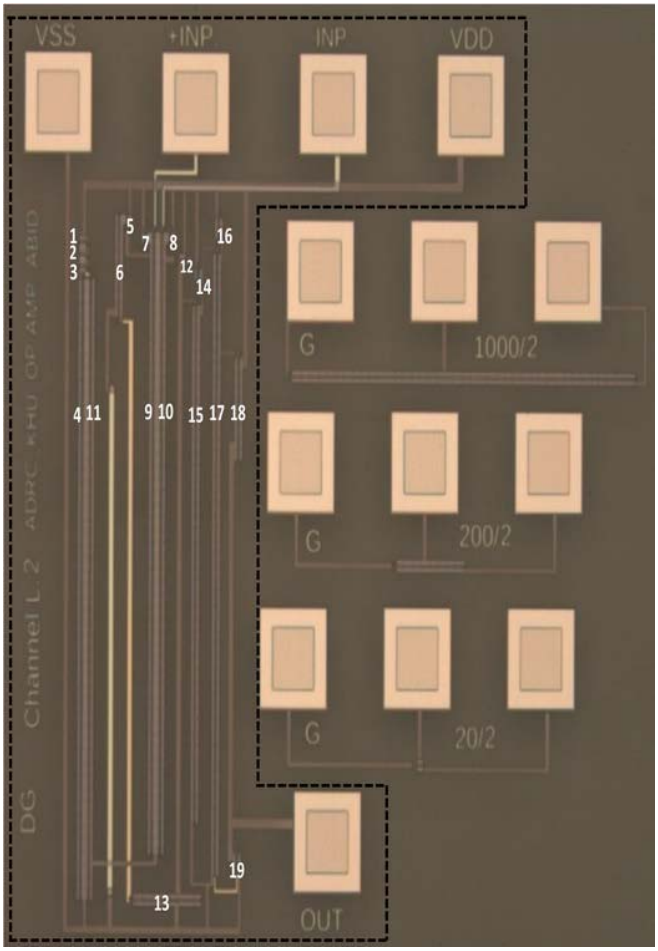

FIGURE 3. **(a) The optical image of the fabricated op-amp (in black dotted delineated region). TFT positions are marked with white colored numbers ranging from 1 to 19 corresponding to T1 to T19 TFT listed in Table 1. By comparing geometrical values listed in Table 1 with the optical image, it is expected that a reader gets a clear insight of this fabricated op-amp circuit.**

Like many other reports [10]–[12], [15], [24], [25], it can be broadly divided into three stages: the 1st stage comprises of the input terminal, a current mirror, and single-ended converter stage.

The 2nd stage ensures proper amplification and 3rd stage works as an output buffer. The op-amp circuit might look similar as with the recent report [12]. Although the total no. of 19 TFTs is same as like in [12], we have used more diode-connected TFT in the input stage current mirror path (T1-T3), and unlike cascaded output buffer we used single stage output buffer in the 3rd stage. Moreover, only this report constitutes with coplanar DG TFT structure, and rigorous 2-μm a-IGZO process for the whole circuit ensures the novelty of this proposed op-amp circuit.

Most of the TFTs (13 among 19), i.e., about 69% are utilized in the 1st stage. Gate of T9 and T10 acts as the input differential signal receiver point while T7-T10 with the tail bias current of T11 makes the differential amplifier part [10]. This stage is crucial, as it is responsible for accepting an input differential signal and subsequently amplifying it with the stable tail current (T11) using a current mirror. Finally, it delivers the signal to the single ended conversion node (between T12 and T13) to propagate through the 2nd stage.

The 2nd stage consists of 4 TFTs (T14-T17) which is basically a cascaded common source amplifier [12], [15]. Large amplification being ensured in this part. As the gain parameter (ß) is responsible for desired boosting, we have

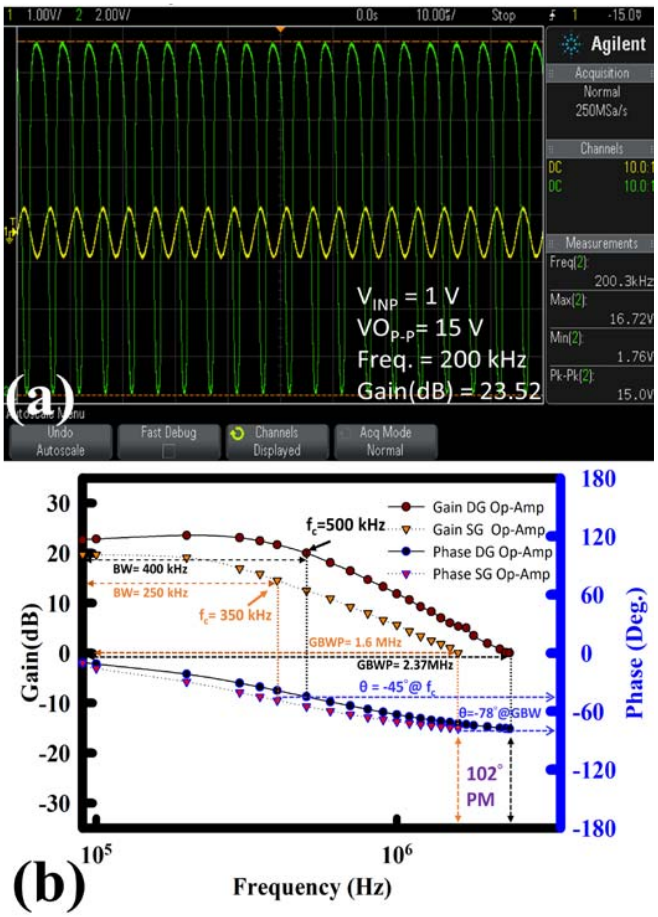

FIGURE 4. (a) Shows the measured input and output waveform for the frequency of 200 kHz . Gain and phase response with frequency is plotted in (b). Cutoff (f_c) and unit gain frequency (f_{ug}) of DG TFT op-amp are 500 kHz, 2.37 MHz while for SG that counts 350 kHz and 1.6 MHz respectively. It is clear that DG TFT op amp is almost 1.5 times broader in the aspect of f_c and f_{ug}. Phase response is similar for the both types with a phase margin (PM) of 102°. Bode plots shows the distinguishable superiority of DG TFT op amp over the SG TFT op-amp.

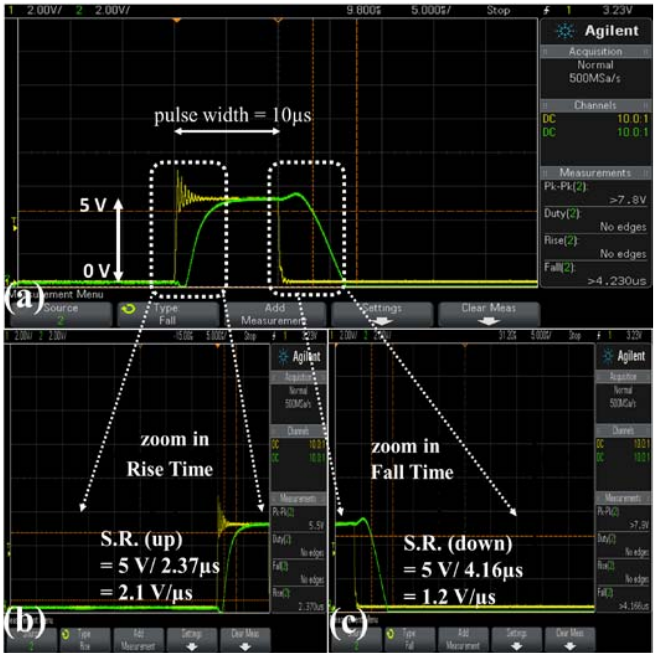

FIGURE 5. (a) The measured step response output data. Yellow line represents input and green line represents the output. The "zoom in" from both sides of the output response shows the op amp up and down slew rate in (b) and (c) respectively.

chosen a larger width TFT. ßratio between (T14-T15) is 50 and (T16-T17) is 30. Therefore, the ideal theoretical gain is 7.07 and 5.48 respectively, which has been calculated from the square root of the respective ßratio [8].

And finally, the 3rd portion is a single stage buffer, which ensures proper transferring of the output signal to the desired load. We have selected the geometry of the 3rd stage TFTs (T18-T19) to obtain a stable output. But TFT ßratio falls to a low value of 5 which eventually leads to a lower transconductance. Since the overall gain is mainly contributed by the input stage [13], the aspect ratios of the final stage output TFTs should not be affected much. The theoretical gain (square root of beta ratio) of the output stage TFTs (T18, T19) is quite similar with [10], [15] and measured performance is better than [12], and [14] in the aspect of f_c, f_{ug}, GBWP, and PM. This is a priority for achieving a stable output [12], [15]. We have checked the feasibility of this op-amp circuit through SMART SPICE software (SILVACO Inc.). For simulation, we have used Rensselaer Polytechnic Institute Amorphous Silicon TFT's Model (RPI a-Si Model, Level 35). Validity of the model was verified through fitting the TFT and simulated result of the op-amp performance.

III. RESULTS AND DISCUSSION

In Fig. 1(c) and (d), the measured transfer and output curve (TFT W/L = 20 µm /2 µm) has been plotted and compared for both types. For a gate to source voltage (V_{GS}) of 5V the drain current of DG TFT is almost 2.5 times higher in comparison with the SG TFT. The transfer curve of the DG TFT is more stable than that of the SG TFT as in Fig. 1(c). No depletion for the former type whereas clear depletion property for the latter type. Comparing with SG TFT, improved transfer and higher output is a well-established phenomenon for the DG TFT [17]-[22], [26], [27]. The threshold voltage (V_{th}), maximum field-effect mobility (μ_{fe-Max}), and subthreshold swing (SS) for DG and SG TFT by measurement is 0.1 V, −1.8 V, 18.4 cm^2/V.s, 13.52 cm^2/V.s, 0.35 V/dec., and 0.85 V/dec. respectively.

With the circuit diagram in Fig. 2(a) and layout design in Fig. 2(b), TFT position and dimension can be fully understood. Fig. 3. (a) shows the optical image of the fabricated op-amp (in the black dotted delineated region). TFT positions are marked with white colored numbers ranging from 1 to 19 corresponding to T1 to T19 TFT listed in TABLE 1. By comparing geometrical values listed in TABLE 1 with the optical image in Fig. 3(a), a reader can get a clear insight into this fabricated op-amp circuit.

TABLE 2. Literature review with previous works and different technologies.

Parameter	This Work		[12]	[11]	[15]	[10]	[13]	[14]
Year	2019		2018	2016	2015	2013	2010	1994
TFT	a-IGZO		a-IGZO	a-IGZO	a-IGZO	a-IGZO	a-Si	poly-Si
Process	Vacuum		Solution	Vacuum	Vacuum	Vacuum	Vacuum	Vacuum
Substrate	Glass		Glass	Flexible	Glass	Flexible	Glass	Glass
Topology	NMOS diode		NMOS diode	Pseudo CMOS	NMOS diode	NMOS diode	Positive Feedback	CMOS
Supply Voltage [V]	±10		15	-	±15	5	25	20
TFT/Capacitor	19/0		19/0	13/0	18/0	16/0	14/0	10/3
TFT Structure	Coplanar		Inverted Staggered/ SG	Inverted Staggered/ SG	Inverted Staggered/ SG	Inverted Staggered/ SG	BCE/ SG	Coplanar/ SG
Channel Length Variability/ Minimum (μm)	DG Fixed/2	SG Fixed/2	(50-250)/ 50	Fixed/ 12	(10-60)/ 10	(6-90)/ 6	Fixed/ 8	Fixed/ 15
A_v (dB)	23.52	19.6	24.6	19.4	24.5	18.7	42.5	56
f_c (kHz)	500	350	0.47	6.8	6	108	2	10
f_{ug} (kHz)	2370	1600	2	-	32	472	30	300
GBWP (kHz)	7500	3342	8*	37.8	100*	930*	266*	6309*
PM (Deg.)	102	102	-	-	-	-	80	-
Slew Rate (Up/down) [v/μs]	2.1 /1.2	4.8 /1	0.005 /0.007	-	-	0.88 /1.1	0.004 /0.005	-
Power Consumption [mW]	51		-	-	-	0.9	3.55	-
Chip Area [mm x mm]	0.5 x 1.4		4.0 x 2.6	7.8 x 7.8	1.35 x 0.95	2.6 x 0.8	3.4 x 1.5	-

'*' indicates calculated data from the article and '-' means data not provided

We applied sinusoidal differential input of 1 V_{pp} (peak to peak) generated by a signal generator (Segye SG-1355) to the '+INP' contact. '−INP' contact point is put as grounded as like in [15]. To bias the opamp, ± 10 V were applied to 'VDD' and 'VSS' terminal respectively. The output signal obtained from the 'OUT' pad by using an oscilloscope (Agilent 2012A). The load capacitance (C_L) in Fig. 2(a) represents the oscilloscope load cap of 12 pF.

In Fig. 4. gain and phase response of the fabricated op-amp with frequency is plotted. The good linear response starts from 100 kHz with 23.52 dB gain and at 500 kHz where dB (gain) falls to −3 dB is marked as the cutoff. It ensures a bandwidth (BW) of 400 kHz. For single gate TFT op-amp we get f_c at 350 kHz, so a lesser width BW of 250 kHz. As we advance with frequency, the gain falls drastically, and we mark the unit gain frequency at 2.37 MHz. The power consumption is 51 mW (estimated by SPICE). Another figure of merit for an amplifier is its gain-bandwidth product (GBWP). GBWP has been calculated by multiplying gain, A_v(v/v) with BW [28]. In this case, it accounts as 7500 kHz for DG, and 3342 kHz for SG op-amp. For SG TFT op-amp f_{ug} is 1.6 MHz. It is clear that DG TFT op-amp is almost 1.5 times broader in the aspect of f_c, and f_{ug} than the SG counterpart. The phase response is similar for both types with a phase margin (PM) of 102°. Bode plots show the distinguishable superiority of DG TFT op-amp over the SG counterpart.

Slew rate indicates how fast an op-amp output can follow with the input. To test this, the op-amp connected as a unit gain buffer. Fig. 5(a) represents the measured step response output data. Zoom in data for slew up and down rate are presented in Fig. 5(b) and (c) respectively. The yellow line represents input, and the green line represents the output. 5 V input step voltage is applied with a pulse width of 10 μs. Measured up and down slew rate is 2.1 V/μs and 1.2 V/μs.

TABLE 2 provides a literature review with previous works and different technologies. Gain is comparable to the other a-IGZO reports [12], [15] and higher than [10], [11] these. Even though having SG structured TFT, in [12], and [15] still shows better yield than this current report. We assume this is for using higher supply voltage of ± 15 V. Although a-Si [13] and poly-Si [14] op-amp still show a higher gain, in the context of f_c, f_{ug}, GBWP, PM, and slew rate, this fabricated DG op-amp outperforms all. f_c is 5 times higher than the flexible a-IGZO based one [10] and 50 times than that of the glass-based poly-Si [14] reports. f_{ug} is also 5 times higher than the flexible a-IGZO based one [10] and 79 times of the a-Si [13] based one. GBWP is noticeably wider than all other reports. 102° PM is also supersedes 80° PM of the glass-based a-Si [13] one.

Among the a-IGZO op-amp, [10] provides very attractive and low power consumption because it uses a single supply voltage of 5V. While we use a dual supply voltage of ±10 V. Our TFT numbers is also higher (19 TFTs) comparing to this work [10] (16TFT). Largest TFT width used in [10] is 245 μm whereas in our case it is 1200 μm. Considering all of this, reported high power consumption (51 mW) of this work is justifiable. Having the smaller circuit area of 0.5 mm × 1.4 mm in comparing with all other refs. in TABLE 2 adds an extra advantage in this op-amp design.

IV. CONCLUSION

This paper presented a coplanar DG a-IGZO TFT based op-amp for the first time. Both DG and SG TFT structured op-amp has been fabricated. With a voltage gain (A_V) of 23.52 dB, a cutoff frequency (f_c) of 500 kHz, a unit gain frequency (f_{ug}) of 2.37 MHz and phase margin (PM) of 102°, the DG coplanar op-amp stands as the best performer among the concurrent a-IGZO technology. The 2-um a-IGZO process is the shortest channel length op-amp to the best of our knowledge. As the coplanar structure is promising for high-speed circuits [7], [8], this fabricated op-amp has the potential to keep pace with the ever -demanding faster operation. Thus it can be implemented to a-IGZO based analog electronic circuit applications.

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