A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers

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***Abstract*—In this paper, a new front end ac–dc bridgeless interleaved power factor correction topology is proposed for level II plug-in hybrid electric vehicle (PHEV) battery charging. The topology can achieve high efficiency, which is critical for minimizing the charger size, PHEV charging time and the amount and cost of electricity drawn from the utility. In addition, a detailed analytical model for this topology is presented, enabling the calculation of the converter power losses and efficiency. Experimental and simulation results are included for a prototype boost converter converting universal ac input voltage (85–265 V) to 400 V dc output at up to 3.4 kW load. The experimental results demonstrate a power factor greater than 0.99 from 750 W to 3.4 kW, THD less than 5% from half load to full load and a peak efficiency of 98.9% at 70 kHz switching frequency, 265 V input and 1.2 kW load.**

***Index Terms*—AC–DC power converters, boost converter, bridgeless power factor correction (PFC), interleaved PFC, plug-in hybrid electric vehicle (PHEV) charger.**

I. Introduction

A PLUG-IN hybrid electric vehicle (PHEV) is a hybrid vehicle with a storage system that can be recharged by connecting the vehicle plug to an external electric power source [1]. The most common charger power architecture includes an ac–dc converter with power factor correction (PFC) [2] followed by an isolated dc-dc converter with input and output EMI filters [3], as shown in Fig. 1. Selecting the optimal topology and evaluating power loss in the power semiconductors are important steps in the design and development of PHEV battery chargers. The front-end ac–dc converter is a key component of the charger system. Proper selection of this topology is essential to meet the regulatory requirements for input current harmonics [4]–[6], output voltage regulation and implementation of power factor correction [7].

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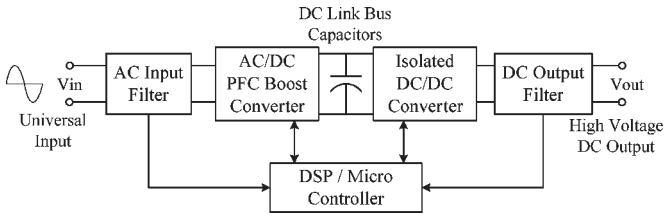

Fig. 1. Simplified system block diagram of a universal battery charger.

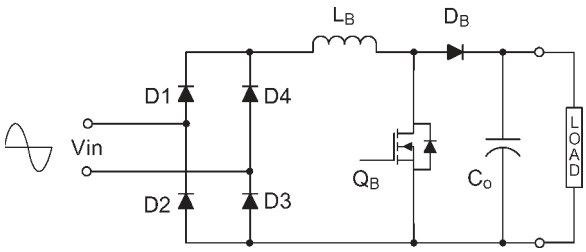

Fig. 2. Conventional PFC boost converter.

In Section II a review of common ac–dc PFC topologies is presented, targeting PHEV battery charging. The proposed novel bridgeless interleaved (BLIL) boost topology is presented in Section III. The circuit operation and steady-state analysis is provided in Section IV. Sections V and VI present the converter analytical and loss modeling. Experimental results are provided in Section VII and the conclusions are provided in Section VIII.

II. Review of Common AC–DC PFC Topologies

The conventional boost converter, bridgeless boost converter and interleaved boost converter are reviewed for application in front-end ac–dc conversion for PHEV battery charging in the following sub-sections.

A. Conventional Boost Converter

The conventional boost topology is the most popular topology for PFC applications. In PFC applications, a dedicated diode bridge is used to rectify the ac input voltage to dc, and this is followed by the boost converter, as shown in Fig. 2. With this topology, the output capacitor ripple current is very high [8] and is the difference between diode current and the dc output current. Furthermore, as the power level increases, the diode bridge losses significantly degrade the efficiency, so dealing with the heat dissipation in a limited area becomes problematic.

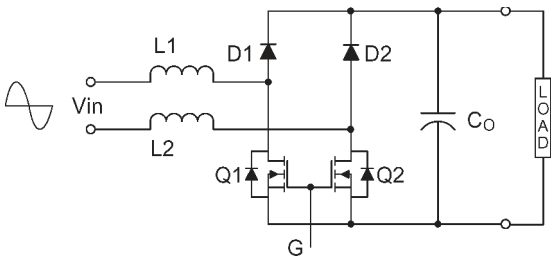

Fig. 3. Bridgeless PFC boost converter.

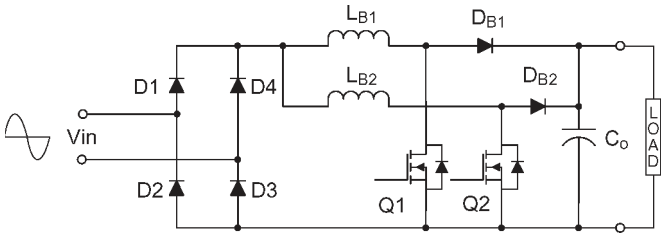

Fig. 4. Interleaved PFC boost converter.

Due to these constraints, this topology is good for a low to medium power range, up to approximately 1 kW. For power levels greater than 1 kW, typically, designers parallel semiconductors in order to deliver greater output power. The inductor volume also becomes a problematic design issue at high power because of the limited core size available for the power level and the heavy wire gauge required for winding.

B. Bridgeless Boost Converter

In comparison to the boost ac–dc PFC converter, the bridgeless boost PFC topology avoids the need for the rectifier input bridge, yet it maintains the classic boost topology [9]–[16], as shown in Fig. 3. It is an attractive solution for applications at power levels greater than 1 kW, where power density and efficiency especially critical. This topology solves the problem of heat management in the input rectifier diode bridge, but it introduces increased EMI [17], [18]. Another disadvantage of this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low frequency transformer or an optical coupler. Also, in order to sense the input current, complex circuitry is needed to sense the current in the MOSFET and diode paths separately, since the current path does not share the same ground during each half-line cycle [11], [19].

C. Interleaved Boost Converter

The interleaved boost converter, illustrated in Fig. 4, consists of two boost converters in parallel, operating 180° out of phase [20]–[22]. The input current is the sum of the two inductor currents in L_{B1} and L_{B2}. Interleaving yields several advantages. The ripple currents in these inductors are out of phase, so they tend to cancel each other out, and therefore reduce the high frequency input ripple current caused by the boost switching action, so the input EMI filter can be smaller [23]–[25].

Additionally, the topology also inherently has the advantage of parallelling semiconductors to reduce conduction losses.

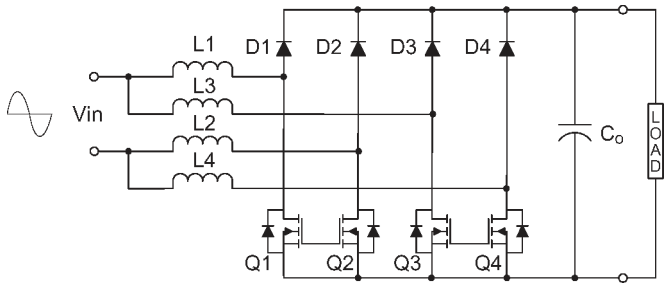

Fig. 5. Proposed BLIL PFC boost converter.

TABLE I
COMPARISON OF AC–DC PFC TOPOLOGIES FOR PHEV BATTERY CHARGING

Topology	Conventional PFC	Bridgeless PFC	Interleaved PFC	BLIL PFC
Power Rating	< 1000 W	< 2000 W	< 3000 W	**> 3000 W**
EMI / Noise	Fair	Poor	**Best**	Fair
Capacitor Ripple	High	High	**Low**	**Low**
Input Main Ripple	High	High	**Low**	**Low**
Magnetic Size	Large	Medium	**Small**	**Small**
Efficiency	Poor	Fair	Fair	**Best**
Cost	**Low**	Medium	Medium	High

Finally, interleaving also reduces output capacitor high frequency ripple. One significant drawback of the interleaved boost PFC converter is that similar to the boost PFC converter, it retains the problem of heat management in the input diode bridge.

In the following section, a new BLIL boost PFC converter is proposed. The proposed topology achieves high efficiency at power levels above 3 kW due to the elimination of the boost diode rectifier bridge and it features low EMI due to interleaving, which is an inherently attractive feature of the boost and interleaved boost PFC topologies.

III. PROPOSED BLIL BOOST TOPOLOGY

The BLIL PFC converter shown in Fig. 5 is proposed to address the problems discussed in Section II. This converter retains the same semiconductor device count as the interleaved boost PFC converter. In comparison, it requires two additional MOSFETs and two fast diodes in place of four slow diodes used in the input bridge of the interleaved boost PFC converter.

A detailed converter operation and steady-state analysis is given in the following section. Table I summarizes the advantages and disadvantages of the proposed topology and the three topologies reviewed in Section II.

IV. CIRCUIT OPERATION AND STEADY-STATE RIPPLE ANALYSIS

To analyze the circuit operation, the input line cycle has been separated into the positive and negative half cycles. Operation for each of the half-line cycles are explained in Sections IV-A

and B that follow. In addition, the detailed circuit operation depends on the duty cycle, therefore positive half cycle operation analysis is provided for $D > 0.5$ in Sections IV-C and $D < 0.5$ in Section IV-D.

A. Positive Half Cycle Operation

Referring to Fig. 5, during the positive half cycle, when the ac input voltage is positive, Q1/Q2 turn on and current flows through L1 and Q1 and continues through Q2 (and partially its body diode) and then L2, returning to the line while storing energy in L1 and L2. When Q1/Q2 turn off, energy stored in L1 and L2 is released as current flows through D1, through the load and returns through the body diode of Q2 back to the input mains.

With interleaving, the same mode happens for Q3/Q4, but with a 180° phase delay. The operation for this mode is Q3/Q4 on, storing energy in L3/L4 through the path L3-Q3-Q4-L4 back to the input. When Q3/Q4 turn off, energy is released through D3 to the load and returning through the body diode of Q4 back to the input mains.

B. Negative Half Cycle Operation

Referring to Fig. 5, during the negative half cycle, when the ac input voltage is negative, Q1/Q2 turn on and current flows through L2 and Q2 and continues through Q1 (and partially its body diode) and then L1, returning to the line while storing energy in L2 and L1. When Q1/Q2 turn off, energy stored in L2 and L1 is released as current flows through D2, through the load and returns through the body diode of Q1 back to the input mains.

With interleaving, the same mode happens for Q3/Q4, but with a 180° phase delay. The operation for this mode has Q3/Q4 on, storing energy in L3/L4 through the path L4-Q4-Q3-L3 back to the input.

C. Detailed Positive Half Cycle Operation and Analysis for $D > 0.5$

The detailed operation of the proposed BLIL PFC converter depends on the duty cycle. During any half cycle, the converter duty cycle is either greater than 0.5 (when the input voltage is smaller than half of output voltage) or less than 0.5 (when the input voltage is greater than half of output voltage).

Fig. 6 shows the three unique operating interval circuits of the proposed converter for duty cycles greater than 0.5 during positive half cycle operation. Waveforms of the proposed converter during these conditions are provided in Fig. 7.

Since the switching frequency of the proposed converter is much higher than the frequency of the input line voltage, input voltage v_i is considered constant during one switching period T_s. The input voltage is given by

$$v_{\text{in}}(\theta) = \sqrt{2} V_s \sin(\theta). \tag{1}$$

In a positive half cycle of the input voltage, the duty ratio of the proposed converter determines the following voltage

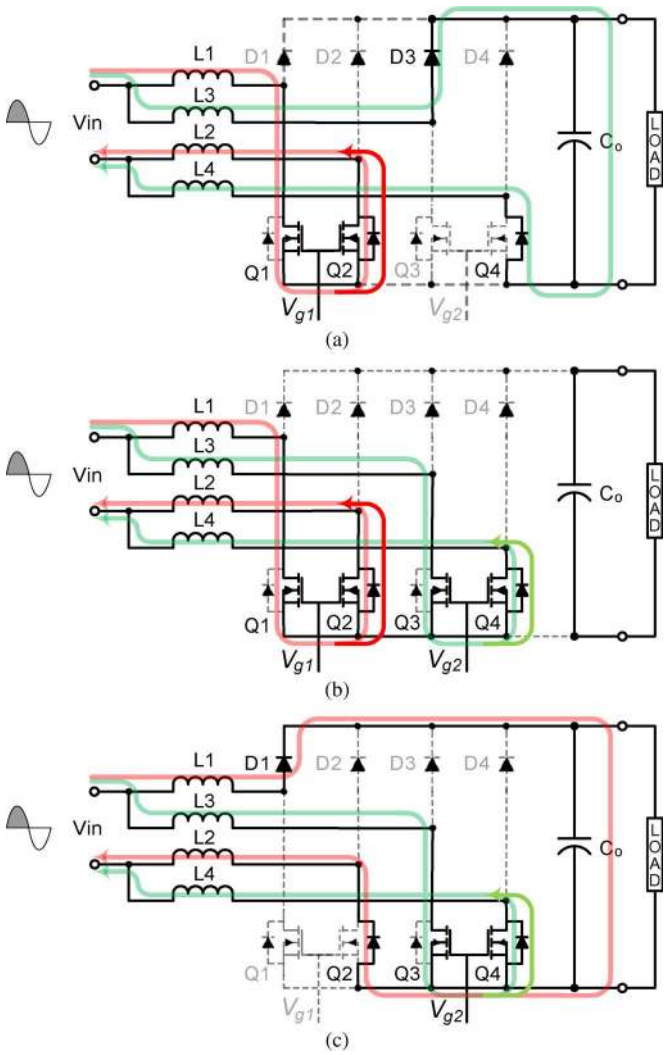

Fig. 6. (a) Interval 1: Q1 and Q2 are "ON," and body diode of Q4 conducting. (b) Interval 2 and 4: Q1, Q2, Q3, and Q4 are "ON." (c) Interval 3: Q3 and Q4 are "ON," and body diode of Q2 conducting.

relation:

$$\frac{V_o}{v_i} = \frac{1}{1-D}. \tag{2}$$

The intervals of operation are explained as follows. In addition, the ripple current components are derived, enabling calculation of the input ripple current, which provides design guidance to meet the required input current ripple standard.

Interval 1 $[t_0 - t_1]$*:* At t_0, Q1/ Q2 are ON, and Q3/Q4 are off, as shown in Fig. 6(a). During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The ripple currents in Q1 and Q2 are the same as the current in series inductances L1 and L2, where the ripple current is given by

$$\Delta i_{\text{L1}} = \frac{1}{L_1 + L_2} v_i (1-D) T_s. \tag{3}$$

The current in series inductances L3 and L4 decreases linearly and transfers the energy to the load through D3, C_o and body

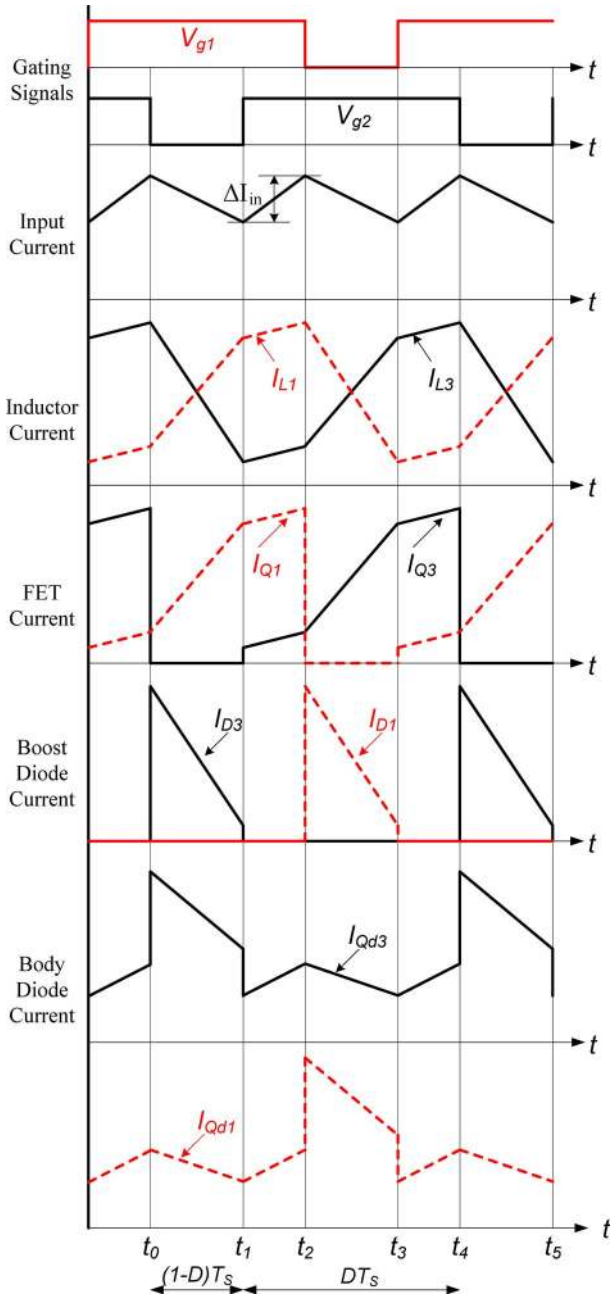

Fig. 7. BLIL PFC boost converter steady-state Waveforms at $D > 0.5$.

diode of Q4. The ripple current in series inductances L3 and L4 is given by

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4}(V_o - v_i)(1-D)T_s. \tag{4}$$

Assuming matched inductors, L1–L4, the input ripple current is the sum of currents in L1/L2 and L3/L4

$$\Delta I_{\mathrm{in}} = \frac{1}{L_1 + L_2} V_o (1-D)T_s. \tag{5}$$

In the steady-state, the input ripple current in intervals 2–4 is the same as interval 1.

Interval 2 $[t_1 - t_2]$*:* At t_1, Q3/Q4 are turned on, while Q1/Q2 remain on, as shown in Fig. 6(b). During this interval, the current in the four inductors each increase linearly, storing energy in these inductors. The ripple currents in Q1 and Q2 are the same as the ripple current in series inductances L1 and L2 as given by

$$\Delta i_{\mathrm{L1}} = \frac{1}{L_1 + L_2} v_i \left(D - \frac{1}{2}\right) T_s. \tag{6}$$

Similarly, the ripple currents in Q3 and Q4 are the same as the ripple current in series inductances L3 and L4

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4} v_i \left(D - \frac{1}{2}\right) T_s. \tag{7}$$

Interval 3 $[t_2 - t_3]$*:* At t_2, Q1/Q2 are turned off, while Q3/Q4 remain on, as shown in Fig. 6(c). During this interval, the current in series inductances L3 and L4 increases linearly and stores the energy in these inductors. The ripple currents in Q3 and Q4 are the same as the ripple current in series inductances L3 and L4

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4} v_i (1-D)T_s. \tag{8}$$

The current in L1 and L2 decreases linearly and transfers the energy to the load through D1, C_o, and body diode of Q2. The ripple current in series inductances L1 and L2 is given by

$$\Delta i_{\mathrm{L1}} = \frac{1}{L_1 + L_2}(V_o - v_i)(1-D)T_s. \tag{9}$$

Interval 4 $[t_3 - t_4]$*:* At t_3, Q3/Q4 remain on, while Q1/Q2 are turned on, as shown in Fig. 6(b). During this interval, the currents in the four inductors each increase linearly, storing energy in these inductors. The ripple currents in Q1 and Q2 are the same as the ripple currents in L1 and L2

$$\Delta i_{\mathrm{L1}} = \frac{1}{L_1 + L_2} v_i \left(D - \frac{1}{2}\right) T_s. \tag{10}$$

Similarly, the ripple currents Q3 and Q4 are the same as the ripple current in series inductances L3 and L4

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4} v_i \left(D - \frac{1}{2}\right) T_s. \tag{11}$$

D. Detailed Positive Half Cycle Operation and Analysis for $D < 0.5$

Fig. 8 shows the operating interval circuits of the proposed converter for duty cycles smaller than 0.5 during the positive half cycle. The waveforms of the proposed converter during these conditions are shown in Fig. 9. The intervals of operation are explained as follows.

Interval 1 $[t_0 - t_1]$*:* At t_0, Q1 and Q2 turn off, while Q3 and Q4 remain off, as shown in Fig. 8(a). During this interval, the current in series inductances L1 and L2 decreases linearly and transfers the energy to the load through D1, C_o, and body diode of Q2. The ripple current in series inductances L1 and L2 is

$$\Delta i_{\mathrm{L1}} = \frac{1}{L_1 + L_2}(V_o - v_i)\left(\frac{1}{2} - D\right) T_s. \tag{12}$$

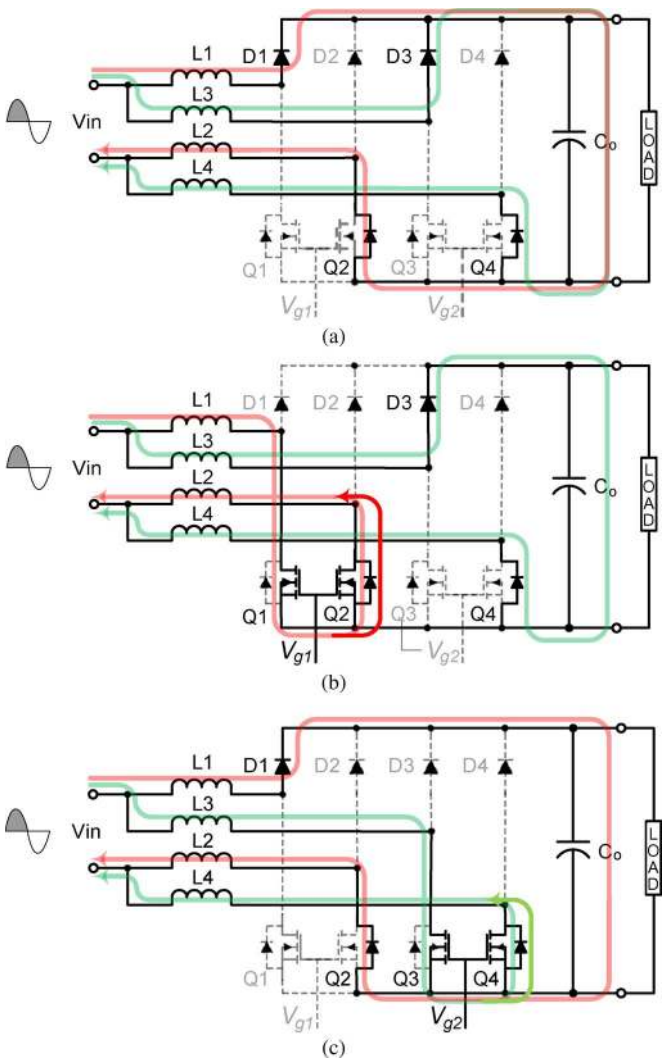

Fig. 8. (a) Interval 1 and 3: Body diodes of Q2 and Q4 conducting. (b) Interval 2: Q1 and Q2 are "ON," and body diode of Q4 conducting. (c) Interval 4: Q3 and Q4 are "ON," and body diode of Q2 conducting.

In addition, the current in the series inductances L3 and L4 also decreases linearly, transferring the energy to the load through D3, C_o, and body diode of Q4. The ripple current in series inductances L3 and L4 is

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4}(V_o - v_i)\left(\frac{1}{2} - D\right)T_s. \tag{13}$$

Interval 2 $[t_1 - t_2]$*:* At t_1, Q1/Q2 turn on, while Q3/Q4 remain off, as shown in Fig. 8(b). During this interval, the current in series inductances L1 and L2 increases linearly, storing energy in these inductors. The ripple currents in Q1 and Q2 are the same as the current in series inductances L1 and L2, where the ripple current is given by

$$\Delta i_{\mathrm{L1}} = \frac{1}{L_1 + L_2} v_i D T_s. \tag{14}$$

The current in series inductances L3 and L4 decreases linearly and transfers the energy to the load through D3, C_o, and body

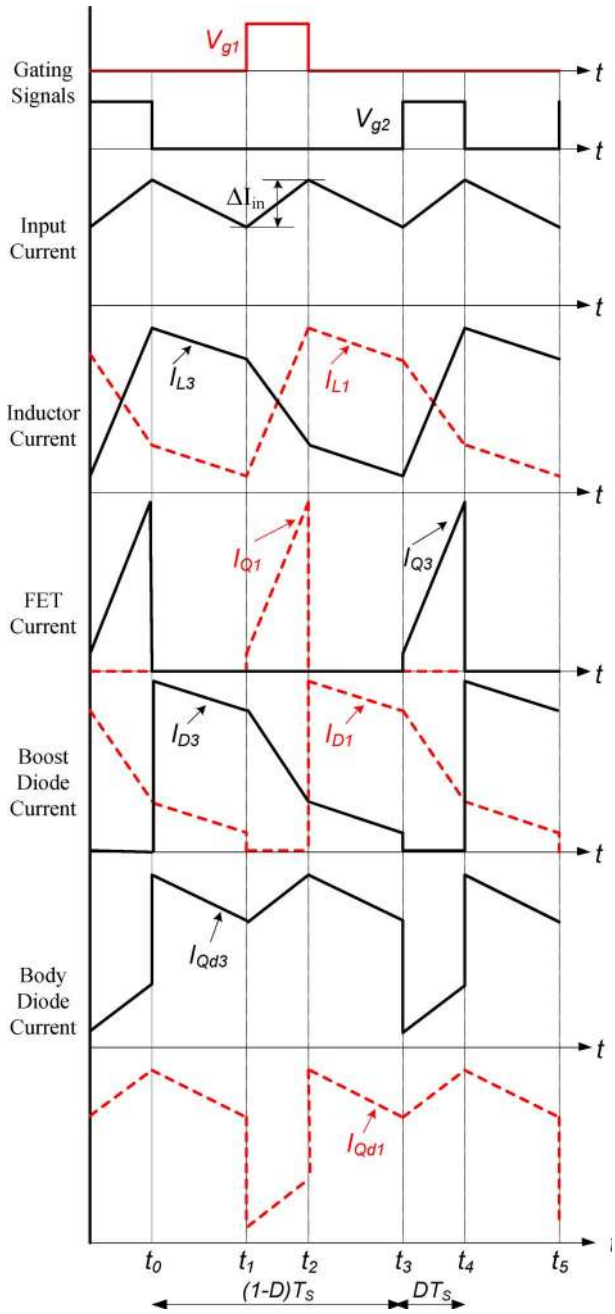

Fig. 9. BLIL PFC boost converter steady-state waveforms at $D < 0.5$.

diode of Q4. The ripple current in L3 and L4 is

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4}(V_o - v_i) D T_s. \tag{15}$$

Assuming matched inductors, L1–L4, the input ripple current is the sum of the currents in L1/L2 and L3/L4

$$\Delta I_{\mathrm{in}} = \frac{1}{L_1 + L_2} V_o D T_s. \tag{16}$$

In the steady-state, the input ripple current in intervals 1, 3, and 4 is the same as interval 2.

Interval 3 $[t_2 - t_3]$*:* At t_2, Q1/Q2 are turned off, while Q3/Q4 remain off, as shown in Fig. 8(a). During this interval, the current in series inductances L1 and L2 decreases linearly

and transfers the energy to the load through D1, C_o, and body diode of Q2. The ripple current in series inductances L1 and L2 is given by

$$\Delta i_{\mathrm{L1}} = \frac{1}{L_1 + L_2}(V_o - v_i)\left(\frac{1}{2} - D\right)T_s. \tag{17}$$

Similarly, the current in the series inductances L3 and L4 also decreases linearly, transferring the energy to the load through D3, C_o, and body diode of Q4. The ripple current in series inductances L3 and L4 is

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4}(V_o - v_i)\left(\frac{1}{2} - D\right)T_s. \tag{18}$$

Interval 4 $[t_3 - t_4]$*:* At t_3, Q3/Q4 are turned on, while Q1/Q2 remain off, as shown in Fig. 8(c). During this interval, the current in series inductances L3 and L4 increases linearly and stores the energy in these inductors. The ripple currents in Q3 and Q4 are the same as the current in series inductances L3 and L4, where the ripple current is given by

$$\Delta i_{\mathrm{L3}} = \frac{1}{L_3 + L_4}v_i D T_s. \tag{19}$$

The current in series inductances L1 and L2 decreases linearly and transfers the energy to the load through D2, C_o, and body diode of Q4. The ripple current in L1 and L2 is

$$\Delta i_{\mathrm{L1}} = \frac{1}{L_1 + L_2}(V_o - v_i)D T_s. \tag{20}$$

The operation of converter during the negative input voltage half cycle is similar to the operation of converter during the positive input voltage half cycle.

V. Analytical Modeling

In order to properly select the power stage components of a converter and calculate the associated power losses, it is necessary to perform a current stress analysis. To do so, analytical expressions are required; including RMS switch and inductor current stresses and average diode current stress. In a typical boost converter, the MOSFET and diode current waveforms are pulsed-width modulated, with both the duty cycle and peak amplitude varying with the ac input, so analytical modeling is challenging, and is most often performed using circuit simulation. However, without an effective mathematical method for determining these RMS and average values, the design and selection of power stage components can be flawed. Therefore, this sub-section proposes an analytical model that can be used for all boost derived PWM PFC regulators.

The following assumptions were made in order to analyze the converters and to derive the stress equations:

a) continuous conduction mode (CCM) operation is assumed;
b) unity power factor is assumed. i.e., the line current is in phase and shape with the input line voltage—a sinusoidal waveform;
c) the PFC output voltage is dc with no voltage ripple.

In a typical boost converter, the converter MOSFET duty cycle is given by

$$\delta_Q(\theta) = 1 - \frac{|V_{\mathrm{in}}(\theta)|}{V_o} = 1 - \frac{V_{\mathrm{PK}}\,|\sin(\theta)|}{V_o}. \tag{21}$$

Assuming the inductor current is a sinusoidal waveform

$$i_L(\theta) = I_{\mathrm{PK}}\,|\sin(\theta)|\,. \tag{22}$$

The converter MOSFET duty cycle RMS and its RMS current can be derived, respectively

$$\delta_{Q\text{-rms}} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(1 - \frac{V_{\mathrm{PK}}\,|\sin(\theta)|}{V_o}\right)^2 d\theta} \tag{23}$$

$$I_{Q\text{-rms}} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[I_{\mathrm{PK}}\,|\sin(\theta)|\,(\delta_{Q\text{-rms}})\right]^2 d\theta}. \tag{24}$$

The high frequency inductor current ripple is assumed to be half of peak inductor current in each channel for an interleaved boost converter

$$\Delta I_{\mathrm{RP}} = \frac{1}{2}\frac{I_{\mathrm{PK}}}{2}. \tag{25}$$

The high frequency ripple component of the inductor current is assumed to be a triangler waveform with a fixed duty cycle, so the RMS current in each inductor is defined by

$$I_{L\text{-rms}} = \sqrt{\left(\frac{1}{\sqrt{2}}\frac{I_{\mathrm{PK}}}{2}\right)^2 + \left(\frac{1}{2\sqrt{3}}\Delta I_{\mathrm{RP}}\right)^2} = \frac{5}{4\sqrt{3}}\frac{P_{\mathrm{in}}}{V_{\mathrm{PK}}}. \tag{26}$$

The boost diode duty cycle is given by

$$\delta_D(\theta) = 1 - \delta_Q(\theta) = \frac{V_{\mathrm{PK}}\,|\sin(\theta)|}{V_o}. \tag{27}$$

Therefore, the instantaneous boost diode current and its average current can be derived, respectively

$$I_D(\theta) = I_{\mathrm{PK}}\,|\sin(\theta)|\,\frac{V_{\mathrm{PK}}\,|\sin(\theta)|}{V_o} \tag{28}$$

$$I_{D\text{-ave}} = \frac{1}{\pi}\int_0^{\pi} I_{\mathrm{PK}}\,|\sin(\theta)|\left(\frac{V_{\mathrm{PK}}\,|\sin(\theta)|}{V_o}\right)d\theta. \tag{29}$$

The output capacitor current has high frequency and low frequency components. The low frequency component is simply given by

$$I_{C\text{-rms(LF)}} = \frac{I_o}{\sqrt{2}} = \frac{\sqrt{2}}{2}\frac{P_o}{V_o}. \tag{30}$$

And the high frequency RMS ripple current component is [20]

$$I_{C\text{-rms(HF)}} = \frac{P_{\mathrm{in}}}{V_o} = \sqrt{\frac{16V_o}{6\pi V_{\mathrm{PK}}} - \frac{P_o^2}{P_{\mathrm{in}}^2}}. \tag{31}$$

TABLE II
SUMMARY OF THE COMPONENT CURRENT STRESSES FOR THE CONVENTIONAL BOOST, BRIDGELESS, INTERLEAVED BOOST, AND BLIL PFC TOPOLOGIES

Topology	Conventional Boost PFC	Bridgeless PFC
Inductor RMS Current	$\sqrt{\frac{97}{48}}\frac{P_{in}}{V_{PK}}$	$\sqrt{\frac{97}{48}}\frac{P_{in}}{V_{PK}}$
Input Bridge Diode Average Current	$\frac{2}{\pi}\frac{P_{in}}{V_{PK}}$	Not Applicable
Fast Diode Average Current	$\frac{P_{in}}{V_o}$	$\frac{1}{2}\frac{P_{in}}{V_o}$
MOSFET RMS Current	$\frac{P_{in}}{\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$	$\frac{P_{in}}{\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$
MOSFET Intrinsic Body Diode Average Current	Not Applicable	$\frac{1}{2}\frac{P_{in}}{V_o}$
Output Capacitor RMS Ripple Current (Low Frequency)	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$
Output Capacitor RMS Ripple Current (High Frequency)	$\frac{\sqrt{2}}{2V_o}\sqrt{3P_{in}^2-2P_o^2}$	$\frac{\sqrt{2}}{2V_o}\sqrt{3P_{in}^2-2P_o^2}$

Topology	Interleaved Boost PFC	Bridgeless Interleaved PFC
Inductor RMS Current	$\frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}}$	$\frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}}$
Input Bridge Diode Average Current	$\frac{2}{\pi}\frac{P_{in}}{V_{PK}}$	Not Applicable
Fast Diode Average Current	$\frac{P_{in}}{2.V_o}$	$\frac{1}{4}\frac{P_{in}}{V_o}$
MOSFET RMS Current	$\frac{P_{in}}{2\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$	$\frac{P_{in}}{2\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$
MOSFET Intrinsic Body Diode Average Current	Not Applicable	$\frac{1}{4}\frac{P_{in}}{V_o}$
Output Capacitor RMS Ripple Current (Low Frequency)	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$
Output Capacitor RMS Ripple Current (High Frequency)	$\frac{P_{in}}{V_o}\sqrt{\frac{16}{6\pi}\frac{V_o}{V_{PK}}-\frac{P_o^2}{P_{in}^2}}$	$\frac{P_{in}}{V_o}\sqrt{\frac{16}{6\pi}\frac{V_o}{V_{PK}}-\frac{P_o^2}{P_{in}^2}}$

This analysis was used to derive the RMS and average currents in the proposed and reviewed topologies. Table II provides a summary of the component current stresses for the conventional boost converter, bridgeless boost converter, interleaved boost converter and a BLIL boost converter.

As can be noted, in both the bridgeless topology and BLIL topology, a new loss has been introduced in the intrinsic body diodes of the MOSFETs, but since input bridge rectifiers were eliminated, there is some efficiency gain for these topologies. In addition, the low frequency RMS ripple current through the output capacitors is constant—independent of interleaving. However, the high frequency ripple current is reduced significantly, as illustrated in Fig. 10. Finally, it is observed that for constant output power, as the input voltage increases, the high frequency ripple reduces.

VI. LOSS MODELING

A loss analysis was performed—in part using the equations presented in Section V. The loss distribution of the semiconductors is provided in Fig. 11 for the four topologies investigated. Results are presented for the following operating conditions: $V_{\text{in}} = 240$ V, $P_o = 3400$ W, $V_o = 400$ V, and $f_{sw} = 70$ kHz. The regular diode losses consist of only conduction losses in bridge rectifier diodes, i.e., reverse recovery losses were neglected. Due to the low reverse recovery characteristics of SiC diodes, these diodes were selected for the 70 kHz PFC circuits.

Therefore, high frequency reverse recovery losses were also neglected, so that only conduction losses were considered. Switching, conduction, gate charge and 1/2 CV^2 losses are included in the MOSFET total losses. The inductor loss analysis was neglected for this comparison.

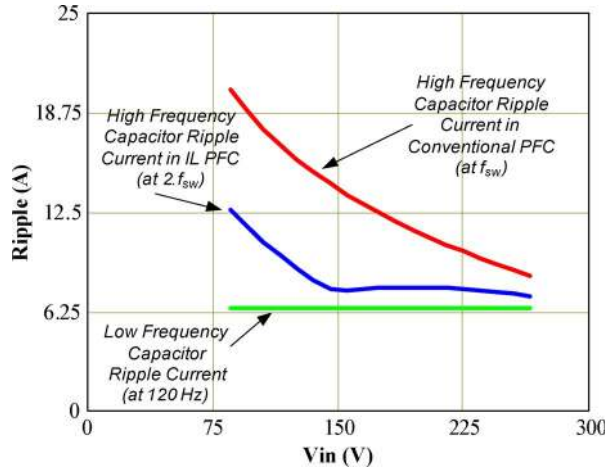

Fig. 10. RMS ripple current through output capacitors versus input voltage for BLIL converter; $V_o = 400$ V, $P_o = 3400$ W and $f_{sw} = 70$ kHz.

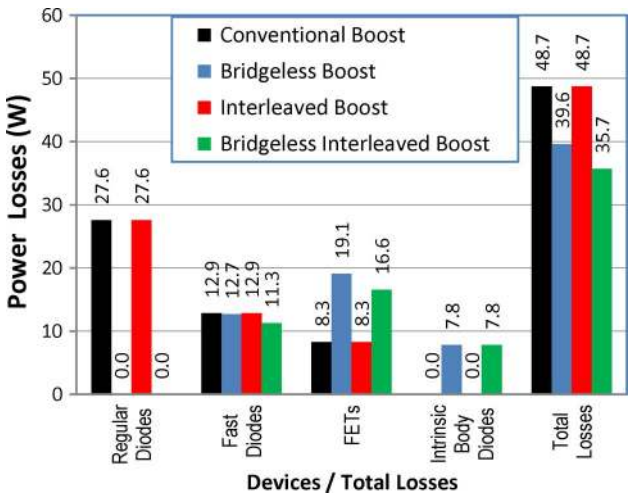

Fig. 11. Comparison of the loss distribution in the semiconductors at: $V_{\rm in} = 240$ V, $V_o = 400$ V, $P_o = 3.4$ kW and $f_{sw} = 70$ kHz.

The regular diodes in the input bridge rectifiers have the largest share of losses among the boost topologies, which require the input bridge rectifier. The bridgeless topologies eliminate this large loss component (27.6 W). However, the tradeoff is that the MOSFET losses are higher and the intrinsic body diodes of the MOSFETs conduct, producing new losses (7.85 W). The fast diodes in the BLIL PFC have slightly lower power losses, since the boost diode average current is lower in these topologies. Overall, the MOSFETs are under more stress in the bridgeless topologies, but most importantly, the total semiconductor losses for the proposed BLIL boost converter are 37% lower than the benchmark conventional boost, 10% lower than the bridgeless boost and 37% lower than the interleaved boost.

Since the bridge rectifier losses are so large in the boost topologies, and interleaving reduces MOSFET RMS current stress, it was expected that BLIL boost converter would have the lowest power losses among the four topologies studied. Also, it is noted that the losses in the input bridge rectifiers were 56% of total losses for both the conventional boost PFC converter and the interleaved boost PFC converter. Therefore, eliminating the input bridge in a PFC converter is justified, despite the fact that additional MOSFET losses are introduced.

Finally, it is noted that with interleaving, the core loss is also reduced since the core volume can be reduced by approximately 25%–30%. In addition, since the current in the inductors are reduced by the factor of two, both ac and dc winding copper losses will be reduced.

Fig. 12. Breadboard prototype of the BLIL PFC boost converter.

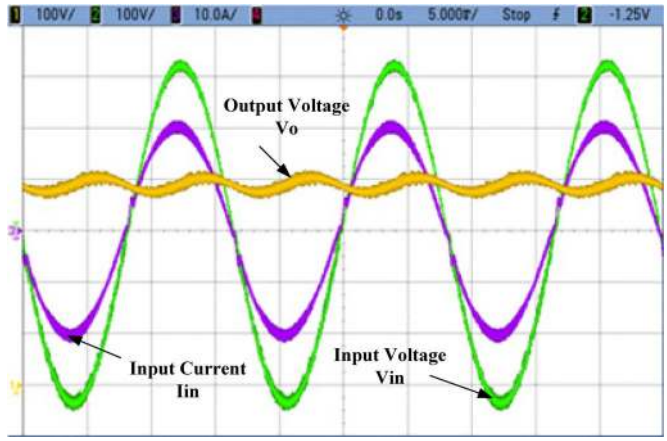

Fig. 13. Output voltage, input voltage and input current; Test condition: $P_o = 3.4$ kW, $V_{\rm in} = 240$ V, $I_{\rm in} = 15$ A. Ch1 $= V_o$ 100 V/div. Ch2 $= V_{\rm in}$ 100 V/div. Ch3 $= I_{\rm in}$ 10 A/div.

VII. Experimental Results

An experimental prototype was built to verify the operation of the proposed converter. A photo of the prototype is provided in Fig. 12.

Waveforms of the input voltage, input current and PFC bus voltage of the converter are provided in Fig. 13 for the following test conditions: $V_{\rm in} = 240$ V, $I_{\rm in} = 15$ A, $P_o = 3400$ W, $V_o = 400$ V, $f_{sw} = 70$ kHz. The input current is in phase with the input voltage, and its shape is nearly perfectly sinusoidal, as expected.

Waveforms of the MOSFET gating signal—$V_{\rm G1}$, sensed MOSFET current through the current transformer, $I_{\rm Q1}$, inductor current, $I_{\rm L1}$, and the boost diode current, $I_{\rm D1}$, are provided

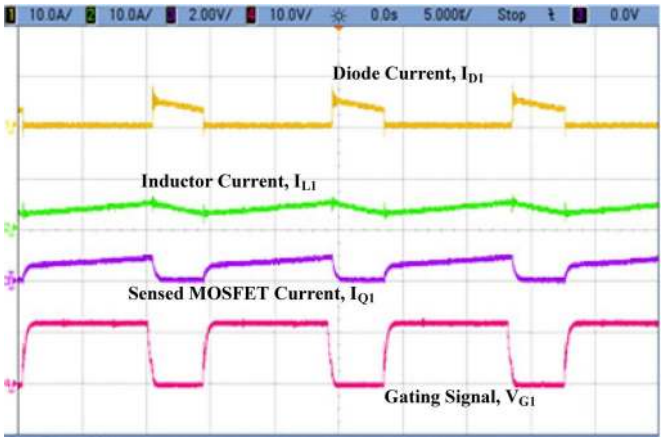

Fig. 14. Gating signal, inductor, diode, sensed MOSFET current for $D > 0.5$: Ch1 $= I_{\mathrm{D1}}$ 10 A/div. Ch2 $= I_{\mathrm{L1}}$ 10 A/div. Ch3 $= I_{\mathrm{Q1}}$ 2 V/div. Ch4 $= V_{\mathrm{G1}}$ 10 V/div.

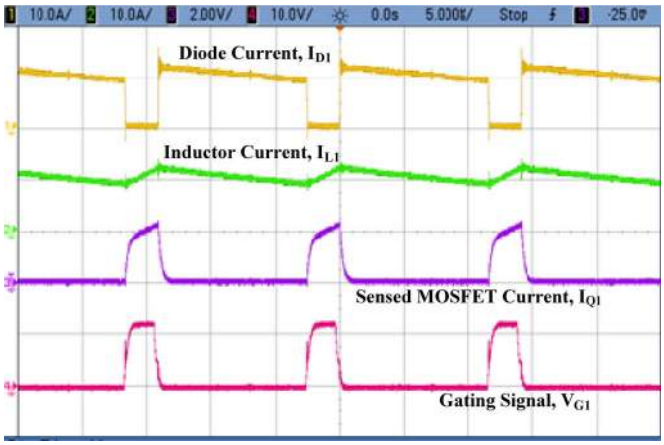

Fig. 15. Gating signal, inductor, diode, sensed MOSFET current for $D < 0.5$: Ch1 $= I_{\mathrm{D1}}$ 10 A/div. Ch2 $= I_{\mathrm{L1}}$ 10 A/div. Ch3 $= I_{\mathrm{Q1}}$ 2 V/div. Ch4 $= V_{\mathrm{G1}}$ 10 V/div.

in Fig. 14 for duty cycles greater than 0.5 and Fig. 15 for duty cycles less than 0.5. Waveforms of the input current, inductor currents in L1 and L3, and sensed MOSFET current are provided in Fig. 16. The input current ripple cancelation due to interleaving is clearly exhibited. Compared to the conventional Boost PFC converter (at equal power), the reduced ripple in the input current decreases the conducted-EMI noise and helps reduce the EMI filter size.

Component information is provided in Table III for the semiconductors and powertrain components of the proposed BLIL PFC converter.

In order to verify the quality of the input current in the proposed topology, its harmonics up to the 39th harmonic are given and compared with the EN 61000-3-2 standard in Fig. 17 for 120 V and 240 V input. All converter harmonics are well below IEC standard, which is required for PHEV chargers.

Curves of the input current total harmonic distortion are provided in Fig. 18 for full load at 120 V and 240 V input. It is noted that the input current THD is less than 5% from half load to full load.

Power factor is another useful parameter to show the quality of input current. The converter power factor is provided in Fig. 19 for the entire load range at 120 V and 240 V input. The power factor is greater than 0.99 from half load to full load.

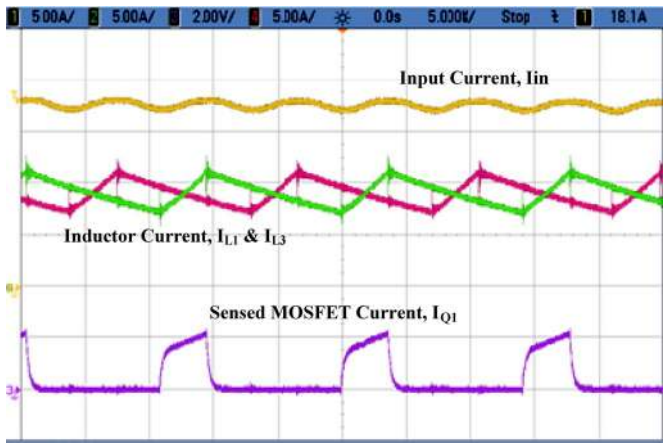

Fig. 16. Input current, boost inductors, sensed MOSFET current for $D < 0.5$: Ch1 $= I_{\mathrm{in}}$ 5 A/div. Ch2 $= I_{\mathrm{L1}}$ 5 A/div. Ch3 $= I_{\mathrm{Q1}}$ 2 V/div. Ch4 $= I_{\mathrm{L3}}$ 5 A/div.

TABLE III
KEY COMPONENTS USED FOR THE BLIL BOOST CONVERTER PROTOTYPE

Device	Part # / Value	# of devices	Unit Price $US
Fast Diode	CSD10060	4	2.30
MOSMOSFET	IPP60R099CP	4	3.15
Inductor	77071 core / 400 µH	4	1.530
Capacitor	EKXJ451ELL820 / 82 µF	10	0.58
SMD CT 1:100	B78302A7760A003	4	0.46
Controller	UCC28070	1	2.418
Driver	MIC4124	1	1.298

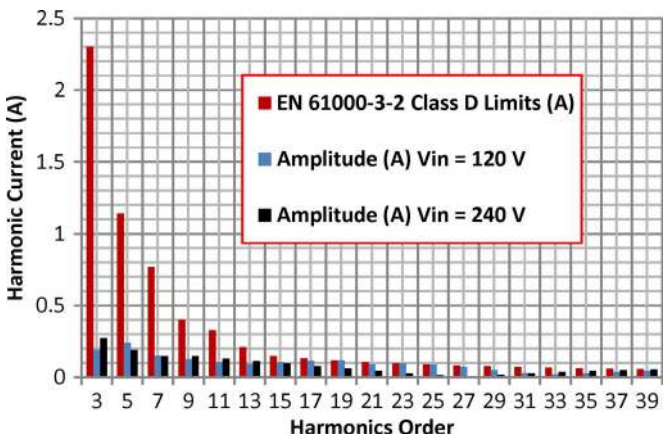

Fig. 17. BLIL Input current harmonics at $P_o = 1700$ W for $V_{\mathrm{in}} = 120$ V and at $P_o = 3400$ W for 240 V.

The measured efficiency of converter versus output power for different input voltages is provided in Fig. 20. With the proposed BLIL PFC converter a peak efficiency of 98.9% was reached at 265 V input and 1.2 kW output power. High efficiency over the entire load range is achieved with this

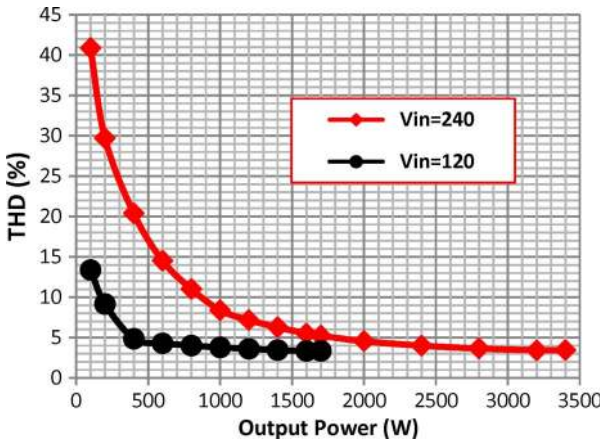

Fig. 18. Total harmonics distortion versus output power at: $P_o = 1.7$ kW for $V_{\rm in} = 120$ V and $P_o = 3.4$ kW for 240 V.

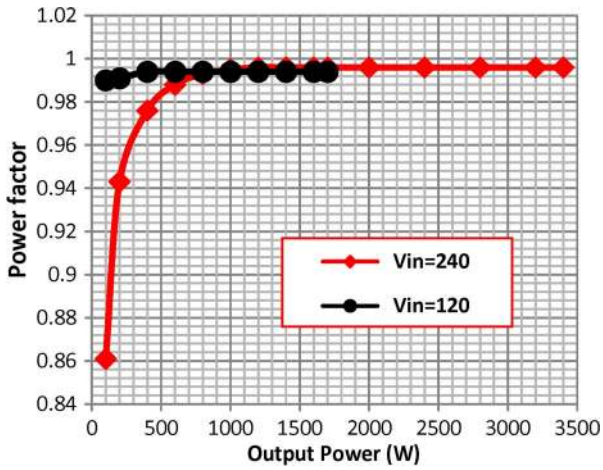

Fig. 19. Power Factor versus output power at: $P_o = 1.7$ kW for $V_{\rm in} = 120$ V and $P_o = 3.4$ kW for 240 V.

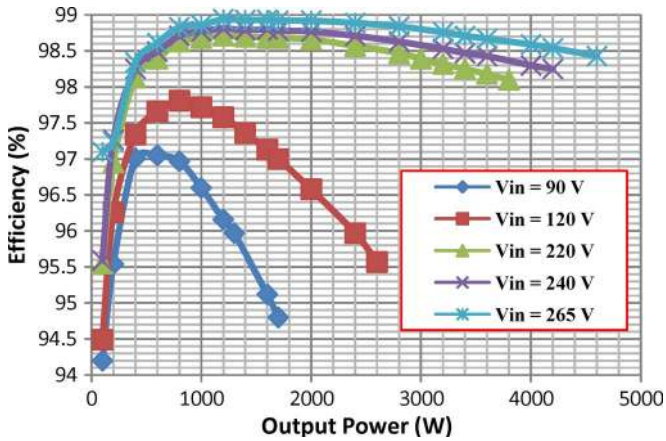

Fig. 20. Measured efficiency versus output power at: $V_{\rm in} = 90$ V, $V_{\rm in} = 120$ V, $V_{\rm in} = 220$ V, $V_{\rm in} = 240$ V, and $V_{\rm in} = 265$ V.

topology, reducing the need for heatsinks and active cooling systems. Furthermore, high efficiency means that more of the limited input power is available to charge the batteries, reducing charging time and electricity costs.

VIII. Conclusion

A novel BLIL boost PFC topology has been presented in this paper for application in the front-end ac–dc converter in PHEV battery chargers. The proposed topology has been analyzed and its performance characteristics have been presented. In addition, an analytical stress model was presented. The model can be used for the proposed topology, the conventional boost PFC topology, the interleaved boost PFC topology and the conventional bridgeless PFC topology, enabling the modeling of power losses and efficiency.

Experimental results presented include waveforms, and efficiency and input current harmonic data. The input current harmonics at each harmonic order were compared with the EN 61000-3-2 standard limits. The input current THD is less than 5% from half load to full load and the converter is compliant with the EN 61000-3-2 standard. The converter power factor was also provided for the full load power range at 120 V and 240 V input. The power factor is greater than 0.99 from half load to full load. The proposed converter achieved a peak efficiency of 98.9% at 70 kHz switching frequency, 265 V input and 1.2 kW output power.

Since the proposed topology shows high input power factor, high efficiency over the entire load range, and low input current harmonics, it is a potential option for single phase PFC in high power level II battery charging applications.

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