A High-Power, Fixed-Tuned, Millimeter-Wave Balanced Frequency Doubler

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Abstract— **We report on the design and evaluation of a 40 GHz to 80 GHz (40/80 GHz) high-power, wide-band, fixed-tuned balanced doubler. The active device is a single GaAs chip comprising a linear array of six planar Schottky varactors. The varactors and a quartz microstrip circuit are embedded in a split waveguide block. We have achieved a measured 3 dB fixed-tuned bandwidth of 17 % and measured flange-to-flange peak efficiency of 48 % at an input power level of 200 mW. The doubler operates at near peak efficiency (45 %) at an input power of 250 mW. We have cooled the block to 14 K and achieved an efficiency of 61 % at an input power level of 175 mW and an efficiency of 48 % at an input power level of 365 mW. Emphasis has been placed on making the design easy to fabricate and scalable to higher frequencies.**

Index Terms— **Frequency multiplier, balanced doubler, varactor, finite-element method, HFSS.**

I. INTRODUCTION

There is a demand for millimeter-wave and submillimeter-wave power sources, primarily for use as local oscillators in heterodyne radiometers for remote sensing, atmospheric physics, and radio astronomy. An ideal source for most of these applications, and particularly for those which involve space qualification, would exhibit high output power and efficiency, large electronically tuned bandwidth (fixed mechanical tuning), high tolerance to mechanical and thermal stress, high reliability, low noise, low mass and low cost.

Systems using frequency multipliers based on GaAs Schottky varactors and a fundamental oscillator, such as a Gunn-effect diode, have been used to achieve some of these goals. Until very recently, the most successful millimeter-wave multipliers relied on whisker-contacted GaAs varactors to minimize shunt capacitances for high frequency operation [1]. However, high quality planar varactors have recently been developed [2] and incorporated into successful millimeter-wave multipliers [3], [4]. These systems are mechanically reliable and exhibit high efficiency and power handling. Unfortunately, these systems have limited fixed-tuned bandwidth and are challenging to assemble.

Our 40/80 GHz balanced doubler design is derived from a prototype 80/160 GHz balanced doubler reported by Erickson [1], [3], [4]. Balanced doublers use EM mode orthogonality to isolate the input and output frequency circuits and thus do not require distributed filters which are lossy and tend to degrade the multiplier bandwidth. One way to achieve orthogonal input and output frequency modes in a balanced doubler is by placing an even number of varactors in anti-series at the junction between a balanced and unbalanced transmission line as shown in Fig. 1. If the incident power at frequency ω_o is in a balanced mode, then the output radiation at $2\omega_o$ is generated in an unbalanced mode.

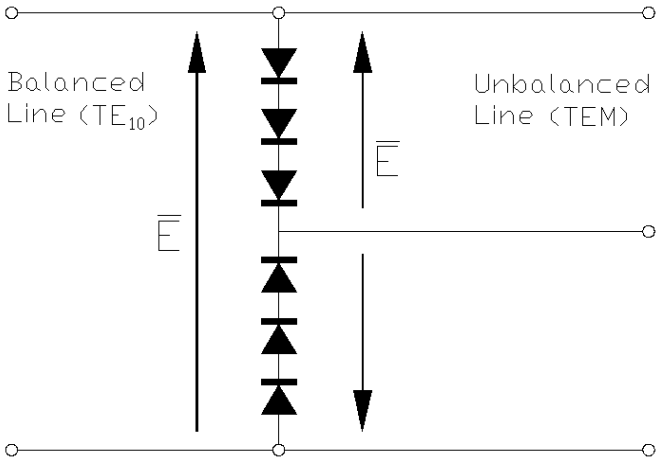


Fig. 1. Balanced frequency doubler schematic.

The prototype 80/160 GHz multiplier [1] achieved record output power and efficiency at 160 GHz. The design incorporated two whisker contacted varactors mounted on a machined cylindrical metal pin. The pin acted as an output waveguide probe, a low pass filter, a DC bias line and a center conductor in a quasi-coaxial structure which supported a TEM mode. A successful modification was made to the design [3], [4], by replacing the two whisker contacted varactors with a planar varactor chip. This modification increased the mechanical reliability of the multiplier and resulted in higher output power and efficiency.

There are four important advantages in the prototype 80/160 GHz balanced multiplier; i) the balanced design eliminates the need for lossy distributed filters, ii) the rectangular waveguides and the coaxial line have low loss, iii) DC bias is easily provided to the varactors through the metal pin, and iv) the design is amenable to the use of multiple varactors in a planar package, resulting in high power handling and reliability. There are also, however, two important limitations; i) it is difficult to mount the pin in the waveguide block and to solder the varactor chip to the pin, and ii) the output frequency matching circuit is limited by the pin geometry resulting in a rather narrow fixed-tuned

bandwidth. A pair of Teflon transformers located in the input and output waveguides improve the multiplier efficiency by providing a wide range of mechanical tuning. However, these transformers cannot be adjusted during operation. Also, the transformers are located some distance away from the varactors which further compromises the instantaneous bandwidth. In the new 40/80 GHz doubler design, we kept all of the important advantages of the prototype 80/160 GHz multiplier while significantly increasing the fixed tuned bandwidth and making the multiplier easier to machine and assemble.

II. OVERVIEW OF THE IMPROVED 40/80 GHz DESIGN

Fig. 2 shows a sketch of the 40/80 GHz planar balanced doubler. There are no adjustable mechanical tuners in this design, but rather a fixed indium backshort. We replaced the metal pin in the 80/160 GHz prototype design with a quartz substrate. The center conductor for the TEM line, an output waveguide probe and an RF blocking filter for the DC biasing network are photolithographically formed on the quartz substrate. This allows for a high degree of flexibility and control of the center conductor dimensions and therefore substantial control over the embedding impedance at the output frequency. Another advantage is the ease and low cost of producing the quartz circuits in large numbers.

The input radiation is incident on the varactors in a balanced mode (TE_{10}) in reduced-height Q-band waveguide. However, the input radiation can propagate beyond the varactor chip toward the E-band output waveguide. EM simulations using Hewlett-Packard's High Frequency Structure Simulator (HFSS) show that the center conductor and quartz dielectric in this quasi-coaxial region only slightly perturb the TE_{10} mode. At a point between the varactor chip and the output waveguide, the width of the quasi-coaxial waveguide section is sufficiently reduced to cut off propagation of the fundamental frequency, creating an effective input frequency backshort. The reduced-width section, more appropriately termed as enclosed suspended microstrip, extends to the output waveguide. The position of the backshort and the length of the reduced-height waveguide section between the varactors and the full-height input waveguide are design parameters that were used to obtain an acceptable input frequency embedding impedance.

The output frequency is generated by the varactors in an unbalanced mode (TEM) and is free to propagate to the output waveguide. However, there are a number of propagating modes supported by the input waveguide at the output frequency. The lowest order of these modes which can couple to the output frequency TEM field distribution is the TM_{11}. The TM_{11} mode can be cutoff by sufficiently reducing the input waveguide height and thus the output frequency radiation is restricted to the output circuit.

The machining of the block, the formation of the backshort and the mounting of the varactor chip and circuit are relatively simple. Two bond wires (1 mil) are attached to pads along the outer edge of the quartz circuit and a DC bias wire is soldered to the opposite end of the circuit. The varactor chip is then soldered [5] at each end to the bond wire pads and additionally to a third pad provided at the center conductor. The entire circuit is then placed in the split waveguide block, the two bond wires are soldered to the block and the bias wire is soldered to a DC feed.

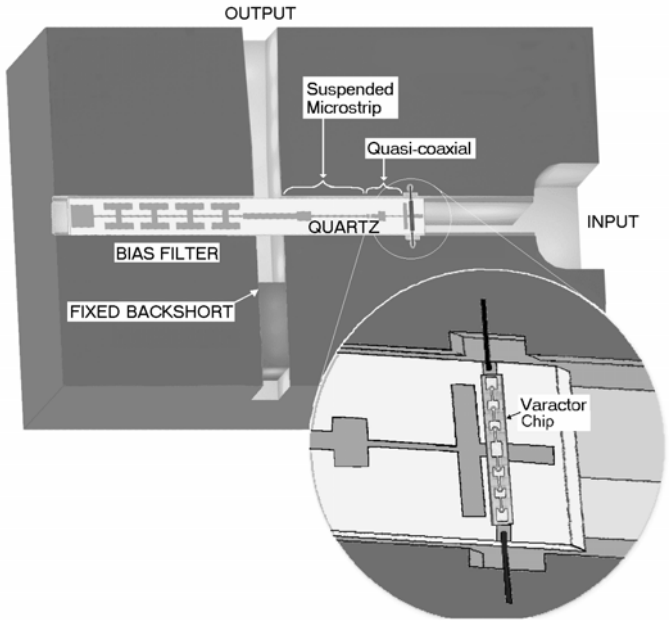


Fig. 2. 40/80 GHz planar balanced frequency doubler. The exploded view shows the planar varactor chip facing up for illustrative purposes.

III. DESIGN METHODOLOGY

The harmonic balance analysis described in [6], Hewlett-Packard's Microwave Design System (MDS), and the harmonic analysis of Penfield-Rafuse [7] were used to determine a range of optimum embedding impedances for maximum doubler efficiency. The embedding impedances provided by the distributed circuit are frequency dependent and the embedding impedances required for optimum multiplier efficiency are dependent on frequency and on semiconductor device parameters.

With about 200 mW of available power in the 35-45 GHz band, our goal was to maximize the power output of the doubler in the corresponding 70-90 GHz band. Power handling in Schottky varactors is determined mainly by the epitaxial doping, the anode size, the number of varactors on the chip and thermal properties. Power handling can be increased by lowering the epitaxial layer doping since this will lead to larger reverse breakdown voltage. However, decreasing the epitaxial doping increases the series resistance resulting in more power dissipation in the varactor, lower multiplier efficiency and higher ambient temperatures which can ultimately lead to increased failure rates. For a given epitaxial doping, larger anodes can handle more power, but the required embedding impedances are inversely proportional to anode size and there are practical limits

on the range of impedances that can be matched. Stacking varactors in series increases the power handling capability and increases the impedance of the varactor circuit. However, stacking is limited by the physical size of the reduced-height waveguide where the chip is mounted.

Velocity saturation was another factor in choosing the epitaxial layer doping [8]. The maximum current in the undepleted epitaxial region can be calculated based on the maximum average electron velocity, v_{max}, the epitaxial doping, N_D, the charge of an electron, q, and the anode cross sectional area, A, $I_{sat} = qN_DAv_{max}$. The maximum average electron velocity for GaAs is approximately $2x10^5$ m/s. At higher frequencies, it is necessary to reduce the anode diameter to reduce the net capacitance and thus it may be necessary to increase the epitaxial layer doping to forestall the onset of velocity saturation.

We chose a linear array of 6 varactors with an epitaxial layer doping of $1x10^{17}$ cm^{-3} and a buffer layer thickness of 8 µm, the skin depth for GaAs at 40 GHz. The varactors, designated as type SB13T1, were fabricated at the University of Virginia Semiconductor Device Laboratory. Fig. 3 shows a scanning electron micrograph of the SB13T1 planar varactor chip. The finger lengths are 50 µm, the ohmic contact pads are 3200 μm^2, and the semi-insulating GaAs substrate is 75 µm thick. The overall chip dimensions are 800x90x75 µm. Three versions of the SB13T1 chip were fabricated with anode diameters of 12, 13 and 14 µm. We calculated a series resistance of 0.8 Ω per varactor (13 µm anodes) which includes contributions from the spreading resistance, epitaxial layer resistance, substrate resistance and resistance in the ohmic contacts [9]. There is some degree of uncertainty in the series resistance calculation. Measured values at DC tended to be closer to 1.2 Ω and RF values may be even higher due to skin effects. The series resistance could be further elevated due to heating. The reverse breakdown voltage was measured to be approximately 14 V at 1 µA reverse current. Using the specified doping levels and anode sizes for the SB13T1, we calculated I_{sat} greater than 400 mA while harmonic balance simulations for this varactor indicate peak currents of approximately 90 mA at an input power level of 200 mW.

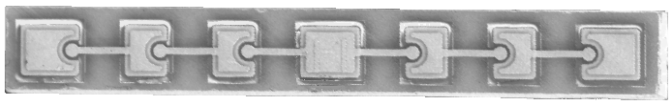
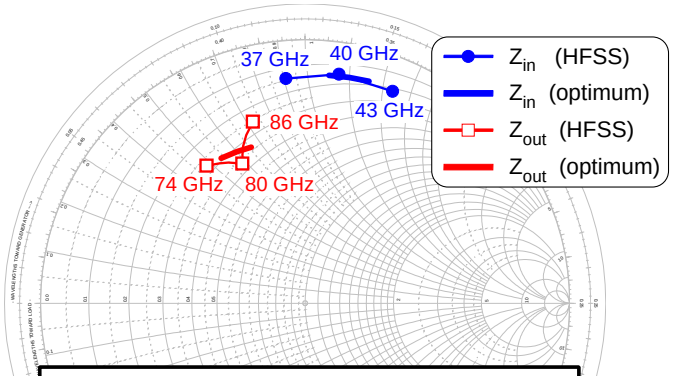


Fig. 3. UVA type SB13T1 linear varactor array comprising 6 Schottky varactors.

We used HFSS and MDS to model all parts of the waveguide block, quartz circuit and varactor chip. HFSS ports were attached to probes at each anode to calculate the individual varactor embedding impedances. A large number of geometrical perturbations of the waveguide, varactor chip and quartz circuit were analyzed in HFSS and MDS to determine a range of embedding impedances that could be provided by each configuration. The calculated circuit impedance data was compared to the optimum varactor embedding impedance data and a circuit and block design which provided the best match over the widest bandwidth was chosen. A sample of the optimum and calculated embedding impedances is shown in Fig. 4. The embedding impedances change slowly with frequency and thus a relatively large bandwidth is achieved without using mechanical tuners.



f_{out} (GHz)	Z_{in} (Ω)		Z_{out} (Ω)	
	HFSS	Optimum	HFSS	Optimum
74	8 + j44	9 + j65	14 + j24	17 + j33
80	8 + j56	8 + j60	18 + j29	16 + j30
86	12 + j73	8 + j55	13 + j36	15 + j27

Fig. 4. Optimum and HFSS calculated embedding impedances for the 40/80 GHz balanced doubler circuit.

The circuit, block and backshort were fabricated according to the HFSS simulation geometry. Most of the HFSS modeling was done with lossless materials to substantially reduce the finite element convergence time and memory requirements. HFSS simulations indicated that the return loss for the transition from the suspended microstrip to the output waveguide [10] was better than 25 dB across the band from 70-90 GHz.

IV. MEASURED PERFORMANCE AT 290 K

Power levels were measured using HP437 meters with Q-band and W-band power sensors. Since the doubler block incorporated an E-band output waveguide flange, an E-W waveguide adapter was used. The reference planes for all power measurements were the input waveguide flange on the doubler block and the W-band flange on the waveguide adapter at the output. No corrections were made for losses within the multiplier block or in the external waveguide adapter.

The graph in Fig. 5 shows measured output power and efficiency versus input power for varactors with 12 µm and 13 µm anodes. The quartz circuit was the same in both cases. The peak efficiency was 48 % at 82 GHz for the varactor chip with 12 µm anodes and 46 % at 78 GHz for the varactor chip

with 13 µm anodes. Input power was provided from a Gunn-effect oscillator capable of delivering over 200 mW in the 37-43 GHz band and from several klystrons operating in the 35-45 GHz band with output power typically in excess of 300 mW.

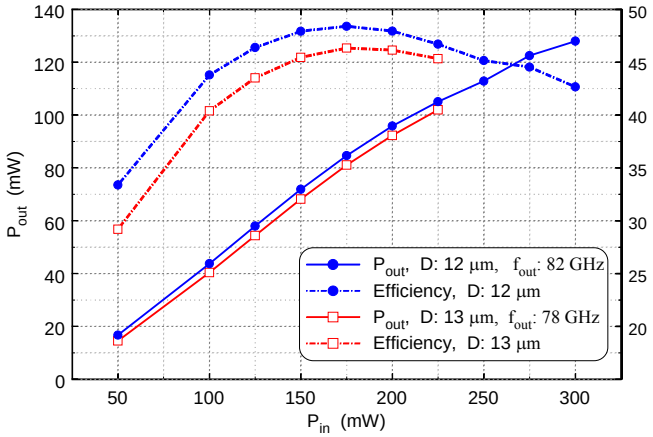


Fig. 5. Measured output power and efficiency versus input power for two different varactor chips.

Fig. 6 shows measured output power versus output frequency for the same 12 µm and 13 µm anode varactors. The input power for these measurements was 200 mW. Tuning was provided through an external electronic DC bias supply. The measured 3 dB fixed-tuned bandwidth of 17 % is typical for this version of the quartz circuit.

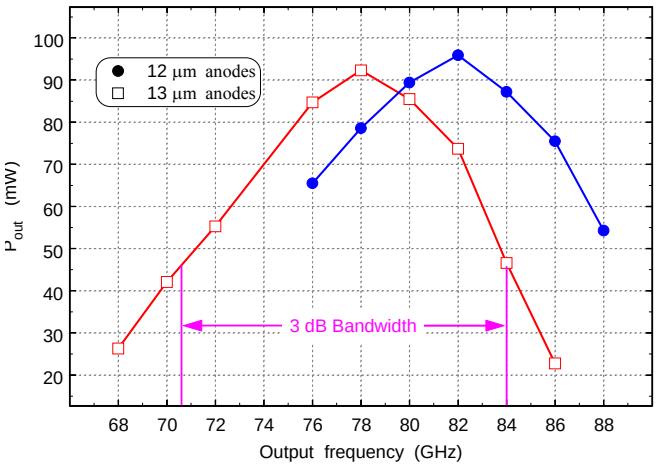


Fig. 6. Measured output power versus output frequency for an input power level of 200 mW.

Fig. 7 shows the measured input reflected power versus output frequency for the 12 µm and 13 µm anode chips. The reflected power measurements were made with an HP8565E spectrum analyzer through a directional coupler. The spectrum analyzer was also used to monitor the input frequency. Reflected power levels were typically less than 1 % of the incident power at the center of the band, indicating a good input impedance match.

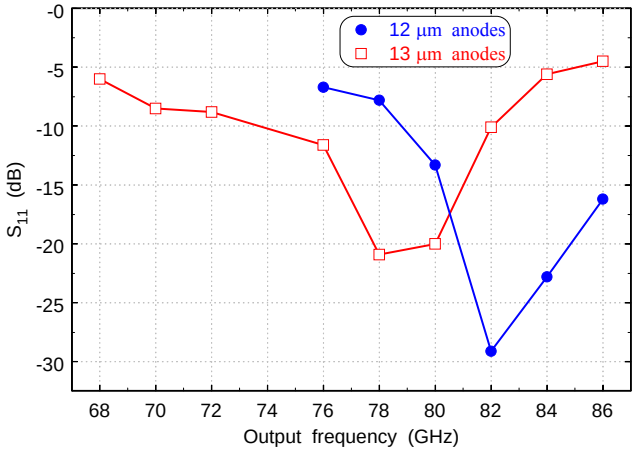


Fig. 7. Measured input power reflection coefficient vs output frequency at P_{in} = 200 mW.

The quality of the output impedance match was evaluated by attaching a 1 inch section of E-band waveguide to the doubler output waveguide flange, inserting a Teflon quarter-wave transformer, and measuring the output power as a function of the transformer position. The input power level was held constant at 200 mW. The output power was measured to be 94 mW prior to the insertion of the Teflon. With the Teflon transformer inserted in the output waveguide, the measured output power extrema were 72 mW and 85 mW. Using this data, we calculated the SWR in the output waveguide to be less than 1.6 (without the Teflon transformer), indicating a very good output impedance match. This calculation assumes that the available output power from the doubler is constant and is unperturbed by the transformer position.

A graph of measured DC bias voltage and current versus output frequency is shown in Fig. 8. These curves were obtained from measurements with the 13 µm anode chip and 200 mW input power, but are typical for the six chips we evaluated. The voltages and currents shown in Fig. 8 are those measured at the DC supply and thus the voltage across each varactor is one third that shown in the graph and the current through each varactor is one half that shown in the graph. The graph in Fig. 6 shows that the peak efficiency for this varactor occurred at 78 GHz. At this frequency, the bias current through each varactor was 100 µA. Forcing the DC current to zero resulted in only a very small degradation in efficiency.

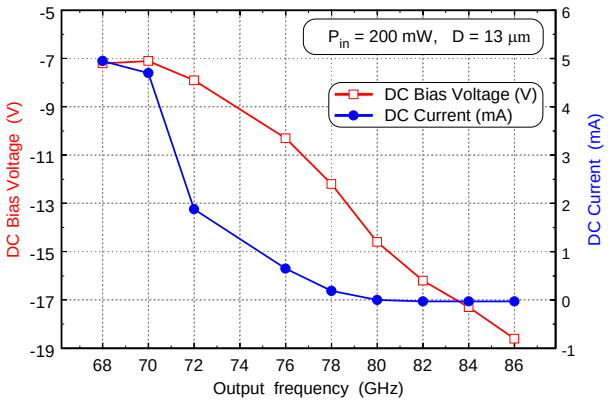


Fig. 8. Measured DC current and bias voltage vs output frequency for the 13mm anode chip.

V. COMPARISON OF SIMULATED AND MEASURED DATA

The waveguide and circuit losses were estimated using HFSS port solves at each distinct cross section in the block. The electrical conductivity of Au and the loss tangent of quartz were taken to be 4.1×10^7 S/m and 10^{-4} respectively. No corrections were made for conductor surface roughness, although actual measured waveguide losses are typically much higher than those based on conductivity and skin depth [11]. The loss in the E-W waveguide adapter was measured using an HP8510 vector network analyzer. The waveguide probe, hammerhead filter and indium backshort losses were estimated using a full HFSS adaptive analysis. The results are summarized in Table 1.

Table 1. Estimated waveguide and circuit losses based on Au conductivity and quartz loss tangent.

Loss location and frequency	Loss (dB)
Input waveguide, 40 GHz	0.02
Quartz circuit, 40 GHz	0.01
Quartz circuit, 80 GHz	0.14
Output probe and filter, 80 GHz	0.04
Indium backshort, 80 GHz	0.01
Output waveguide, 80 GHz	0.05
Waveguide adapter, 80 GHz	0.15
Total	0.42

Two measured output power curves and three simulated output power curves are shown in Fig. 9. The measured curves are the same as shown in Fig. 6. The simulated curves were generated using a harmonic balance analysis with an input power of 200 mW, zero biased junction capacitance of 140 fF and the circuit embedding impedances calculated by HFSS. The peak simulated output power of 145 mW occurred using the calculated series resistance of 0.8 Ω per varactor and the estimated external circuit losses of 0.42 dB. The discrepancy between the peak output power of this simulated curve and the measured peak output power is 1.8 dB. The two remaining simulated curves in Fig. 9 were generated by introducing additional loss mechanisms sufficient to equate the simulated to the measured output power. In one case this was done by using a series resistance of 2.5 Ω. In the second case, the calculated 0.8 Ω series resistance and a total of 2.2 dB in unspecified external circuit losses were used. The actual losses probably result from a combination of both mechanisms.

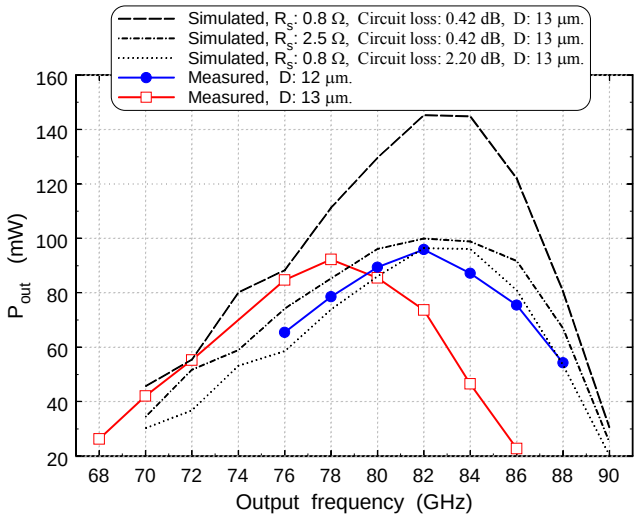


Fig. 9. Simulated and measured output power vs output frequency at P_{in} = 200 mW.

There are three additional factors which may reduce the multiplier efficiency; i) some power may get converted to higher harmonics, ii) the real part of the embedding impedance is actually somewhat higher than the simulated values due to circuit losses and iii) there is a small imbalance in the embedding impedances for varactors near the center conductor and varactors near the waveguide walls. HFSS simulations indicate that the imbalance is negligible for the TE_{10} mode at the input frequency, but is slightly more pronounced for the radially dependent EM field distribution at the output frequency. It may be possible to reduce the effect by altering the spacing between the varactors.

There is a discrepancy in the peak frequency of the measured and simulated data in Fig. 9. The simulated data was generated using a zero biased junction capacitance of 140 fF which corresponds to an anode diameter of 13 µm and epitaxial layer doping of 1×10^{17} cm^{-3}. However, the simulated peak frequency of 82 GHz corresponds to the measured peak frequency for the 12 µm anodes. We attribute this discrepancy to uncertainties in the actual varactor anode diameter and epitaxial layer doping.

Fig. 10 contains several plots of simulated and measured output power and DC current versus input power. The three simulated results were obtained using the calculated embedding impedances from HFSS and the estimated series resistance of 0.8 Ω per varactor. The measured output power data for the 12 µm anode chip is the same as shown in Fig. 5. Again, good agreement is obtained between the simulated and measured data when an additional 2.2 dB of loss is included.

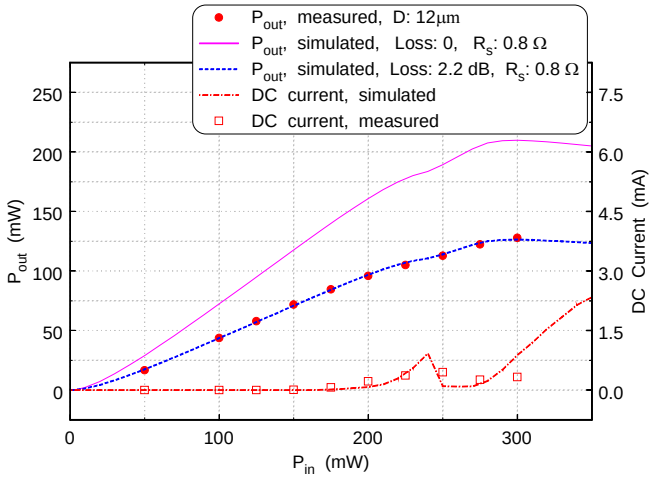


Fig. 10. Simulated and measured output power and DC current vs input power at 82 GHz.

For input powers in the range of 200-250 mW, there is an inflection in the simulated output power curves which coincides with an inflection in the measured data. Parametric oscillation can be ruled out as a cause for the inflection since the harmonic balance simulations do not model this effect. We interpret this inflection as a crossover between two operating regimes. For input power levels below 200 mW, optimum efficiency is achieved by steadily increasing the reverse bias voltage as the input power increases. In this regime, the DC current remains near zero (indicating a varactor mode of operation) and the bias voltage essentially tunes the average varactor capacitance to yield the best impedance match to the circuit. For input power levels above 250 mW, the optimum operating point is dominated by the need to minimize power dissipation in the series and junction resistances.

VI .MEASURED PERFORMANCE AT CRYOGENIC TEMPERATURES

For many applications, particularly in radio astronomy, it may be feasible to cool the multiplier. For these applications, it is necessary to determine the temperature dependence of the multiplier output power, efficiency and bandwidth and to determine if the multiplier can survive thermal cycling. Only a minor temperature dependence is expected in the circuit losses and embedding impedances. However, the electron mobility in GaAs has a strong temperature dependence. There is a peak in the electron mobility near 100 K for an epitaxial doping of $1x10^{17}$ cm^{-3} [12], [13]. Since the series resistance is inversely proportional to the electron mobility, an increase in multiplier efficiency is expected at cryogenic temperatures [14]. A reduction in dissipated power in the varactor will also improve the reliability of the multiplier.

The cryogenic performance of the doubler was measured at the National Radio Astronomy Observatory's Central Development Laboratory. A dewar was outfitted with waveguides and vacuum windows at both the input and output frequencies. These components were calibrated by measuring the insertion loss as a function of temperature. The input and output power measurements shown below are referred to the waveguide flanges on the doubler block. The specified temperatures are referenced to the multiplier block. The Schottky junction temperatures are expected to be somewhat higher due to power dissipation in the device. Fig. 11 shows a measured efficiency of 61 % at 78 GHz for an input power level of 150 mW and block temperature of 14 K. The efficiency rolls off to 48 % at an input power of 365 mW (P_{out} = 175 mW).

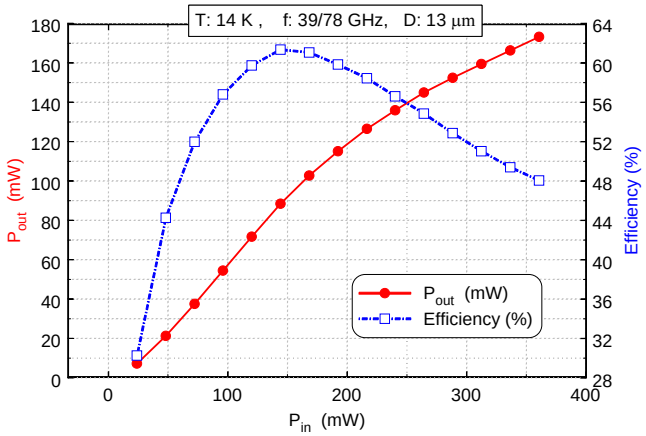


Fig. 11. Measured output power and efficiency vs input power for the 13 µm anode chip at 14 K.

Fig. 12 shows measured efficiency versus input power at four different temperatures. There is an increase in efficiency from 46 % at 295 K to 61 % at 14 K. Also, the input power level for peak efficiency drops as the block temperature is decreased. Both of these phenomena are probably attributable to the temperature dependent electron mobility in GaAs.

The fixed-tuned 3 dB multiplier bandwidth is largely dependent on the embedding impedances provided by the circuit. Since these impedances have only a very small temperature dependence, the fixed-tuned bandwidth is not expected to have a strong temperature dependence. The two plots in Fig. 13 show measured efficiency for the 13 µm anode chip as a function of frequency at block temperatures of 295 K and 14 K. The input power in both cases was held constant at 200 mW. The fixed-tuned 3 dB bandwidth for both curves is approximately 17 %.

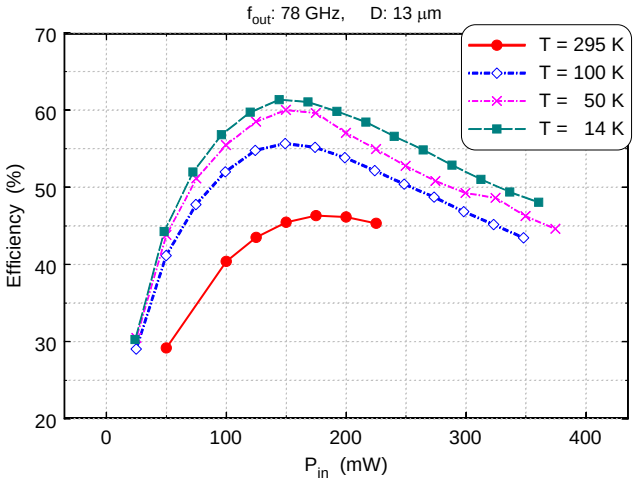


Fig. 12. Measured efficiency vs input power for various block temperatures. The output frequency is 78 GHz.

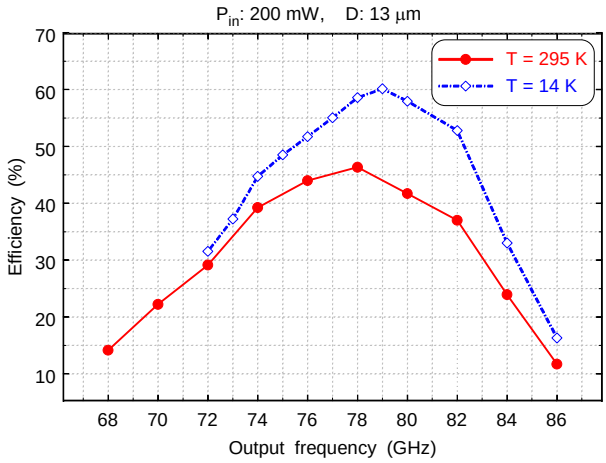


Fig. 13. Measured efficiency vs frequency at block temperatures of 295 K and 14 K.

VII. CONCLUSIONS

We have designed and evaluated a high-power, wide-band, fixed-tuned 40/80 GHz balanced frequency doubler. The doubler uses a single GaAs chip comprising a linear array of 6 planar Schottky varactors. The varactor chip and a quartz circuit are housed in a split waveguide block.

With the waveguide block at room temperature, the measured 3 dB fixed-tuned bandwidth was 17 % for an input power of 200 mW. The peak efficiency of 48 % occurred at an output frequency of 82 GHz and input power of 200 mW. We compared the measured results to harmonic balance simulations using the calculated embedding impedances from HFSS. The measured fixed-tuned bandwidth of 17 % was in excellent agreement with the simulated bandwidth and the measured peak output power was within 1.8 dB of the simulated result. The 1.8 dB discrepancy between the measured and simulated results may be due to additional circuit losses and an elevated temperature dependent series resistance in the varactors.

We also evaluated the multiplier at cryogenic temperatures in a calibrated dewar. The measured efficiency was 61 % at an input power of 150 mW and a block temperature of 14 K. The efficiency dropped to 48 % at an input power of 365 mW (P_{out} = 175 mW). The 175 mW output power level should be sustainable at cryogenic temperatures. The 3 dB output power bandwidth was approximately 17 % at both 14 K and 295 K, and exhibited only a weak temperature dependence.

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