IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 11, 2020, accepted March 20, 2020, date of publication April 1, 2020, date of current version April 15, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2984800

A High-Precision Bandgap Reference With a V-Curve Correction Circuit

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This work was supported by the Ministry of Science and Technology under Grant MOST 108-2221-E-150-039.

ABSTRACT In this study, a precision bandgap reference with a v-curve correction (VCC) circuit is presented. The proposed VCC circuit generates a correction voltage to reduce the temperature drift of the reference voltage and achieves a low temperature coefficient (TC) in a wide temperature range. The proposed bandgap reference was designed and fabricated using a standard TSMC 0.18-μm 1P6M CMOS technology with an active area of 0.0139 mm^2. The measured results show that the proposed bandgap reference achieves a TC of 1.9–5.28 ppm/°C over a temperature range of −40 °C to 140 °C at a supply voltage of 1.8 V. In addition, the circuit demonstrated a line regulation of 0.033 %/V for supply voltages of 1.2 – 1.8 V at room temperature.

INDEX TERMS Bandgap reference, line regulation, temperature coefficient (TC), temperature drift, v-curve correction (VCC) circuit.

I. INTRODUCTION

Bandgap references are essential building blocks in analog and mixed-signal circuits, such as linear regulators, A/D converters, D/A converters, and power converters for their high precision and temperature independence [1]–[17]. An accurate reference voltage must be stabilized over supply voltage and temperature variations. To achieve a low temperature coefficient (TC) over a wide temperature range, several curvature-correction techniques have been developed. Zhou *et al.* [7] realized exponential curvature compensation and logarithmic curvature compensation to reduce the temperature drift of a reference voltage. Andreou *et al.* [8] proposed a complementary-to-absolute-temperature (CTAT) current to fine-tune a curvature correction and thus achieve a new level of performance. Ma and Yu [10] proposed an opposite high-order curvature compensation by using MOS transistors operating in a weak inversion region for cancelling nonlinear temperature dependence. These cited bandgap references had an improvement in TC over wide temperature ranges.

In this study, a bandgap reference with an innovative v-curve correction (VCC) circuit is proposed and demonstrated; it effectively reduces the variation in the reference voltage and obtains a low TC in a wide temperature range. The proposed VCC circuit generates an opposite curvature correction to compensate the curvature of the reference voltage. The proposed bandgap reference occupies an area of 117 × 119 μm^2 in a standard TSMC 0.18-μm 1P6M CMOS process. The experimental results indicate that an average TC of 3.66 ppm/°C is realized over a temperature range of 180 °C and a line regulation of 0.033 %/V is achieved from a supply of 1.2 to 1.8 V.

The associate editor coordinating the review of this manuscript and approving it for publication was Artur Antonyan.

II. PROPOSED BANDGAP REFERENCE WITH A V-CURVE CORRECTION CIRCUIT

A temperature-independent voltage is often designed by combining a positive-TC voltage, a negative-TC voltage, and appropriate weight. Two opposite-TC voltages (V_{PT} and V_{NT}) can be achieved by using temperature characteristics of bipolar junction transistors, as discussed in related studies [2]–[14]. However, the curvature of a temperature-independent voltage is often presented in concave and convex. In this study, a VCC circuit is proposed to improve the curvature of a reference voltage in a wide temperature range.

Fig. 1 shows two design compensations of the proposed VCC circuit for convex curvature voltage; addition of a v-curve correction voltage or subtraction of an inverted v-curve correction voltage. The same compensation methods

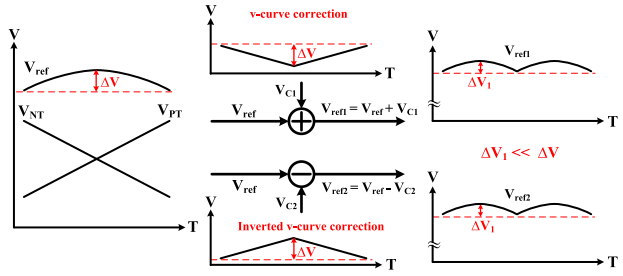


FIGURE 1. Compensation design of the proposed v-curve correction technique.

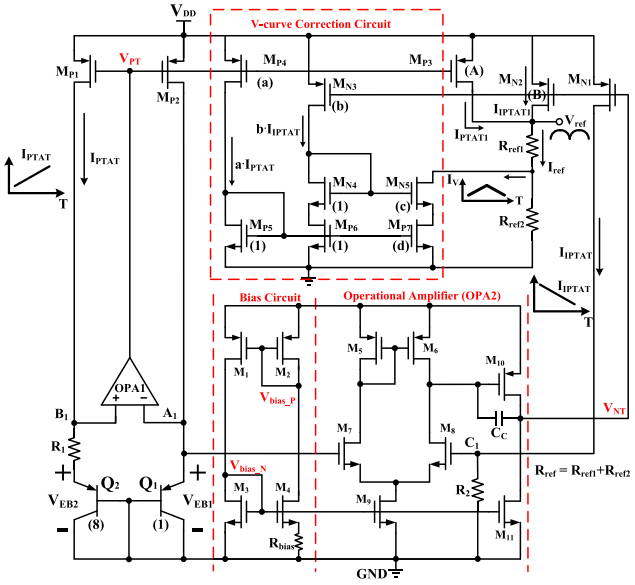


FIGURE 2. Complete circuit of the proposed bandgap reference with a v-curve correction circuit.

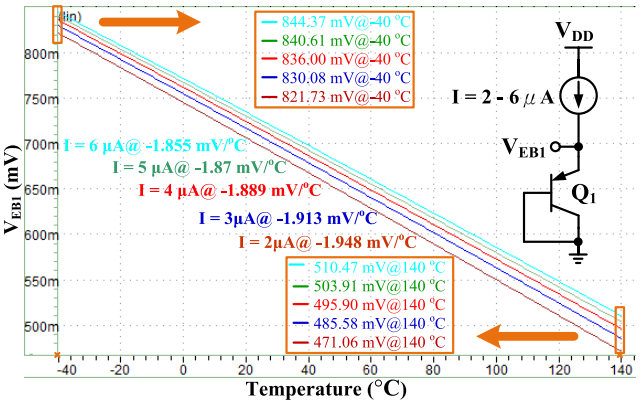


FIGURE 3. Temperature dependence of the emitter–base junction voltage V_{EB1} at different operating currents.

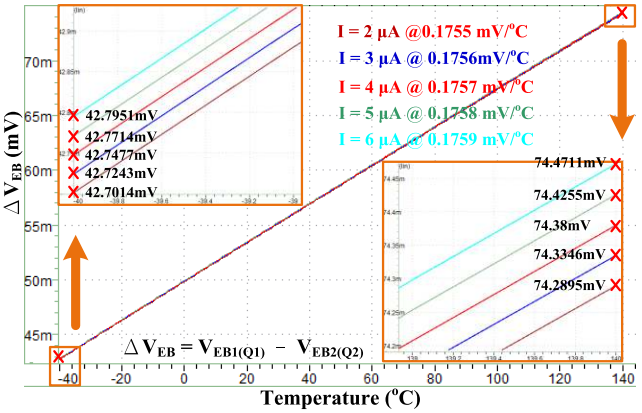


FIGURE 4. Temperature dependence of ΔV_{EB}.

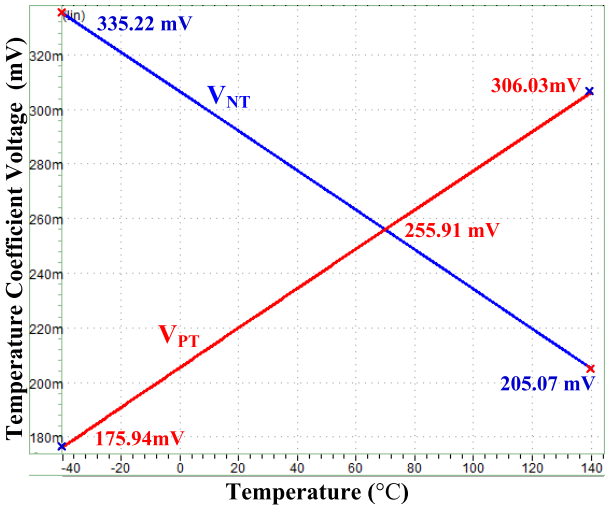
can also be implemented on the concave curvature voltage. The complete circuit of the proposed bandgap reference comprises a low-voltage bandgap reference and a VCC circuit as shown in Fig. 2. The low-voltage bandgap reference [4], [6], [8] provides a reference voltage below 1V. The proposed VCC circuit generates a correction voltage having opposite-curvature curves to effectively reduce the temperature drift of a reference voltage. The detailed fundamentals and analysis of the proposed bandgap reference are described as follows.

A. LOW-VOLTAGE BANDGAP REFERENCE CIRCUIT

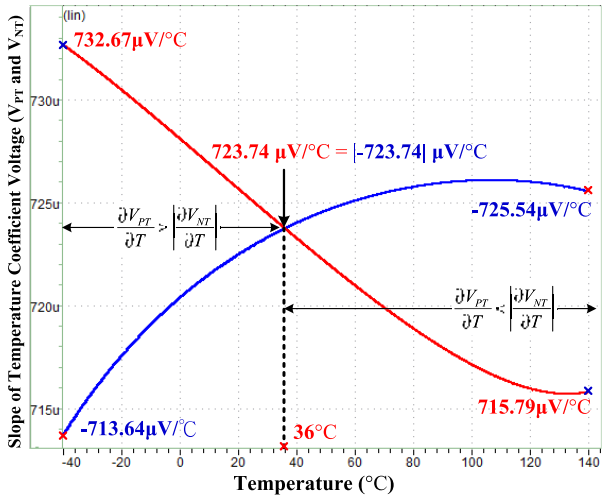
The low-voltage bandgap reference [4], [6], [8] comprises two bipolar transistors (Q_1 and Q_2), two operational amplifiers (OPA1 and OPA2), three resistors (R_1, R_2 and R_{ref}), and a current mirror circuit (M_{N1}, M_{N2}, and $M_{P1} - M_{P3}$). The area ratio of Q_1 and Q_2 is 1:8 to obtain the best possible layout matching. The emitter-base junction voltage V_{EB1} of Q_1 was simulated at different operating currents (2–6 μA) over a temperature range of 180 °C (−40 ° C to 140 °C). The simulation result indicated a negative TC of −1.855 to −1.948 mV/°C as shown in Fig. 3. The difference (ΔV_{EB}) in the two junction voltages (V_{EB1} and V_{EB2}) has a TC of approximately 0.175 mV/°C, as shown in Fig. 4. Thus, the negative TC of V_{EB1} can be canceled by the positive TC of ΔV_{EB} amplified about ten times. The amplifier OPA1 maintains an equal voltage at nodes A_1 and B_1, and a proportional-to-absolute-temperature (PTAT) current I_{PTAT} is realized through R_1 and Q_2. The amplifier OPA2 gives an equal negative-TC voltage at nodes A_1 and C_1, and a negative-TC current I_{IPTAT} is generated from M_{N1} to R_2. Thus, a temperature-independent current I_{ref} can be achieved by combining two opposite-TC currents, I_{PTAT1} and I_{IPTAT1}, which are designed by adjusting the size ratios of the current mirror circuit. Thus, a reference voltage of less than 1 V is provided by multiplying I_{ref} and R_{ref}, as described in (1).

$$\begin{aligned} V_{ref} &= \left(\frac{A \cdot \Delta V_{EB}}{R_1} + \frac{B \cdot V_{EB1}}{R_2}\right) \cdot \left(R_{ref1} + R_{ref2}\right) \\ &= \left(A \cdot I_{PTAT} + B \cdot I_{IPTAT}\right) \cdot \left(R_{ref1} + R_{ref2}\right) \\ &= \left(I_{PTAT1} + I_{IPTAT1}\right) \cdot R_{ref} = I_{ref} \cdot R_{ref} \end{aligned} \tag{1}$$

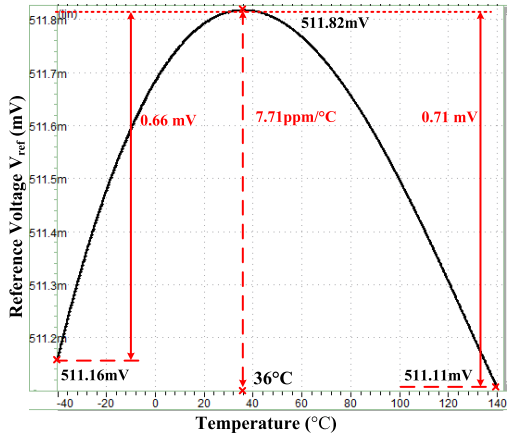
Both OPA1 and OPA2 are implemented using a two-stage amplifier with an n-channel input pair in the proposed bandgap reference. The gate voltage of M_7 is carefully considered because the emitter-base junction voltage V_{EB1} falls



(a)



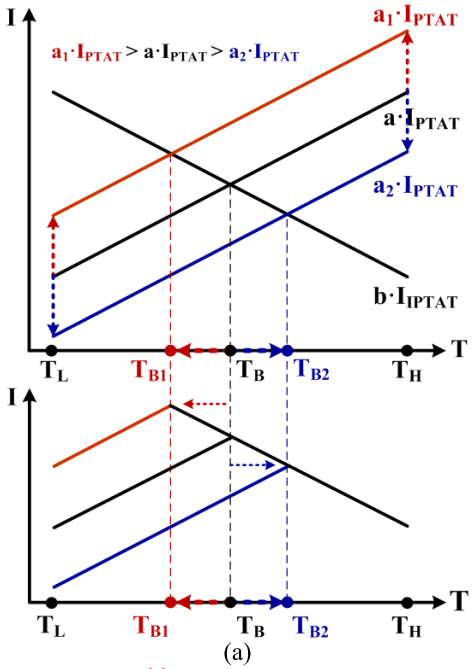
(b)



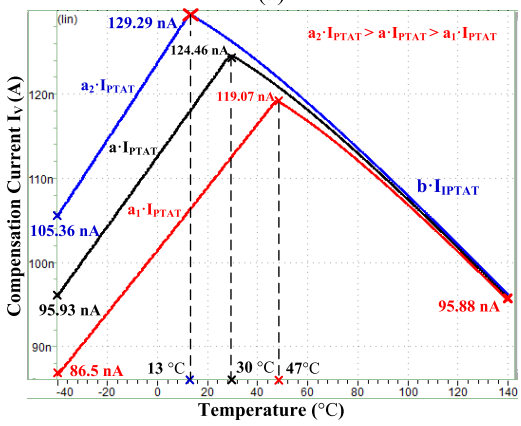
(c)

FIGURE 5. Post-layout simulation results of (a) two opposite-TC currents (I_{PTAT1} and I_{IPTAT1}), (b) temperature slopes of two opposite-TC voltages and (c) reference voltage.

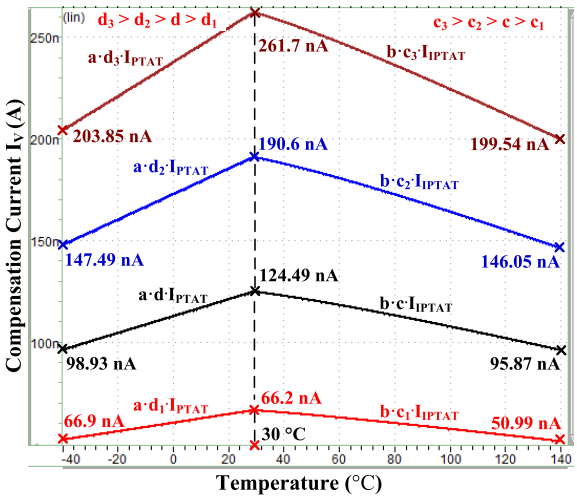
to 503.91 mV at 5μA at the highest temperature (140 °C) as shown in Fig. 3. The gate voltage of M_7 is given by



(a)



(b)



(c)

FIGURE 6. (a) Design concept, (b) temperature boundary and (c) magnitude of the compensation current.

$V_{GS7} + V_{DS9} \approx 0.5$ V. Furthermore, if the amplifier with an n-channel input pair is replaced with an amplifier with a p-channel input pair, the supply voltage is limited by V_{EB1} at a low temperature. The minimum supply voltage of the amplifier with a p-channel input pair is evaluated by $V_{EB1} + V_{SG} + V_{SD} \approx 1.35$ V.

B. PROPOSED V-CURVE CORRECTION CIRCUIT

The simulation results show two opposite-TC voltages (V_{PT} and V_{NT}), temperature slopes of two opposite-TC voltages and the reference voltage of the low-voltage bandgap reference over a temperature range of 180 °C (−40 °C to 140 °C), as shown in Fig. 5. In a temperature range of −40 °C to 140 °C, the positive-TC voltage V_{PT} is from 175.94 mV to 306.03 mV and the negative-TC voltage V_{NT} is from 335.22 mV to 205.07 mV. To analyze the variations of temperature slopes, we take the derivative of two opposite-TC voltages with respect to T as shown in Fig. 5(b). Because the temperature slope (732.67 – 723.74 μV/°C) of the positive-TC voltage V_{PT} is larger than the temperature slope (−713.64 −723.74 μV/°C) of the negative-TC voltage V_{NT} between −40 °C to 36 °C, a positive-TC voltage is achieved from 511.16 to 511.82 mV. Furthermore, because the temperature slope (723.74 – 715.79 μV/°C) of V_{PT} is lower than the temperature slope (−723.74 – 725.54 μV/°C) of V_{NT} between 36 °C to 140 °C, a negative-TC voltage is achieved from 511.82 to 511.11 mV. The TC of the reference voltage with a convex curvature is 7.71 ppm/°C, which is formed by combining the opposite-TC voltages as shown in Fig. 5(c). In this study, an inverted VCC circuit is proposed to effectively reduce the variation in reference voltage with a convex curvature under a wide temperature range. The proposed VCC circuit only uses seven transistors (M_{N3}–M_{N5} and M_{P4}–M_{P7}) and its operation is discussed as follows.

First, two compensation ranges are determined by adjusting the mirrored currents $a{\cdot}I_{PTAT}$ and $b{\cdot}I_{IPTAT}$. When the negative-TC current $b{\cdot}I_{IPTAT}$ is larger than the positive-TC current $a{\cdot}I_{PTAT}$ between T_L and T_B, the transistor M_{N3} operates in the triode region and $a{\cdot}I_{PTAT}$ is a dominant current through M_{N3}, M_{N4}, and M_{P6}. However, when $b{\cdot}I_{IPTAT}$ is smaller than $a{\cdot}I_{PTAT}$ between T_B and T_H, the operation of the transistor M_{P6} is changed from the saturation region to the triode region and $b{\cdot}I_{IPTAT}$ grows into a dominative current, as shown in Fig. 6. Furthermore, the temperature boundary of the two compensation ranges can be shifted for different temperature drifts of reference voltage. If the positive-TC current $a{\cdot}I_{PTAT}$ is raised to $a_1 \cdot I_{PTAT}$ in the fixed current $b{\cdot}I_{IPTAT}$, the temperature boundary shifts from T_B to T_{B1}, as shown in Fig. 6(a). However, if $a{\cdot}I_{PTAT}$ is reduced to $a_2 \cdot I_{PTAT}$, the temperature boundary shifts to T_{B2}. In a similar design, the temperature boundary can be moved by adjusting the negative-TC current $b{\cdot}I_{IPTAT}$ at a fixed current $a{\cdot}I_{PTAT}$. Fig. 6(b) shows simulation results for three different compensation boundaries (13 °C, 30 °C and 47 °C) that are designed by adjusting the mirrored current $a{\cdot}I_{PTAT}$. Moreover, the magnitude of a compensation current is determined by adjusting the size ratios of the transistors M_{N4}, M_{N5}, M_{P6}, and M_{P7} for different reference voltage variations, as shown in Fig. 6(c). The proposed reference voltage with a v-curve correction voltage is given as follows:

$$\begin{aligned} V_{ref} &= \left(\frac{A \cdot \Delta V_{EB}}{R_1} + \frac{B \cdot V_{EB1}}{R_2}\right) \cdot R_{ref} \\ &\quad - \left(\frac{a \cdot d \cdot \Delta V_{EB}}{R_1} + \frac{b \cdot c \cdot V_{EB1}}{R_2}\right) \cdot R_{ref2} \\ &= (A \cdot I_{PTAT} + B \cdot I_{IPTAT}) \cdot R_{ref} \\ &\quad - (a \cdot d \cdot I_{PTAT} + b \cdot c \cdot I_{IPTAT}) \cdot R_{ref2} \\ &= (I_{PTAT1} + I_{IPTAT1}) \cdot R_{ref} \\ &\quad - (a \cdot d \cdot I_{PTAT} + b \cdot c \cdot I_{IPTAT}) \cdot R_{ref2} \\ &= I_{ref} \cdot R_{ref} - (a \cdot d \cdot I_{PTAT} + b \cdot c \cdot I_{IPTAT}) \cdot R_{ref2} \end{aligned} \quad (2)$$

The resistor R_{ref2} is only part of the output resistor R_{ref}, as shown in Fig. 2. The transistors M_{N5} and M_{P7} drain an inverted v-curve current I_V from the resistor R_{ref2}. This operation is similar to the addition of v-curve current to the

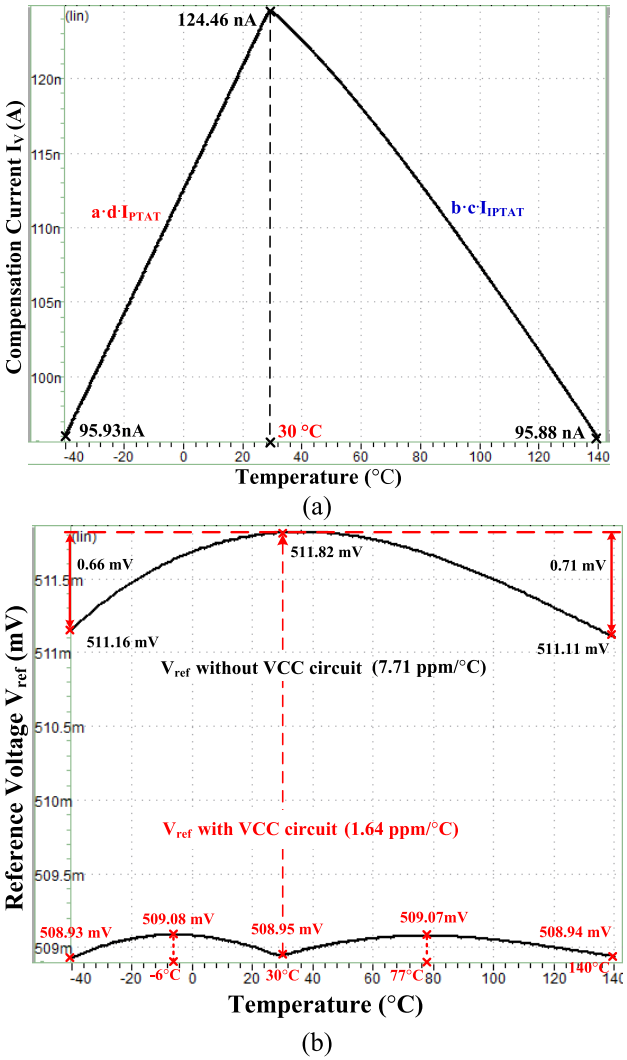


FIGURE 7. Post-layout simulation results of (a) an inverted v-curve correction current and (b) the corrected reference voltage.

reference voltage for convex-curvature correction. Fig. 7 shows the simulation results of an inverted v-curve compensation current, the uncorrected reference voltage and the corrected reference voltage over a temperature range of 180 °C (−40 °C to 140 °C). An inverted v-curve compensation current (95.88 – 124.46 nA) multiplied by resistor R_{ref2} to correct the voltage variation (0.71 mV) of the reference voltage. Compared with the simulation results of the low-voltage bandgap reference, the TC of the proposed reference voltage exhibits a 78.8 % reduction, from 7.71 to 1.64 ppm/°C, as shown in Fig. 7(b). The variation of the reference voltage is decreased from 0.66 to 0.15 mV in the temperature range −40 °C to 30 °C. A voltage variation of 0.71 mV is reduced to 0.13 mV in the range 30 °C to 140 °C. The reference voltage is less than 1.74 to 2.89 mV after compensation, which is caused by the inverted v-curve compensation current drawn from the output. To analyze process variations and mismatches, 500 runs of post-layout Monte Carlo simulations were performed and the results are shown in Fig. 8. Of the total runs, 401 runs achieved a TC of less 2 ppm/°C, with a minimum of 1.64 ppm/°C. Fig. 9 presents the simulation results of the proposed reference voltage in the BJT corners.

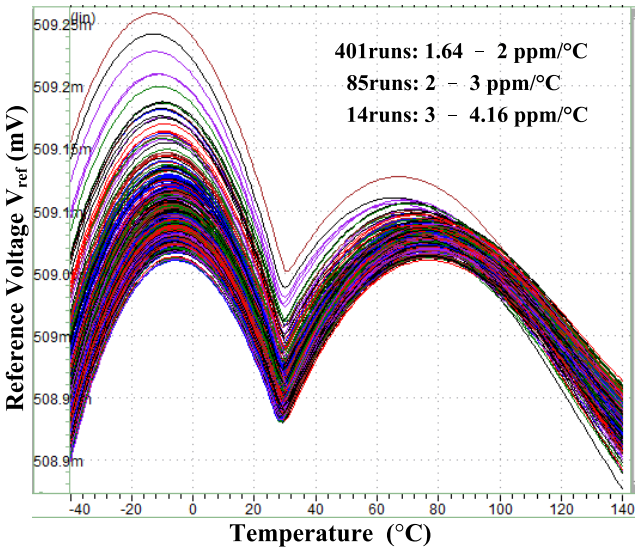


FIGURE 8. TC for 500 runs of the Monte Carlo simulations.

III. EXPERIMENTAL AND COMPARISON RESULTS

The proposed bandgap reference with a VCC circuit was fabricated using a standard TSMC 0.18-μm 1P6M CMOS technology. Fig. 10 depicts a physical micrograph of the proposed bandgap reference chip. The active chip area was 117 × 119 μm^2. V_{ref} of the bandgap reference as a function of the supply voltage was measured using a programmable voltage source and an oscilloscope. Fig. 11 shows the V_{ref} at each step voltage, which was measured by applying a staircase sweep voltage ranging from 0.6 to 1.8 V at room temperature. The experimental result indicates a constant voltage of 494.5 mV with a 0.2 mV variation under a 0.6 V

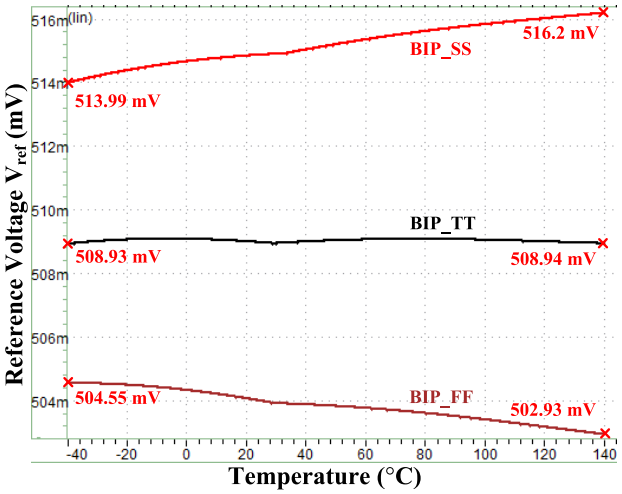


FIGURE 9. Simulation results of the proposed reference voltage in the BJT corners.

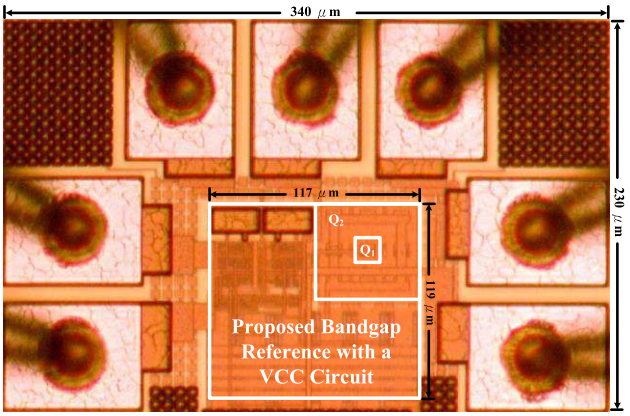


FIGURE 10. Physical micrograph of the proposed bandgap reference chip.

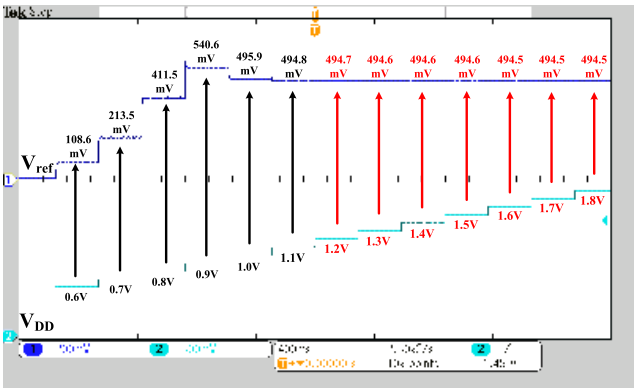


FIGURE 11. Measured output voltage at each step voltage from 0.6 to 1.8 V.

supply voltage variation. Thus, the line regulation of the proposed bandgap reference was 0.033 %/V across a voltage supply of 1.2–1.8 V. The TC of V_{ref} was measured in a programmable temperature chamber. Fig. 12 shows the V_{ref} and TC distribution, which were measured from −40 °C to 140 °C

TABLE 1. Comparisons of the proposed bandgap reference.

Specifications	2012 [8] IEEE JSSC	2014 [10] IEEE TCAS-I	2015 [11] IEEE TCAS-I	2017 [16] IEEE TCAS-I	2019 [17] IEEE TCAS-I	This work
Supply Voltage(V)	2.5	1.2	1.2	1.8	3.3	1.8
Current Consumption(μA)	38	36	120	28	94	26.3
Reference Voltage(mV)	617.7	767	735	547	2470	494.5
Best TC(ppm/°C)	3.9	3.4	4.2	3.05	0.9	1.9
Average TC(ppm/°C)	4.9	4.91	9.3	6.11	3	3.66
Standard Deviation (σ)	N/A	N/A	N/A	N/A	1.87 mV	0.018mV
Temp Range(°C)	-15 to 150	-40 to 120	-40 to 120	-40 to 140	-45 to 125	-40 to 140
Line Regulation(%/V)	0.039	0.054	N/A	0.08	N/A	0.033
PSRR (dB)	N/A	-84@400 Hz	-30@100 kHz	N/A	-83@dc	-68@566 Hz
Active Area(mm^2)	0.102	0.036	0.063	0.0094	0.0616	0.0139
Trimming	YES	YES	NO	NO	YES	NO
Technology	CMOS 0.35μm	CMOS 0.18μm	CMOS 0.13μm	CMOS 0.18μm	CMOS 0.35μm	CMOS 0.18μm

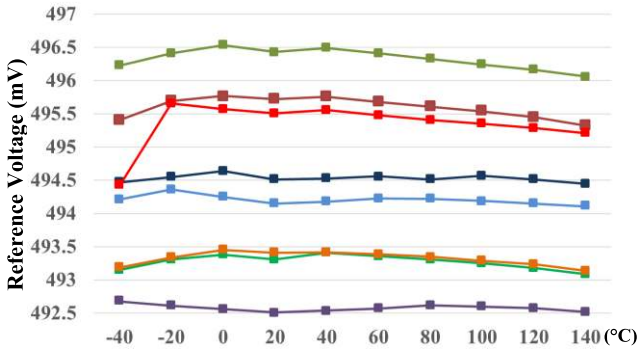


FIGURE 12. Measured temperature dependence of the reference voltage at a supply voltage of 1.8 V.

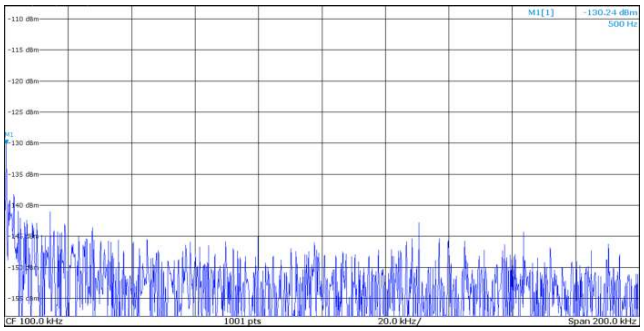


FIGURE 13. Measured noise spectrum of the proposed bandgap reference at room temperature.

at a 1.8 V supply voltage. The experimental results demonstrate that the proposed bandgap reference achieved a TC of 1.9–5.28 ppm/°C over a 180 °C temperature range in eight samples. The average TC was approximately 3.66 ppm/°C. The measurement results of the reference voltage differ from the simulation results by 12.45 – 16.45 mV, and these errors are mainly due to the process variation of the resistance. After measuring the output resistance R_{ref}, it is found that the output resistance is 0.9kΩ less than the expected design resistance. Table 1 compares the performance of the bandgap reference described in this study to those of previous bandgap references [8]–[12]. Fig. 13 shows the measured noise spectrum of the reference voltage V_{ref} without a decoupling capacitor from 1 Hz and 200 kHz. The results of using the signal and spectrum analyzer (R&S FSW8) prove that the highest noise density of −130.24 dBm was at 500 Hz.

IV. CONCLUSION

In this study, a precision bandgap reference was fabricated using a standard CMOS 0.18-μm process. The chip area of the bandgap reference with test pads was 0.078 mm^2. The experimental results confirmed that the proposed VCC reduces the variation of the reference voltage over a wide temperature range and has a temperature coefficient improvement of 72.5%. The designed v-curve correction voltage can effectively reduce the temperature drift of the reference voltage. The best TC of the proposed bandgap reference was 1.9 ppm/°C in a temperature range of −40 °C to 140 °C with a 1.8 V supply voltage. The measured output voltage achieved a 0.2-mV variation from a supply voltage of 1.2−1.8 V at room temperature. Therefore, the proposed bandgap is suitable for advanced CMOS circuits.

ACKNOWLEDGMENT

The authors would like to thank the Taiwan Semiconductor Research Institute for technical support.

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