A high-resolution self-timed zero-crossing-based Incremental $\Delta\Sigma$ ADC

Georgios Karykis

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TU Delft Delft University of Technology

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Georgios Karykis

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Delft University of Technology
Faculty of
Electrical Engineering, Mathematics and Computer Science

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A high-resolution self-timed zero-crossing-based Incremental $\Delta\Sigma$ ADC

by

Georgios Karykis

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Supervisor(s):

Dr.ir. Michiel A.P. Pertijs

Chao Chen, M.Sc.

Reader(s):

Dr.ir. Michiel A.P. Pertijs

Dr. Marco Spirito

Dr.ir. Jaap Hoekstra

Dr.ir. Robert H.M. van Veldhoven

Abstract

This thesis discusses the design and verification of a high-resolution self-timed incremental $\Delta\Sigma$ ADC. The first self-timed incremental $\Delta\Sigma$ ADC was presented by C.Chen et.al at ISSCC 2013 and this work targets to improve the resolution, linearity and energy-efficiency of a self-timed ADC. Unlike conventional $\Delta\Sigma$ ADCs, a self-timed ADC is capable of arranging the timing itself and does not rely on a dedicated clock, saving energy and reducing system complexity. This work is tailored for energy-constrained integrated sensor interfaces, where resolution and linearity requirements are often above 16-bit.

For the implementation of the self-timed ADC, the knowledge of the charge-transfer completion of the switched-capacitor integrators of the loop-filter is necessary for the generation of the self-timed control signals. Zero-crossing-based (ZCB) switched-capacitor integrators were employed before in the design of the self-timed I$\Delta\Sigma$ ADC because the knowledge of the end of the charge-transfer is available. This thesis focuses on the systematic noise and linearity design of the first ZCB integrator of the self-timed ADC, building on the implementation of C.Chen et.al (ISSCC 2013), which is the state-of-the-art $\Delta\Sigma$ ADC design that is employing comparator-based or zero-crossing-based switched capacitor (CBSC/ZCBSC) circuits up to now.

An improved prototype chip of self-timed incremental $\Delta\Sigma$ ADC was implemented in NXP 1P5M 0.16μm CMOS process. A second-order single-ended $\Delta\Sigma$ modulator was designed accordingly and verified using pre-layout and post-layout simulations. The results of these simulations show that the improved prototype achieves resolution of approximately 16.7-bit, linearity of 1LSB with respect to 17-bit, when the modulator is operating for 1000 incremental cycles. The conversion time is less than 1.01ms, while the chip consumes less than 26μA from a 1V supply. This performance corresponds to a Schreier FOM of the ADC of 168.8dB, which is the best among CBSC/ZCB $\Delta\Sigma$ ADCs and fairly close to the state-of-the-art of OTA-based ADCs for Instrumentation & Measurement or audio applications.

Keywords: Energy-efficient, high-resolution, incremental $\Delta\Sigma$ ADC, self-timed, zero-crossing-based integrator.

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Chapter 1

Introduction

Incremental $\Delta\Sigma$ Analog-to-Digital converters (ADCs) are an attractive choice for the digitization of low-frequency signals often found in sensor applications. Incremental ADCs rely on a high-frequency dedicated oversampling clock. However, in energy-constrained sensor applications, where the signals of interest are infrequent and slowly varying (e.g. environmental signals), the generation of the high frequency clock may be a bottleneck in terms of energy consumption. In [1], a 14-bit self-timed incremental $\Delta\Sigma$ ADC has been proposed to solve this problem. This thesis is building up on this, targeting to improve the resolution and linearity of the self-timed I$\Delta\Sigma$ ADC above 16-bit in an energy-efficient way. Special attention is paid in the design of the first ZCB integrator of the loop-filter as it is the most performance critical component of the entire ADC.

At the beginning of this chapter, the concept of the self-timed Incremental $\Delta\Sigma$ ADC is briefly introduced, including its potential advantages and operating principle, highlighting the crucial role of zero-crossing-based circuits in the implementation without any dedicated oversampling clock. This is followed by a short discussion on the challenges and targets of this work, based on related prior work. At this point the objectives of this project are summarized and a brief description of the solution is presented. Finally, the structure of the rest of the thesis is described.

1-1 Concept: Self-timed Incremental $\Delta\Sigma$ ADC using ZCB SC circuits

This work is a follow-up of the world's first self-timed incremental $\Delta\Sigma$ ADC [1], which demonstrates the capability of operation without dedicated external clocks. The most important benefit of this strategy is the reduction the overall system complexity and power consumption. This comes from the fact that the oversampled clock generation circuitry (oscillators and/or PLLs) can be avoided and the clock generation functionality can be replaced by an asynchronous state machine. Furthermore, for input signals with very low activity (environmental signals) the conversions are performed in an irregular manner and thus, the power

consumption of the clock generation circuitry can be an important factor of the overall energy consumption.

The self-timed nature of the ADC in [1] was realized using a mixed-signal self-timed approach, in which hand-shaking between the analog signal processing circuitry and digital control is necessary. In this approach, the analog circuit has to be capable to generate a completion signal of the underlying analog function (e.g. integration, amplification etc) which is used by the digital control circuit in order to control the operation.

In the context of a discrete-time incremental $\Delta\Sigma$ modulator, the timing of the successive sampling and charge transfer phases of the switched-capacitor integrators can be arranged effectively by a 2-state asynchronous state machine, provided that the completion signals of the charge-transfer process of the SC integrators are available. In a conventional OTA-based implementation of a SC integrator, however, the signals are settling following an exponential trajectory and because of that an indicator of completion is not available. This fundamental limitation was bypassed in [1], by changing the charge-transfer mechanism utilizing zero-crossing based switched-capacitor integrators. Zero-crossing based SC (ZCBSC) circuits are based on the Comparator-based SC (CBSC) circuits that were introduced in [2]. Comparator-based and zero-crossing-based SC circuits have been mainly used in the design of pipeline ADCs in advanced CMOS technologies [2] [3] [4], in order to overcome the difficulties of realizing high-performance and low-power OTAs that are operating with low supply voltage.

The circuit diagram of a ZCB SC integrator is shown in Figure 1-1(a). This circuit and its

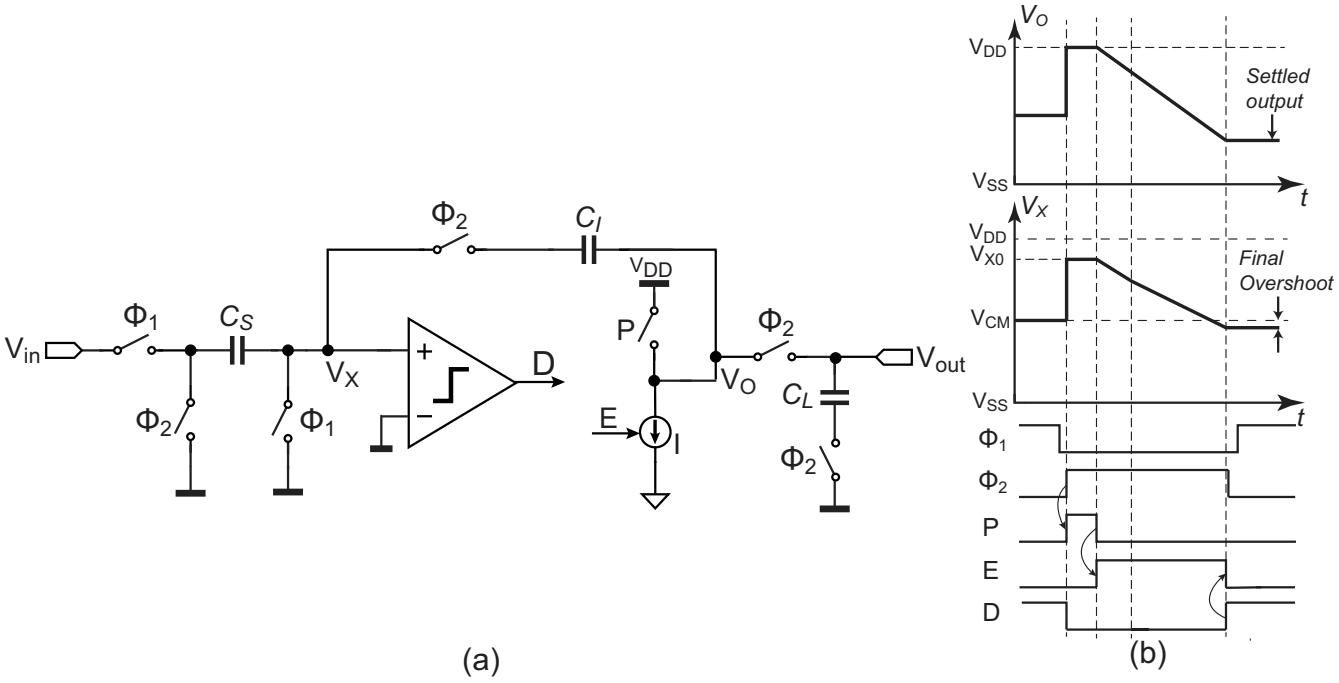


Figure 1-1: Circuit diagram (a) and waveforms of operation (b) of a ZCB SC integrator [5].

operation are very similar to an OTA-based SC integrator, but the OTA is replaced by a zero-crossing detector that is detecting the virtual-ground condition and a gated current source that is responsible for the charge transfer. The operation of a ZCB integrator is visualized in

the waveforms of Figure 1-1(b). While the sampling phase Φ_1 is identical with a OTA-based integrator, the charge-transfer phase Φ_2 of the ZCB integrator begins with presetting the output node to the supply V_{DD}. Because of this, the virtual-ground node V_X is preset higher than V_{CM} to a level that depends on the charge sampled on C_S and the previously integrated charge on C_I. Right after the preset, the gated current source is enabled to discharge the capacitive feedback network of the integrator forcing the signals to follow a linear trajectory. Once V_X reaches V_{CM}, the ZCD detects the virtual ground condition, the current source is turned-off and the output voltage is sampled.

It is important to remark that it is not important how V_O evolves towards its final value, but only how accurate its final value is, since we are dealing with a sampled-data system. As a result, the functionality of a ZCB integrator is identical with the OTA-based integrator and furthermore, the knowledge of completion of the charge transfer is available which enables purely self-timed operation in the $\Delta\Sigma$ ADC of [1].

1-2 Challenges and target specifications

As mentioned before, the main motivation for the development of ZCB circuits was the difficulty to design high-gain and closed-loop stable opamps in advanced CMOS processes, due to low supply voltages and degraded intrinsic gain of transistors. Apart from this, a few important advantages are present in zero-crossing based circuits concerning their energy-efficiency compared to the OTA-based structures. First, the ZCD only *detects* the virtual-ground condition but it does not force it, so intuitively it is expected to be more energy-efficient. Also, the ZCB circuits are open-loop, so frequency compensation is not needed to guarantee stability. Furthermore, inspecting the noise analysis of ZCB circuits the effective noise-bandwidth of the ZCD is lower than the steady-state noise bandwidth of an OTA [2], which means that lower power is needed to meet a target specification for noise. Therefore, circuitry based on zero-crossings is expected to demonstrate higher energy efficiency compared to OTA-based designs.

In Table 1-1 the performance of all the reported $\Delta\Sigma$ ADCs based on CBSC/ZCBSC circuits are summarized. Also, in Table 1-2 state-of-the-art designs of incremental $\Delta\Sigma$ ADCs with application to integrated sensor interfaces or biomedical sensor arrays (including hybrid ADCs and extended range incremental ADCs), along with two audio $\Delta\Sigma$ ADCs are summarized in order to facilitate a comparison between ZCB ADCs with conventional OTA-based ADCs.

When inspecting these two tables, it becomes directly clear that the reported energy-efficiency (in terms of FOM_S) is much lower for the designs that are based on CBSC/ZCB circuits, which contradicts the previously claimed advantages of these techniques. Also, the achieved resolution and linearity are limited in case of CBSC/ZCB $\Delta\Sigma$ ADCs. The best design is the first prototype self-timed ADC which achieves 14.8-bit resolution and INL of 1LSB w.r.t. 14-bit, demonstrating the highest energy efficiency among the CBSC/ZCB designs, but still far from the state-of-the-art of high resolution $\Delta\Sigma$ ADCs.

Moreover, the demonstrated performance of the CBSC/ZCB $\Delta\Sigma$ ADCs is limited in terms of linearity to at most 14-bit and resolution to at most 15-bit [1], although higher values are required in integrated sensor interfaces. Therefore, it is very interesting to explore ways to

Table 1-1: Performance comparison of prior CBSC/ZCB ΔΣ ADCs

	[6]	[7]	[8]	[9]	[1]
Architecture	ΔΣ2 - FD	ΔΣ2 - FD	ΔΣ4 - PD	ΔΣ2 - SE	IADC2 - SE
Process	$0.18\mu m$	$45nmLP$	$90nm$	$3\mu mTFT$	$0.16\mu m$
Area (mm^2)	0.21	0.0448	0.33	26	0.45
$V_{DD}(V)$	1.8	1.1	1	11.2	1
Sampling frequency	2.56 MHz	50 MHz	1 MHz	400 kHz	750 kHz
OSR	64	30	48	128	500
Bandwidth (Hz)	20 kHz	833 kHz	1 MHz	1.56 kHz	667 Hz
Dynamic Range (dB)	71	54.3	70	69	81.9
Peak SNR (dB)	65.3	47.7	66	65.6	81.9
Power	$0.42mW$	$630\mu W$	$5.94mW$	$63.3mW$	$20\mu W$
FOM_W (pJ/step)	6.98	1.91	1.82	13.03	1.46
FOM_S (dB)	147.8	145.5	152.3	112.9	157.1

$FOM_W = \frac{Power \cdot T_{conv}}{2^{(SNR-1.76)/6.02}}$. $\quad FOM_S = \text{SNR} + 10 \cdot \log\frac{1}{\text{Power} \cdot \text{T}_\text{conv}}$.

improve the resolution and linearity of a ZCB ADC and bring them to a level higher than 16-bit. Another interesting question is why the energy-efficiency of ZCB ΔΣ ADCs is far below the state-of-the-art of ΔΣ ADCs. The limitations of the energy-efficiency have to be explored targeting to an improvement of the achievable energy-efficiency, if possible to the level of OTA-based ΔΣ ADCs. This can be done having as starting point the best design of ZCB ΔΣ ADCs [1] and find out what is limiting the achievable performance. One straightforward approach could be the extension of [1] to a third or higher-order ΔΣ modulator. Another interesting research direction could be the extension of [1] to a fully-differential implementation.

All the previously mentioned alternatives should be carefully examined and based on their feasibility the realization of an improved self-timed ZCB incremental ΔΣ ADC should be possible. Achieving higher resolution and linearity (higher than 16-bit) is of primary interest as well as demonstrate higher energy-efficiency. In Table 1-3, the target specifications of the improved self-timed ΔΣ ADC are summarized.

1-3 Brief description of solution

This work has as basis the first prototype self-timed IΔΣ ADC [1] and focuses on finding ways of improving its performance and energy-efficiency. The work was based on the analytical estimation of noise and linearity of the first integrator, targeting to reveal trade-offs that are useful for design. A fairly accurate noise model has been developed, which was verified by revisiting the measurement of the first prototype, after fixing some accuracy problems of the measurement setup. Also, the linearity of the ZCB integrator has been analyzed, but the accuracy of this model is not good. As a result, a simulation-based linearity design procedure has been followed.

Table 1-2: Performance comparison of state-of-the-art OTA-based Incremental ΔΣ ADCs and audio ΔΣ ADCs

	[10]	**[11]**	**[12]**	**[13]**	**[14]-III**	**[15]**
Architecture	10bit SAR + IADC1-FD	6bit SAR + IADC2-PD	IADC2-FD + 11bit SAR	IADC2-FD + IADC1-FD	ΔΣ3-PD: inverter-based	ΔΣ3-PD: inverter-based
Process	$0.6\mu m$	$0.16\mu m$	$0.18\mu m$	$65nm$	$0.18\mu m$	$0.35\mu m$
Area (mm^2)	1.64	0.375	3.5	0.2	0.715	0.207
$V_{DD}(V)$	3.3	1.8	1.8	1.2	0.7	1.5
Sampling freq.	5 MHz	50 kHz	45.2 MHz	96 kHz	4 MHz	2.4 MHz
OSR	256	400	45	192	200	120
Bandwidth	9.75 kHz	121.5 Hz	500 kHz	250 Hz	20 kHz	20 kHz
Dynamic range (dB)	84.6	119.8	90.1	99.8	85	92.6
Peak SNDR (dB)	70.7	119.8	86.3	90.8	81	87.9
Power	$64\mu W$	$6.3\mu W$	$38.1mW$	$10.7\mu W$	$36\mu W$	$140\mu W$
FOM_W (pJ/step)	1.17	0.32	1.46	0.76	0.098	0.173
FOM_S (dB)	166.4	182.8	157.1	173.5	172.4	174

$FOM_W = \frac{Power \cdot T_{conv}}{2^{(SNR-1.76)/6.02}}$. $\quad FOM_S = \text{SNR} + 10 \cdot \log\frac{1}{\text{Power} \cdot \text{T}_\text{conv}}$.
SE: single-ended, PD: pseudo-differential, FD: fully-differential.
IADCx: x-order Incremental ΔΣ ADC, ΔΣx: x-order ΔΣ ADC.
SAR: SAR ADC [16].

Table 1-3: Design specifications of improved self-timed ADC

Specification	**Performance**
Technology	NXP 0.16μm 1P5M CMOS
Active Chip Area (mm^2)	<0.7
Supply Voltage (V)	1
Supply Current (μA)	lowest possible $<26\mu A$
Conversion Time (ms)	<1.5
Resolution (bits)	>16.5
SNR (dB)	>90
INL (LSB)	<1LSB w.r.t.16-bit
FOM_W (pJ/conv.-step)	lowest possible (<1.48)
FOM_S (dB)	highest possible (>164)

Then, the extension to a differential topology for the ZCB integrator was explored. It turned out that a fully-differential implementation was not possible in this project, due to the inability to bring the signal-dependent input-referred error of the integrator to an acceptable level that would permit to meet the linearity requirement of <1LSB w.r.t 16-bit. However, a pseudo-differential ZCB integrator was found not to be capable of meeting our linearity specification, but it was not implemented, mainly due to shortage in design time during this project. As a result, a single-ended implementation was decided to be utilized in this prototype as well.

Based on the noise analysis that has been developed, it was revealed that a 3^{rd}-order modulator is not necessarily going to help to fulfill the targets of this project, in a more energy-efficient way, compared to a 2^{nd}-order modulator. Also, due to an important implementation issue of the 3^{rd}-order CIFF topology when it is realized using ZCB integrators, the idea of extending to a 3^{rd}-order modulator was put aside. Using a second-order $\Delta\Sigma$ modulator, similar to the first prototype and resizing accordingly the two ZCB integrators of the loop-filter, the achievable resolution is 16.7-bit, while the achievable linearity is 1LSB w.r.t. 17-bit, based on simulation results. To achieve this the modulator is operating for 1000 incremental cycles, having a conversion time less than 1.01ms, while consuming less than $26\mu W$ from a 1V supply. As a result, the energy-efficiency was slightly improved and brought closer to the state-of-the-art designs of OTA-based $\Delta\Sigma$ ADCs.

1-4 Thesis organization

Apart from this introductory chapter, the rest of the thesis is organized as follows.

Chapter 2 contains a brief introduction of the working principle and system-level consideration of incremental $\Delta\Sigma$ ADCs, focusing on the noise behavior as a function of number of the number of incremental cycles and the order of the modulator. This chapter, also, provides a brief description of the circuit-level implementation of [1], focusing on the special circuit techniques and design choices that enable to demonstrate state-of-the-art performance among ZCB $\Delta\Sigma$ ADCs.

Chapter 3 tackles the extensive noise and linearity analysis of the most critical building block of a ZCB $\Delta\Sigma$ ADC: the first ZCB SC integrator which utilizes correlated level-shifting for linearity improvement. In this analysis, all the non-ideal effects of the circuit-level implementation are taken into account, resulting to a design-oriented noise estimation that is fairly accurate. Regarding the linearity estimation, it was observed that the analysis is not very successful to capture the dominant source of non-linearity, so a simulation-based design procedure was concluded to be suitable.

Chapter 4 discusses the accuracy limitations of the measurement setup that was designed for the characterization of the design in [1]. The updated measurement results for noise and linearity, along with an updated performance summary of the previous prototype are also presented.

Chapter 5 describes the design of the first integrator of the improved self-timed ZCB incremental $\Delta\Sigma$ ADC, after a broad design space exploration on the implementation of an improved ZCB ADC including the options of extension to a higher-order modulator and the realization of a fully-differential structure. The simulation results for noise and linearity of the designed integrator are presented in the end.

Chapter 6 presents all the implementation details of the improved self-timed ADC prototype, besides the design of the first integrator, followed by a description of the layout of the ADC. Finally, the top-level pre-layout and post-layout simulation results of the implemented ADC are attached, including a performance summary, along with a comparison with the other state-of-the-art CBSC/ZCB and OTA-based $\Delta\Sigma$ designs.

This thesis ends with a short summary of this thesis work in Chapter 7. Also, suggestions for future work and potential improvements are highlighted.

Chapter 2

System-level overview of Incremental $\Delta\Sigma$ ADC and description of previous prototype

Since this project is a follow-up of the previously proposed world's first self-timed Incremental $\Delta\Sigma$ ADC [1], it is instructional to briefly summarize the circuit techniques and design choices used in [1] that led to achieve high performance at state-of-the-art energy efficiency among the CBSC/ZCB designs. The impact of these choices will be clearly understood and quantified after the in-depth analysis of ZCB SC integrator, that is following in Chapter 3. The description of the first prototype follows after a brief overview of the working principle and system-level considerations in the design of Incremental $\Delta\Sigma$ converters, focusing on the noise and linearity behavior as a function of number of incremental cycles N and loop-filter order.

2-1 $\Delta\Sigma$ ADC: Incremental operation

$\Delta\Sigma$ ADC is the most-used architecture in applications that demand high resolution and accuracy. This is because their operation is not relying on precise analog elements, unlike their Nyquist rate counterparts, but employ simple analog blocks in order to achieve adequate performance. The obtained performance of $\Delta\Sigma$ ADCs stems from two aspects: First of all, the sampling of the input signals at a much higher rate than the bandwidth, which is called oversampling, and results in attenuation of the total in-band noise density. In theory, the obtained resolution increases by half a bit by doubling the oversampling ratio, which is defined as $\frac{f_s}{2BW}$. Second, the loop filter is moving the quantization error outside the signal band, which in the end it is filtered out by the decimation filter. This so-called noise-shaping results in much higher increase in resolution than 0.5 bits per doubling of OSR, which has been proven very attractive for implementation in CMOS technology; speed is being traded for resolution. In the end, the oversampled data are decimated (low-pass filtered and re-sampled) producing

the Nyquist-rate multi-bit output of the ADC. The theory and operation of these classical ΔΣ ADCs is extensively discussed in [17] and [18].

These classical ΔΣ A/D conversion schemes are utilized in applications where a running waveform needs to be digitized, for instance in telecommunications or audio applications. In these cases, the output spectral properties are important and the performance is quantified in terms of dynamic range (DR) or Signal-to-noise ratio (SNR). In contrast, in sensor applications the underlined signals have narrow bandwidth and extremely accurate sample-by-sample mapping is necessary. Besides the high resolution, which is typically expressed in Effective-number-of-bits (ENOB), low offset and gain errors and very high linearity, which is characterized by Integral non-linearity (INL), are demanded under the stringent restriction of low power consumption [19]. In this case, ΔΣ converters can be utilized in single-shot fashion: The ADC is powering up, performs a single conversion and then is powers down again. This special case of ΔΣ converters tailored for Instrumentation and Measurement (I&M) applications are called Incremental ΔΣ ADCs, whose a block diagram is shown in Figure 2-1. More detailed analysis on the concept, properties and design of Incremental ΔΣ ADCs can be found in [19], [20],[21], [22] and [23]

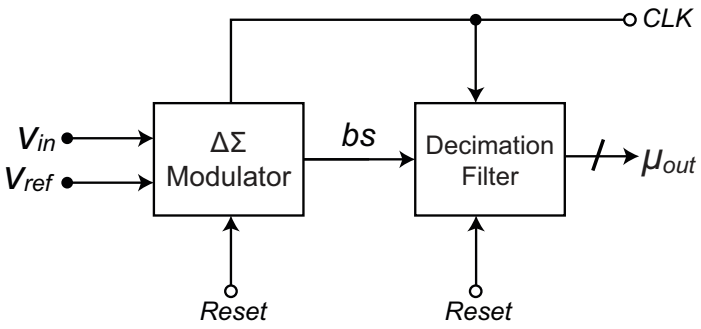


Figure 2-1: Block diagram of an Incremental ΔΣ converter.

The operation for a single conversion of an Incremental ΔΣ is as follows: First, all the memory elements of the modulator, i.e., the switched capacitor (SC) integrators of the loop filter, and the decimation filter are reset. Then, a fixed number of steps depending on the target resolution are performed and in each cycle the bitstream output of the modulator is determining the feedback signal of the loop filter. Also, the decimation filter which has much simpler implementation compared to free-running ΔΣ ADCs, is working in parallel with the modulator and filters out the quantization noise and produces the output of the ADC without creating significant timing overhead. Typical implementations of the decimation filters of an k-order ΔΣ are sinc^k filters [20] or a matched filter [24] (or so-called cascade-of-integrators [20]) which has the same impulse response with the analog loop-filter. Another alternative, when periodical noise needs to be suppressed is a higher-order sinc^m filter [20].

The operation of an Incremental ΔΣ converter is instructive to be described using time-domain analysis and derivation of the output signal of the integrators of the loop filter at cycle n. For example, this is demonstrated for the 2^{nd}-order Boser-Wooley structure with an input feed-forward path, which was used in [1] and shown in Figure 2-2.

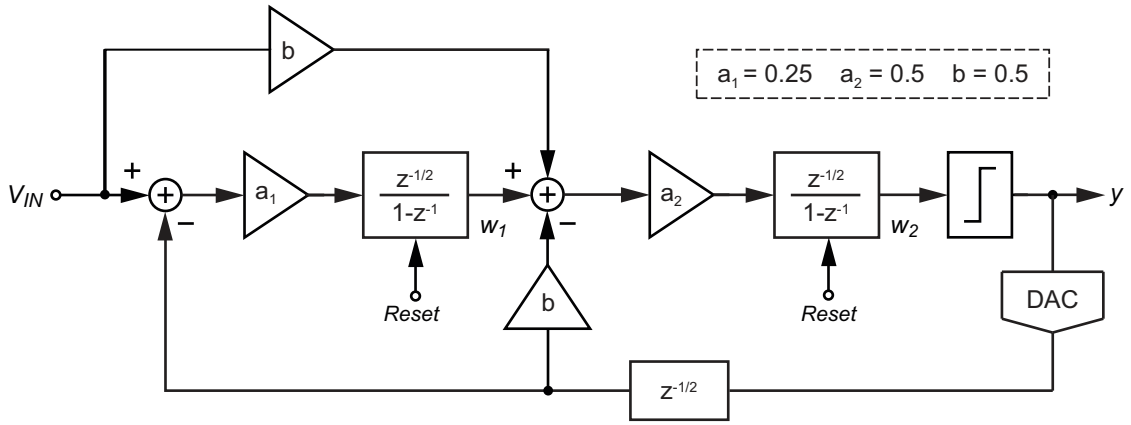


Figure 2-2: Block diagram of second-order Boser-Wooley modulator with input feed-forward path [25].

As noticed before, both integrators are reset before each conversion and the input signal is assumed constant throughout the conversion. The output samples of the two half-delay integrators at the sample time index i are given by

$$w_1[i] = w_1[i-1] + a_1 V_{\text{in}} - a_1 y[i] V_{\text{ref}} \tag{2-1}$$

$$w_2[i] = w_2[i-1] + a_2 w_1[i] + a_2 b \cdot V_{\text{in}} - a_2 b \cdot y[i] V_{\text{ref}} \tag{2-2}$$

where $y[i]$ is the output of the single-bit quantizer and V_{ref} is the reference voltage of the ADC. These two expressions can be rearranged and the non-iterative outputs of the two integrators after the n-th iteration are

$$w_1[n] = a_1 n \cdot V_{\text{in}} - a_1 \sum_{i=1}^{n} y[i] \cdot V_{\text{ref}} \tag{2-3}$$

$$w_2'[n] = \left\{ a_1 a_2 \sum_{i=1}^{n} i + a_2 b \cdot n \right\} \cdot V_{\text{in}} - \left\{ a_1 a_2 \sum_{i=1}^{n} \sum_{j=1}^{i} y[j] + a_2 b \sum_{i=1}^{n} y[i] \right\} \cdot V_{\text{ref}} \tag{2-4}$$

Hence, by operating the modulator for N cycles, we can derive the ratio of the input voltage over the reference μ_{out} by re-arranging the expression (2-6), as follows

$$\frac{V_{\text{in}}}{V_{\text{ref}}} = \frac{2a_1}{a_1 N(N+1) + 2b \cdot N} \left\{ \sum_{i=1}^{N} \sum_{j=1}^{i} y[j] + \frac{b}{a_1} \sum_{i=1}^{N} y[i] \right\} + \frac{2}{a_1 a_2 N(N+1) + 2a_2 b N} w_2[N] \tag{2-5}$$

where $w_2[N]$ is the final value of the second integrator. The first term of the previous expression is the estimation of the input voltage and the second term is representing the quantization error. It is readily clear that the estimation of the input can be retrieved by a simple digital

filter which processes the output bitstream $y[i]$ of the analog modulator. This filter is the previously mentioned matched decimation filter. On the other hand, the quantization error

$$Q_{err} = \frac{2}{a_1 a_2 N(N+1) + 2a_2 bN} \cdot w_2[N] \cdot V_{\text{ref}} \tag{2-6}$$

determines the achieved resolution of the ADC; For an ADC with k-bit ENOB the quantization error should be upper-bounded by the V_{LSB} of k-bits: $V_{\text{LSB}} = \frac{2V_{\text{ref}}}{2^k}$. Thanks to the stability of the modulator, $w_2[N]$ is bounded by $[-V_{ref}, +V_{ref}]$, but in practical case this cannot be used for an accurate estimation, as the exact output swing of the second integrator at the last cycle is not known. However, the converter can be simulated using a MATLAB script for the whole input range, as done in [25] and a much clearer picture of the quantization error behavior can be obtained.

2-2 Noise and linearity performance as function of Number of cycles N

The achievable resolution of an Incremental ΔΣ ADC is limited by two uncor related noise processes: quantization noise of the ADC and intrinsic (thermal) noise generated by the building blocks of the modulator (e.g. switched capacitor integrators). Most often, resolution is quantified using the Effective-number-of-bits (ENOB) which is defined as

$$\text{ENOB(bits)} = \left(20 \cdot \log_{10} \frac{\text{A}}{\delta_{rms}} - 1.76\right) \Big/ 6.02 \tag{2-7}$$

where δ_{rms} is the standard deviation of the decimated outputs and A is the stable input range of the converter. An equivalent definition comes from the restriction that for an ENOB-bit converter, the maximum error has to be lower than one LSB voltage: $V_{\text{LSB}} = \frac{\text{A}}{2^{\text{ENOB}}}$, as stated in [23].

Therefore, it is crucial to balance thermal and quantization noise properly in order to arrive at a power efficient design. On one hand, the quantization noise depends on the order of the modulator's loop filter, as well on the number of cycles N; Higher order loop filter shapes the quantization noise more aggressively, leading to lower number of cycles N for a target ENOB, considering only quantization noise. This seems beneficial, as operating for fewer cycles means lower conversion time and apparently lower energy per conversion. On the other hand, thermal noise exhibited by the integrators of the loop filter manifests itself as variance of the decimated output, but its highly attenuated, thanks to oversampling and noise shaping: The input-referred noise power of the first integrator is suppressed by a factor of N, while the input-referred noise of the second integrator is suppressed by a factor N^2 and so on [12]. Thus, in a proper design, since $N \gg 1$, thermal noise is typically dominated by the noise of the first integrator and the variance of the decimated output, considering only thermal noise, is equal with the input-referred noise power of the first integrator attenuated approximately by a factor N. It is evident that by operating for higher number of cycles, averaging attenuates thermal noise and this could be exploited in order to relax the specification of the input-referred noise of the first integrator. Also, since lowering input-referred noise power of an integrator

$\overline{v^2_{n,in,INT}}$ is associated with higher power consumption, it seems beneficial to exploit the trade-off between N and $\overline{v^2_{n,in,INT}}$ in order to arrive in an optimal design in terms of power efficiency. Therefore, it is suggested to achieve a ratio of 50% : 50% between the two noise sources, although most often thermal noise is slightly dominant [24].

In order to quantify the noise performance as a function of N, the minimum N that is required in order to achieve a specific ENOB is estimated for first, second and third order loop filter, taking into account only quantization noise. This is done, having as basis the analysis presented in [23], where the following expressions for ENOB of an Incremental $\Delta\Sigma$ ADC were derived.

- For a 1st order Incremental $\Delta\Sigma$ modulator: $\text{ENOB}_1 = \log_2(N-1) \simeq \log_2 N$ [23].
- For a 2nd order Incremental $\Delta\Sigma$ modulator: $\text{ENOB}_2 = \log_2(A \cdot \frac{N \cdot (N-1)}{2!})$ [23]. This is approximated by $\text{ENOB}_2 \simeq 2 \cdot \log_2 N + \log_2 A - 1$, where A is the normalized stable input range of the modulator with respect to the reference voltage V_{ref}, which in this case is limited to 0.75. Thus, $\text{ENOB}_2 \simeq 2 \cdot \log_2 N - 1.415$.
- For a 3rd order Incremental $\Delta\Sigma$ modulator implemented with Cascaded Integrators, Feed-forward structure (CIFF) [20] [21]: $\text{ENOB}_3 = \log_2(A \cdot bc_1c_2 \frac{N \cdot (N-1) \cdot (N-2)}{3!})$, which is approximated by $\text{ENOB}_3 \simeq 3 \cdot \log_2 N + \log_2 A + \log_2(bc_1c_2) - 2.6$, where b, c_1, c_2 are the scaling factors of the integrators of the loop filter. For this 3rd order modulator, the normalized stable input range is limited to $A = 0.67$ and for practical values of the scaling factors [23], $\text{ENOB}_3 \simeq 3 \cdot \log_2 N - 6.6$. These expressions are visualized in Figure 2-3.

Furthermore, the decimated output variance due to thermal noise is dominated by the input-referred noise of the first integrator, as the effect of noise in preceding stages is strongly attenuated by the loop filter [17]. It was proven in [23] that the decimated output variance as a function of input-referred thermal noise power of the first integrator $\overline{V^2_{n,in,INT1}}$ is

$$\overline{V^2_{n,out,thermal}} = k \cdot \frac{\overline{V^2_{n,in,INT1}}}{N} \tag{2-8}$$

where k is a constant depending on the modulator's order and $k = 1, \frac{4}{3}, \frac{9}{5}$ for 1st, 2nd and 3rd order modulators, respectively. Thus, a simple estimation of the ENOB, considering only thermal noise can be done as

$$\text{ENOB}_{\text{thermal}} = \log_2\left(\frac{A}{\sqrt{k \cdot \frac{\overline{V^2_{n,in,INT1}}}{N}}}\right) \tag{2-9}$$

For example, the estimation of $\text{ENOB}_{\text{thermal}}$ is shown as a function of N in Figure 2-3, along with the achievable ENOB in case only quantization noise is taken into account for the two cases where the input-referred RMS noise of the integrator is $V_{n,in,INT1} = 100\mu V$ and $V_{n,in,INT1} = 400\mu V$.

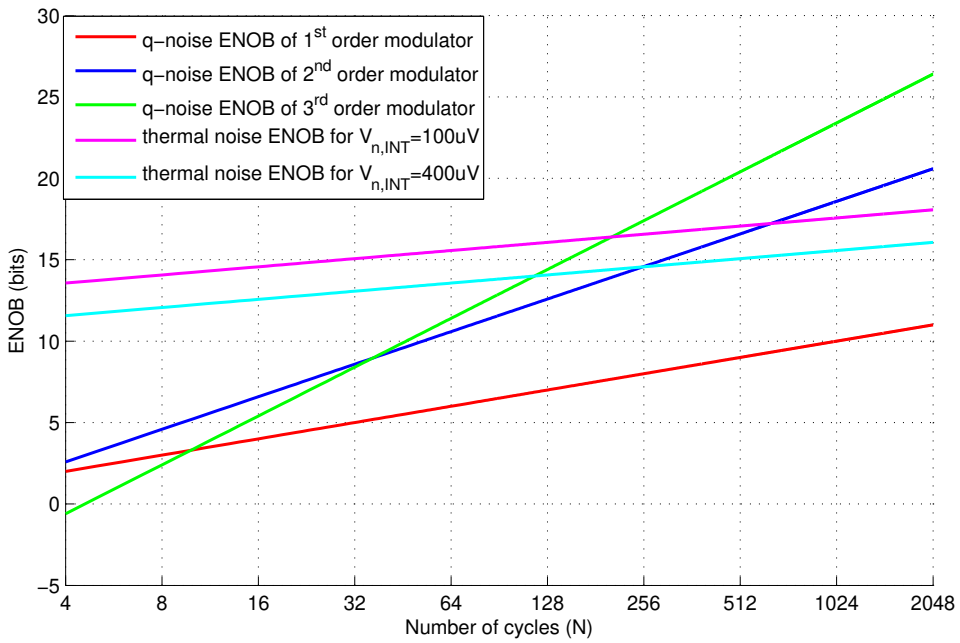


Figure 2-3: ENOB as a function of N considering only quantization noise or only thermal noise.

In Figure 2-3 the trade-off between quantization and thermal noise is clearly shown. Since the achievable ENOB, is always below the lowest of the two curves, for a specific value of N, ENOB is limited either by quantization noise (low N) or by thermal noise (high N). Since $\overline{V^2_{n,in,INT1}}$ is determining the height (but not the slope) of the estimation of $\text{ENOB}_{\text{thermal}}$, an optimal design is established for the combination of N and $\overline{V^2_{n,in,INT1}}$ for which the target ENOB is met, under minimum power consumption. A more accurate approach, is to estimate using MATLAB simulation the quantization noise power σ_q^2 of a modulator and the decimated output thermal noise power $\overline{V^2_{out,thermal}}$ and then calculate the ENOB based on the (2-7), using

$$\delta_{\text{rms}} = \sqrt{\overline{V^2_{out,thermal}} + \sigma_q^2}. \tag{2-10}$$

The value of δ_{rms} is in essence the output-referred noise of the ADC, which is equal to its input-referred noise.

The achievable linearity of the Incremental ΔΣ ADC that is using a single-bit quantization is not suffering from the non-linearity induced by the feedback DAC and is, essentially, limited by the signal-dependent input-referred error of the first integrator **[12]**. Thanks to the noise shaping of the loop-filter, the contribution of the succeeding integrators is highly suppressed [17]. In an OTA-based design, the signal dependency of the input-referred error of the integrator comes from settling error, slewing and finite DC gain of the OTA and DC gain variation with the output swing. Specifically, OTA's finite DC gain and gain variation are a recognized as the most critical error sources [11] [12]. In any case, the input-referred error of the integrator has to be designed carefully in order to achieve the target linearity.

2-3 Description of the first prototype of self-timed IΔΣ ADC

2-3-1 Top-level description and self timed operation

The first prototype of self-timed Incremental ΔΣ ADC [1] was employing a second-order modulator with input feed-forward path, which is shown in Figure 2-2 operating for $N = 500$. The most important merit of this topology is that the first integrator only processes quantization error (no signal component) and thus its output swing is stabilized and limited (around 0.3V)[25]. As a result, the design of the first integrator regarding its linearity performance is relaxed, due its lower output swing.

The two integrators of the modulator are operating in a ping-pong fashion; while the one integrator is sampling, the other one is integrating, and vice versa. The most important building block is the zero-crossing-based SC integrator, whose basic operating principle was briefly described in Chapter 1. A block diagram of the modulator used in [1], which employs two Zero-crossing based integrators and a clocked comparator is shown in Figure 2-4. In this implementation, the feedback signal of the second integrator is applied during the sampling phase Φ_2 of the integrator, while for the first integrator during its charge-transfer phase Φ_2. This choice was preferred as this scheme doesn't increase power consumption and doesn't introduce extra kT/C noise at the input of the first integrator.

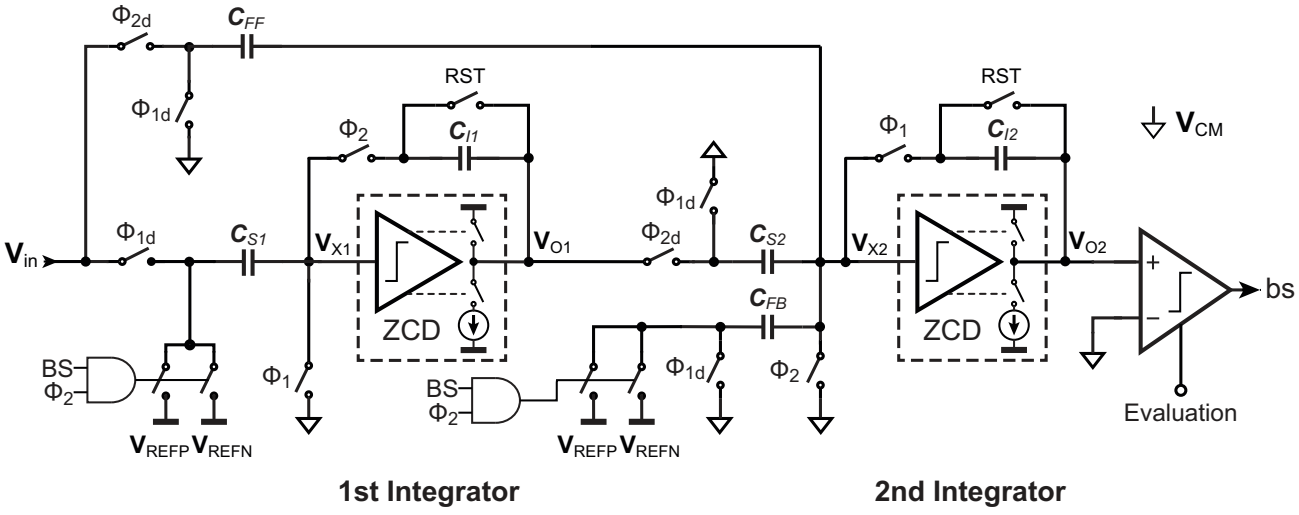


Figure 2-4: Block diagram of the self-timed IΔΣ modulator used in [1].

As was already pointed out in Chapter 1, the knowledge of the completion of the charge transfer process is inherently available, in the operation of a ZCB integrator. Based on this knowledge, an asynchronous controller can be built in order to control the sampling and charge-transfer phases of the two cascaded half-delay integrators, i.e. generate the two non-overlapping clock signals Φ_1 and Φ_2 (and the delayed versions of them), under the assumption that the duration of the sampling phase is never exceeding the charge-transfer phase. In this case, this event-based controller is a simple asynchronous state machine with two states (Φ_1 and Φ_2), which are triggered by each other by the completion signals of the charge transfer. This process is illustrated in Figure 2-5.

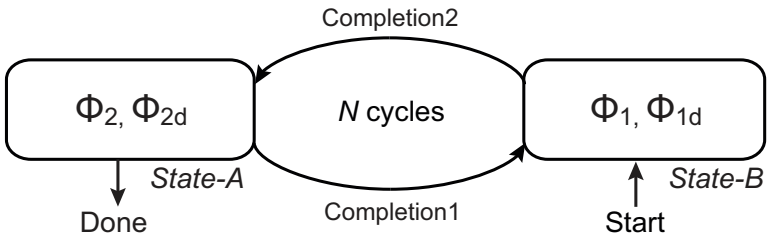


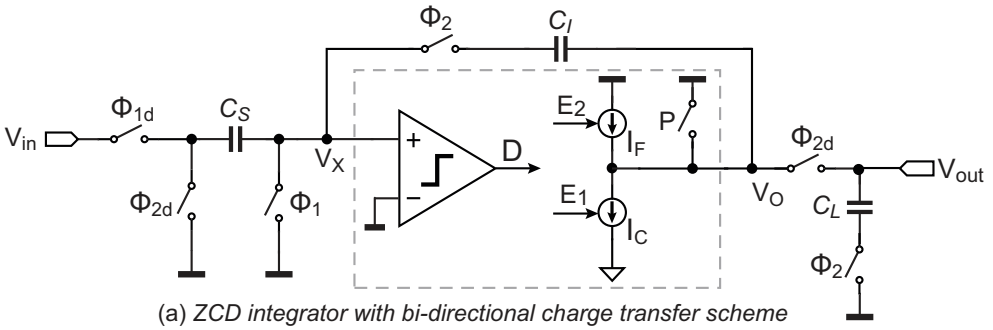
Figure 2-5: Asynchronous state machine for the generation of the self-timed clock signals [25].

As a result, the timing of one conversion is as follows: Initially, the ADC is powered down waiting for a startup control signal that triggers the conversion. Once the startup pulse is present, reset of the two integration capacitors C_{I1} and C_{I2} is performed and after the reset pulse the state machine gets in Φ_1 state. In this state, the first integrator is sampling the input signal and the second integrator is performing charge transfer. Once the charge transfer of the second integrator is completed, the state machine is triggered by the completion signal to Φ_2, when the first integrator is performing charge transfer and the second is sampling the output of the first. When the first integrator is completing the charge transfer, Φ_1 state is triggered again and this process continues for a predefined number of cycles N of the modulator. The completion of the conversion is detected by keeping track of the number of performed cycles and comparing with N. Upon the completion of the conversion, the state machine is generating a control signal ($Done$) and the modulator powers down.

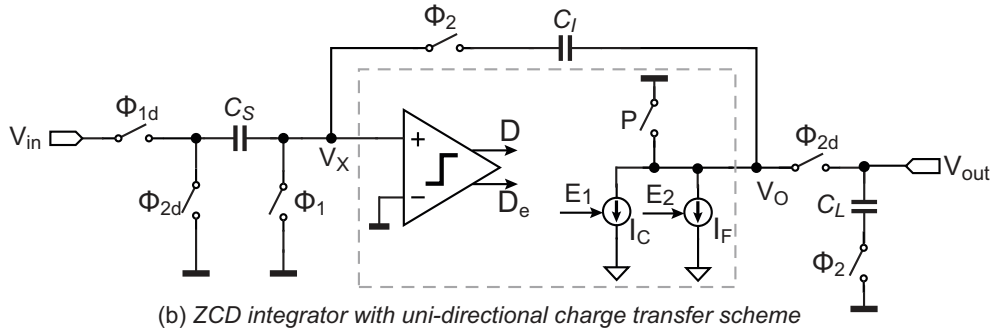
2-3-2 ZCB SC integrator: Coarse-fine charge transfer mechanism

As briefly introduced in Chapter 1, the Zero-crossing based switched-capacitor integrator is the most important building block of the self-timed ADC. Therefore, it is crucial to recognize and mitigate the non-idealities of the integrator, in order to achieve the needed accuracy of integration. The static accuracy of the ZCB integrator is dominated by the overshoot at the virtual ground node V_X, due to the finite response time of the ZCD. The constant part of the overshoot results to offset, which is most often (to some extent) tolerable, while the signal-dependent component creates non-linearity. Specifically, the overshoot at V_X is proportional to the delay time of the ZCD and the magnitude of the charging current source. Moreover, if the integration is needed to be faster, the ramp-rate will be necessarily steeper, leading to a larger error. It is, therefore, straightforward that a coarse-fine charging scheme is necessary in order to decouple accuracy from speed and enhance the accuracy of ZCB integrator. In principle, this coarse-fine scheme can take the form of either bi-directional [2] or uni-directional charge transfer [7], as can be seen in Figure 2-6. In [1] the uni-directional charge transfer scheme was implemented, because of its advantages over the bi-directional scheme, that will become clear from the following analysis of the operation of both schemes.

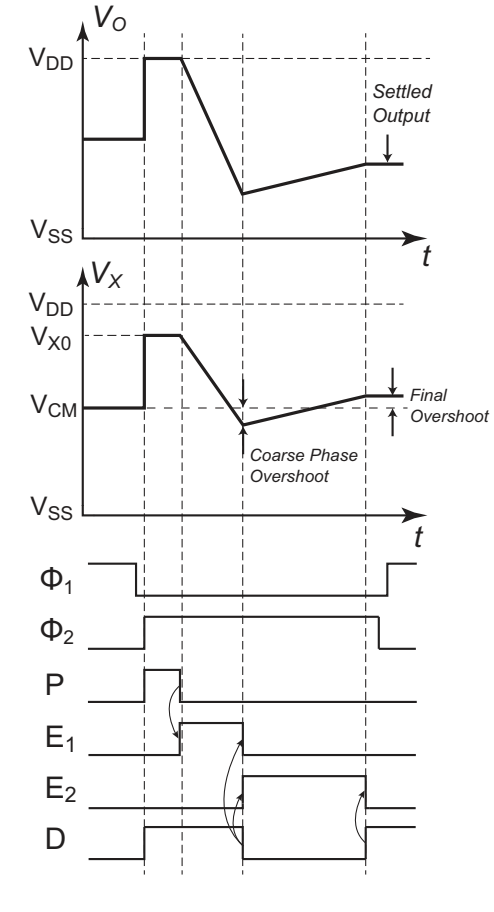
The operation of both alternatives of ZCB SC integrators' charge transfer (Φ_2) begins with a short preset phase (P), when the output node is shorted to V_{DD}. Thus, the initial



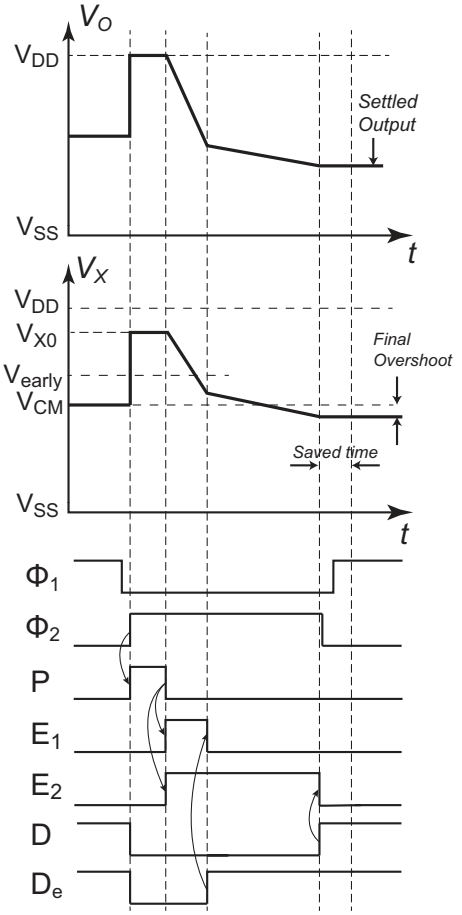
(a) *ZCD integrator with bi-directional charge transfer scheme*



(b) *ZCD integrator with uni-directional charge transfer scheme*



(c) Waveforms *of bi-directional charge transfer*



(d) Waveforms *of uni-directional charge transfer*

Figure 2-6: Dual-rate ZCB integrator implementation alternatives.

condition of V_X, due to charge conservation, is

$$V_{X0} = \frac{(V_{DD} - V_{IN})C_S + (\frac{3}{2}V_{DD} - V_O{}')C_I}{C_S + C_I} \tag{2-11}$$

where $(V_{IN} - V_{CM}) \cdot C_S$ is the sampled input charge during the sampling phase (Φ_1). The preset level of V_X depends on the sampled charge and the integrated charge of the previous cycle $(V'_O - V_{CM}) \cdot C_I$, and, in order to ensure correct operation, V_{X0} needs to be higher than V_{CM}. This condition limits input and output swings, as the condition $V_{X0} \geq V_{CM}$ is equivalent to $\frac{V_{IN} - V_{CM}}{V_{DD} - V_O{}'} \geqslant \frac{C_I}{C_S}$. Right after preset phase, the coarse charge transfer phase follows, while the nodes V_O and V_X ramp down rapidly, as can be seen in the waveforms of Figure 2-6.

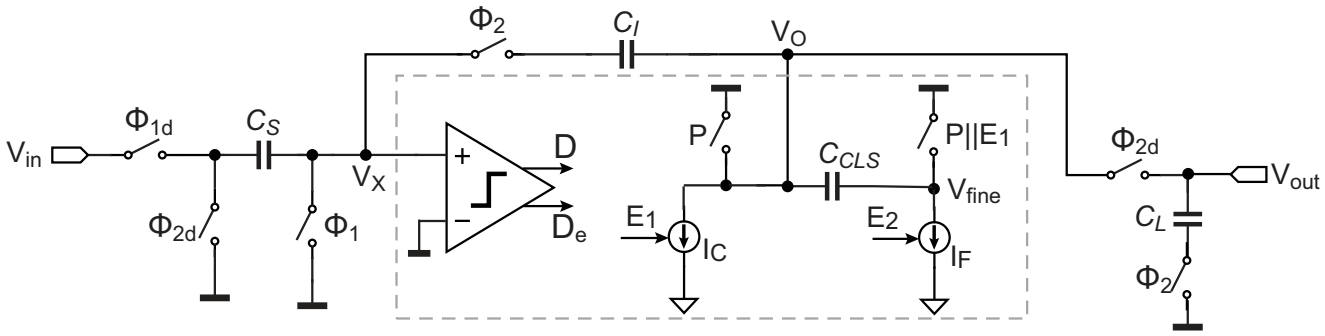
The difference between the two alternatives is the strategy for switching from coarse to fine phase. For the bi-directional scheme, the coarse surrent source is active, until the ZCD detects the virtual ground $V_X = V_{CM}$, when the coarse current source is switched-off. Since the ZCD has a finite response time, there is coarse phase overshoot on V_X, which is then corrected by turning-on the fine current source I_F, which has opposite polarity and much lower magnitude than I_C . During the fine charge transfer phase, the nodes V_O and V_X ramp up, with relatively low ramp rate, until the ZCD detects again the virtual ground. Because, $I_F \ll I_C$ the final overshoot is relatively low.

In contrast, the uni-directional scheme is based on the concept of early-threshold detection, so is based on the assumption that the ZCD is capable of detecting also the crossing of (another) slightly higher level than V_{CM}, V_{early}. Upon the level crossing of V_{early}, the transition from coarse to fine phase is triggered, by switching-off I_C. During fine phase, I_F which has the same polarity with I_C, ramps down V_O and V_X until the moment that the virtual ground is detected. At the moment of the virtual ground detection, I_F is switched-off and the charge transfer is completed. In both cases, the coarse and fine phase duration are signal dependent.

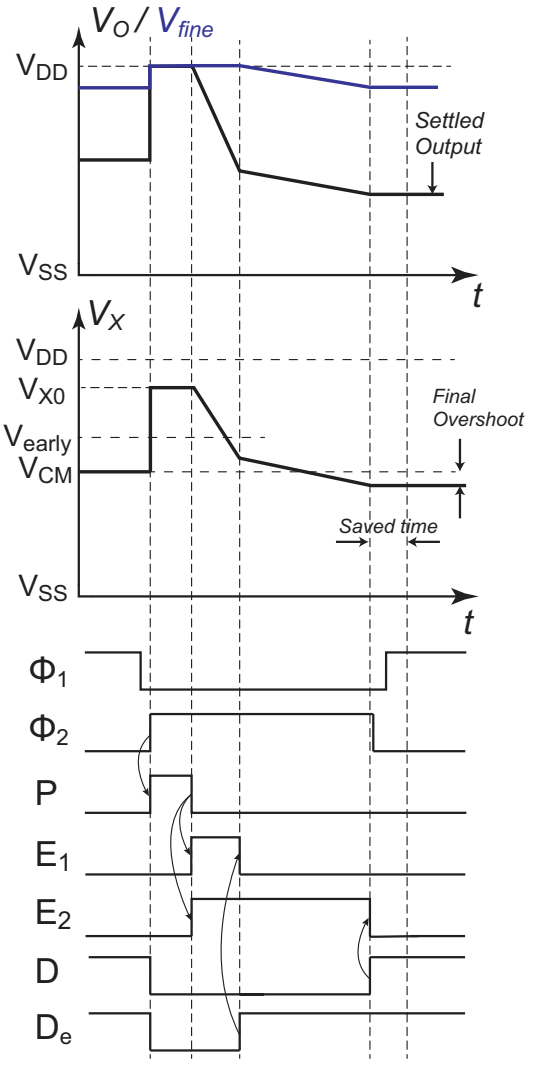
As a result, the uni-directional charge transfer scheme is inherently capable of achieving similar virtual ground accuracy with the bi-directional scheme, while operating for shorter time, because of the gradual reach of the virtual ground, instead of recovering from a potentially large overshoot. Moreover, the energy consumption is lower, because the successive charging and discharging of the capacitive network is avoided.

2-3-3 ZCB integrator: Correlated level shifting

So far, in the analysis of the ZCB integrator, we are dealing with ideal current sources and ZCD and therefore, there is no mechanism that is creating a signal dependent component on the overshoot of V_X has been identified. In reality, for example, current sources have finite output impedance, leading to variation of the ramp rate. Consequently, the fine phase overshoot of the ZCB integrator will be signal dependent, due to the ramp-rate variation of fine phase, even if ZCD has constant delay. Furthermore, the ZCD is a continuous time comparator, whose response time is ramp rate dependent [2]. These two effects have been recognized to limit the linearity of the ZCB integrator [25][8], leading to the conclusion that in order to minimize the signal-dependent error the signal dependency of the current I_F has to be minimized and the delay of the ZCD has to be minimized and stabilized.



(a) Uni-directional ZCB SC integrator with Correlated level shifting



(b) Waveforms *of uni-directional charge transfer with CLS*

Figure 2-7: ZCB integrator employing Correlated level shifting.

The current source induced non-linearity of zero-crossing based circuits, can be effectively reduced by utilizing the correlated level-shifting (CLS) technique, as introduced in [26]. The essence of this technique is the removal of the dependence of the swing of the fine current source from the output voltage of the integrator, by capacitively coupling the output of the current source with V_O, using a level-shifting capacitor C_{CLS}, as shown in Figure 2-7. When CLS is adopted in ZCB circuits, the operation is not altered and the operation of the ZCB integrator with uni-directional charge transfer of Figure 2-6 is visualized in Figure 2-7. During preset, both the output node V_O and the fine current source output node V_{fine} are pulled to V_{DD}. Next, during the coarse charge transfer phase (E_1), V_O is ramping down, while V_{fine} remains shorted with the supply until the beginning of the fine phase. During the fine phase (E_2), V_O and V_{fine} are slowly ramping down until the virtual ground is detected by the ZCD. Because, the ramp rate during the fine phase is relatively low, the swing of the fine current source is very small. Interestingly, V_{fine} follows the same waveform in every cycle, which is independent of the output voltage of the integrator. Moreover, the swing of V_{fine} is exactly the same (assuming constant ZCD delay), under the assumption that the coarse phase overshoot is signal-independent. This leads to stabilization of fine charging current waveform in every cycle (independent of V_O), which results to absolutely constant final overshoot at V_X. However, the exact swing of the fine current source is a function of the ZCD delay as well, which is slightly ramp-rate dependent in practice. As a result, the delay of the ZCD should be designed to be signal-independent and this is possible in practice by minimizing the ramp-rate variation during the fine phase.

Furthermore, the limited swing of V_{fine} which is always close to V_{DD} is creating the possibility to utilize well-known transistor-level design techniques that increase the output impedance of a current source but need larger voltage headroom, for instance use a cascode current source. The utilization of correlated level shifting in a ZCB SC integrator is greatly beneficial and almost cost-free, as the only penalty that is is associated with it is the slightly increased power consumption and timing overhead during the coarse charging phase due to the increased load.This is happening because C_{CLS} is appearing as extra load at the output of the integrator during the coarse phase.

2-3-4 Circuit-level implementation details

In order to complete the overview of the first prototype of self-timed Incremental ΔΣ ADC [1], a brief summary of the circuit level implementation of the critical blocks of the ZCB SC integrator is presented. Here, the gated current sources and zero-crossing detector implementation are briefly discussed and their designed parameters are outlined. Also, the design choices regarding the capacitors and sizing of the switches of the ZCD integrator are completing this overview. The effect of these design choices in the performance of ZCB integrator is not tackled here, but will be made clear with the analysis that is following in Chapter 3.

First of all, the coarse current source is implemented with a single transistor, as can be seen in Figure 2-8, biased with a simple current mirror. The unit element sizing was $1\mu m/10\mu m$, biased to conduct approximately $100nA$ and the coarse current is programmable, as $k = \{10, 20, 30, ...50\}$ unit elements can operate in parallel. The coarse current varies thus from $I_C = 1\mu A$ to $I_C = 5\mu A$ and its output impedance was simulated to be $R_{out,coarse} = 800M\Omega$ at low frequencies. The fine current source is implemented with a cascoded transistor current source, sized as shown in Figure 2-8, biased as such to conduct approximately

$I_F = 100nA$. The output impedance of the fine current source was simulated to be approximately $R_{out,fine} = 38G\Omega$ at low frequencies. The gating of both current sources was implemented with a series switch, as this solution provides the fastest switching among all alternatives [8].

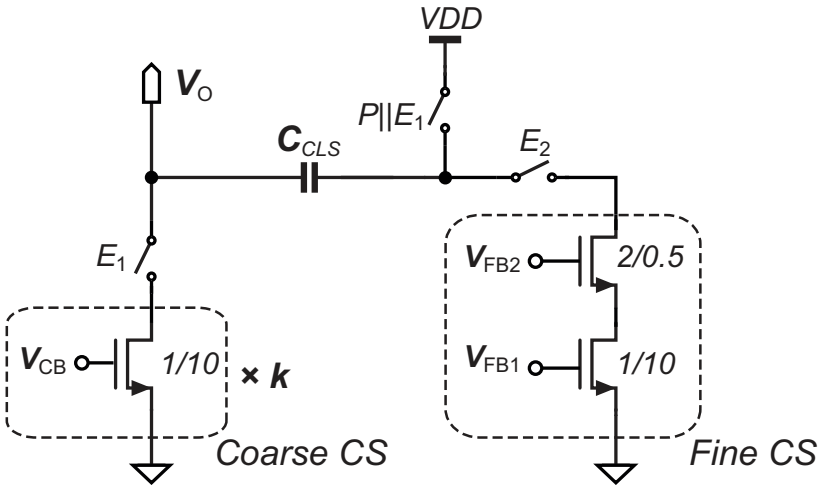


Figure 2-8: Gated current sources implementation in [1].

Next, the Zero-crossing detector, being a continuous time comparator, was implemented with a cascade of a low-noise autozeroed inverter-based preamplifier followed by a wideband crossing detector, as visualized in Figure 2-9(a). Auto-zeroing was utilized primarily to control the common mode voltage of the inverter preamp, but also because of the immunity to supply noise that is provided and attenuation of the flicker noise. The preamplifier is autozeroed during the sampling phase of the ZCB integrator, specifically during the fine charge transfer phase of the other ZCB integrator. Furthermore, the early-threshold detection capability was implemented, by level-shifting the output voltage of the preamplifier V_{int}, by means of a series level-shifting capacitor C_{off}, that is precharged accordingly (to V_{off}) during the preset phase of the ZCB integrator, as can be seen in Figure 2-9(b). The generation of V_{off} was done on-chip using a simple diode voltage reference, but also can be provided off-chip. Finally, the ZCD parts are powered down, using current starving switches, during the periods in time in which they are not necessary, in order to save power.

The design parameters of the ZCD that are critical for the noise and linearity performance are the maximum transconductance of the preamplifier ($g_{m,tot}$), preamp's time constant (τ), the preamplifier's response time during the fine phase (t_I) and the band-limiting capacitor of the preamplifier, which is used to control its response time and time constant. Last but not least, the current consumption of the preamplifier is of great interest. These parameters are summarized for both integrators of the modulator in Table 2-1.

Finally, the capacitor values in the implementation of both ZCB integrators are summarized in Table 2-2. Also, the switches were implemented by a single NMOS transistor, except from the modulator's PMOS feedback switches controlled by $\overline{bs}$ and the minimum length ($0.16\mu m$) was used for all. The designed widths of all switches of both integrators was $0.8\mu m$, except from the modulator's feedback switches and the switches close to virtual ground of the integrators towards the integration capacitor. The latters' width was $0.4\mu m$, while the NMOS

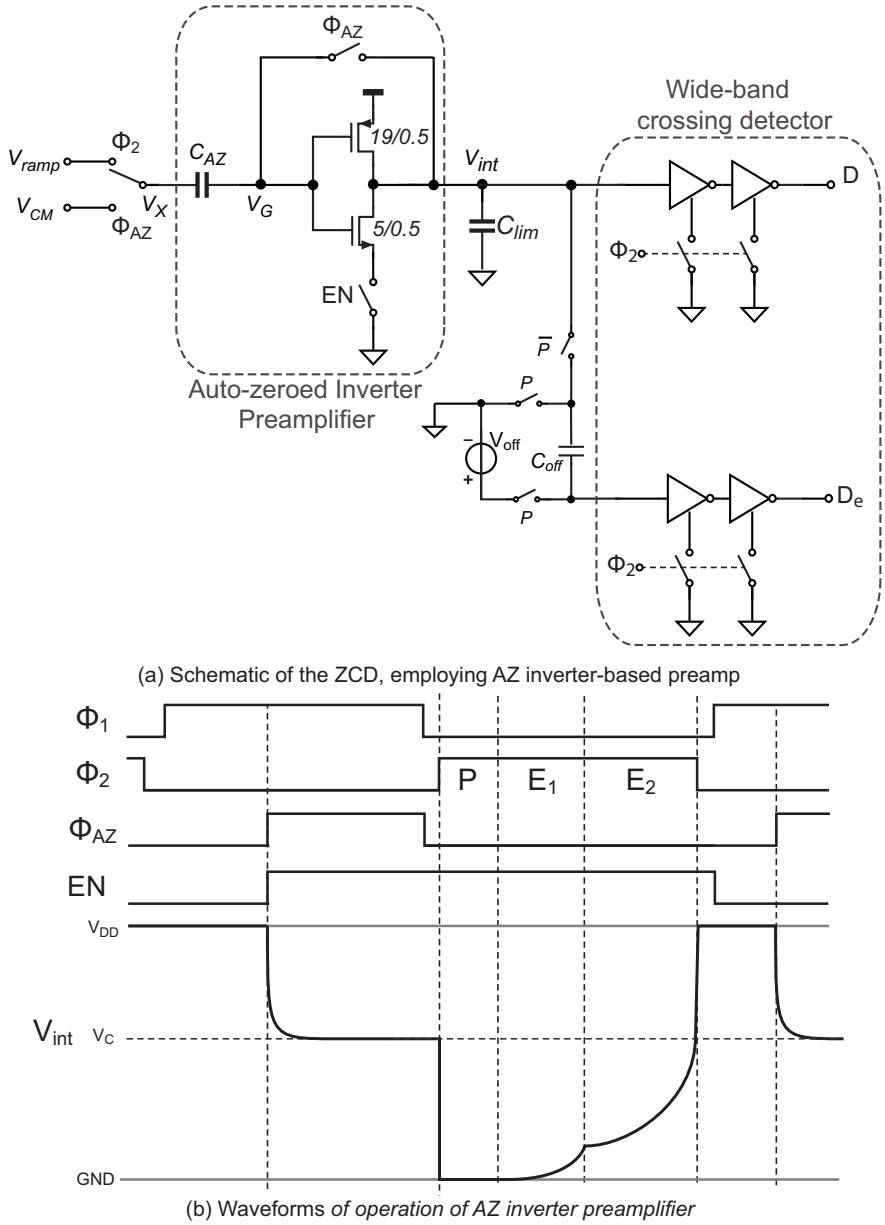


Figure 2-9: Circuit diagram and operation of the ZCD in [1].

feedback switches were $1.2\mu m$ and PMOS feedback switches $2.4\mu m$ wide. The driving voltage of switches (except from feedback switches) was boosted to around 1.85V (higher than supply voltage V_{DD}), using clock boosters. The on-resistance of the $0.8\mu m$ switches was simulated to be $R_{on} = 1.2k\Omega$, the on-resistance of the $0.4\mu m$ switch was $R_{on} = 2.1k\Omega$. For the feedback switches, $R_{on,NMOS} = 800\Omega$ and $R_{on,PMOS} = 890\Omega$.

Table 2-1: Design parameters of the inverter-based preamplifiers of the ZCDs in [1]

Parameters	1st Integrator	2nd Integrator
Peak bias current I_0	9.03μA	2.75μA
Maximum transconductance $g_{m,tot}$	135μA/V $\times$ 2	40μA/V $\times$ 2
Time constant τ	75ns	75ns
Response time t_I	65ns	50ns
Band-limit capacitor C_{lim}	200fF	55fF

Table 2-2: Capacitor values used in ZCB integrators in [1]

Capacitor	1st Integrator	2nd Integrator
Sampling capacitor C_S	500fF	200fF
Integration capacitor C_I	2pF	400fF
Correlated level shifting capacitor C_{CLS}	400fF	400fF
Feedback capacitor C_{FB}	—	200fF
Feed-forward capacitor C_{FF}	—	200fF

2-4 Summary

This chapter started with a short presentation of the system-level considerations in the design of an Incremental ADC, examining noise and linearity. Next, the design techniques that were utilized in the previous design, such as the use of a uni-directional coarse-fine charge transfer and correlated level-shifting and design choices, including the implementation of current sources and ZCDs were briefly reviewed. The impact of all the aforementioned design choices on the performance of the ZCB SC integrator will be examined in Chapter 3, where all the performance trade-offs in the design of the ZCB integrator will be revealed.

Chapter 3

Noise and linearity analysis of ZCB SC integrator with CLS

The purpose of this chapter is the analysis of the noise and linearity of a ZCB SC integrator with CLS. After an overview of the behavior of the ZCD with ramp inputs, the noise of the ZCB integrator is presented, including all the apparent noise contributors, followed by an estimation of the input-referred noise of the previous design [1] based on the developed noise model. Next, the circuit-level non-idealities of the ZCB integrator that harm its linearity performance are described, including an estimation of their contribution to the total input-referred signal-dependent error of the ZCB integrator. The presented noise and linearity analyses are similar to the analyses of a CBSC gain stage presented in [2] and [27] and is expanding the analysis of the ZCB SC integrator described in [25], taking into account more circuit-level non-idealities and phenomena.

3-1 Closer overview of ZCD response to ramp input

The first step of the analysis of the ZCB integrator is the description of the response of the ZCD to ramp inputs and the recognition of the error sources of the charge transfer process. For convenience, the schematic of the ZCB integrator with CLS of Figure 2-7 is repeated in Figure 3-1 and the underlying signals in its ramp response are shown in Figure 3-3.

The ZCD of Figure 3-1 is a continuous time comparator, consisting of a cascade of a low-noise autozeroed inverter preamplifier loaded by a bandlimiting capacitor C_{lim} and a wideband crossing detector stage, as noted in section 2-3-4. The inverter-based preamplifier can be modeled by an ideal transconductance amplifier, as can be seen in Figure 3-2.

The output response of the preamp fed by a step ramp input with ramp-rate M ($V_X = M \cdot t \cdot u(t)$) is

$$V_{int}(t) = M \cdot A_0 \Big[t - \tau(1 - e^{-t/\tau}) \Big] u(t) \qquad [2] \tag{3-1}$$

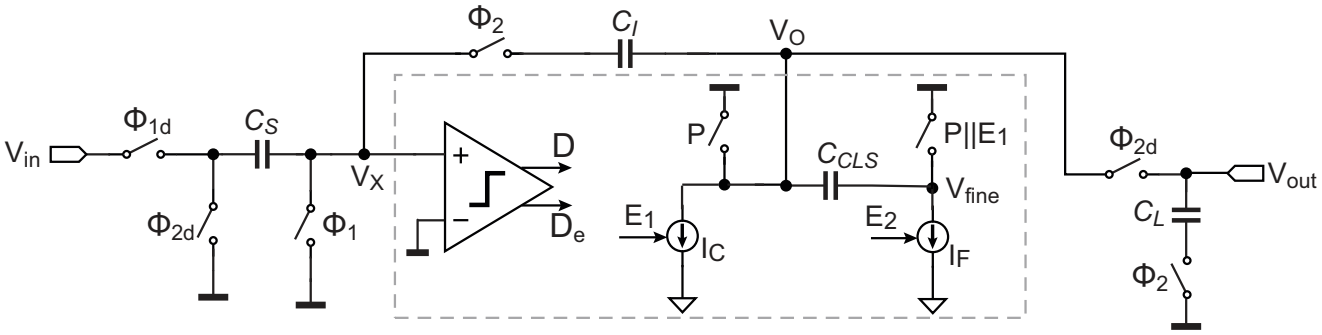


Figure 3-1: ZCB integrator employing Correlated level shifting.

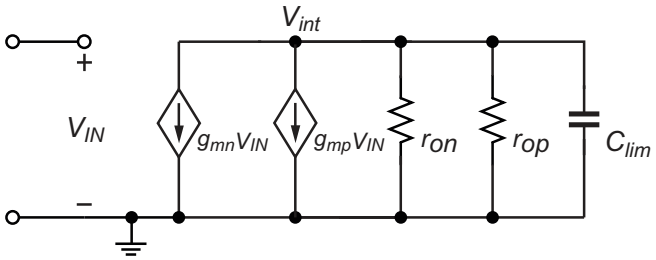


Figure 3-2: AZ Inverter-based preamp small-signal model during charge transfer phase.

where $A_0 = (g_{mn} + g_{mp}) \cdot (r_{on} \parallel r_{op})$ is DC gain of the preamplifier and τ is the preamp's output time constant $\tau = (r_{on} \parallel r_{op}) \cdot C_{lim}$.

The response of the ZCD is visualized in Figure 3-3 for a uni-directional charge transfer process.

Right after preset phase both coarse and fine current sources are turned on and V_X is ramping down with ramp-rate

$$M_{X,coarse} = M_{O,coarse} \cdot \frac{C_I}{C_S + C_I} = \frac{I_C + I_F}{C_L + C_{CLS} + C_I \parallel C_S} \cdot \frac{C_I}{C_S + C_I}. \tag{3-2}$$

The crossing of the early threshold V_{early} is detected by the ZCD after a small delay $t_{d,coarse}$ and the coarse current source is switched off. The coarse phase overshoot at V_X (from V_{early}) equal to $V_{X,OV,coarse} = M_{X,coarse} \cdot t_{d,coarse}$. Then, V_X is continuing the ramp roll-off with much lower rate

$$M_{X,fine} = M_{O,fine} \cdot \frac{C_I}{C_S + C_I} = \frac{I_F}{C_L + C_I \parallel C_S} \cdot \frac{C_I}{C_S + C_I}. \tag{3-3}$$

and the preamplifier's output V_{int} is rising according to (3-1), as shown in Figure 3-3. The output of the preamplifier is reaching the inverter's common mode voltage V_C with delay t_i, after V_X crosses V_{CM}, which is the moment when the input of the inverter V_G is crossing V_C due to autozeroing. This time t_i that the output of the preamplifier takes to reach the threshold V_C is defined as the preamplifier's response time. Because the wideband crossing detector is not responding instantaneously, there is a small delay t_c (after t_i), until the detection of the zero-crossing by the ZCD (rise of output D). With the rise of D, the fine current source is switching off with delay $t_d = t_i + t_c$ after the zero-crossing at V_X, creating a

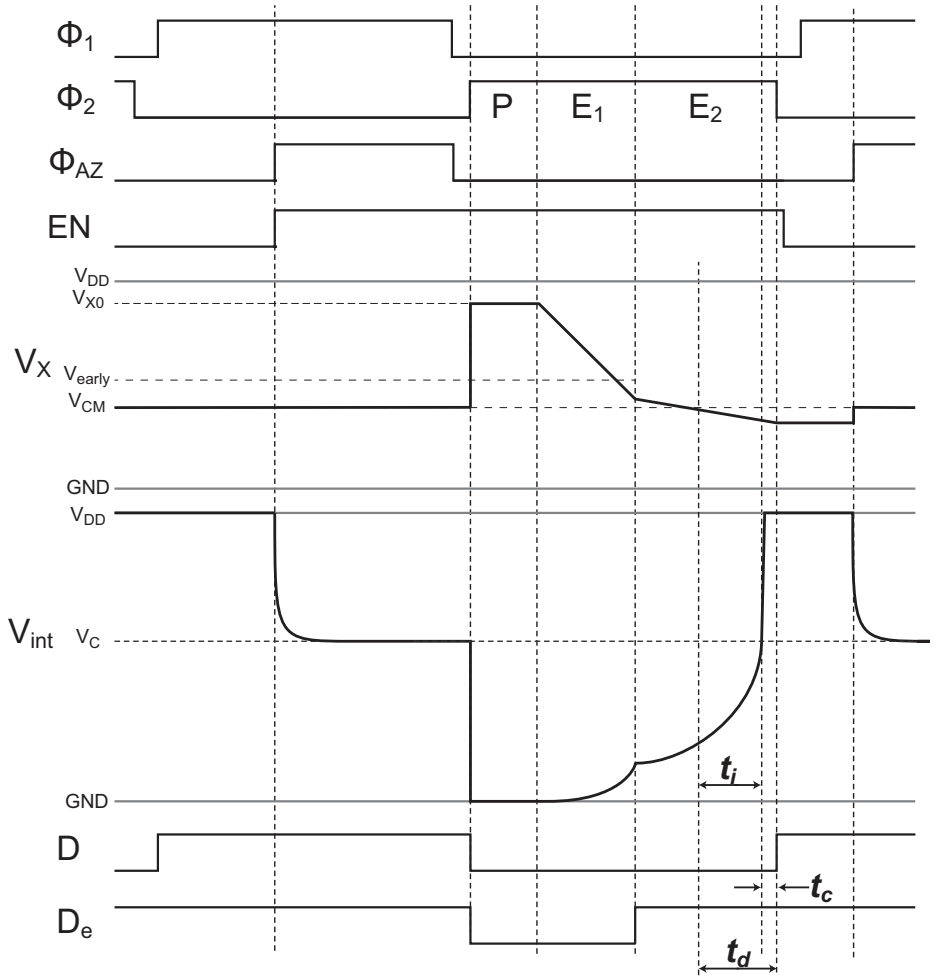


Figure 3-3: Waveforms of ZCD during charge transfer phase.

fine-phase overshoot at V_X equal to $V_{X,OV,fine} = M_{X,fine} \cdot t_d$. In the previous, the most often negligible delay of the digital control circuitry was not taken into consideration. The values of g_{mn}, g_{mp}, r_{on} and r_{op} are varying with V_X in the implementation with inverter preamp, but even in case they were constant it is impossible to solve (3-1) analytically to obtain an exact expression for the response delay t_i. In [28] the limiting behavior was considered in two extremes: when $t_i \ll \tau$, where the preamplifier is considered as an ideal $g_m C$ integrator and when $t_i \gg \tau$, where the preamplifier is operating in steady state. The preamplifier's response time in these two extremes is

$$t_i = \begin{cases} \dfrac{V_C}{M_{X,fine} \cdot g_{m,tot}} \cdot \dfrac{1}{r_{on} \parallel r_{op}}, & \text{for } t_i \gg \tau \quad (3\text{-}4) \\ \dfrac{2 \cdot V_C \cdot C_{lim}}{M_{X,fine} \cdot g_{m,tot}}, & \text{for } t_i \ll \tau \quad (3\text{-}5) \end{cases}$$

where $g_{m,tot} = g_{mn} + g_{mp}$. The preamplifier's response delay and output time constant are key parameters for the noise design of the ZCD preamp as will be revealed in subsection 3-2-2.

It is greatly important to note that since the modulator is operating on sampled data of integrators, only the error of the integrated voltage at the end of the charge transfer is important. Specifically, the noise power of the discrete-time integrated voltage at C_I is of interest, as far the noise performance is concerned. The input-referred noise power of the integrator will then be the noise power across the sampling capacitor due to sampling process (i.e. the well-understood kT/C_S) added to the to the noise power referred to the virtual ground node V_X at the end of the charge transfer. The latter component is equivalent to noise power across the sampling capacitor C_S at the end of the charge transfer phase [29]. As far as the static error is concerned, the input-referred error of the integrator is dominated by the final overshoot at node V_X, under the assumption that there is nothing adding error charge to C_I from the output side [2]. The overshoot at V_X, can be seen as equivalent to finite and non-linear open-loop gain of an OTA, in conventional OTA-based implementations of switched-capacitor integrators [28].

3-2 Noise analysis of the ZCB integrator

3-2-1 Non steady-state noise analysis

Because of the transient nature of ZCB circuits, the conventional steady-state noise analysis is not appropriate. For example, during the fine phase, variation of the charging current I_F due to noise, results in a random walk of the voltages across the capacitors of the feedback network of ZCB integrator of Figure 3-1, leading to noise that is growing larger with time. Also, the preamplifier of the ZCD does not necessarily reach steady-state (for $t_i \ll \tau$), before its output reaches the threshold V_C. In other words, the statistical properties of the noise are varying with time (non-stationary process) and the often-used noise analysis techniques based on the root-mean-square (RMS) value of noise cannot be used to quantify the noise behavior during an individual cycle.

However, the noise performance in this case can be analyzed in time-domain, as proposed in [28], using the auto-correlation function between the underlying non-stationary random processes to estimate their variance. It was also pointed out that even though the statistics of the noise voltages and currents are non-stationary during each cycle, the same operation is performed each clock cycle and the underlying signals are periodically sampled. As a result, the sampled signals have the same statistics each clock cycle, forming a wide-sense stationary (WSS) discrete time series. This property is called wide-sense cyclo-stationarity (WSCS)[30]. This observation led to the development of a periodic filtering frequency domain model in [28] that facilitates the frequency domain analysis of ZCB circuits. Finally, it was also proven and demonstrated in [28] that well-known noise aliasing techniques can be applied to obtain a noise power spectral density (PSD) for the series of samples.

Based on the findings in [28] and [27], a design-oriented estimation of noise in the ZCB integrator can be performed, following a similar approach with [29].

3-2-2 Apparent noise contributors

For the of estimation of the input-referred noise of the ZCB integrator, noise contributions from both the sampling and charge transfer phases have to be added in power, as discussed

in section 3-1. The apparent noise contributors of the charge transfer process are the preamplifier's thermal and flicker noise, thermal noise of the switches, thermal and flicker noise of the fine current source and noise due to autozeroing. The total input-referred noise power of the ZCB integrator will be

$$\overline{V^2_{n,in,INT}} = \overline{V^2_{n,C_S,sampling}} + \overline{V^2_{n,in,ZCD}} + \overline{V^2_{n,V_X,switches}} + \overline{V^2_{n,V_X,I_F}} + \overline{V^2_{n,V_X,AZ}} \tag{3-6}$$

where $\overline{V^2_{n,in,ZCD}}$ is the total input-referred noise of the ZCD and $\overline{V^2_{n,V_X,switches}}$ and $\overline{V^2_{n,V_X,I_F}}$ are the noise powers of switches and I_F referred to the virtual ground node V_X. The estimation of all these apparent noise contributors will be outlined, based on the methodology that was introduced in [27], providing design guidelines for the suppression of all contributors and the impact on power consumption. It is noteworthy that the proper balance of all these contributors is of great importance in order to achieve low-noise operation under high power efficiency.

Noise of the sampling phase

A fundamental limitation of noise performance of the integrator is the sampling noise during the phase Φ_1, when the input of the integrator is sampled on C_S. The noise behavior of this sampling process is well-understood [31] and similar to OTA-based designs, the noise power is $\overline{V^2_{n,C_S,sampling}} = kT/C_S$, where k is the Boltzmann's constant and T is the absolute temperature. The only way to suppress this contributor is to use larger sampling capacitor C_S, an option that increases the power consumption of the integrator.

Input-referred noise of the ZCD

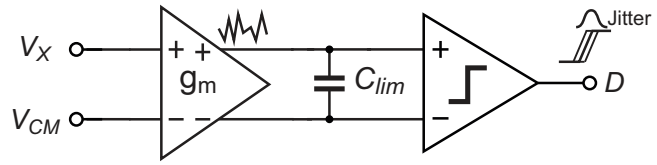
The noise contribution of the ZCD has been recognized as the most critical in the design of ZCB circuits [2]. Noise at the output of the ZCD will influence the moment of virtual-ground detection, which is equivalent to jitter on the ZCD delay. If the ZCD is modeled with an input-referred noise voltage source, the threshold level is appearing noisy, resulting in variation of the moment that the ZCD detects the threshold crossing. This is again equivalent to jitter on the ZCD delay and input-referred noise power can be calculated based on the assumption that the generated jitter power is exactly the same in both cases. This argument is visualized in Figure 3-4.

Since the ZCD is composed of a cascade of a band-limiting preamplifier and a wide-band crossing detector (as shown in Figure 2-9), the noise of second stage is suppressed by the gain of the preamp and can be neglected. The thermal noise of the transconductance amplifier can be modeled with an output current PSD of $S_{n,o} = 4kTG_n$, where G_n is the equivalent output noise conductance. In case of the inverter-based preamp $S_{I,o} = 4kT\gamma g_{m,tot}$ and $\gamma = 2/3$, thus

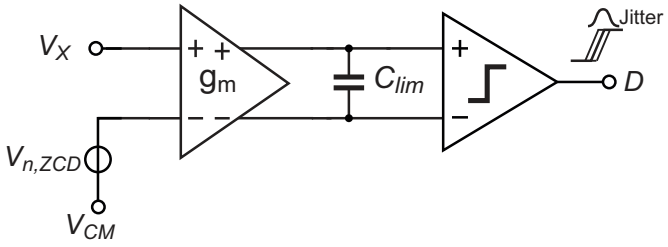
$$S_{I,o} = \frac{8}{3}kT(g_{mn} + g_{mp}). \tag{3-7}$$

The variance of the output voltage of the preamplifier can be calculated according to [27] as

$$\sigma^2_{V_{n,V_{int}}}(t) = \frac{1}{2} \cdot S_{I,o} \cdot \int_0^t h(a)da \tag{3-8}$$



(a) Noisy preamp results in ZCD jitter at output threshold crossing



(b) Noiseless preamp with input referred noise results in the same jitter at the input threshold crossing

Figure 3-4: ZCD noise modelling.

where $S_{I,o}$ is the preamplifier's noise single-sided PSD and $h(t)$ is the impulse response from the noise source to the output of the preamp, which in case of the transconductance preamp is $h(t) = \frac{1}{C_{lim}} e^{-t/\tau}$. The resulting time-variant output noise power of the preamplifier is then

$$\sigma^2_{V_{n,V_{int}}}(t) = \frac{kT}{C_{lim}} G_n R_O [1 - e^{-2t/\tau}] u(t) \tag{3-9}$$

where R_O is the output resistance of the preamp.

The conversion of noise voltages to timing jitter happens when a threshold detector is sensing a noisy signal [30]. The output-referred noise voltage of the preamp results in jitter, through the rate of change of V_{int}. The variance of threshold crossing time is then

$$\sigma^2_{t_i} = \sigma^2_{V_{n,V_{int}}}(t_i) \cdot \left(\frac{dV_{int}(t)}{dt}\bigg|_{V_{int}=V_C} \right)^{-2} \tag{3-10}$$

For the input-referred noise of the ZCD $\overline{V^2_{n,in,ZCD}}$ the equivalent jitter power is calculated as

$$\sigma^2_{t_i} = \overline{V^2_{n,in,ZCD}} \cdot \left(\frac{dV_X(t)}{dt}\bigg|_{V_X=V_{CM}} \right)^{-2} \tag{3-11}$$

Consequently, the equivalent input-referred noise, that is resulting to the same time jitter power with the output-referred noise of the preamp is

$$\overline{V^2_{n,in,ZCD}} = \frac{\sigma^2_{V_{n,V_{int}}}(t_i)}{\left|A_N(t_i)\right|^2} \tag{3-12}$$

where $\left|A_N\right|$ is the noise gain which is a function of the response time t_i of the preamp

$$\left|A_N(t_i)\right| = \left(\frac{dV_{int}(t)}{dt}\bigg|_{t=t_i} \right) \Big/ \left(\frac{dV_X(t)}{dt}\bigg|_{t=t_i} \right) \tag{3-13}$$

Taking into account when V_X is a ramp with a ramp rate M, V_{int} is described by (3-1), the noise gain can be calculated [27]

$$|A_N(t_i)| = A_0(1 - e^{-t_i/\tau})u(t_i) \tag{3-14}$$

According to (3-12), (3-9) and (3-14) the equivalent input-referred noise power the ZCD will become

$$\overline{V^2_{n,in,ZCD}} = 4kTR_N \cdot \frac{1}{4\tau}\coth\left(\frac{t_i}{2\tau}\right)u(t_i) \tag{3-15}$$

where $4kTR_N$ is the input-referred noise PSD of the preamplifier with $R_N = G_n/g^2_{m,tot}$ the input-referred noise resistance of the preamplifier. The second part of (3-15) is the non-stationary effective noise bandwidth of the preamp $NBW(t_i, \tau)$. The function of effective noise bandwidth is visualized for practical values of t_i and τ in Figure 3-5. The noise power

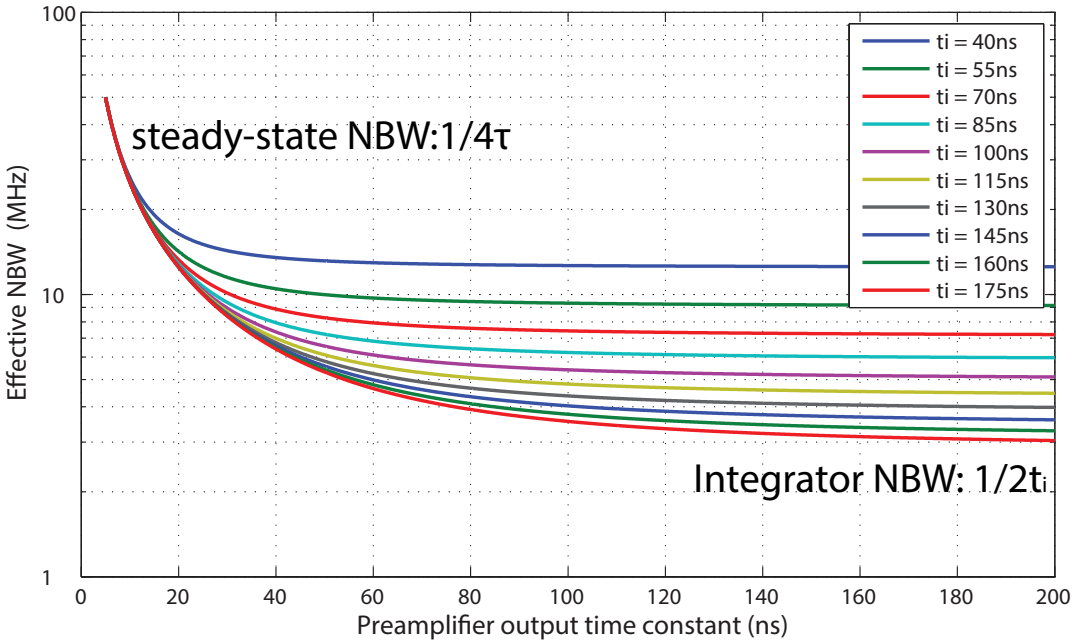


Figure 3-5: Effective noise bandwidth as function of t_i and τ.

$\overline{V^2_{n,in,ZCD}}$ is representing broadband noise, but since we are dealing with a sampled-data system, the noise contributor is subject to noise aliasing. Thus, the input-referred thermal noise PSD of the ZCD then needs to be scaled with $\frac{NBW(t_i,\tau)}{f_s/2}$ [29], where f_s is the average[1] sampling frequency of the SC integrator. However, the input-referred noise power of the ZCD remains equal to (3-15).

It is interesting to observe the limiting behavior of equivalent noise bandwidth at the

[1]The charge transfer duration of the integrators is signal dependent. For a first order estimation, the average sampling frequency should be used, which is derived by transient simulation of the ZCB integrator.

graphs of Figure 3-5:

$$NBW(t_i,\tau) = \begin{cases} \frac{1}{4\tau}, & \text{for } t_i \gg 2\tau \quad (3\text{-}16) \\ \frac{1}{2t_i}, & \text{for } t_i \ll 2\tau \quad (3\text{-}17) \end{cases}$$

where (3-16) is the noise bandwidth of the preamp that is operating in steady-state, while (3-17) is the noise bandwidth of an ideal gmC integrator. Apart from the behavior at the extremes, it is noteworthy to notice that allowing the preamplifier to operate with higher response time t_i, in order to have more time to do noise averaging, the NBW and the input-referred noise of the ZCD are lower. The penalties that are associated with higher t_i are larger input-referred error of the ZCB integrator and higher power consumption.

In order to illustrate the power consumption trade-off, the current consumption and the output V_{int} of the inverter preamplifier are plotted in Figure 3-6 along the entire charge transfer. The inherent adaptive biasing of the inverter is clearly illustrated here, as the current consumption is observed to be maximum around the threshold crossing instant, exactly when the $g_{m,tot}$ is needed to be maximum. Also, during t_i the inverter preamp is conducting approximately its maximum current, which is determined by the designed transconductance $g_{m,tot}$ and the g_m/I_d ratio of the transistors [32]. Since the input-referred noise of the ZCD depends on $NBW(t_i,\tau)$ and $g_{m,tot}$, these two parameters have to be designed properly so that the target $\overline{V^2_{n,in,ZCD}}$ is met under the lowest power consumption. This means that first of all the transconductance efficiency g_m/I_d of the transistors should be as high as possible and that the combination of t_i and $g_{m,tot}$ should be optimized.

Furthermore, the noise performance of the ZCD is typically suffering from $1/f$ (flicker) noise [31] exhibited by the transistors of the preamp. The input-referred $1/f$ single-sided PSD of a transistor is $S_{1/f}(f) = \frac{K}{C_{OX}WLf}$ [31], where K is a process-dependent parameter and C_{OX} is the oxide capacitance per unit area, leaving the area of the transistor $W \cdot L$ the only design variable. Interestingly, in case of the autozeroed preamplifier, the $1/f$ noise is not contributing to the input-referred noise of the ZCD, as autozeroing is acting as a high-pass filter on $1/f$ noise, with cut-off frequency equal to the frequency at which autozeroing is performed f_{AZ} [33]. As a result, as far as $1/f$ corner frequency is lower than f_{AZ}, the $1/f$ noise contributor should be neglected.

Input-referred noise due to switches

During the charge-transfer phase, there are four switches along the feedback capacitive network of the integrator that are conducting, exhibiting thermal noise, due to their finite on-resistance $R_{on} = \frac{1}{K'\frac{W}{L}V_{od}}$,where K' is a process-dependent parameter, $\frac{W}{L}$ is the designed switch dimension and V_{od} is the transistor overdrive voltage. The equivalent circuit can be seen in Figure 3-7. Thermal noise from these switches results in two noise contributors during the charge transfer phase. The first one is noise at the virtual ground node during the preamplifier's response time, while the second is noise across the integration capacitor C_I at the sampling moment of the output of the integrator. These two noise contributors have the same source, but are uncorrelated as they occur in different time instants.

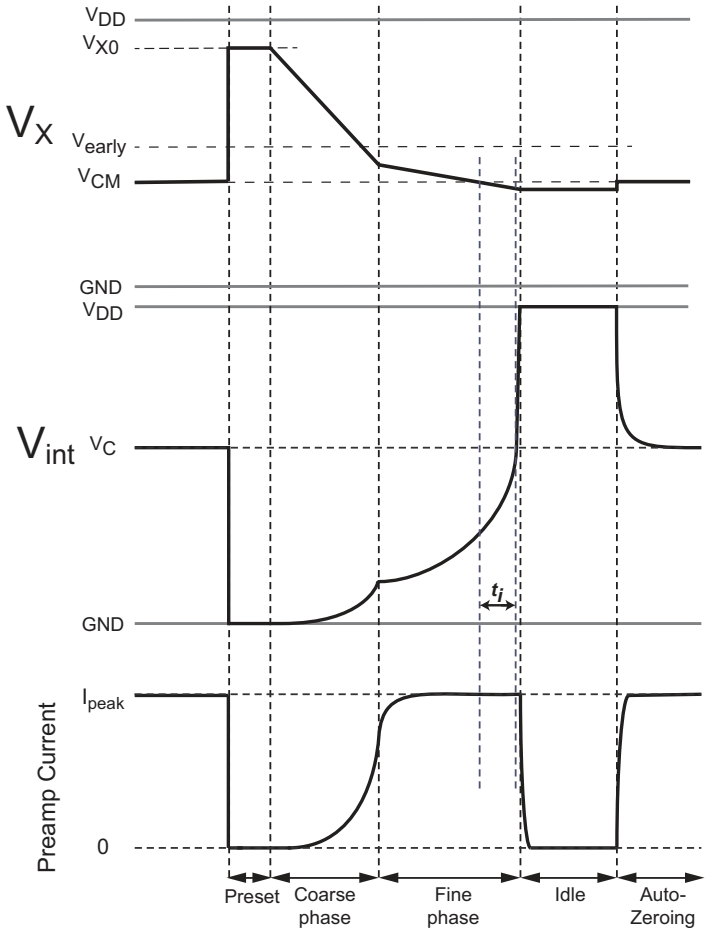


Figure 3-6: Current consumption and voltage response of inverter preamp during charge transfer.

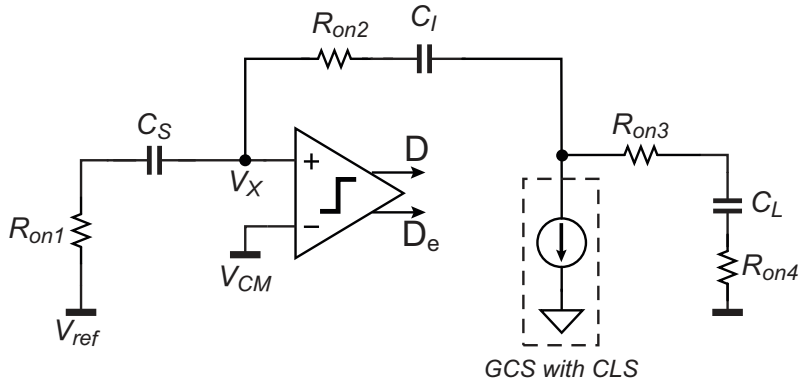


Figure 3-7: Noise due to switch on-resistance during charge transfer of ZCB integrator.

Examining the noise during the preamp's response, the switch and capacitor network is exhibiting an equivalent white noise PSD at the virtual ground node V_X equal to

$$S_{R,n,eq} = 4kT \cdot R_{n,eq}, \tag{3-18}$$

with

$$R_{n,eq} = R_{on2} + R_{on1} \cdot \left(\frac{C_S}{C_S + C_I \parallel C_L} \right)^2 + (R_{on3} + R_{on4}) \cdot \left(\frac{C_S + C_I \parallel C_S}{C_S + C_I \parallel C_S + C_L} \right)^2 \quad (3\text{-}19)$$

The noise from switches at V_X is filtered by the preamplifier in a similar manner with the input-referred thermal noise of the preamp, resulting in jitter in ZCD decision with exactly the same noise-bandwidth $NBW(t_i, \tau)$. Also, similar to the input-referred thermal noise of the ZCD, the noise of switches during preamp's response is subjet to noise aliasing and its broadband noise power spectral density has to be scaled with $\frac{NBW(t_i,\tau)}{f_s/2}$. As a result, the input-referred noise power due to switches during preamp's response

$$\overline{V^2_{n,in,switches-resp,sampl}} = 4kT \cdot R_{n,eq} \cdot NBW(t_i, \tau) \quad (3\text{-}20)$$

Also, this noise contributor is equivalent to the switch noise during the charge transfer of conventional OTA-based SC integrators [29], where the OTA bandwidth is filtering the switch noise. Ways to lower this contributor are to reduce the on-resistance of the switches, by using wider devices in order to lower the noise resistance at V_X, $R_{n,eq}$ of (3-19) and also design for lower the effective noise bandwidth $NBW(t_i, \tau)$. The strategy of lowering $R_{n,eq}$ is effective, especially establishing $R_{n,eq} < R_n$ but it may degrade the linearity of the integrator if we exaggerate, due to stronger charge injection and clock feed-through, as will explained in subsection 3-3-1.

When the preamplifier's output reaches V_C, the wideband-crossing detector trips, with a small delay t_c, as shown in Figure 3-3. During t_c, the preamp is not filtering the switch noise anymore and the feedback switch capacitor network is open-loop. Thus, the switch noise results in kT/C noise sampled onto the capacitors. We are primarily interested in the noise across C_I, as noise across C_L is appearing as output-referred noise of the ZCB integrator, that is heavily suppressed thanks to noise shaping of the modulator. Also, noise across C_S is not of interest, as it doesn't contribute to the integrated noise voltage. The kT/C noise across C_I is the kT/C noise of $C_{eq} = C_S \parallel C_I \parallel C_L$, through the capacitive divider from C_{eq} to the integration capacitance C_I. Therefore, the input-referred contributor will be

$$\overline{V^2_{n,in,switches-sampl}} = \frac{kT}{C_{eq}} \cdot \left(\frac{C_S \parallel C_L}{C_S \parallel C_L + C_I} \right)^2 \cdot \left(\frac{C_I}{C_S} \right)^2 \quad (3\text{-}21)$$

This contributor, along with the sampling phase kT/C_S noise and thermal noise due to fine current source (that will be quantified soon) is practically posing a limit on the minimum capacitances that need to be used in ZCB integrator. The energy consumption associated with the swing of the output voltage of the integrator V_O after the preset phase is $E_{swing} = C_T \cdot (V_{DD} - V_{swing})$, where $C_T = C_L + C_{CLS} + C_I \parallel C_S$ is the output capacitance. In the first prototype, $C_T = 1pF$ and the output swing is from 0.35V to 0.65V. An estimation of the average energy consumption for an integrator can be made using the average output voltage as $E_{swing} = 1pF \cdot 0.5V = 0.125pJ/cycle$, and the energy per conversion for the 1^{st} integrator of [1] is $500 \cdot E_{swing} = 60pJ/conv.$.

Finally, the total input referred noise contributor of switch noise during the charge transfer of the ZCD integrator will be the sum of the two uncorrelated noise contributors

$$\overline{V^2_{n,V_X,switches}} = \overline{V^2_{n,in,switches-resp}} + \overline{V^2_{n,in,switches-sampl}} \quad (3\text{-}22)$$

Input-referred noise of fine current source

Another noise contributor of the charge transfer process is the noise of the fine current souce I_F, which is meaningful only after the preamplifier's input threshold crossing instant. Noise before this moment only affects the duration of the charge transfer, but does not result in error on the integrated charge. The noise contribution of I_F consists of the random walk on integrator's feedback capacitive network during two independent time intervals: the preamp's response time t_i and during the threshold detection delay t_c.

During preamp's response time t_i, the preamplifier is filtering the random walk on the capacitive network, resulting in jitter in ZCD decision which is negatively correlated with the jitter due to preamplifier's output noise, as analyzed in [28]. Based on the analysis employing the periodic filtering model in [27] which was directly applied also in [8], the input-referred noise power during t_i for white current source noise with power spectral density $S_{I_F}(0)$ is

$$\overline{V^2_{n,in,I_F/t_i}} = \frac{S_{I_F}(0)}{C^2_{out}} \cdot t_i \left(\frac{C_I}{C_S + C_I} \right)^2 \tag{3-23}$$

where $C_{out} = C_L + C_S \parallel C_I$. Similarly, the input-referred noise power during t_c is

$$\overline{V^2_{n,in,I_F/t_c}} = \frac{S_{I_F}(0)}{C^2_{out}} \cdot t_c \left(\frac{C_I}{C_S + C_I} \right)^2 \tag{3-24}$$

As a result, the total input-referred noise due to the fine current source will be the sum of the previous two uncorrelated contributors, and thus

$$\overline{V^2_{n,in,I_F}} = \overline{V^2_{n,in,I_F/t_c}} + \overline{V^2_{n,in,I_F/t_c}} = \frac{S_{I_F}(0)}{C^2_{out}} \cdot (t_i + t_c) \left(\frac{C_I}{C_S + C_I} \right)^2 \tag{3-25}$$

The above expressions are for a preamplifier that is operating as an ideal integrator ($t_i \ll \tau$), as in this case the noise power is maximized and the jitter correlation is minimum. This was adopted because it provides a worst case estimate of the noise due to I_F, as can be understood from the analysis in [27]. The noise power from the current source is proportional to t_i, therefore low $S_{I_F}(0)$ is required if t_i is designed to be large. The thermal noise PSD of I_F, $S_{I_F}(0)$, can be lowered by biasing the current source with lower g_m, thus lowering the charging current level. Also, for given t_i and $S_{I_F}(0)$, the noise due to I_F can be effectively decreased by increasing C_{out}. In order to keep the same speed of charge transfer, the required fine current has to linearly increase with C_{out}, while the input-referred noise is dropping with C^2_{out}.

Input-referred noise due to auto-zeroing

Auto-zeroing is an effective way to attenuate the flicker noise of the preamplifier that is seen in Figure 2-9, but sampling noise of this process is contributing to the overall input-referred noise of the ZCB integrator. The sampled noise across the auto-zeroing capacitor C_{AZ} can be seen as noise of the threshold of the ZCD, which directly leads to noise across the sampling capacitor C_S at the end of the charge transfer process. This auto-zeroing noise is not filtered by the preamplifier and the input-referred noise power is

$$\overline{V^2_{n,V_X,AZ}} = \frac{kT}{C_{AZ} + C_{lim}} \tag{3-26}$$

As it is evident when inspecting (3-26), this contributor is depending only on the capacitance levels of C_{AZ} and C_{lim} and doesn't pose any significant restriction in terms of power consumption.

3-2-3 Estimation of noise performance of the first prototype

Making use of the previous analysis of the apparent noise contributors, the total input-referred noise powers of the first ZCB integrator, as well as, the ADC of [1] can be estimated. Calculating the noise power of the individual contributors based on the design choices of [1] the total input-referred noise voltage of the integrator is estimated to be $v_{n,in,INT1} = 199.8\mu V$ while the effective noise-bandwidth is $NBW = 8.2MHz$. In this estimation, the thermal noise due to switches during preamp's response was found to be dominant, followed by the thermal noise contributor of the ZCD preamp.

Using MATLAB simulation to estimate the quantization error of the modulator (Figure 2-2) for $N = 500$, the quantization error range was found to be approximately $Q_r = 18\mu V$. The equivalent quantization noise standard deviation, assuming that the error is uniformly distributed within its range will be $\sigma_q = \frac{Q_r}{\sqrt{12}}$ [16]. Since, this uniformity assumption is quite far from reality and the quantization error appears busier close its the borders the σ_q is higher and a 30-50% scaling should be adopted. Thus, taking 30% margin, the σ_q becomes

$$\sigma_q = \frac{Q_r}{\sqrt{12}} \cdot 1.3 = 5.196\mu V \tag{3-27}$$

The estimation of the total input-referred RMS noise of the ADC, according to (2-10) and (2-8) for $k = 4/3$, taking into account only the intrinsic noise of the first integrator, will be

$$v_{n,in,ADC} = \sqrt{\sigma_q^2 + \frac{4}{3} \cdot \frac{\overline{v_{n,in,INT1}^2}}{N}}. \tag{3-28}$$

This is resulting to $v_{n,in,ADC} = 12.33\mu V$. This value is quite far from the input-referred noise of the ADC reported in [1]. Possible reasons for this, besides the presence of an unmodelled contributor, are an artifact of the measurement setup or the effect of supply noise.

3-3 Linearity analysis of the ZCB integrator with CLS

3-3-1 Non-linear error due to switches

Unlike OTA-based switched-capacitor circuits, which settle to steady-state during the charge-transfer phase, current is still flowing through the switches of ZCB circuits at the instant the output voltage is sampled. Output-dependent variations in the voltage drop across these switches, whether from variations in switch on-resistance or current, lead to errors in the integrated voltage of the ZCB integrator.

Referring to Figure 3-7, IR drop across the on-resistances R_{on2}, R_{on3} and R_{on4} will only create error on the sampled output voltage V_O and not across the integration capacitor

C_I [34]. Because this error is not integrated each cycle, but appears only at the output of the integrator, it is heavily suppressed by the noise-shaping of the modulator and hardly contributes to the total input-referred error. In contrast, voltage drop across R_{on1} is creating error on the integrated voltage equal to $-\frac{C_S}{C_I} \cdot R_{on1} \cdot I_F \frac{C_S \parallel C_I}{C_L + C_S \parallel C_I}$. As a result, the input-referred error is

$$V_{in,err-sw} = -R_{on1} \cdot I_F \cdot \frac{C_S \parallel C_I}{C_L + C_S \parallel C_I} \tag{3-29}$$

with its constant part leading to offset and its signal-dependent part creating non-linearity.

In context of the $\Delta\Sigma$ modulator, the switch with on-resistance R_{on1} is representing the feedback connection of the 1^{st} integrator that is applied during the charge-transfer phase, as shown in Figure 2-4. The feedback connection is implemented with the top-plate of C_S switched between the positive and the negative reference voltages, via an PMOS and a NMOS unboosted switch respectively.

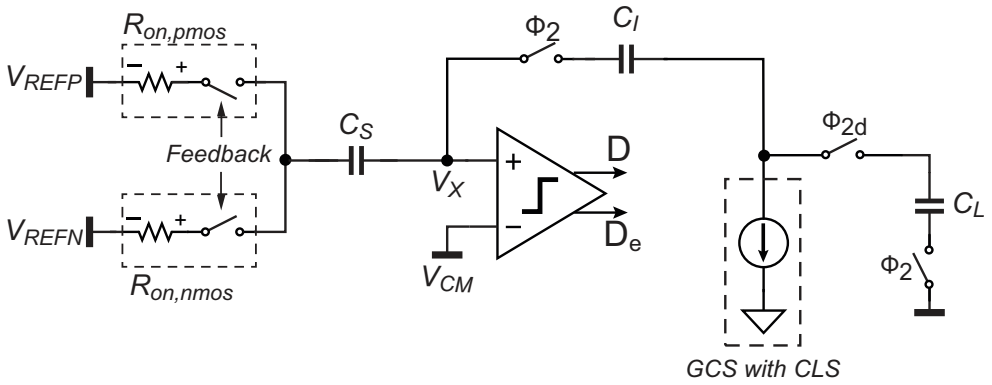


Figure 3-8: Feedback switches on-resistance induced error.

Due to inherent systematic mismatch between NMOS and PMOS switches, a voltage dependent error is created due to the IR drop across these switches, according to (3-29), with R_{on1} to take the value of $R_{on,nmos}$ or $R_{on,pmos}$ depending on the feedback signal, as shown in Figure 3-8. Hopefully, if the variation of I_F is assumed negligible, the mismatch between $R_{on,nmos}$ and $R_{on,pmos}$ is leading to a slight (but constant) change of the reference voltages from their ideal values, which leads to small system-level gain error of the ADC, which is tolerable. Besides, for finite variation of I_F, the variance of the voltage drops across the feedback switches from the baseline value is creating non-linearity. The most effective way to limit the non-linear error is to lower the on-resistance of these switches by increasing their $\frac{W}{L}$ and trying to achieve equal relatively voltage drop variances for the NMOS and PMOS switches with respect to the whole output range of the ZCB integrator.

Other switch non-idealities that harm the accuracy of both the sampling phase and introduce error on the integration capacitor C_I at the end of the charge transfer phase are clock feedthrough and charge injection. To be specific, the switches at the two ends of C_I introduce error charge on C_I at the sampling instant. Also, the accuracy of sampled input on C_S is degraded, contributing to offset and non-linearity. Assuming a total switch gate capacitance C_G, the charge being fed through from the switch (distributed to source, drain

and substrate) is given by

$$Q_{clkfeedthrough} = C_G \cdot V_{drive} \tag{3-30}$$

where V_{drive} is the gate driving voltage. The switch gate capacitance is proportional to oxide capacitance per unit area (C_{OX}) and the switch area $W \cdot L$. Regarding charge injection, the total charge in the channel of a switch that is conducting can be approximated as

$$Q_{channel} = C_{OX} \cdot WL \cdot (V_{GS} - V_{TH}) = C_{OX} \cdot WL \cdot (V_{drive} - V_S - V_{TH}) \tag{3-31}$$

A common approximation is that half of the charge is distributed to source and drain respectively [35]. However, as the impedance on each side of the switch is different and the clock fall time is finite, this is not entirely correct. Both equations above show that the switch area must be minimized to reduce the non-idealities due to switching. In order to entirely remove the signal dependent part of the charge injection, $V_{drive} - V_S$ must not be dependent on the source voltage of the switch, something which is achievable by switch bootstrapping [16] or by introducing dummy switches [31]. The latter options that was not considered, as it turned out that the errors caused by these two mechanisms were not very significant.

3-3-2 Non-linear error due to ramp-rate variation

The finite response time of the ZCD, in combination with the ramp-rate variation due to signal dependency of I_F create signal dependency of the overshoot voltage at V_X from V_{CM}. This overshoot voltage is equal to the error voltage that is integrated on C_I every cycle and is not suppressed by the noise shaping of the modulator. If the time delay between the zero-crossing instant and the turn-off moment of the fine current source is denoted as t_d, the overshoot at V_X can be expressed mathematically as

$$V_{X,OV} = \int_0^{t_d} M_{X,fine}(t) \cdot dt = \int_0^{t_d} \frac{I_F(t)}{C_L + C_S \parallel C_I} \cdot \frac{C_I}{C_S + C_I} \cdot dt \tag{3-32}$$

If $I_F(t)$ was constant, the overshoot would be constant and the integrator would be perfectly linear, suffering only from finite offset equal to $+V_{X,OV}$. In actual implementation, both the charging current sources have finite output impedance due to channel-length modulation effect of MOSFETs [31] and assuming $R_{out,fine}$ is the output impedance of I_F the fine current will be

$$I_F = I_{F0} \cdot \left(1 + \frac{V_{fine}}{R_{out,F}}\right) \tag{3-33}$$

with I_{F0} representing the baseline current and V_{fine} the swing of the current source. $R_{out,fine}$ is depending on the actual implementation and biasing of the current source, as well as, on the level of the charging current. As the coefficient λ of channel length modulation slightly varies with the V_{DS} voltage of the transistor, $R_{out,fine}$ is expected to slightly vary with V_{fine}. Considering the ZCB integrator, without employing correlated level shifting, the swing of the fine current source is identical with the output swing of the integrator and the possible ways to enhance accuracy are to increase $R_{out,F}$ or limit the swing of V_O. However, increasing $R_{out,F}$ is tricky in this case because with supply voltage of around $1V$, the biasing of a cascode current source that can operate with $V_{min} = 0.35V$ is not a straightforward task, if not impossible.

Hopefully, when utilizing correlated level shifting, as described in subsection 2-3-3, the swing of the fine current source is limited and in ideal case is independent of the swing of V_O,

giving the opportunity to introduce a cascode fine current source. Thus, the overshoot $V_{X,OV}$ is stabilized also, because of the identical trajectory of V_{fine} in every integration cycle. This stabilizes the waveform of I_F in every cycle making it signal independent in ideal case with constant coarse phase overshoot. The residue signal dependency of V_{fine} and correspondingly of I_F will be due to the variance of the final point of V_{fine} trajectory of Figure 2-7, caused by the signal-dependent coarse phase overshoot on V_O, due to finite coarse current source output impedance. Based on the analysis of the ZCB integrator with CLS done in [34] and [25], assuming a coarse current source with baseline current I_{C0}, output impedance $R_{out,C}$ and coarse phase ZCD delay of $t_{d,coarse}$, the fine current at the end of the charge transfer is

$$I_F = I_{F0} - \frac{t_{d,coarse}}{R_{out,F} \cdot C_{CLS}} \cdot I_{C0} - \frac{V_O}{R_{out,F}} \left(\frac{R_{out,C} \cdot C_{CLS}}{t_{d,coarse}} \right)^{-1} \quad [25] \tag{3-34}$$

Under the assumption $t_{d,coarse}$ is not signal dependent, the V_O-dependent part of I_F is

$$I_{F,var} = \frac{V_O}{R_{out,F}} \left(\frac{R_{out,C} \cdot C_{CLS}}{t_{d,coarse}} \right)^{-1} \quad [25] \tag{3-35}$$

and the effective output impedance of the fine current source with CLS has boosted now to

$$R_{out,F,eq} = R_{out,F} \left(\frac{R_{out,C} \cdot C_{CLS}}{t_{d,coarse}} \right) \quad [25] \tag{3-36}$$

In order to estimate the non-linearity of the ADC caused by fine phase ramp-rate variation, the overshoot of (3-32) can be estimated, for a constant delay $t_d = 75ns$ and assuming I_F to take its extreme values during the whole t_d, predicted by (3-34). This assumption is corresponding to a worst-case scenario for the signal-dependency of I_F. This procedure leads to an estimated range of $V_{X,OV}$ (i.e. input-referred signal-dependent error range) for an output swing from 0.35V to 0.65V of less than $2\mu V$. This input-referred signal-dependent error variance is rather small and in any case is not expected to be the dominant non-linear effect of a $\Delta\Sigma$ modulator with INL at the level of 1LSB w.r.t. 14bit. The previous estimation was done using the circuit-level parameters noted in subsection 2-3-4, under the worst-case assumption that $t_{d,coarse}$ is varying by $\pm 20\%$ from its baseline value of $10ns$. Of course, t_d is by any means constant, as it is modulated by the ramp-rate of V_X, causing excess non-linearity in the overshoot voltage. Furthermore, for a uni-directional charging scheme, regardless the polarity of V_O, both even and odd harmonics are expected to be present in $V_{X,OV}$, even in fully-differential realizations.

3-3-3 Non-linear error caused by turn-off transients of current sources

Besides switch and ramp-rate variation, the off-transients of both coarse and fine current sources induce non-linear charge on C_I at the end of the charge transfer. The coarse current source current during its off-transient, contributes to the coarse phase overshoot on V_O which in turn, affects the swing of the fine current source creating variability on the fine current. Regarding the fine current source, while it is turning off, it introduces error charge to the feedback capacitive network, with the error charge across C_I to be of importance. The constant part of this error charge is leading to offset, but the signal-dependent part creates

non-linearity that cannot be corrected. This error contributor is hard to analyze and the most efficient design strategy is to quantify its importance using transient simulation. The output current of the current sources can be monitored and ultimately, the integrated charge across C_I in each cycle (having a small constant input of the ZCB integrator) in order to observe the overall signal dependency.

3-4 Summary

In this chapter, the noise and linearity analysis of a ZCB SC integrator with CLS have been presented. After a short introduction on the behavior of the ZCD with ramp inputs, a design-oriented estimation of input-referred noise of ZCB integrator was presented, including all the apparent noise contributors, such as the thermal noise of switches, the fine current source and ZCD thermal noise, which has been recognized as the most critical one. Based on this analysis, the total noise of the first integrator of the first prototype was estimated. Furthermore, apparent circuit non-idealities, like the finite on-resistance of switches, that lead to linearity degradation of ZCB SC integrator were explored. The ramp-rate variation, which is widely recognized as the dominant non-linear effect, turned out to be much less significant, when correlated level-shifting is utilized, to effectively stabilize I_F across the output swing of the integrator.

Chapter 4

Noise and linearity measurement results of the first prototype

4-1 Existing Measurement setup

For the performance characterization of the first prototype self-timed ADC, a measurement setup has been built [25], whose a block diagram can be seen in Figure 4-1. This setup was

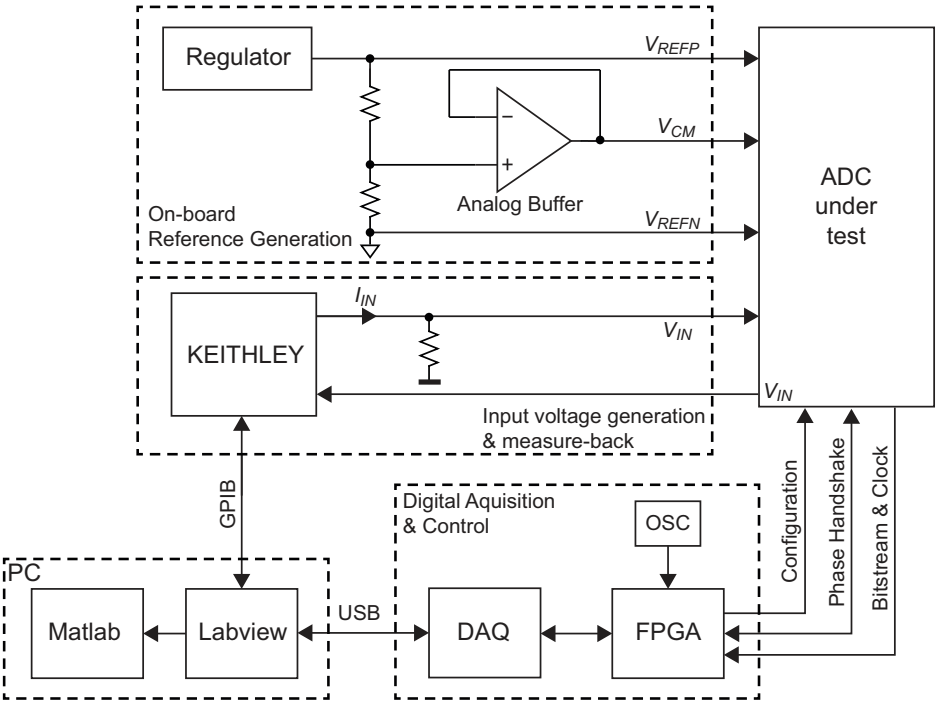


Figure 4-1: Block diagram of the measurement setup of the first prototype [25].

based on an NI M-series Data acquisition device (DAQ) and an Altera Cyclone-IV E-series FPGA was used to implement the off-chip part of the control logic (cycle counting and $\Phi_1/\Phi 2$ asynchronous generation). The performance critical parts of the setup are the input voltage (V_{IN}) and ADC reference voltage (V_{REFP} and V_{REFN}) generation. The input voltage was generated using a precision Keithley-2400 current source meter [36], feeding a shunt on-board resistor ($\simeq 120\Omega$). The reference was generated using an on-board LDO, the LP38511-ADJ [37] from Texas Instruments.

4-2 Noise measurement

The noise characterization of the ADC involves the measurement of the sample-to-sample standard deviation of the decimated output, δ_{rms} for a number of consecutive conversions keeping the input voltage constant. The δ_{rms} represents the output-referred RMS noise of the ADC and the resolution (ENOB) of the ADC can be derived by (2-7).

Inspecting the datasheet of LP38511-ADJ [37], it can be concluded that the noise PSD of the reference is suffering from flicker noise at low-frequencies, that are in-band for the measurement. Thus, even the input was completely noise-free, the measured noise of the ADC would be degraded by the noise of the reference. When providing the input of the ADC using a voltage divider between V_{REFP} and V_{REFN}, using the so-called ratiometric measurement approach, the noise of input and reference are fully correlated and thus the noise measurement gets more accurate. Following this approach, the resolution of the first prototype was measured as a function of incremental cycles N, performing 100 conversions at a single input point. The results of this measurement are shown in Figure 4-2.

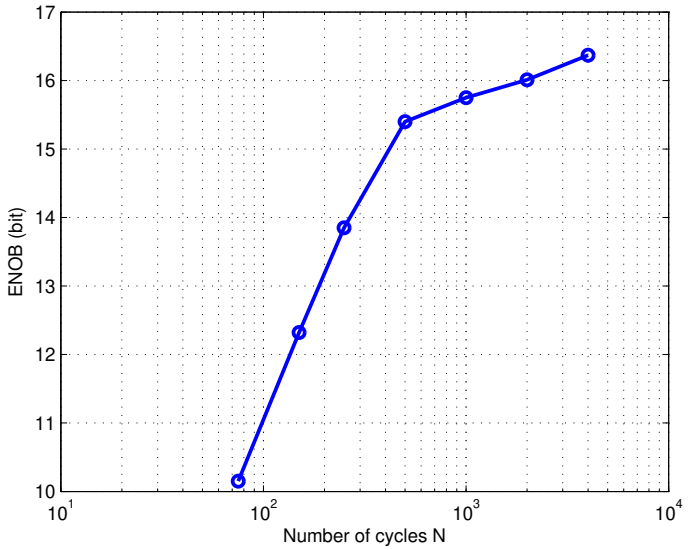


Figure 4-2: Measurement result of the first prototype for the resolution (ENOB) as a function of N.

Specifically, for $N = 500$, the input-referred RMS noise was measured to be $14.3\mu V$, that, according to (2-7), is equivalent, to ENOB=15.4bits with respect to a stable input range of

$0.7V$. This measurement result is in quite close agreement with the analytical estimation of the input-referred RMS noise of the ADC that was done based on the analysis of Chapter 3, that resulted to an estimated input-referred noise of $12.33\mu V$. This agreement is a sign of validity of the noise analysis and the utilization of the developed noise model is expected to be useful in the design of an improved self-timed ADC.

4-3 Linearity measurement

The measurement of linearity is involving DC sweep of the input voltage (provided by Keithley-2400 source meter), measurement of the decimated output and plot the ADC transfer function (decimated output versus the input voltage). After this, the integral non-linearity (INL) of the ADC, can be obtained by calibrating out offset and gain error from this plot, calculating the deviation of each point from the best-fitting straight line. In order to suppress noise in the linearity measurement, the number of incremental cycles should be maximized and multiple decimated output samples per input voltage are averaged. Furthermore, for enhanced accuracy, the input DC voltage of the ADC is measured back by the source-meter in a 4-wire configuration [36] for each input step (Figure 4-1).

Even when taking all these noise suppression measures, the INL results of the ADC were not reproducible, which is a clear indication that the measurement setup is suffering from noise. The possible noise sources are ground noise, noise from Keithley-2400 that affects the input of the ADC or noise of the reference voltage V_{REFP} that is generated from the reference LDO. Using the voltage meter of Keithley-2400, it was possible to inspect the stability of input voltage of the ADC and V_{REFP} in order to trace the dominant noise source. It was observed that Keithley-2400 is capable to provide a very precise and low-noise current, which generates an accurate enough input voltage for the ADC. However, the V_{REFP} was measured to be very noisy with respect the accuracy that was targeted to measure.

Fortunately, in the existing measurement setup, there was a possibility of using an external reference voltage. Also, a precision voltage source was available, the Yokogawa GS200 [38] that was measured to be capable of generating a stable and accurate enough reference voltage. Making use of this, an accurate linearity measurement was possible and the measured INL of the ADC is plotted in Figure 4-3. The measured INL was within -0.7LSB to 0.6LSB, relative to a 14-bit output code.

In order to show the repeatability of the linearity measurement, the INL plots of 5 consecutive measurements are plotted in Figure 4-4, along with the INL plot of Figure 4-3. It was observed that the measurement was still not noise-free, but the fixes of the measurement setup that were performed were enough in order to reveal the actual linearity pattern of the previous design.

Finally, in order to illustrate the sample-to-sample variation of the linearity measurement, the INL plots of 3 consecutive measurements of another sample (with larger steps of input voltage) are shown in Figure 4-5, along with the INL plot of Figure 4-3. Interestingly, the same pattern of INL is observed in this experiment as well.

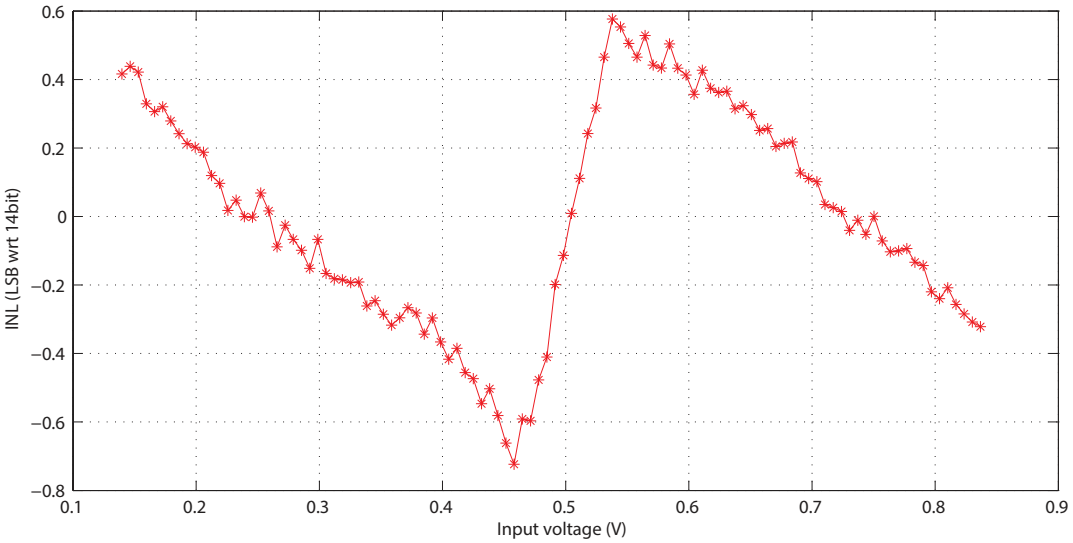


Figure 4-3: Measurement result of the INL of the first prototype [1].

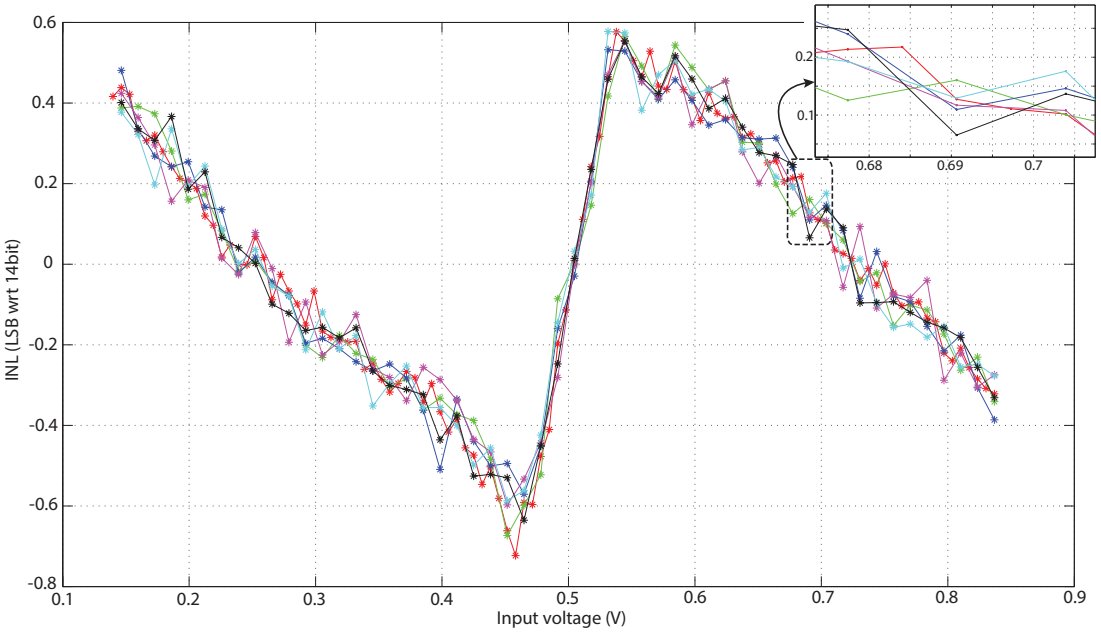


Figure 4-4: Measurement results of the INL of the first prototype of 6 consecutive runs.

4-4 Performance summary

The performance of the first prototype self-timed $\Delta\Sigma$ ADC is now summarized in Table 4-1. In order to be able to compare with other ADCs and get a feeling of the energy-efficiency, the two most-often used figures of merits (FOM) for the comparison of ADCs should be used.

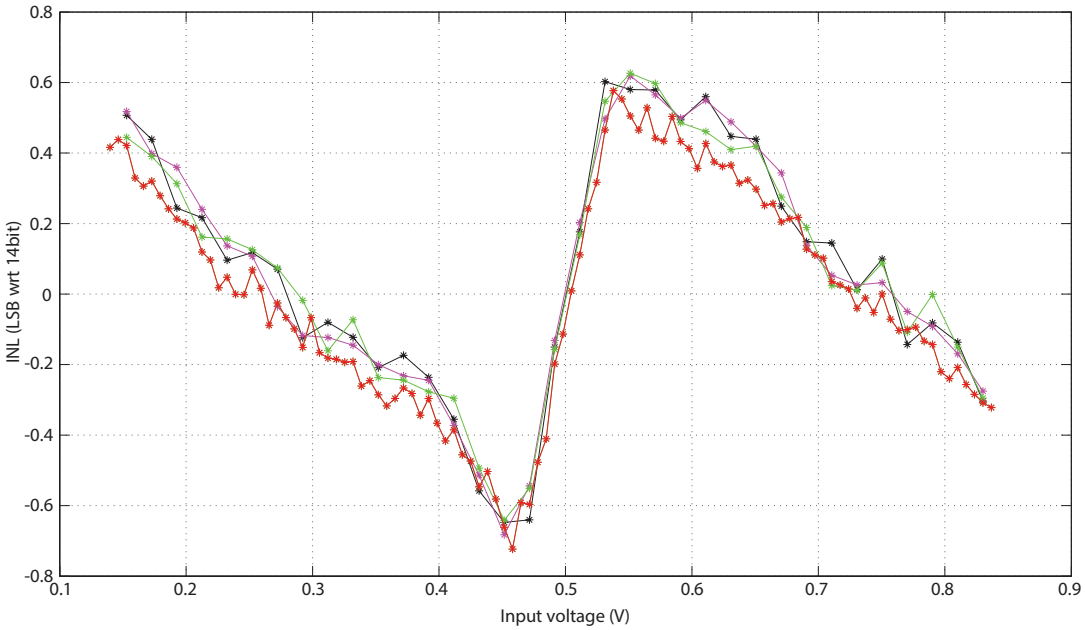


Figure 4-5: Measurement of the sample-to-sample variation of the INL of the first prototype [1].

Table 4-1: Updated Performance Summary of the first prototype [1]

Specification	Performance
Technology	NXP 0.16μm 1P6M CMOS
Active Chip Area (mm^2)	0.45
Supply Voltage (V)	1
Supply Current (μA)	Analog: 10 Digital: 9.8
Conversion Time (ms)	< 0.75
Stable Input Range (V)	0.15 - 0.85
Input-Referred RMS Noise (μV)	14.3
SNR (dB)	84.76
INL (LSB)	-0.7 - 0.6†
FOM$_W$ (pJ/conversion-step)	1.05
FOM$_S$ (dB)	163.04

† Relative to a 14-bit output code.

The first one is the Walden FOM,

$$FOM_W = \frac{Power \cdot T_{conv}}{2^{(SNR-1.76)/6.02}} \quad [\text{pJ/conversion} - \text{step}] \tag{4-1}$$

where for the Incremental ADC the Nyquist-rate bandwidth is replaced by with the inverse of the convesion time T_{conv}. In the previous expression, the signal-to-noise ratio SNR of the ADC should be calculated as

$$\text{SNR} = 20 \cdot \log_{10} \frac{\text{Stable Input Range}}{2\sqrt{2} \cdot \text{Input Referred RMS Noise}} \tag{4-2}$$

In the expression for SNR, a crest-factor correction of $2\sqrt{2}$ was included to take into account the fact that the noise of the Incremental ADC is not characterized using an input full-scale sinusoid. Besides, the second expression of FOM that is typically used in the comparison of high resolution ADCs is the Schreier FOM [17]:

$$FOM_S = \text{SNR} + 10 \cdot \log \frac{1}{\text{Power} \cdot \text{T}_{\text{conv}}} \quad [\text{dB}] \ ^{1} \tag{4-3}$$

where again the Nyquist-rate bandwidth is replaced with the inverse of the conversion time T_{conv}.

4-5 Summary

In this chapter, the measurement results for noise and linearity of the first prototype of self-timed Incremental $\Delta\Sigma$ ADC have been presented. It was found that the noise performance was superior, compared to the results reported in [1], which improves slightly the energy efficiency of the previous design. On the other hand, the measured linearity was worse, but in this case the measured INL plot was reproducible. Furthermore, the result of the noise measurement is in close agreement with the estimation of noise performance that was done in subsection 3-2-3, which proves the validity of the noise analysis presented before. This agreement is extremely useful as a path is drawn for the improvement of the resolution of the ADC in an energy-efficient way.

On the contrary, the linearity of the ADC was found to be slightly higher than 1 LSB with respect to 14-bit codes, although it was expected to be much better according to the analysis of the ramp-rate variation induced non-linearity. This means that the linearity analysis based on the ramp-rate variation (ignoring the importance of the off-transients of the current sources) fails to capture the dominant source of non-linearity, which poses difficulties in the design. It apparent that another mechanism is creating non-linearity, with the off-transients of the fine current source becoming a key suspect. Finally, the disagreement of the analytical estimation with the measurement results suggests to follow a design procedure based on simulation of the non-linearity, as the analytical estimation seems not very effective.

[1] For thermal-noise dominated designs, DR $\approx$ SNR.

Chapter 5

Design for improved self-timed ZCB I$\Delta\Sigma$ ADC

This chapter is primarily focusing on the design of the first integrator, as the most performance critical component in the design of an improved self-timed I$\Delta\Sigma$ ADC. Initially, the design procedure of the entire ADC (focusing on the first integrator) is outlined. Then, the system-level design considerations of the ADC are tackled, including modulator order and topology and the architecture of the ZCB integrator that will be employed. Afterwards, the noise and linearity design of the first integrator are described and finally, simulation results for noise, linearity and power consumption of the first integrator that will be used to improve the performance of the self-timed ADC are summarized.

5-1 Design procedure

Based on the knowledge that the noise and linearity performance of the entire I$\Delta\Sigma$ ADC vastly depend on the first integrator, the majority of the design efforts are focused on its optimization. However, smart system-level design of the ADC and understanding of the top-level trade-offs in the design will generate the opportunity of achieving the target specs for improved noise and linearity with higher energy-efficiency. As a result, design-space exploration is necessary in order to conclude on the modulator order, number of incremental cycles N, noise allocation and architecture of the ZCB integrator. In this step, the noise specification of the ZCB integrator is decided as well.

Following, the feasibility of use of a ZCB integrator topology starts with the estimation of the achievable linearity. The best way to perform this is through simulation of the input-referred error of the ZCB integrator. This is performed using transient simulation, where the integrator is fed with a constant small input and is let to integrate for multiple cycles. The integrated voltage across C_I at the end of each cycle can be captured and after normalizing the integration steps over their average value and scaling with the inverse of the integrator's

constant $\frac{C_I}{C_S}$ the signal-dependent component of input-referred error of the integrator is then derived for the entire output swing. For instance, following this procedure, the integration error of the first integrator of [1] was derived and visualized in Figure 5-1. In the same figure, the simulation result for the INL of the previous design can also be seen. Using 8 input voltage points, the INL was simulated to be approximately 0.8LSB with respect to 14bit.

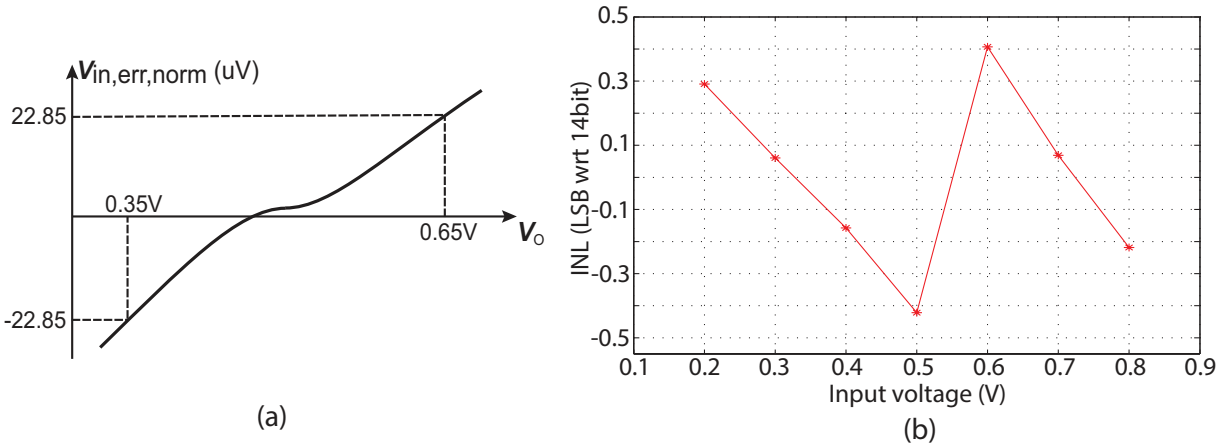


Figure 5-1: Linearity simulation results for the first integrator in [1]: (a) Signal-dependent component of input-referred error of the first integrator in [1], (b) Simulated INL of the first prototype [1]

If we try to estimate the linearity of the ADC, based on the simulation of the input-referred error of the first integrator (Figure 5-1(a)), following similar procedure with the estimation of INL in OTA-based designs [12] we will end up with an estimation that is much better compared to the simulated INL ((Figure 5-1(b)), because the non-linear component of the error in Figure 5-1(a) is small compared to the error bounds. Interestingly, when an approximation of this input-referred error pattern was used in a Matlab simulation of the non-linearity, the resulting estimation of INL was around 0.3 LSB with respect to 14bit, which is much better compared to the simulated INL (Figure 5-1(b)) and the measured INL Figure 4-3 of the previous design [1]. Probably, this mismatch between the reality and the estimation of the INL based on the simulated input-referred error of the integrator comes from the inaccuracy of the simulated error. A possible reason for this is that in the context of the modulator, the integrator is not working under the same conditions with the simulation testbench, because is not operating with a small input voltage, but processes the entire input range of the ADC. In this work, the simulated input-referred error was used as an indicator of the linearity performance, based on the correspondence of the simulation results of the previous design that are shown in Figure 5-1. All the design choices were judged based on the behavior of the input-referred error and was concluded that the simulated input-referred error needs to be suppressed in order to arrive to a design with better linearity.

Following this procedure for all the alternatives, the feasible options are short-listed and the best candidate can be found. After this, if the linearity estimation of the examined topology is close to the requirement, the integrator's noise performance is tackled. First, the target specification of the integrator's input-referred noise should be estimated based on the balance between q-noise and thermal noise and the number of incremental cycles N for a

target noise performance of the ADC. Based on the analysis of section 3-2 the ZCB integrator can be sized accordingly to meet the target specification taking a moderate design margin into account. The noise design should be then verified through simulation with two feasible simulation solutions for this task to be PSS/Pnoise simulation and transient noise simulation. Then, the linearity design should be revisited again, taking the necessary measures to ensure that the signal-dependent error is low enough to meet the linearity specification of the ADC. The noise and linearity design are not independent of each other and typically iterations are present in the design procedure.

After the design of the integrator is completed the ADC can be built and extensive verification of the toplevel performance is mandatory. For the noise performance, a transient noise simulation of multiple conversions using constant input voltage will give an estimation of the ADC's input-referred noise, calculating the point-to-point standard deviation of the decimated outputs δ_{rms}. Regarding the linearity performance, an input sweep has to be performed, using transient simulation. The INL of the ADC can then be estimated following the same procedure with the linearity measurement of the ADC that described in section 4-3.

5-2 System-level considerations

5-2-1 Modulator order

The first step of the design process of an improved self-timed I$\Delta\Sigma$ ADC is the decision of the modulator order and architecture. Possible candidates for this implementation are a second-order Boser-Wooley modulator with input feed-forward path (Figure 2-2) or an extension to a third-order architecture (with both feed-forward (CIFF) and feed-back topologies (CIFB) [17] to be considered). Between CIFF and CIFB, the CIFF architecture is in general preferred, as the integrators of the loop-filter are processing only quantization noise, a fact that relaxes the requirements from the first integrator [39] [40]. The final choice should be made with respect to the optimization of the total energy consumption of the ZCD per conversion that is needed in order to meet the target resolution (ENOB).

As presented in Chapter 1, the resolution specification for the improved self-timed ADC is ENOB $>$ 16.5bit. For the second-order modulator, with stable input range of $A_2 = 0.7V$, according to (2-7), the input-referred RMS noise specification of the ADC that achieves ENOB = 16.5bit is $v_{n,in,ADC2} = 6.1\mu V$. Similarly for a third-order modulator, assuming operation under the maximum (theoretical) stable input range of $A_3 = 0.67V$, the input-referred RMS noise specification is $v_{n,in,ADC3} = 5.85\mu V$, according to (2-7). Furthermore, from the analysis of subsection 2-2, the total input-referred noise of the ADC suffers from quantization noise and intrinsic noise of the transistors, with the input-referred noise of the first integrator to be assumed as the only intrinsic noise contributor for $N \gg 1$, and thus

$$v_{n,in,ADC} = \sqrt{\sigma_q^2 + k \cdot \frac{\overline{V_{n,in,INT1}^2}}{N}} \tag{5-1}$$

with $k = 4/3$ for a second order modulator and $k = 9/5$ for a third order modulator. Following the 40%:60% rule for the balance between quantization and thermal noise, we can estimate σ_q for total input-referred noise of ADC of $6\mu V$, resulting to $\sigma_q = 3.8\mu V$.

Based on the previous calculation of σ_q, the number of incremental cycles N can be estimated, making use of the $ENOB_q$ versus N plots of Figure 2-3, having as specification $\text{ENOB}_\text{q} = 17.5\text{bit}$ which corresponds to the target value of $\sigma_q = 3.8\mu V$. The corresponding approximate N was found to be $N_2 \simeq 1024$ and $N_3 \simeq 256$ for the 2^{nd} and 3^{rd} order modulators respectively. For the two cases, the specification of the input-referred RMS noise of the first ZCB integrator can be derived from

$$v_{n,in,INT1} = \sqrt{(\overline{V^2_{n,in,ADC}} - \sigma_q^2) \cdot \frac{N}{k}} \tag{5-2}$$

and the calculated values are $128.8\mu V$ and $55.4\mu V$ respectively. These specifications compared to the $v_{n,in,INT1} \simeq 200\mu V$ of the first prototype that was operating for $N_{init} = 500$, revealing the need to suppress noise by a factor of 3.6 for a third-order design and a factor of 1.56 for a second-order design.

In order to suppress the noise of the integrator, all the individual noise contributors should be suppressed. To establish a first-order estimate of the power penalty we will round the noise reduction factors to 4 and 2 respectively and consider only the noise of the preamplifier of the ZCD, because it is the most critical block for the energy consumption of the ZCB integrator. Also, if an inverter-based structure is employed to serve as a preamplifier, due to the inherent dynamic biasing of the inverter, the ZCD power consumption is dominated by the current that flows during the fine phase of the integrator and the current consumption of the preamp during auto-zeroing. The fine phase current consumption and is consisting of

- Current consumption during the preamp's response time t_i (depending on the designed $g_{m,tot}$ and $\frac{g_m}{I_d}$ of the transistors and is proportional to t_i)
- Current consumption of the preamp before V_X reaches virtual ground (depending on the designed $g_{m,tot}$ and $\frac{g_m}{I_d}$ of the transistors and the fine phase duration until V_X reaches virtual ground).

Similarly, the current consumption during autozeroing is depending on the designed $g_{m,tot}$ and $\frac{g_m}{I_d}$ of the preamplifier's transistors and is proportional to the autozeroing period.

As analyzed in subsection 3-2-2, the input-referred noise of the ZCD can be lowered by increasing g_m or decreasing the effective $NBW(t_i, \tau)$. Specifically, the input-referred noise of the ZCD is proportional to $\sqrt{NBW(t_i, \tau)}$ and inversely-proportional to $\sqrt{g_{m,tot}}$. If we decide not to alter NBW, $g_{m,tot}$ has to be scaled by $16\times$ for the 3^{rd} order modulator and $4\times$ for 2^{nd} order modulator to scale the noise contribution of ZCD to the desired levels. This means that the energy consumption of a single cycle increases by $16\times$ and $4\times$ for the two cases, with the overall energy consumption to scale with $\frac{N_3}{N_{init}} \cdot 16\times \simeq 8\times$ and $\frac{N_2}{N_{init}} \cdot 4\times \simeq 8\times$. If we decide to keep g_m the same and play only with NBW to meet the target noise specification for the ZCB integrator, the NBW should be reduced by $16\times$ and $4\times$ for 3^{rd} and 2^{nd} order case, respectively. For these requirements, according to (3-15), the designed t_i and τ pairs for the two cases should be $t_i = 1.04\mu s$ $(16\times)$ with $\tau > 1.06\mu s$ and $t_i = 260ns$ $(4\times)$ with $\tau > 280ns$. However, these options of $t_i = 260ns$ and $t_i = 1.04\mu s$ are not realistic, as they are

associated with a large increase of duration of the charge transfer, degradation of the linearity performance and probably unacceptable offset of the integrator. Besides, the increase of t_i to this level will make the noise design for the fine current source a hard task, posing the need of use of a large C_L which is not preferred.

On the other hand, a more realistic option is to operate with $t_i = 115ns$ (with $\tau > 130ns$) that leads to a decrease of the NBW by a factor of $\simeq 2$. In order to meet the noise specification in the two cases, $g_{m,tot}$ is needed to be adjusted accordingly. This strategy will require $8\times$ increase in $g_{m,tot}$ for the 3^{rd} order modulator and $2\times$ increase for the 2^{nd} order modulator. Thus, considering the increase of energy consumption in one cycle, we should expect the energy consumption of the fine phase before the virtual ground condition to increase by $8\times$, while the energy consumption during preamp's response increases by $16\times$ and the energy consumption of the autozeroing process increases by $8\times$ for the case of 3^{rd} order modulator. Similarly, 2^{nd} order modulator the single-cycle energy consumption scaling factors are $2\times$, $4\times$ and $2\times$ respectively. This will result to an increase of the overall energy consumption per conversion by slightly more than $\frac{N_3}{N_{init}} \cdot 8\times \simeq 4\times$ for the 3^{rd} order case and slightly more than $\frac{N_2}{N_{init}} \cdot 2\times \simeq 4\times$ for the 2^{nd} order case.

From this first-order estimation of the energy consumption scaling, we can conclude that utilizing a higher-order modulator topology is not necessarily helpful in order to improve the energy efficiency of a high resolution ZCB I$\Delta\Sigma$ ADC. Of course, the noise allocation plays very important role in the design, but the more relaxed $v_{n,in,INT1}$ specification of the 2^{nd} order modulator, in combination with the way that the energy consumption scales make the 2^{nd} order modulator more suitable candidate for improving the resolution and probably the energy-efficiency of the self-timed ADC.

Furthermore, the argument of using a second order topology is reinforced further by the presence of implementation difficulties in the design of a third-order modulator using ZCB integrators. First of all, a feed-forward (CIFF) modulator topology seems the best alternative, because of the lower sensitivity to integrators' non-idealities and lower swing of the first integrator. In a CIFF modulator, an analog adder is necessary before the quantizer, which for for single-bit $\Delta\Sigma$ converters can be implemented passively using switched capacitors [41]. In this case, a feed-through path is created between the first and third integrator outputs because they are operating during the same clock phase. In OTA-based implementations, this is not a problem as each OTA will force virtual ground at its input continuously. As the ZCB integrators only detect when the virtual ground condition and then turn-off their current source, it is evident that each integrator will turn-off at different times. As a result, while one integrator gets in idle state after the completion of the charge transfer and the other is still operating, the integrated voltage of the idle integrator will be corrupted by the other integrator, harming the operation of the whole ADC. This issue is solvable in principle, but proper operation dictates the use of more clock phases for the integrators with apparent expenses in conversion time, digital circuit complexity and power consumption. On the other hand, the feed-back (CIFB) topologies [17] do not suffer from this issue, as there is no feed-forward path between the integrators, but the significantly larger output swing of the first integrator [42] will make the linearity design of the first integrator tricky.

Consequently, because of the implementation difficulties of designing a 3^{rd} order CIFF modulator using ZCB integrators and the estimation that the utilization of a 3^{rd} order modu-

lator topology will not necessarily result to a more power efficient design of a higher resolution self-timed ZCB ADC, a 2^{nd} order $\Delta\Sigma$ modulator was decided to be used.

5-2-2 Matlab simulation of 2^{nd}-order modulator with input-FF path

Once it is concluded that the extension to a third order modulator is hardly beneficial, the reuse of the topology of Figure 2-1, that was used in [1], seems the most suitable option, mainly because of the limited output swing of the first integrator. The second-order modulator with input feed-forward path was simulated in Matlab, in order to obtain the output swings of the two integrators and estimate the quantization noise for $N = 1000$. In Figure 5-2 the results of this simulation are shown.

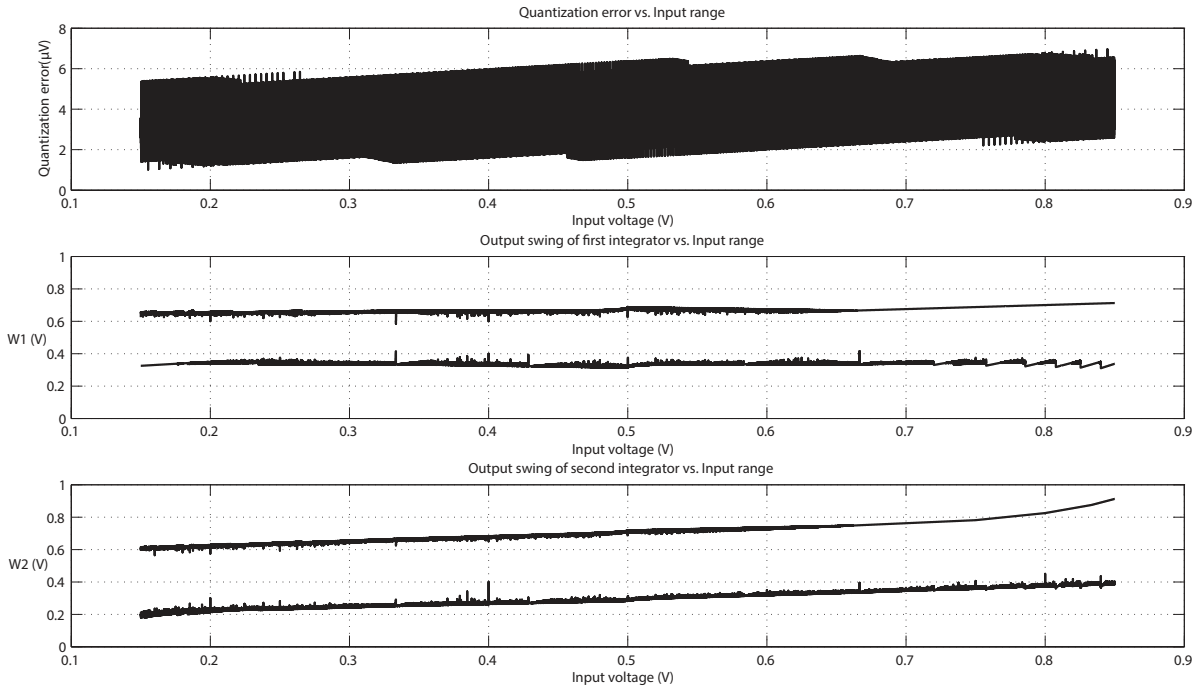


Figure 5-2: Quantization noise and integrators' swings for 2^{nd}-order modulator with input feed-forward path for $N = 1000$.

The swing of the first integrator was simulated to be limited to 300mV (from 0.35V to 0.65V), which will be really useful for the linearity design, because the simulated input-referred error of the ZCB integrator was observed to increase rapidly as the output swing increases. Also, an estimate of the quantization noise can be made, observing the quantization error range, which was $4.4\mu V$ in worst case. If this quantization error was uniformly distributed between its borders, the quantization noise standard deviation would be $\sigma_q = \frac{4.4\mu V}{\sqrt{12}} = 1.27\mu V$, but since it is observed busier close to the border, a margin around 30% should be taken into account. Thus, the quantization noise standard deviation should be estimated

after simulation as

$$\sigma_q = \frac{4.4\mu V}{\sqrt{12}} \cdot 1.3 = 1.65\mu V \tag{5-3}$$

This simulated value of σ_q is significantly lower than the theoretical value predicted by the analysis in subsection 2-2. The reason for this is that the swing of $w_2[N]$ is much lower than $[-V_{ref}, +V_{ref}]$ for the entire input range. This gives the opportunity to operate the converter, with a balance between quantization and thermal noise higher than 60%:40%. By allowing thermal noise to dominate, the specification of the input-referred noise of the first integrator will be relaxed. For instance, in order to arrive to a design with ENOB = 16.8bit (which corresponds to $v_{n,in,ADC} = 6.1\mu V$) with $N = 1000$, the specification of $v_{n,in,INT1}$ becomes $160.8\mu V$. This fact seems very beneficial and should be utilized in the design of a higher-resolution self-timed ADC with improved energy-efficiency.

5-2-3 Design space exploration for the implementation of ZCB integrator

Fully-differential ZCB integrator

Until now, only the single-ended implementation of the ADC was taken into account. However, a fully differential implementation is generally preferred, because the signal range is effectively doubled with simultaneous increase of input-referred noise of an integrator by a factor of $\sqrt{2}$. Thus, the SNR is inherently increased, creating the potential of reducing the power consumption. Also, a fully-differential implementation is typically less susceptible to power supply and ground noise and interference [31], while the effect of many non-idealities during the charge-transfer of the ZCB integrator (e.g. switch IR drops and switching effects) are in first-order cancelled by handling signals differentially.

Consequently, a fully-differential implementation of the ZCB integrator seemed very promising and was realized, including all the performance-enhancement methods (correlated level-shifting and uni-directional 2-phase charging scheme) that were used in [1]. Besides, a Common-mode feedback (CMFB) mechanism is mandatory in this implementation and this functionality was included. A circuit diagram of this integrator can be seen in Figure 5-3.

The operation of the fully-differential ZCB integrator is very similar with the single-ended one with the difference that the signals in two brances are following complementary trajectories. After preset, the positive output is ramping down, while the negative output is ramping up, until the point that the early threshold condition is detected by the differential ZCD, as visualized in Figure 5-4. Then, during the fine charging phase, the two branches are settling with much lower ramp rates until the moment of virtual ground detection by the ZCD.

In this implementation, two CMFB alternatives have been investigated: A conventional switched-capacitor CMFB circuit [43] and a differential-difference amplifier (DDA) based CMFB topology [44] (using a simple current-mirror OTA). In both cases, the CMFB signal is controlling the gates of both coarse-fine charging NMOS current sources in order to stabilize the output common-mode to $\frac{V_{DD}}{2}$. Both the alternatives were verified through simulation, where it was observed that the the output common mode was effectively stabilized during the coarse phase roll-off.

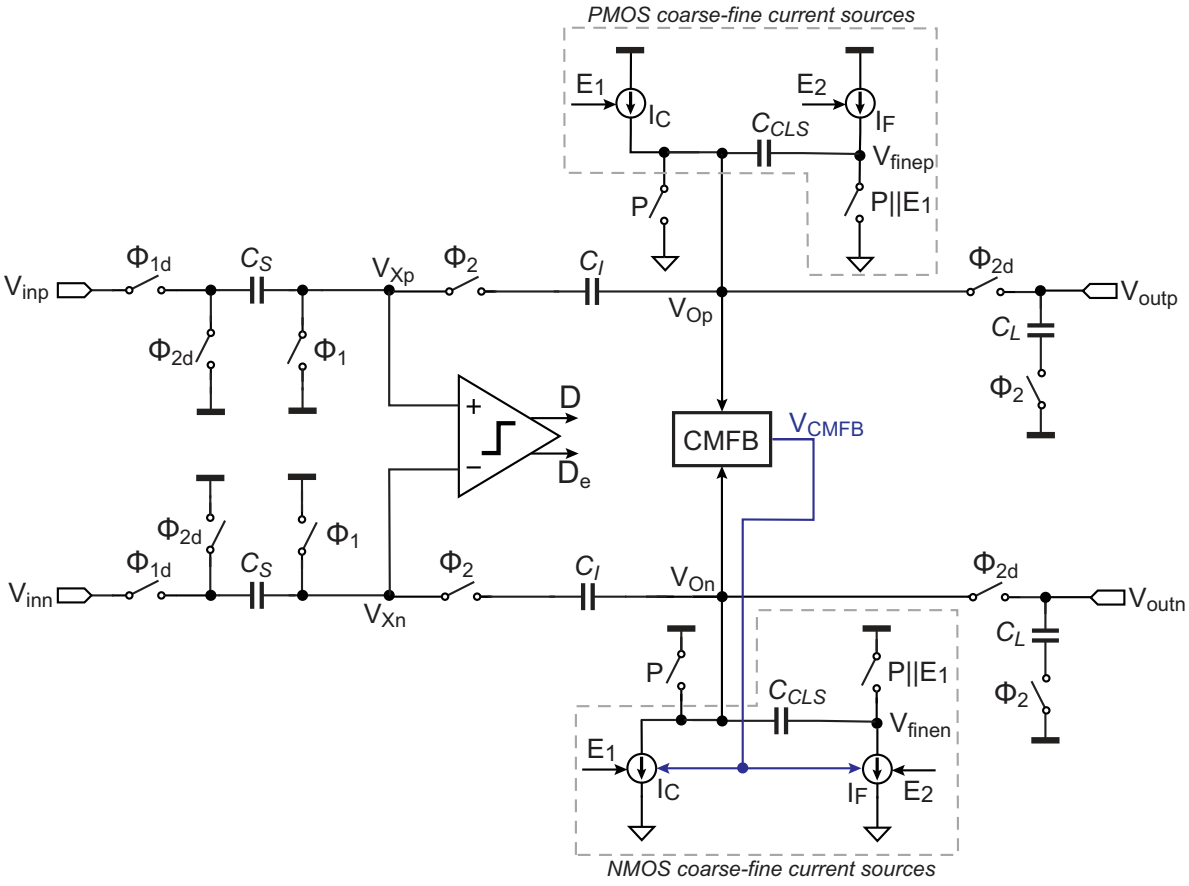


Figure 5-3: Circuit diagram of the fully-differential ZCB integrator with CMFB.

The first step towards the realization of a fully-differential ZCB integrator, before the noise design, is the estimation of its non-linearity, following the procedure of simulation of the signal-dependency of the input-referred error. In this step, it became clear that the realization of the differential structure performing with linearity above 16bit is a hardly achievable task within the timeframe of this project. The topology of Figure 5-3, was built using ideal switches and capacitors and a Verilog-A [45] model for the ZCD (tunable delay). Operating the ZCD without delay, the simulated range of the integration error across an output range of $[-0.3V, 0.3V]$ was approximately $185\mu V$ which results to a signal-dependent input-referred error range of $740\mu V$, which has a significantly non-linear inverse-U shape. This is predicted to lead to an achievable linearity for the ADC around the level of 11bit, which is far below the target of this design.

A possible reason for the large signal-dependent error range that was observed in simulation was the systematic mismatch between NMOS and PMOS current sources off-transients at the end of fine phase. Although the output common-mode is effectively stabilized before the turn-off of the coarse current sources, a large common-mode jump is observed at the coarse current sources turn-off moment. This jump is heavily signal dependent and cannot be corrected during the fine phase because of the small magnitude of fine currents. This common-mode instability, however, is expected to be tolerable (and/or correctable) in the

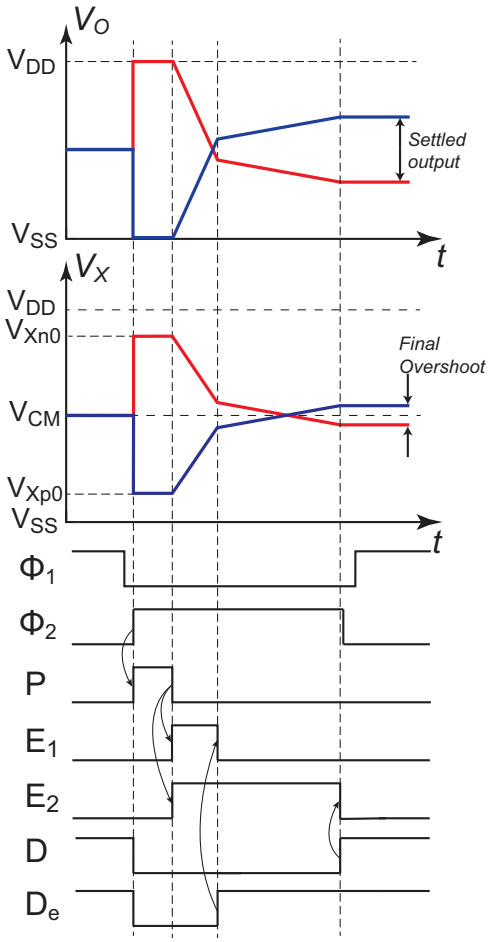


Figure 5-4: Signal waveforms of the fully-differential ZCB integrator during charge transfer.

context of a $\Delta\Sigma$ modulator, as it is expected to lead to common-mode error of the integrator. In contrast, this heavily signal-dependent coarse phase overshoot at the output, that is caused by the asymmetry off-transients of the NMOS-PMOS current sources is affecting the swing of the fine current sources. This is expected to further contribute to the asymmetry of the fine current sources off-transients. After this experiment, it was decided that a fully-differential topology is hardly realizable within the timeframe of this project, because of the high (simulated) signal-dependency of the input-referred error of the integrator.

Pseudo-differential ZCB integrator

Although, a fully-differential implementation seems not a realistic target for this project, a pseudo-differential topology for the ZCB integrator is feasible, employing two single-ended integrators for the two branches. A circuit diagram of the pseudo-differential alternative can be seen in Figure 5-5. Since, there are only NMOS charging current sources, the non-linearity issue of the differential integrator is not present anymore and the signal-dependent error of the integrator can be brought to the desired level. The operation of the pseudo-differential integrator is very similar to the single-ended one, as the two branches are operating indepen-

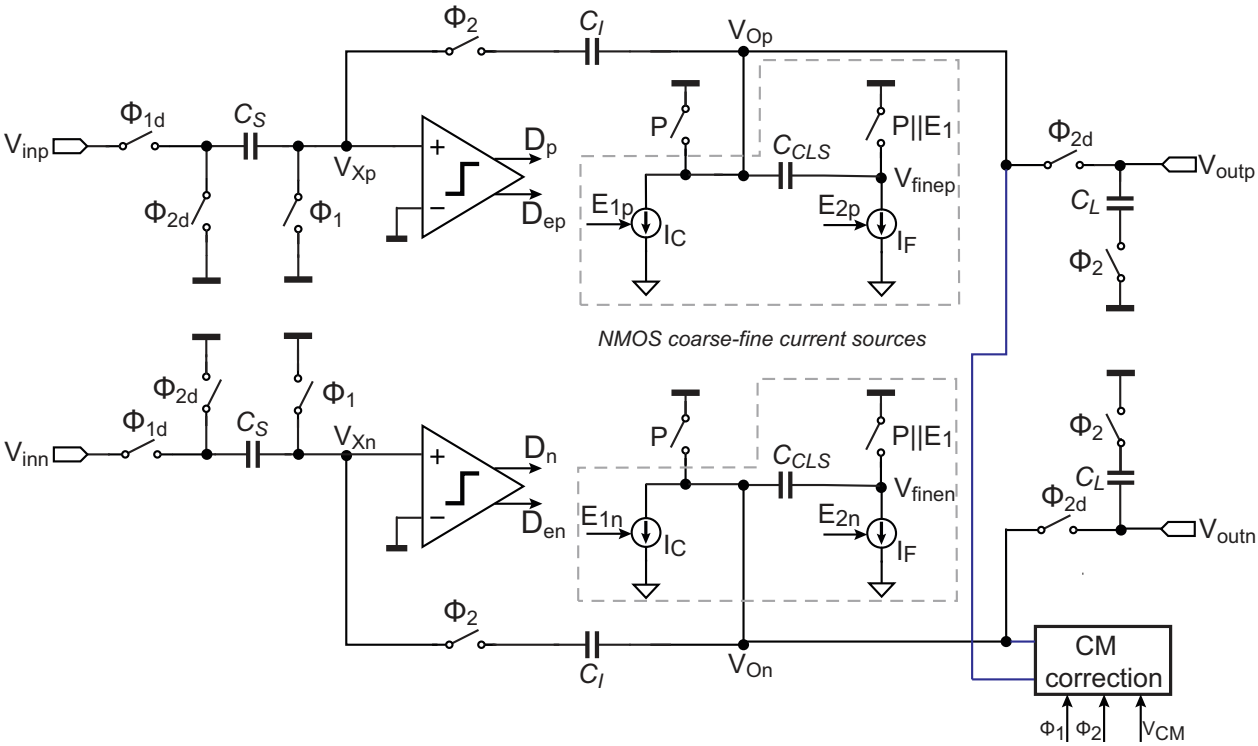


Figure 5-5: Circuit diagram of the pseudo-differential ZCB integrator with CM correction.

dently and the only difference is that the output is sensed differentially. The underlying signals during the charge-transfer phase are visualized in Figure 5-6. Also, in the pseudo-differential topology there is no special need for common-mode control during the charge transfer phase, as the mismatch between same type (NMOS) current sources is less severe compared to the fully-differential integrator where different type of current sources (NMOS-PMOS) are used in the two branches.

However, because of the fine phase overshoot at the end of the charge transfer, the common-mode of V_O and V_X signals is gradually drifting downwards (common-mode error accumulation) if we operate the integrator multiple times. This potentially harmful to the correct operation in context of an incremental ADC and necessitates the use of a mechanism that corrects the common-mode of the integrated voltage after the completion of the charge transfer (i.e. during the next sampling phase of the integrator). This can be done using small current sources that are pulling up the output nodes of both branches simultaneously until the common-mode is reaching $\frac{V_{DD}}{2}$. This condition is sensed by an auxiliary low-power comparator which is comparing the output common-mode (sensed using a capacitive averaging) with the reference common-mode level V_{CM} [8]. Because the magnitude of these current sources is very small, the residual common-mode error is almost negligible. Following this strategy, common-mode error accumulation is prevented, making the pseudo-differential architecture a feasible alternative for the design of the self-timed IΔΣ ADC.

Considering the achievable performance using the pseudo-differential structure, the signal-dependent integration error for output range between [-0.3V , 0.3V] is expected to be doubled in worst case compared to the single-ended architecture, if we do not take into account the

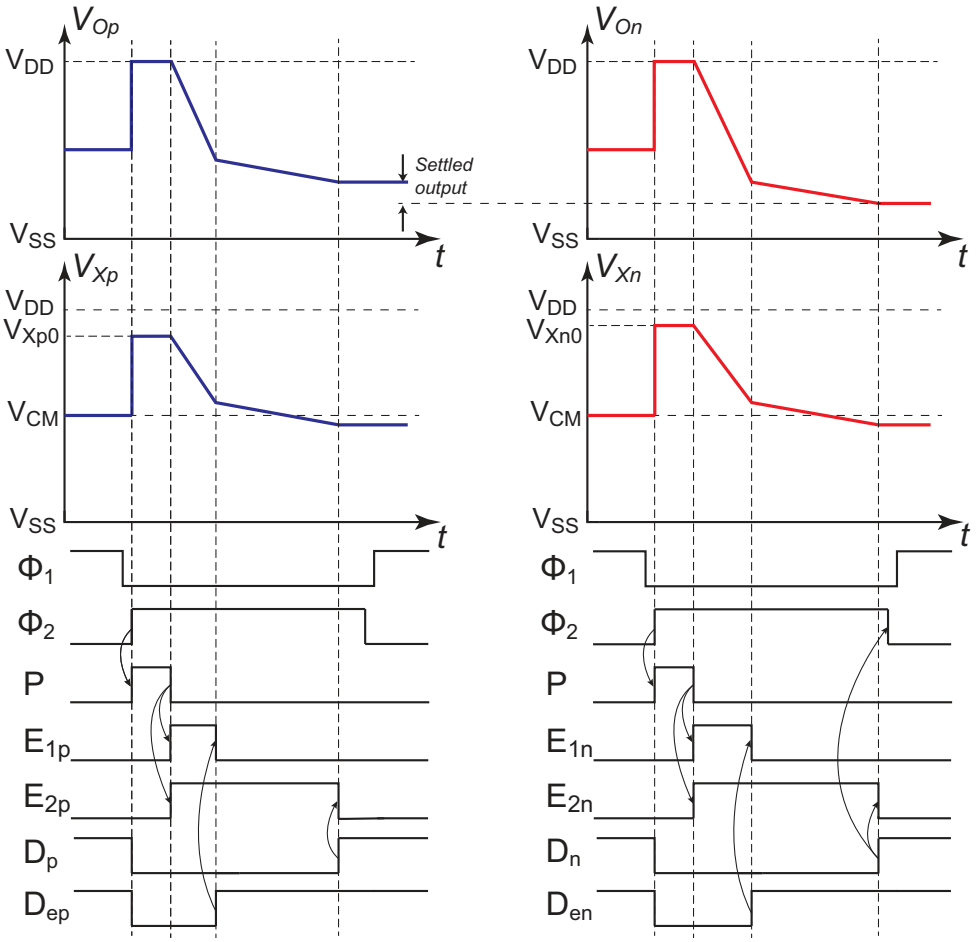


Figure 5-6: Signal waveforms of the pseudo-differential ZCB integrator during charge transfer phase.

cancellation of second-order non-linearity. But, since the input signal range is doubled the linearity of the ADC is not degraded even in this worst case estimation. This is making the pseudo-differential alternative a competitive counterpart of the single-ended architecture, as the potential of first-order cancellation of various non-idealities and elimination of second-order non-linearity are present. Examining the noise behavior, the input-referred noise of the pseudo-differential structure is $\sqrt{2}\times$ higher, thus the SNR is better. On the other hand, the power consumption is effectively doubled, resulting to an energy-efficiency which is equal with the single-ended implementation. Finally, because of great shortage in design time during this project, it was decided not to implement the pseudo-differential ZCB integrator, although it poses tangible benefits especially in the linearity behavior.

As a result, after examining all the possibilities related to the extension to a differential implementation of the integrator, it was concluded that the most realistic alternative for this project is to stay with the single-ended structure for the implementation of the ZCB integrator. A fully-differential integrator turned out to be a not realizable target within this project, as it was estimated that it cannot provide the accuracy that is required. Regarding the pseudo-differential structure, it was adjourned, although it was recognized to pose certain benefits

regarding its linearity behavior, without any degradation in energy efficiency (compared to the single-ended structure), mainly because of great shortage in design time. As a result, in this project the single-ended ZCB integrator was reused. Optimizing its performance towards achieving the specifications set for this project could potentially lead to a design that has superior energy-efficiency. This optimization for noise and linearity is following.

5-3 Noise and linearity design of the ZCB integrator

5-3-1 Noise design

Balance of the noise contributors and circuit-level design choices

The noise design is based on the analytical noise estimation of the ZCB integrator that developed in section 3-2. Specifically, all the apparent noise contributors have to be suppressed and balanced accordingly. According to prior analysis in this chapter, in order to achieve ENOB=16.8 bit using the second-order modulator with $N = 1000$, the specification of total input-referred noise of the first integrator is $v_{n,in,INT1} = 160.8\mu V$. In order to have proper design margin, our design will over-suppress the noise of the integrator aggressively, setting the target to $v_{n,in,INT1} \simeq 100\mu V$. Furthermore, in the new design, the total charge transfer duration is decided to be approximately the same with the first prototype, in order to avoid conversion time overhead. As a result, the specification of the charge-transfer duration is $T_{cycle} \simeq 500 - 550ns$.

First of all, the capacitance levels have to be scaled up and C_S is set to $1.2pF$ with $C_I = 4.8pF$ in order to lower the sampling kT/C_S contributor. The most important design choice is, though, the effective noise-bandwidth, as it plays dominant role for the noise of the ZCD and switches during the preamplifier's response time. In order to lower $NBW(t_i, \tau)$, the preamplifier's response time t_i has to increase while the energy consumption is also increasing. Thus, it is not suggested to operate with $t_i > 120ns$. However, we would like to NBW to be around $2\times$ lower compared to the designed value of the first prototype, thus the target for NBW was set to $\simeq 4.1MHz$. According to (3-15), for $t_i = 115ns$ and $\tau \simeq 140ns$, the effective noise-bandwidth becomes $NBW < 4.6MHz$. Since it is not suggested to operate with higher t_i, it was decided to scale the g_m of the preamp and apparently the equivalent noise resistance of switches R_{eq} in order to achieve adequate values of the ZCD and switches noise contributors.

For the noise of the ZCD, an increase of the g_m is needed and a value of $g_{m,tot} = 450\mu A/V$ was chosen. This increase of the g_m was possible with a substantial increase of the power consumption as will be explained later. Next, the switches noise during preamplifier's response time should by any means be dominant and this contributor can be further suppressed without any significant power consumption penalty by reducing the equivalent noise resistance R_{eq} at V_X. Therefore, wider switches have to be used along the integrator's feedback path and the designed values for the on-resistances are: $R_{on2} = R_{on3} = R_{on4} \simeq 800\Omega$ and $R_{on1} \simeq 600\Omega$. The required width for for R_{on2}, R_{on3} and R_{on4} is $1.2\mu m$. Regarding the bitstream controlled (unboosted) feedback NMOS and PMOS switches which correspond to R_{on1}, the required widths are $1.6\mu m$ for the NMOS switch and $4.2\mu m$ for the PMOS switch.

For the aforementioned design choices, the input-referred noise of the ZCB integrator is estimated to be $v_{n,in,INT1} = 94.8\mu V$. In the new design, the sampling noise kT/C_S is dominating although this is not optimal in terms of energy-efficiency, as lowering the noise of the preamplifier requires higher energy consumption than the suppression of the sampling noise. However, during the design time of this project, the updated measurement results of the first prototype, that presented in Chapter 4, were not available, so the validity of the noise model was not proven. As a result, it was decided to suppress more aggressively the contributors that are related with the charge transfer of the ZCB integrator, as an extra safety measure to guarantee that the targets that were set for this project will be met in the end.

ZCD implementation

The architecture of the ZCD will be very similar with the ZCD of the first prototype, seen in Figure 2-9, as again will be consisting of a transconductance preamplifier and a wide-band crossing detector. The early-threshold generation mechanism is not subject to change, as this is the common way to realize such functionality [4] and any problem was identified to be associated with it. The wideband crossing detector is again a chain of two inverters, as this is the most energy-efficient alternative, but they are slightly downsized in order to save power, at the expense of a small increase of the signal-independent delay time t_c.

For the realization of the preamplifier, an inverter-based structure is preferred, because of the double transconductance $g_{m,tot}$ that is achievable for a given drain current and its inherent dynamic biasing characteristic. Possible candidates for the inverter-based implementation of the preamp are the class-AB inverter amplifier, the cascode-inverter amplifier and the current-starved inverter amplifier, that are shown in Figure 5-7. The cascode-inverter amplifier is superior to the simple inverter amplifier, by means of achieving much higher output resistance and thus providing higher DC gain. In the design of the preamplifier, however, there is no special need for very high output-resistance of the preamplifier, as the preamplifier's time constant τ is possible to be tuned via the band-limiting capacitor C_{lim}. As a result, the alternative of the cascode inverter was not utilized. On the other hand, the current-starved inverter amplifier is employing a current source between the supply and the transistors of the inverter that is providing a regulated supply $V_{DD,inv}$ to the inverter, improving significantly the supply noise rejection of the structure. The disadvantage of the current starved inverter amplifier is that V_{DD} needs to be increased in order to maintain the inverter in its optimal bias point.

Typically, the optimal bias point of a Class-AB inverter amplifier is at the boundary between weak and strong inversion regions [14]. According to [25],[14] the optimal supply voltage of a Class-AB inverter amplifier that is providing operation at the boundary between weak and strong inversion is $V_{DD,optimal} = V_{TN} + |V_{TP}|$, where V_{TN}, V_{TP} are the threshold voltages of the NMOS and PMOS transistors. In the $0.16\mu m$ CMOS process [46], $V_{TN}+|V_{TP}|$ is slightly lower than 1V, so the V_{DD} of the inverter is set to 1V, similar to the previous design [1]. Taking this into account, in the current-starved inverter topology, since we want to bias the inverter at its optimal bias point $V_{DD,inv} = V_{TN} + |V_{TP}| \simeq 1V$, the supply voltage V_{DD} has to be increased, in order to leave voltage headroom for the current source to operate in saturation. It is noteworthy that from the measurement results of the first prototype, the supply noise disturbance does not seem to degrade significantly the performance of the ADC,

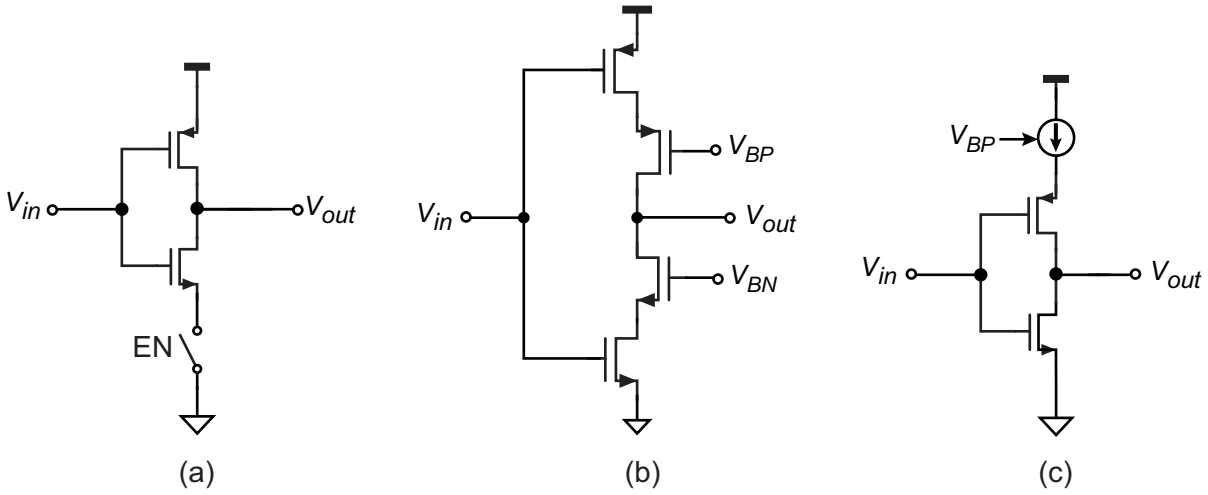


Figure 5-7: Alternatives for the inverter-based implementation of the preamplifier: (a) class-AB inverter amplifier, (b) the cascode-inverter amplifier and (c) the current-starved inverter amplifier.

thanks to the auto-zeroing of the ZCD, the noise shaping of the modulator and the correlated level-shifting mechanism, as analyzed in [14] and [25]. As a result, utilizing the current-starved inverter seems not necessary in this implementation and was decided to employ the simple class-AB inverter amplifier, that was used also in the first prototype, keeping the supply voltage at 1V. This topology was resized accordingly in order to fit in our needs and optimized with respect to optimal power-efficiency.

The inverter structure, loaded by the band-limiting capacitor C_{lim}, should be sized in order to operate with a delay of $t_i = 115ns$ using $I_F \simeq 100nA$, have a time constant $\tau \simeq 135ns$, providing $g_{m,tot} \simeq 450\mu A/V$ at the moment of input-threshold crossing. The sizing of the preamplifier that is fulfilling these requirements is shown in Figure 5-8. The value of C_{lim} that is necessary is $0.6pF$.

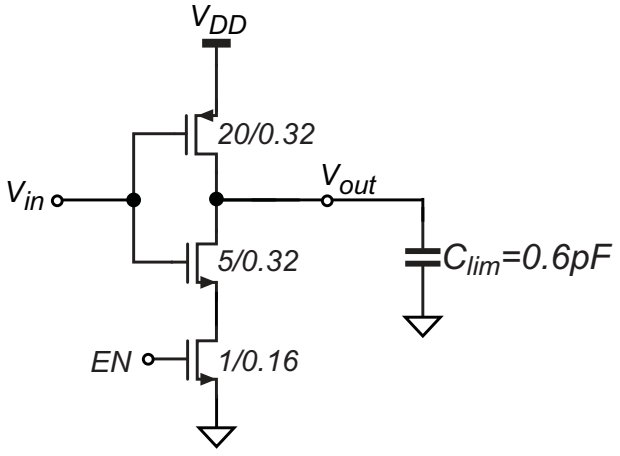


Figure 5-8: Sizing of the inverter-based preamplifier for the first integrator.

In Figure 5-9, the operating point of the designed inverter is compared with the inverter

used in the first prototype. The transconductance efficiency was optimized by pushing the operating point of the transistors closer to weak-inversion [32], achieving g_m/I_d ratio for both the transistors of the new inverter larger than $18.25V^{-1}$, while in the previous design the transconductance efficiency was around $16.1V^{-1}$.

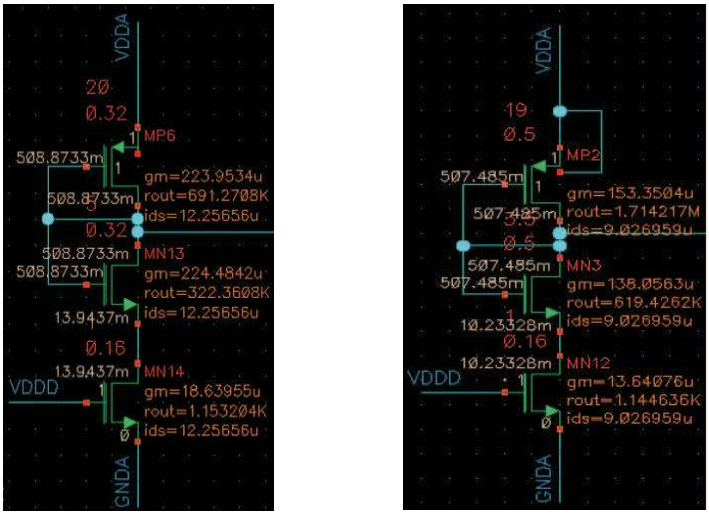


Figure 5-9: Comparison of the operating points of ZCD inverter-based preamplifiers: (a) proposed design, (b) preamplifier used in [1].

In order to verify the argument of cancellation of the flicker noise by employing auto-zeroing, the input-referred noise of the preamplifier was simulated. The input-referred noise PSD was obtained and the $1/f$ noise corner frequency is well below the f_{AZ}. Consequently, the effect of $1/f$ noise of the transistors of the preamplifier, is not expected to contribute significantly to the total input-referred noise of the integrator.

The noise design of the ZCB integrator should be, of course, verified with simulations before proceeding with the design of the other building blocks of the ADC. The simulation results for the input-referred noise of the integrator and the power consumption during the charge-transfer phase are presented in section 5-4.

5-3-2 Linearity design

The linearity design of the ZCB integrator was based on the simulation of the signal-dependency of the input-referred error, taking into account the design choices that are imperative for the noise performance. The linearity optimization process of the integrator was involving Verilog-A modeling of the current sources and use of ideal models for switches in order to examine the importance of the various sources of non-linearity that described in section 3-3.

First of all, after up-sizing the capacitors and keeping the fine current source current level to around $100nA$, the signal dependent input-referred error was already improved and its simulated range was $[-9.155\mu V, 9.155\mu V]$. At this point, in order to bring this range well below $10\mu V$, which is expected to be enough to achieve INL for the ADC better than 1LSB of 16bit, multiple experiments were done by replacing the actual implementation of various

building blocks by ideal models in order to find out the dominant source of non-linearity. The possible suspects were the switches and the current sources, with the ramp-rate non-linearity and the off-transients to be considered.

When replacing the switches with ideal models having the proper values of on-resistance, the simulated signal-dependent error did not change significantly and was concluded that there is no severe problem coming from the switching effects. In contrast, when the current sources were replaced with Verilog-A models having proper output resistances, the signal-dependency of the error was drastically reduced. Also, when only the fine current source was replaced by a Verilog-A model, the signal-dependency was also improved compared to the real case, but was a bit worse than the previous test case with both the current sources replaced by Verilog-A models. Interestingly, when the output resistances of the current sources used in the Verilog-A model were scaled by a factor of 100, the signal-dependent error was not observed to reach the level of the simulation with real current sources. From these series of experiments, it was concluded that the ramp-rate induced non-linearity is not the dominant non-linear mechanism of the charge-transfer process. However, the linearity degradation was assumed to come from the off-transients of the fine current source, with the off-transients of the coarse current source contributing marginally to the ramp-rate induced non-linearity.

After these experiments, the actual design of the current sources was revisited in order to bring the signal-dependent error in spec. Because the off-transients of a cascode current source are related with the area of the bottom transistor, this had to be downsized at the possible expense of lowering the output-resistance. Furthermore, it turned out that the coarse current source is not necessary to be downsized. Both the designed coarse and fine current sources along with their biasing schemes are shown in Figure 5-10.

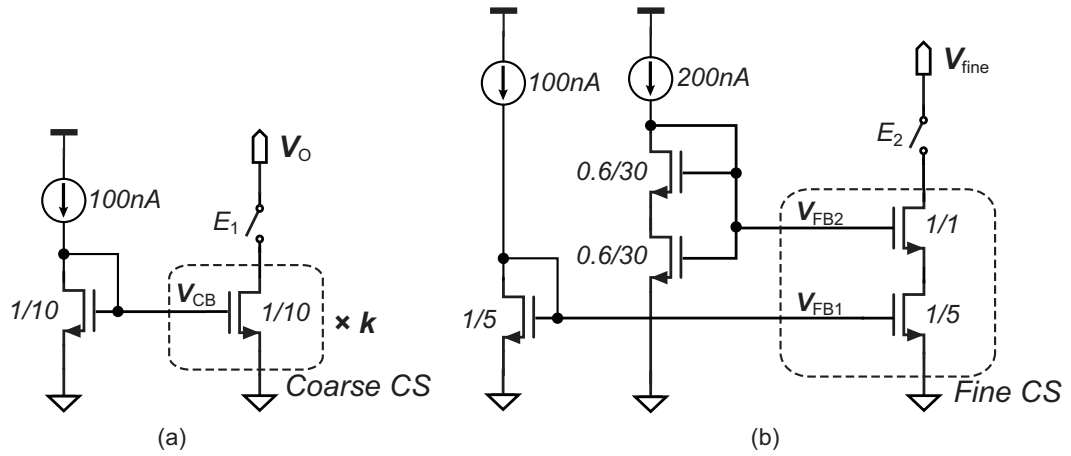


Figure 5-10: Sizing and biasing of charging current sources. (a) Coarse current source, (b) Fine current source

The simulated output resistance of the coarse current source was $R_{out,coarse} = 840M\Omega$, while the output resistance of the fine current source is higher than $26.8G\Omega$ and varies around 2% with its output voltage V_{fine}, as V_{fine} is swept from 720mV to 960mV.

With these design choices and adjustments, the input-referred signal-dependent error of the ZCB integrator was simulated and is visualized in Figure 5-11. The signal-dependent error range, after downsizing the fine current source and using $C_{CLS} = 0.2pF$, was only $5.2\mu V$,

which is expected to be enough to improve the INL of the ADC and push it lower than 1LSB of 16bit. The simulated average charge-transfer duration of the ZCD was $T_{cycle} = 535ns$, with the fine phase was lasting approximately $T_{fine} = 320ns$ on average.

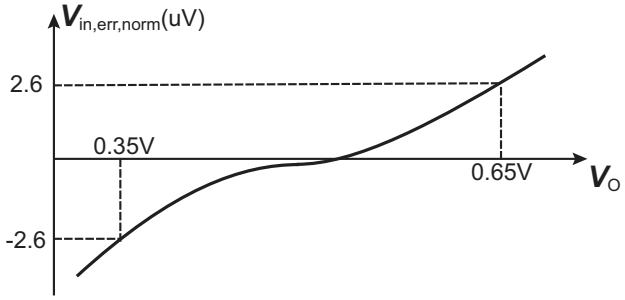


Figure 5-11: Normalized input-referred error of the ZCB integrator.

5-4 Simulation results of the ZCB integrator

The design of the ZCB integrator should be extensively verified by simulation and the simulation results for noise and linearity performance, as well as the power consumption are presented here.

5-4-1 Input-referred noise

The verification of the noise design can be done by means of transient noise simulation or PSS/Pnoise simulation using SpectreRF [47], because we are dealing with a sampled data system which is subject to noise aliasing [48].

The testbench for the PSS/Pnoise simulation of the input-referred noise is shown in Figure 5-12 where the ZCB integrator is used in unity-feedback configuration with the use of two ideal sample-and-hold circuits (implemented in Verilog-A), according to the guidelines in [49] and [47]. This configuration is ensuring the convergence for the PSS/Pnoise simulation and is typically used for such purpose.

The outcome of this simulation was that the input-referred noise of the integrator is $v_{n,in,INT1} = 122.5\mu V$. For the sake of comparison, the first integrator of [1] was simulated using the same testbench, resulting in $v_{n,in,INT1} = 189.22\mu V$.

Performing a transient noise simulation of the ZCB integrator keeping the input voltage fixed to $V_{in} = 0.5V$ and capturing the integrated voltage in the end of each cycle, we can calculate the standard-deviation of the integrated voltage. Using 15 cycles for the transient-noise simulation we get $\delta_{V_I} = 30.075\mu V$. Scaling with the inverse of the integrator's constant $\frac{C_I}{C_S}$, we obtain the input-referred RMS noise of the integrator. The result of this was an input-referred noise of $v_{n,in,INT1} = 120.3\mu V$.

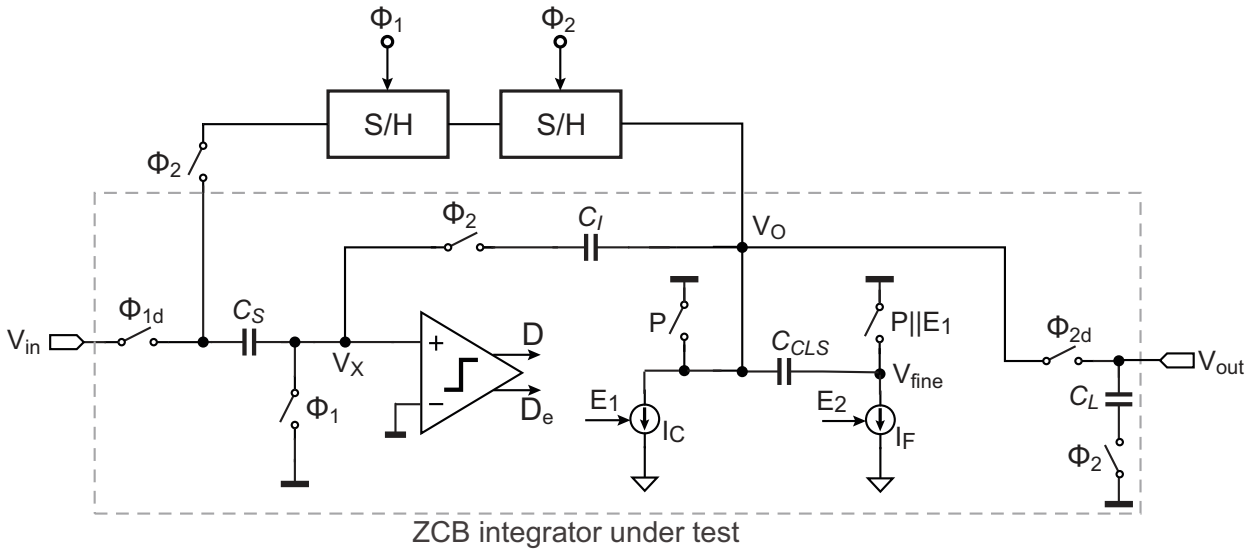


Figure 5-12: Simulation testbench for the input-referred noise of ZCB integrator.

5-4-2 Input-referred error over process corners

The first step in the linearity verification of the ZCB integrator over process corners is to ensure that the current source is functional over all the corners achieving, preferably, output impedance higher than $20G\Omega$. The simulation result of the output-resistance over the 5 corners is summarized in Table 5-1.

Table 5-1: Simulated fine current source output impedance over process corners.

Process corner	Fine current source output resistance
nominal	27.5 GΩ
snsp	29.9 GΩ
fnfp	24.7 GΩ
snfp	35.6 GΩ
fnsp	19.1 GΩ

As a next step, the linearity of the ZCB integrator is simulated over corners, demanding the signal-dependent error to remain in spec under process variations. Unfortunately, it was observed that the integration error behavior is very sensitive to process variations with the integrator operation collapsing in different corners. The main reason of this problematic behavior was found to be the transition from coarse to fine charging phase. For example, in the slow corner, the transition was happening too late, after the virtual ground was reached, making the integration error dominated by the non-linear coarse phase overshoot. In fast corner, the transition was happening too early, increasing very much the swing of the fine current source which was collapsing ($V_{fine} < V_{min}$) before the virtual ground condition establishment. The latter made the signal dependency of the integration error dominated by the ramp-rate variation, as the output resistance of I_F much lower than its designed value. Fortunately, the offset voltage of the early-threshold generation mechanism V_{off} can act as a trimming node and the proper operation of the ZCB integrator can restored over all process

corners. After extensive simulation, the optimal values of V_{off} that is needed to achieve this were found and the input-referred error was brought in spec. The results of this procedure, including the preamp's response time in every process corner are summarized in Table 5-2.

Table 5-2: Input-referred error of ZCB integrator over corners

Process corner	Input-referred error range	t_i	average T_{cycle}	V_{off}
nominal	$5.2\mu V$	115ns	535ns	446mV
snsp	$10.82\mu V$	224ns	805.2ns	492mV
fnfp	$22.04\mu V$	57ns	540ns	395mV
snfp	$8.46\mu V$	109.7ns	573.3ns	500mV
fnsp	$9.15\mu V$	86.5ns	572ns	393mV

5-4-3 Power consumption

The current consumption of the designed ZCB integrator during charge-transfer phase can be monitored using transient simulation, capturing the currents flowing to ground node. The result of this simulation is shown in Figure 5-13. In this figure, the current of the analog part of the ZCD (inverter preamp) is colored red, the current of the digital part of the ZCD (WCD) is colored green and the current of the rest analog circuitry of the integrator (including the current sources and the current reference) is colored blue.

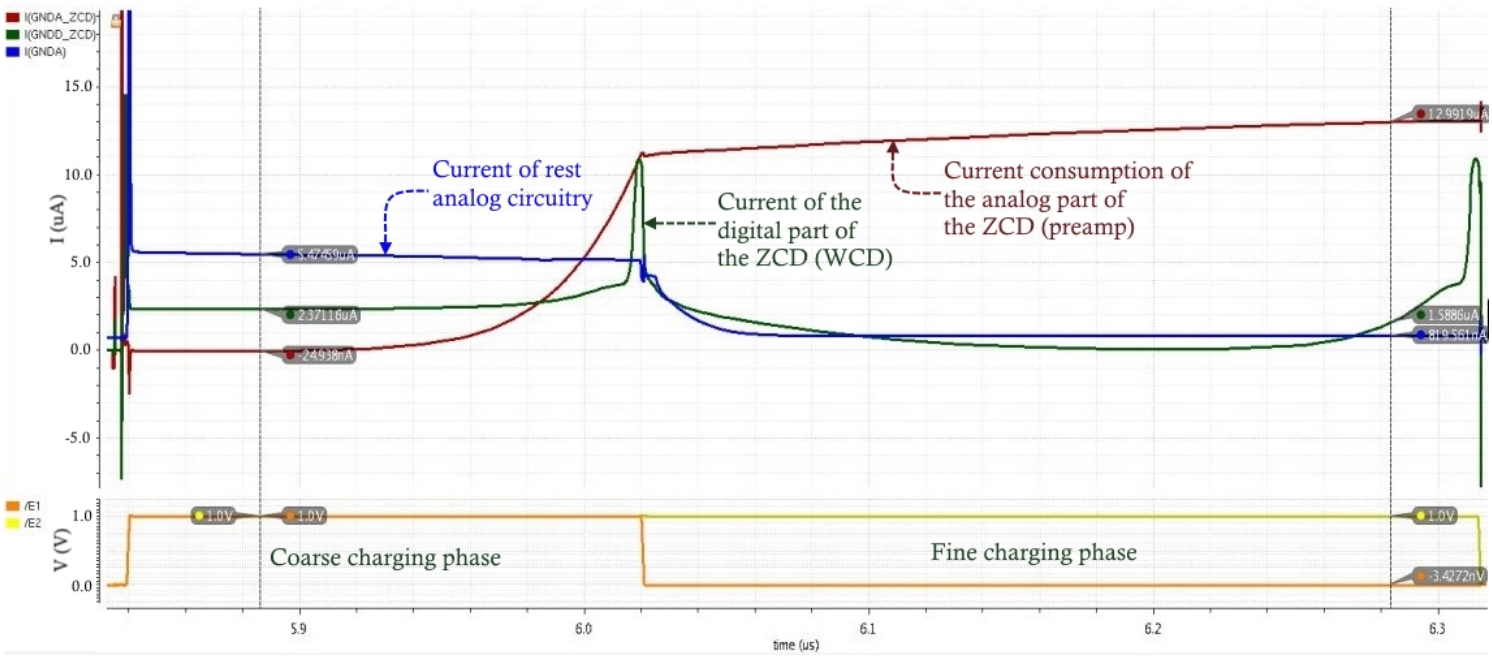


Figure 5-13: Simulation of current consumption of ZCB integrator during charge transfer.

The maximum analog current level is increased by approximately 25%, compared to the first prototype, while the total energy consumption during the charge transfer is expected to increase by a factor of 2×. However, the total energy consumption is not necessarily scaling

by 2×, as a big proportion of energy is consumed during the autozeroing process of the ZCD, which can be optimized by reducing the autozeroing duration which is happening during the fine phase of the second integrator. This will be discussed in the design of the second integrator in section 6-1.

5-5 Summary

In this chapter, the design of the first ZCB integrator for the improved self-timed IΔΣ ADC was treated, after exploring the various system-level modifications that were in principle possible. After realizing that a fully-differential implementation is not possible because of its bad linearity and the shortage of design time that did not permit the realization of the pseudo-differential topology, the new design was decided to be single-ended. Regarding the modulator's topology and order, it was concluded that a higher-order topology would not necessarily lead to improved energy-efficiency so the new design will be based on the same topology as the first prototype.

The improvement in resolution, linearity and energy-efficiency will come, primarily, from the smart design of the first integrator and proper noise allocation. In this chapter, the ZCB integrator was sized in order to achieve input-referred noise and input-referred error that is expected to lead to resolution and linearity better than 16bit, with the lowest possible overhead in power consumption. Generous design margin was taken into account in all design choices in order to ensure the validity of the design, and all the choices were extensively verified by simulations.

Chapter 6

Final Realization

This chapter describes the implementation details of the new prototype self-timed ZCB I$\Delta\Sigma$ ADC, except for the design of the first integrator that was treated in the previous chapter. The discussion starts with the design of the second ZCB integrator of the ADC and continues with a short presentation of the auxiliary circuits, such as the clock boosters, the bitstream quantizer and the current reference that are to great extent reused from the previous design [1], as their proper functionality is proven. After that, the layout of the new test-chip is given and then the pre-layout and post-layout simulation results of the new design, including resolution, linearity, conversion time and power consumption are presented. Finally, the performance summary of the new design and comparison with the state-of-the-art designs of CBSC/ZCB $\Delta\Sigma$ ADCs and OTA-based $\Delta\Sigma$ targeted for sensor interfacing are given.

6-1 Design of the second ZCB integrator

The requirements of the second integrator of the modulator is significantly relaxed compared to the first integrator in terms of noise and linearity. As a result, the second integrator should be a scaled version of the first integrator in order to minimize its power consumption.

In this design, the capacitor levels of the second ZCB integrator were scaled with a factor of 2, thus $C_{S2} = C_{L1} = 0.6pF$ and $C_{I2} = 1.2pF$, $C_{AZ2} = 1.2pF$ and the load capacitor of the integrator was chosen to be $C_{L2} = 0.2pF$. Also, the preamplifier of the ZCD, which is the most current-consuming element of the integrator was scaled with a factor of 4. The sizing of the second preamplifier is shown in Figure 6-1. This sizing resulted to scaling of the maximum current of the preamp by a factor of 4, being $I_{preamp2,max} = 3.37\mu A$, achieving total transconductance of $g_{m,tot2} \simeq 120\mu A/V$ as can be seen in Figure 6-1, where the operating point of the second preamplifier is attached.

Furthermore, when the second integrator is employed in the context of a self-timed $\Delta\Sigma$ modulator, the timing of the two integrators can be asymmetrical and the charge transfer can be designed to be faster in order to obtain savings in conversion time of the ADC. More importantly, since the auto-zeroing of the preamplifier of the first integrator is performed

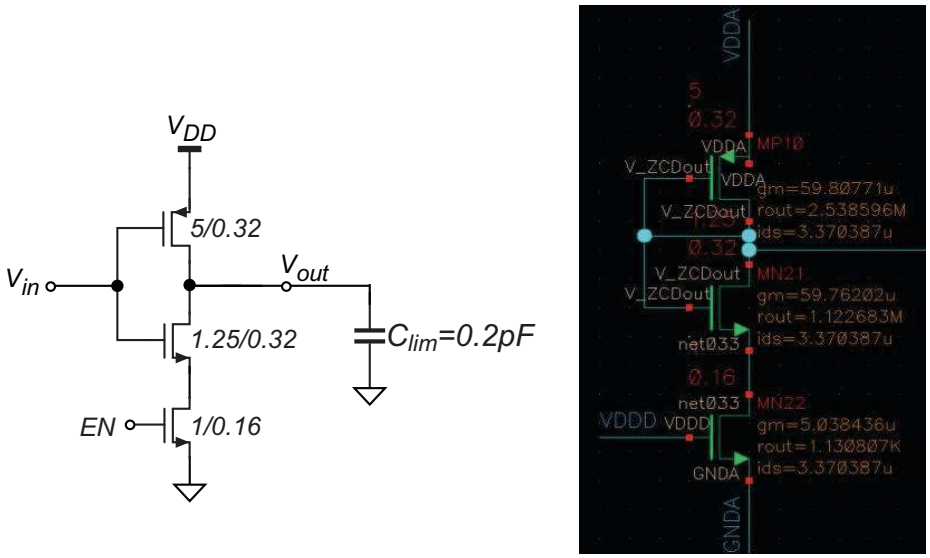


Figure 6-1: Sizing and operating point of the inverter-based preamplifier of the second integrator.

during the fine phase of the second integrator, the fine charge transfer duration is a critical parameter for the energy consumption of the first integrator. The reason for this is that during auto-zeroing the maximum current is flowing through the inverter amplifier. The minimum duration of the auto-zeroing is dictated by the auto-zeroing time constant

$$\tau_{AZ} = \frac{C_{AZ} + C_{lim}}{g_{m,tot}} \tag{6-1}$$

Taking a conservative estimation, the minimum time required for the auto-zeroing operation to be $10\times$ the auto-zeroing time constant. Thus, for the first ZCB integrator with $g_{m,tot} = 450\mu A/V$, $C_{AZ} = 3.6pF$ and $C_{lim} = 0.6pF$, the minimum auto-zeroing time is

$$T_{AZ1,min} = 10 \cdot \tau_{AZ1} = 10 \cdot \frac{C_{AZ1} + C_{lim1}}{g_{m,tot1}} = 93.3ns \tag{6-2}$$

Consequently, in order to avoid unnecessary static power consumption due to auto-zeroing of the first preamplifier, we have to design the second integrator to have fine-phase duration around $T_{fine2} \simeq 100ns$ or apply smart control of the auto-zeroing process introducing extra complexity in the digital circuitry. The first solution was preferred and accomplished by adjusting the magnitude of the fine current source. Setting $I_{fine2} \simeq 180nA$ and $C_{lim2} = 0.2pF$, the preamplifier's response time t_{i2} and time constant τ_2 were $95.6ns$ and $120ns$ respectively. For these design choices and setting $V_{off2} = 448mV$, it was manageable to limit the fine charge transfer duration to $T_{fine2} = 112.5ns$ and total charge-transfer duration to $T_{charge-transfer2} = 290.5ns$ on average.

The design choices for the preamplifier of the second integrator are summarized in Table 6-1, along with the design choices of the preamplifier of the first integrator for comparison. The design of the second integrator was verified through simulations following the same procedure with the design of the first integrator. The signal-dependent input-referred error range

Table 6-1: Design parameters of the inverter-based preamplifiers in the ZCDs

Parameters	1^{st} Int. preamp	2^{nd} Int. preamp
Maximum transconductance $g_{m,tot}$	$450\mu A/V$	$120\mu A/V$
Maximum bias current I_{max}	$12.25\mu A$	$3.37\mu A$
Response time t_i	$115ns$	$95.6ns$
Time constant τ	132ns	154ns
Bandlimiting capacitor C_{lim}	$0.6pF$	$0.2pF$

was simulated to be $65\mu V$, using $C_{CLS2} = 0.1pF$ and the input-referred RMS noise was simulated using transient noise simulation to be $v_{n,in,INT2} = 635\mu V$. These values for noise and signal-dependent error are expected not to harm the performance of the entire ADC.

6-2 Further energy consumption reduction measures

In the design of both ZCB integrators, it has been recognized the the energy consumption is dominated by the current that the preamplifiers consume during fine charge transfer phase and during their auto-zeroing operation. The energy consumption of the preamp during the fine phase can be tuned by lowering the fine charge transfer duration, i.e setting the early threshold of the ZCD closer to V_{CM} adjusting V_{off} accordingly. Also, the energy consumption during the auto-zeroing of one ZCD is proportional to the fine charge transfer duration of the other ZCB integrator. These two factors were taken into account in the design of both ZCB integrators.

Taking a step further, if it was possible to eliminate the need of auto-zeroing in each cycle, apparent energy savings will be present. During the design of the ZCB integrators, it was observed that the charge across the auto-zeroing capacitor is not changing substantially among successive integration cycles, because C_{AZ} is much higher than the input capacitance of the ZCD preamp. Consequently, the opportunity of skipping auto-zeroing cycles is indeed present, having although impact to linearity of the integrators as the threshold of each ZCD will slightly vary from cycle to cycle for the cycles when AZ is not performed. Another disadvantage lies in the suppression of the $1/f$ noise of the ZCD preamplifiers as the cut-off frequency of the $1/f$ noise will be lower. In order to investigate this opportunity, the AZ signal of the ZCDs can be gated using an universal AZ control signal that is controlling in which cycle the auto-zeroing will be performed. This was implemented in a configurable way using an external control signal to control the auto-zeroing processes. The generation of AZ control signal can be done by the state-machine for the generation of the self-timed clocks of the ADC. In this configuration, the duration of auto-zeroing can be optimized as well implementing the necessary logic off-chip in order to limit the AZ duration to approximately $10\times\tau_{AZ}$ of each ZCD.

Another opportunity for energy savings comes from the observation that the swing of the first integrator is limited to $[0.35V, 0.65V]$. So, since the output is preset in every cycle to $1V$, unnecessary expenses in conversion time and energy consumption are present due to the roll-off of V_{O1} from V_{DD} to the actual swing of the integrator. By presetting to a lower

voltage than V_{DD} the majority of these expenses are prevented. This is implemented in the new design, using an external $V_{preset1}$ connection of the chip.

6-3 Implementation of the other sub-blocks of the ADC

In order to implement the ADC, besides the two ZCB integrators, auxiliary circuitry needs to be realized, such as digital logic for the control of the charge-transfer phases of the two ZCB integrators, clock-boosters in order to drive the switches, a bit-stream comparator and a current reference. Also, the generation of the V_{off} voltages that are necessary in the early-threshold generation mechanism of the ZCDs is required. These sub-blocks were present in the first prototype of the self-timed ADC and the proper functionality of the designed blocks in [1] is verified. The requirements from these sub-blocks remain the same in the new design, so these sub-blocks are reused with small modifications. This section is presenting the implementation details of these sub-blocks, including short discussion on the requirements from them.

6-3-1 Generation of V_{off}

As described before, the early-threshold of the ZCDs is implemented using capacitive level-shifting of the preamplifier's output of the ZCD. The level-shifting capacitor C_{off} is needed to be precharged before the beginning of the charge-transfer to a suitable voltage V_{off}. The precharging of C_{off} is done during the preset phase of the ZCB integrator and the V_{off} voltages that are reqired for the two integrators are $V_{off1} = 446mV$ and $V_{off2} = 451mV$. These voltages can be generated on-chip by means of a diode voltage reference as can be seen in Figure 6-2.

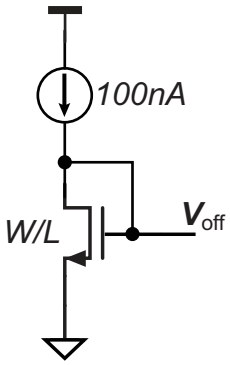


Figure 6-2: Schematic of a diode voltage reference for the generation of V_{off} inside the ZCDs.

The designed dimensions for the two diodes are $W_1/L_1 = 1/16.3$ and $W_2/L_2 = 1/16.85$.

Although this method has been proven functional, it is beneficial to include the possibility of external generation of the V_{off} voltages, although it is consuming two I/O pins of the chip. By doing so, the possibility of trimming the switching point from coarse to fine charging phase remains in order to avoid linearity problems coming from process variations. The configuration

of on-chip or off-chip V_{off} generation is provided using one bit of the configuration shift register of the chip.

6-3-2 Digital control of the charge-transfer

The digital control logic that was designed in [1] is completely matching the requirements of this design, so it was reused, including the layout, with minor modifications. The digital circuitry is generating the preset P and control signals of the current sources E_1, E_2 for both integrators, as well as the auto-zeroing signals AZ_1, AZ_2, based on Φ_1, Φ_2 and the ZCD outputs D, D_e of the ZCB integrators. The control logic has been designed using standard cells available in the design libraries of NXP C14 technology [46] and for the new realization a few blocks were downsized in order to save power, at the expense of the slight increase of the delay time t_c. Implementation details of the self-timed control circuitry can be found in [25]. For the generation of the preset signal, a low-power tunable delay element was utilized [50]. The tuning of the delay is possible via a current starving current source, which is configurable in this implementation, using two bits of the configuration shift register of the chip for each integrator.

6-3-3 Clock boosters

In order to ensure low on-resistance of NMOS switches with low supply voltage, the driving voltage of the switches has to be boosted above V_{DD}. This typically realized using the clock-boosting technique [16] [51] and implementations of a single-output and a double-output clock booster that were used in [1] are shown in Figure 6-3. The double-output clock booster is functional if the inputs are complementary and is used for example to boost the $\Phi_{1,d} - \Phi_{2,d}$ and $AZ_1 - AZ_2$ signals. The single-output clock booster is used to boost Φ_1 and RST_n.

Regarding a clock-booster's input-output behavior, when the input voltage of a is a square-wave between GND and V_{DD} the clock-booster is generating a square-wave with identical timing and ideally doubled amplitude (between GND and $2 \cdot V_{DD}$). In practice, the voltage-boost ratio is lower than 2, because of the finite parasitic capacitance C_p at the clock-booster's output due to gate capacitance of the driven switches and parasitic capacitance of the wiring [51]. In order to ensure that the driving voltage will be $1.85V$ in worst case, the capacitors C_{b1}, C_{b2} of the clock booster have to be adjusted carefully, using the results of post-layout simulation of the ADC.

6-3-4 Bitstream comparator

The accuracy requirements from a bitstream comparator that is used in the context of a $\Delta\Sigma$ ADC are very relaxed, as the error of the comparator due to offset or kick-back noise is highly suppressed by the aggressive noise shaping of the loop-filter. For this reason and high power efficiency due to their negligible static power consumption, the use of a dynamic comparator was chosen in the first prototype. The implemented comparator in [1], which is reused in the new design is shown in Figure 6-4. This comparator is consisting of an input pair with a regenerative latch followed by an SR latch.

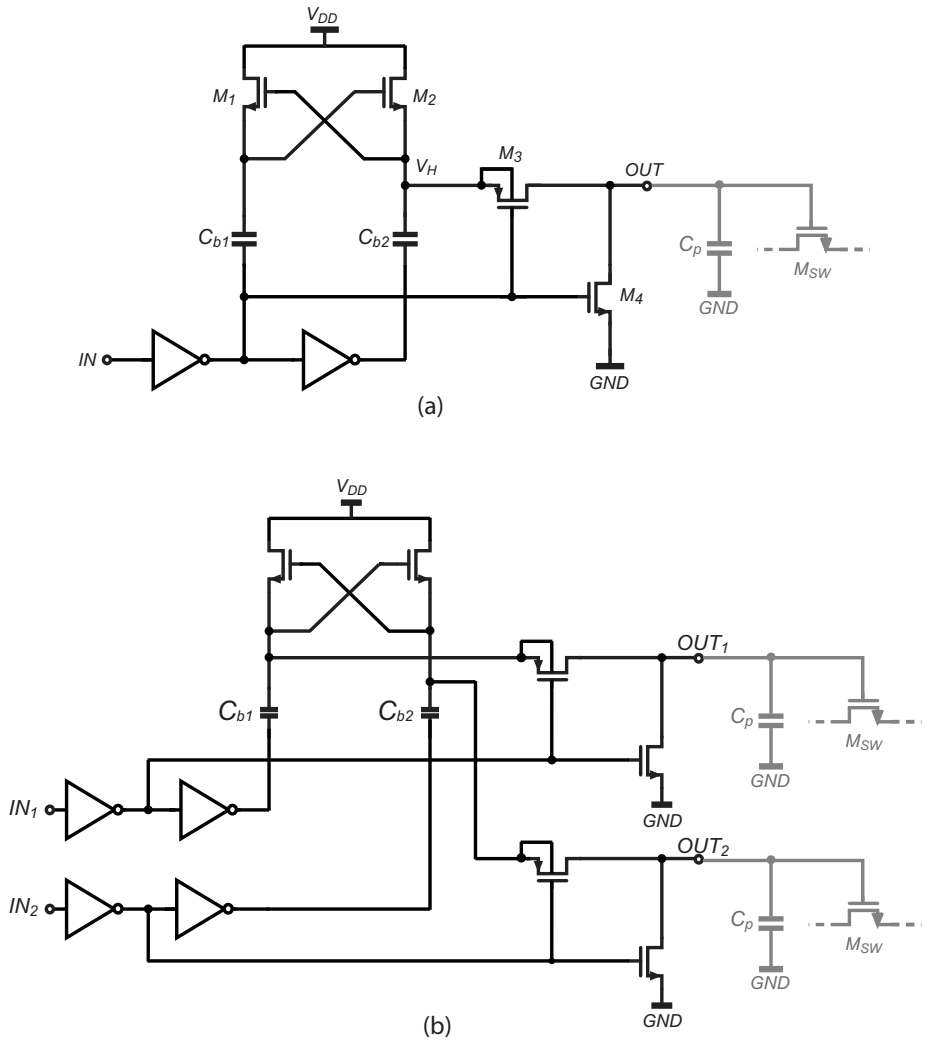


Figure 6-3: Schematics of (a) a single-output clock-booster and (b) a double-output clock booster [25].

The operation of the dynamic comparator is based on the *Latch* input control signal. When *Latch* is low the regenerative latch is reset and is isolated from the input and the SR latch is keeping the reuslt of the previous comparison. With the rise of *Latch*, a new comparison is triggered, with the input voltage altering the equilibrium of the regenerative latch, until it is settling to its new state. The new state of the latch is then latched in the SR latch, providing the new comparison result. In the context of the self-timed ADC, the *Latch* signal of the comparator is the inverse of the fine phase control signal of the second ZCB integrator E_{2n}.

6-3-5 Current reference

For biasing purposes of the gated current sources, diode voltage-references and the delay elements that are present in the digital control circuit of the modulator, a conventional constant-g_m current reference [31], that is insensitive to supply voltage variations was designed in the

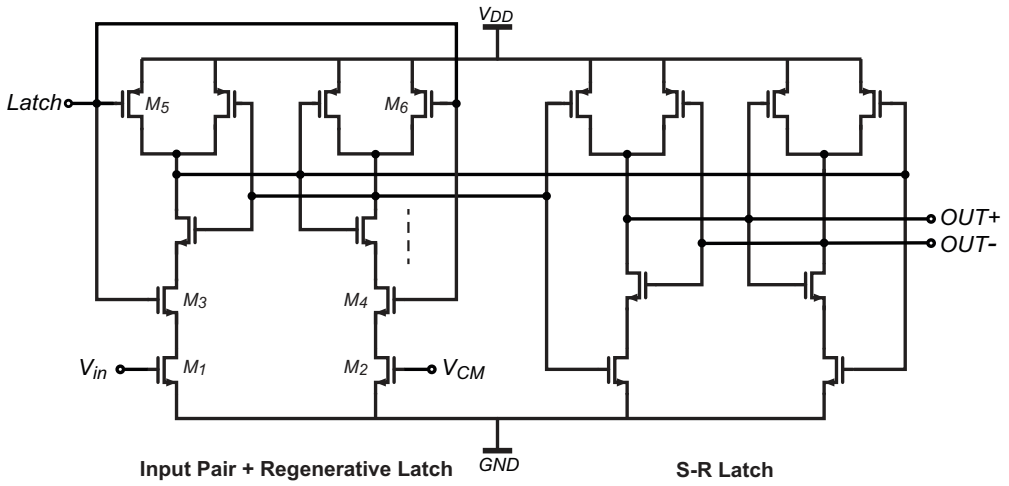


Figure 6-4: Schematic of the dynamic bitstream comparator [25].

prototype chip of [1]. This current reference is matching perfectly the requirements of the new design, thus the design and layout are completely reused in the new chip. The schematic of this current reference, that is including a low-voltage startup circuit is shown in Figure 6-5. According to [31], the output current of this reference is

$$I_{out} = \frac{1}{R_{bias}^2} \cdot \frac{2}{\mu_n C_{OX}(W/L)_1}\left(1 - \frac{1}{\sqrt{k}}\right)^2, \tag{6-3}$$

where k is the aspect ratio of the NMOS transistors of the current reference. Using $R_{bias} = 620k\Omega$ and $k = 10$ the output current of the current reference is $\simeq 100nA$

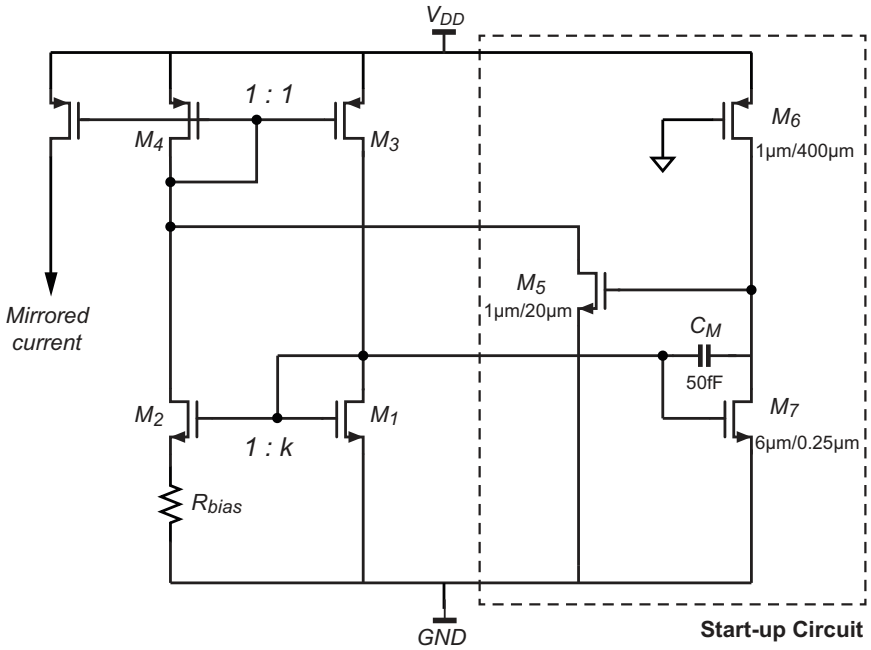


Figure 6-5: Schematic of the current reference, including the start-up circuit [25].

In the previous implementation, the possibility of off-chip generation of the bias current was included, for safety reasons in case of failure of the start-up circuit. This option was remained in the new chip and the selection between on-chip or off-chip reference current generation is done using two bits of the configuration shift register of the chip.

6-4 Configurability and testing features of the chip

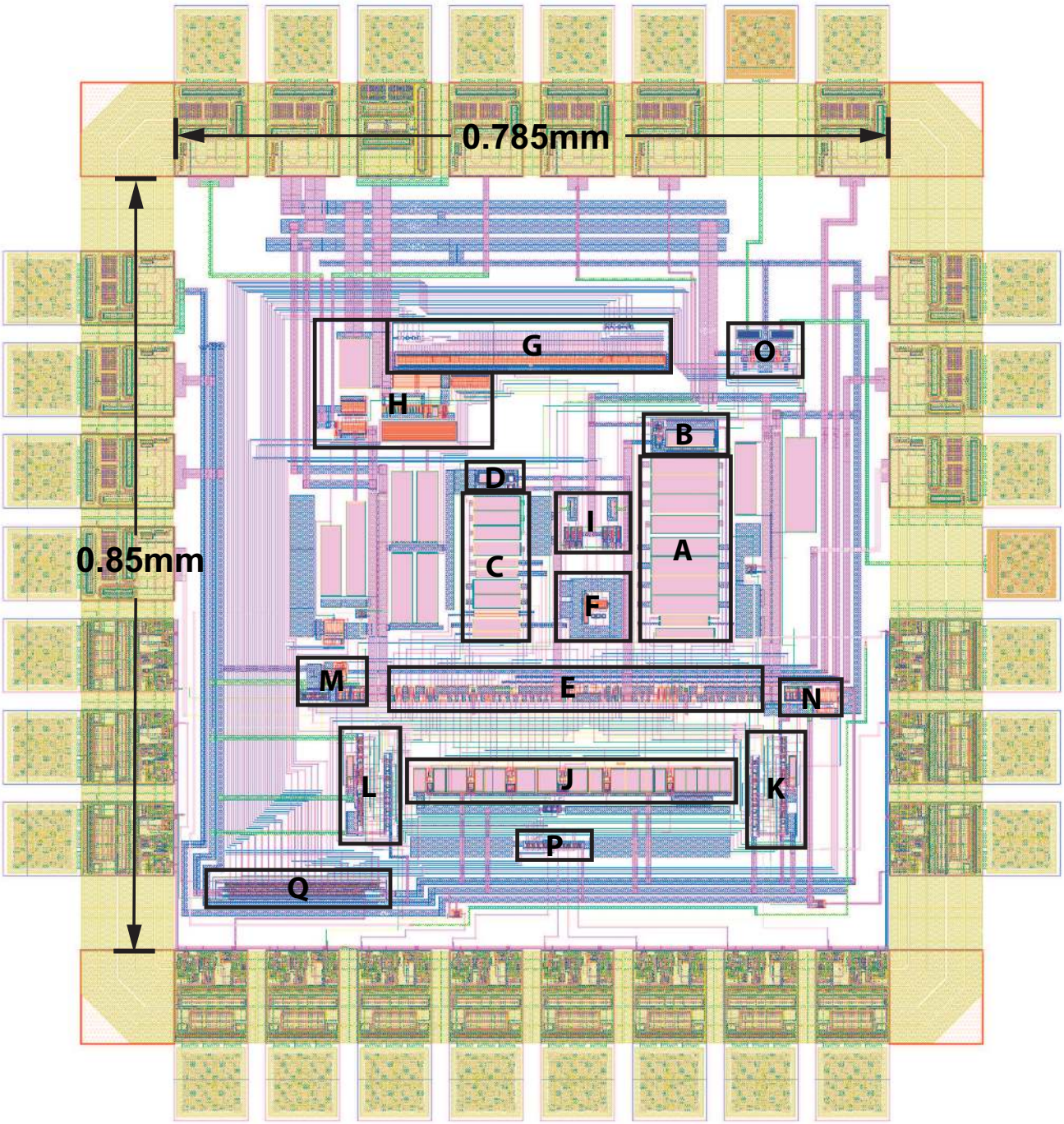
The designed test chip should be able to operate in different modes in order to ensure its proper operation and also enhance the possibility of drawing useful conclusions on the operation of ZCB circuits. Thus, many configuration options are available in the designed chip, which are now summarized:

- On-chip / off-chip V_{off} generation (1 bit in shift register for both integrators)
- Control of magnitude of coarse current sources with 5 steps (3 bits in shift-register for each integrator)
- Control of the correlated level-shifting capacitances with 2 steps: $0.2pF$ or $0.4pF$ for the first integrator and $0.1pF$ or $0.2pF$ for the second integrator (1 bit in shift register for each integrator)
- Control of the magnitude of the fine current source of the second integrator with 2 steps: $90nA$ or $180nA$ (1 bit in shift register)
- Control of the preset duration of the integrators with 3 steps (2 bits in shift register for each integrator)

The first, second and fifth configuration options of the chip were present in the previous design [1], but the third and fourth are introduced in the new prototype. Furthermore, in order to make the chip testing friendly, internal probing of the crucial signals of the operation is mandatory. For this reason, in the previous design an analog multiplexer/buffer and a digital multiplexer have been employed in order to facilitate the monitoring of the ouput signals of the two integrators V_O and the two preamplifiers of the ZCDs V_{int}, as well as, the digital control signals of preset P and control of the current sources E_1 and E_2. The implementation details of these circuits can be found in [25]. This functionality was maintained in the new chip and the required circuitry is reused, as its proper functionality has been proven.

6-5 Layout

The layout of the chip was designed in NXP CMOS14 [46] $0.16\mu m$ 1P5M standard CMOS technology and can be seen in Figure 6-6, where the building blocks of the chip are highlighted. The chip dimensions are $0.785mm \times 0.85mm$ and 30 I/O pads are required with 14 I/Os being analog, 14 I/Os being digital and 2 I/Os do not have ESD protection and are used as outputs of the analog buffer. During the layout design of the chip special care was taken to ensure proper voltage levels at the outputs of the clock boosters and tried to minimize the parasitic capacitance at the input of the first ZCD preamp, as both phenomena have been recognized as limiting factors of the achievable linearity of the converter [25].



A: Capacitors of 1st integrator **B:** Preamplifier of ZCD of 1st integrator **C:** Capacitors of 2nd integrator
D: Preamplifier of ZCD of 2nd integrator **E:** Switches **F:** Fine current sources **G:** Coarse current sources
H: Current reference **I:** Voff generation and offchip control **K:** Control logic of 1st integrator
L: Control logic of 2nd integrator **M:** Bitstream comparator and WCD of 2nd integrator
N: WCD of 1st integrator **O:** Analog output buffer **P:** Digital output buffer **Q:** Shift register

Figure 6-6: Layout of the ADC in 0.16μm 1P5M CMOS.

6-6 Simulation results

After the ADC is built, extensive performance characterization is necessary, performing pre-layout and post-layout simulations. The simulation results of the ADC are following, concerning all the common specifications of Incremental $\Delta\Sigma$ ADCs, such as resolution, conversion time, linearity, as well as power consumption. In the end, a performance summary of the designed ADC is presented and the obtained performance is compared with other state-of-the-art ADCs, tailored for I&M applications.

6-6-1 Pre-layout simulation results

Functional verification

The first step of the characterization procedure of an ADC is its functional verification. This is checked, ultimately, by performing a single conversion, by means of a transient simulation. In this case, the designed ADC performed a conversion with $V_{in} = 0.5000033V$ and the decimated output voltage that obtained was $V_{dec,out} = 0.49709436V$ and the conversion time that was needed was $T_{conv} = 0.9670ms$, taking into account the time that is needed for the configuration of chip and reset of the ADC. Furthermore, in this step, the simulation of the average power consumption of the ADC can be performed, capturing the analog and digital supply currents and extracting their average values during the conversion time interval. The resulting average analog supply current is $I_{V_{DDA}} = 15.89\mu A$, while the average digital supply current is $I_{V_{DDD}} = 9.67\mu A$.

Input-referred noise

Then, the resolution of the ADC was treated and the input-referred noise was simulated, by performing a transient noise simulation for the entire conversion. The decimated output voltages were captured for the 16 points of the simulation and the point-to-point standard deviation of the decimated outputs was calculated to be $\delta_{rms} = 5.155\mu V$[1]. As a result, the input-referred RMS noise of the ADC is $v_{n,in,ADC,prelayout} = \delta_{rms} = 5.155\mu V$. This noise value is fairly close to the expectation $\widehat{v_{n,in,ADC}}$ that can be made based on the simulation of the input-referred noise of the first ZCB integrator [subsection 5-4], where the value of $v_{n,in,INT1} = 120.3\mu V$ was found and the estimated quantization noise standard deviation for $N = 1000$, which is $\sigma_q = 1.65\mu V$ [subsection 5-2-2]. Taking these into account, the estimated input-referred noise of the ADC is

$$\widehat{v_{n,in,ADC}} = \sqrt{\sigma_q^2 + \frac{4}{3} \cdot \frac{\overline{v_{n,in,INT1}^2}}{1000}} = 4.7\mu V. \tag{6-4}$$

Moreover, the simulated input-referred noise of the ADC is corresponding to a resolution of

$$\text{ENOB(bits)} = \left(20 \cdot \log_{10} \frac{0.7}{v_{n,in,ADC,prelayout}} - 1.76\right) \Big/ 6.02 = 16.76\text{bit} \tag{6-5}$$

[1] For the noise simulation, the input voltage source was slightly noisy ($V_{n,in,pk-pk} = 50nV$) in order to trigger quantization noise.

The SNR of the converter can be calculated from the simulated input-referred noise to be

$$\text{SNR} = 20 \cdot \log_{10} \frac{0.7}{2 \cdot \sqrt{2} \cdot v_{n,in,ADC,prelayout}} = 93.63dB^2 \tag{6-6}$$

Linearity (INL) and conversion time

Finally, the linearity of the converter has to be simulated, requiring an input sweep and transient simulation for the whole conversion for each input voltage point. In this case, the input was swept and the results for the decimated output and conversion time for the 15-point input sweep are shown in Table A-1.

Using the input-decimated output pairs of Table A-1, the INL of the ADC can be estimated, by normalizing across the best-fitting straight line. The INL of the ADC, as estimated with this pre-layout simulation is shown in Figure 6-7. The simulated offset of the ADC was found to be $V_{OS,prelayout} = 3.6557mV$, while the gain error was 1.1%. Moreover, the conversion time is visualized in Figure 6-8, with the maximum conversion time being $T_{conv,max} = 1.0016ms$. The offset voltage of the ADC in this test was found to be $V_{OS,pre-layout} = 3.265mV$ with the gain error being 2.1%. The offset and gain error were not optimized in this design, as it is possible to be calibrated out in the digital domain in a practical application. If this is not enough for a particular application, system-level chopping [24] can be applied to effectively minimize offset and gain error of the ADC.

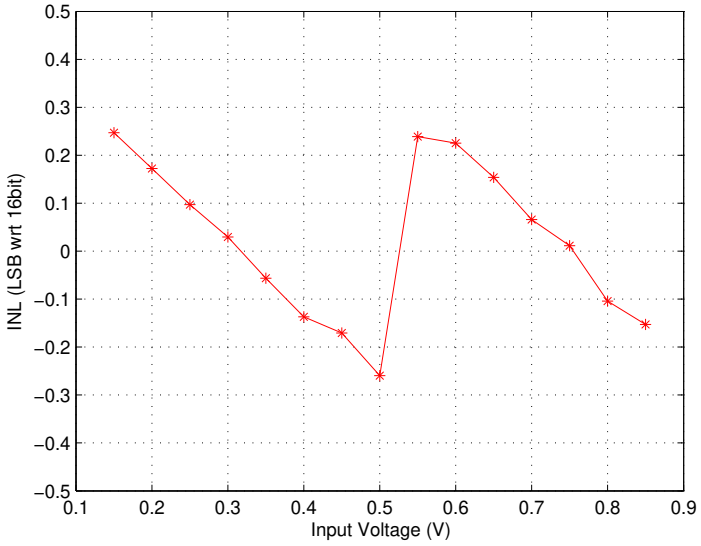


Figure 6-7: Pre-layout simulated INL of the ADC.

[2] A crest-factor $2 \cdot \sqrt{2}$ was included to take into account that the ADC is simulated with a constant input and not with a full-scale sinusoid that is a common practice in performance characterization of general-purpose ADCs.

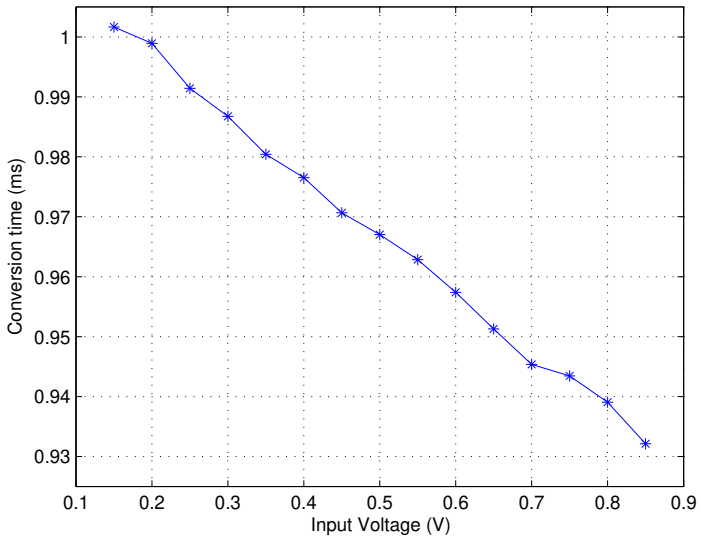


Figure 6-8: Pre-layout simulated conversion time of the ADC as function of input voltage.

6-6-2 Post-layout simulation results

Functional verification

Similarly with the pre-layout verification procedure, the first step of the post-layout verification is to confirm that the functionality of the ADC is correct. Again, a single conversion with $V_{in} = 0.5000033V$ was simulated and the decimated output voltage that obtained was $V_{dec,out} = 0.49561133V$ and the conversion time that was needed was $T_{conv} = 0.9732ms$, taking into account the time that is needed for the configuration of chip and reset of the ADC.

Input-referred noise

The next step, was to simulate the input-referred noise of the ADC with extracted layout. In this case, the whole analog part was extracted, but the digital control of the two integrators was simulated in schematic level, because of the limitation in simulation time. Using 8 points for the transient noise simulation the point-to-point standard deviation of the decimated outputs was $\delta_{rms} = v_{n,in,ADC,postlayout} = 5.565\mu V$. The calculated SNR in this case was 92.96dB and the resolution of the ADC was $ENOB_{post-layout} = 16.67$bit.

Linearity (INL) and conversion time

The linearity performance was simulated after layout extraction (again the digital control of the integrators remained in schematic level), performing an 8-point input sweep. The results for the decimated output and conversion time can be inspected in Table A-2. The INL of the ADC was extracted from these results and is visualized in Figure 6-9. The conversion time

for this input sweep is plotted as well in Figure 6-10. Finally, the offset voltage in this test was observed to be $3.976mV$ and the gain error was 3.45%.

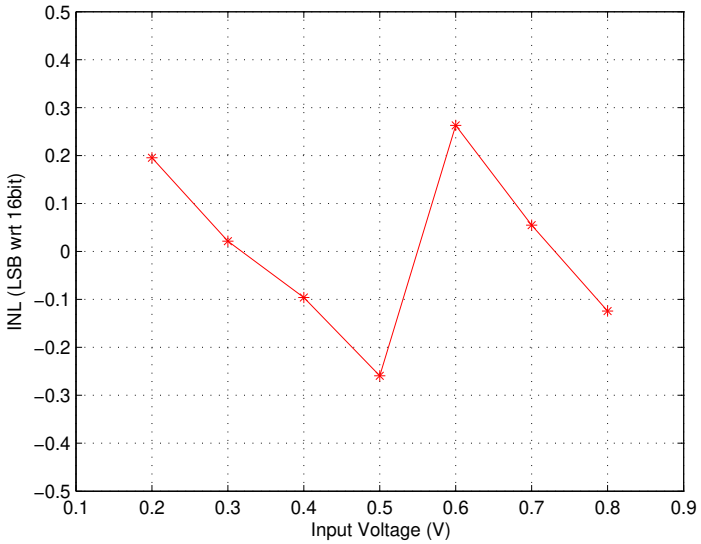


Figure 6-9: Post-layout simulated INL of the ADC.

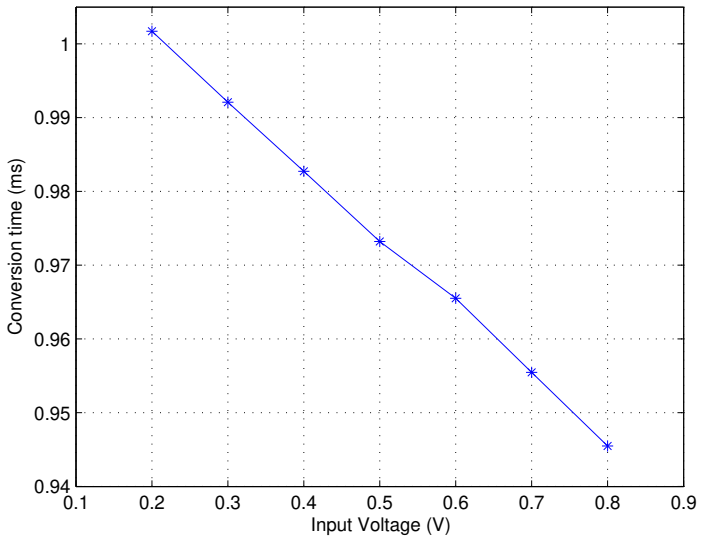


Figure 6-10: Post-layout simulated conversion time of the ADC as function of input voltage.

6-7 Performance summary

The simulated performance of the designed ADC is now summarized in Table 6-2. In order to facilitate comparison with other designed ADCs and quantify the energy efficiency, the two most-used figures of merit (FOM) that were briefly described in section 4-4 are calculated.

Table 6-2: Performance Summary

Specification	Simulated Performance
Technology	NXP 0.16μm 1P5M CMOS
Active Chip Area	0.6675 mm^2
Supply Voltage	1 V
Supply Current	Analog: 15.89μA Digital: 9.67μA
Conversion Time	$<$ 1.01 ms
Stable Input Range	0.15V - 0.85V
Input-Referred RMS Noise (pre-layout)	5.155μV
Input-Referred RMS Noise (post-layout)	5.565μV
SNR (post-layout)	92.96dB
Resolution ($ENOB_{post-layout}$)	16.67bit
INL	-0.255 - 0.27 (LSB)†
FOM$_W$	0.71 pJ/conversion-step††
FOM$_S$	168.8dB†††

† Relative to a 16-bit output code. †† $FOM_W = \frac{Power \cdot T_{conv}}{2^{(SNR-1.76)/6.02}}$.

††† $FOM_S = \text{SNR} + 10 \cdot \log\frac{1}{\text{Power} \cdot \text{T}_{\text{conv}}}$.

As can be seen in Table 6-2, the designed second-order I$\Delta\Sigma$ ADC achieves (post-layout simulated) resolution of approximately 17-bit and linearity of approximately 1 LSB with respect to 17-bit, operating at 1000 incremental cycles. This performance is the best reported among all the CBSC/ZCB $\Delta\Sigma$ ADCs, as can be seen in Table 6-3, in terms of achievable resolution and linearity. Furthermore, the designed ADC consumes in total 25.56μA from 1V supply, having conversion time of 1.01 ms in worst case. This leads to an improved energy efficiency of the ADC which has Schreier FOM of 168.8dB, which is the highest compared to all the prior CBSC/ZCB reported designs. Actually, the new design is improving the energy-efficiency of the first prototype self-timed ADC[1][3] by 5.76 dB. Furthermore, the achieved energy efficiency is very close to the state-of-the-art energy-efficiency of the OTA-based $\Delta\Sigma$ ADC, with exception the design of [11] which is by far superior among all.

6-8 Improved measurement setup proposal

During the characterization time of the first prototype, a few options towards realizing a more robust measurement setup came up. First of all the LDO that was used for the generation of the reference voltage of the ADC was noisy, so a solution of a precision voltage reference should be seeked. Perfect candidates for this are the ADR4520 [52], available from Analog Devices or the LTC6655 [53], available from Linear Technology. Both these alternatives are

[3]referred to its updated performance that is summarized in Table 4-1

Table 6-3: Performance comparison with Prior CBSC/ZCB ΔΣ ADCs

	[6]	[7]	[8]	[9]	[1]	**This work**
Architecture	ΔΣ2 - FD	ΔΣ2 - FD	ΔΣ4 - PD	ΔΣ2 - SE	IADC2 - SE	**IADC2 - SE**
Process	$0.18\mu m$	$45nmLP$	$90nm$	$3\mu mTFT$	$0.16\mu m$	**0.16μm**
Area (mm^2)	0.21	0.0448	0.33	26	0.45	**0.6675**
$V_{DD}(V)$	1.8	1.1	1	11.2	1	**1**
Sampling frequency	2.56 MHz	50 MHz	96 MHz	400 kHz	750 kHz	**990 kHz**
OSR	64	30	48	128	500	**1000**
Bandwidth (Hz)	20 kHz	833 kHz	1 MHz	1.56 kHz	667 Hz	**495 Hz**
Dynamic Range (dB)	71	54.3	70	69	81.9	**92.96**
Peak SNR (dB)	65.3	47.7	66	65.6	81.9	**92.96**
Power	$0.42mW$	$630\mu W$	$5.94mW$	$63.3mW$	$20\mu W$	**25.56μW**
FOM_W (pJ/step)	6.98	1.91	1.82	13.03	1.46	**0.71**
FOM_S (dB)	147.8	145.5	152.3	112.9	157.1	**168.8**

† The reported performance of this work is based on simulation results.

generating higher voltage than 1V, so a resistive divider at the output of the voltage reference is needed. Both these two alternatives are expected to facilitate the measurement of the new ADC, as they are capable of achieving proper level of accuracy for our task.

The second consideration towards the enhancement of the robustness of the measurement setup is based on tailoring it to the exact requirements of measurement. A measurement setup that is based on an Alterra Cyclone II FPGA [54], and a 20-bit DAC, for instance AD5791 [55] available from Analog Devices, for the generation of the input voltage of the ADC is expected to be realizable. In this setup, the use of Labview can be avoided and the control of the measurement procedure and data post-processing can be performed using Matlab. For the measurement data transfer, the solution of using an RS-232 link is possible. In that way, timing overhead of the measurement procedure can be avoided, thus reducing the measurement time, making the setup immune to environmental noise and low-frequency noise and interference.

6-9 Summary

In this chapter, the implementation details of the new prototype, except for the design of the first integrator, were described. Finally, the top-level simulation results of the ADC were presented, achieving 16.7-bit resolution in the post-layout simulation, INL of 0.5LSB with respect to 16-bit, consuming $25.56\mu A$ from a 1V supply and operating for 1.01ms in worst case.

Chapter 7

Conclusions

This final chapter summarizes the work that has been done during this thesis project. It also provides suggestions for future work on the self-timed ZCB IΔΣ ADC.

7-1 Thesis summary

The initial objective of this thesis was to develop an improved prototype of self-timed ZCB IΔΣ ADC, achieving resolution and linearity above 16-bit, while improving (if possible) its energy-efficiency. In order to fulfill this task, the new design is based on the first prototype self-timed IΔΣ ADC [1], making use of all the performance enhancing techniques that have been used before in the design of ZCB circuits, such as inverter-based implementation of the preamplifier of the ZCD, correlated level-shifting and uni-directional coarse-fine charge transfer scheme. Moreover, the options of extension to a differential structure and/or higher order modulator have been examined.

This project is mainly focused on the optimization of the first ZCB integrator of the loop-filter, as it is recognized as the most performance critical block of the ADC. For this purpose the noise and linearity of the ZCB integrator have been analyzed and presented in this thesis. The developed noise model was fairly accurate and has been verified by the updated noise measurement results of the previous design [1], that were obtained during this project. Main motivation for revisiting the measurement of the previous design was, however, the observation that the measurement result of the INL was not reproducible. Also, the knowledge of the actual linearity of the previous design was expected to verify to some extent the linearity analysis of the ZCB integrator and help in the design of the new prototype. The actual linearity of the previous design has been measured successfully, but the result is not close to the expectation that was done based on the linearity analysis, because of the significance of the off-transients of the gated current sources. As a result, in the development of the improved prototype, a simulation-intensive linearity design procedure was found to be the most suitable.

Next, the actual design of the improved ADC was tackled, starting with the possibilities of extension to a third-order modulator and realization of a differential structure for the ZCB integrators. Based on the developed noise model, it has been concluded that utilizing a third-order modulator is not necessarily beneficial. Also, the presence of an issue in the implementation of a 3^{rd}-order CIFF modulator using ZCB integrators was discouraging and the reuse of the 2^{nd}-order modulator topology with input feed-forward path, that was used in [1] was decided. Next, the option of a fully-differential implementation was examined, but because of its large (simulated) signal-dependent input-referred error, probably due to the mismatch of off-transients between NMOS and PMOS current sources turned out to be a non-realistic target of this project. However, a pseudo-differential topology was found to be suitable, but time limitations during this project did not permit its realization. As a result, single-ended ZCB integrators were optimized in order to realize an ADC that meets the target specifications of this project.

Based on the developed noise model, the first ZCB integrator was resized and following a simulation-intensive linearity design procedure, the necessary measures were taken in order to reduce the signal-dependency of the input-referred error of the ZCB integrator. After verifying the design of the first integrator, the second ZCB integrator was designed as a scaled version of the first one. In the end, the design of the ADC was completed, the layout was designed and verified extensively using pre-layout and post-layout simulations.

Based on pre-layout and post-layout simulations, the designed second-order I$\Delta\Sigma$ ADC achieves (post-layout simulated) resolution of approximately 16.7-bit and INL equal to 1LSB w.r.t. 17-bit. To achieve this, the modulator operates for 1000 incremental cycles, having conversion time less than 1.01ms, while consuming less than $26\mu A$ from 1V supply. As a result, an anticipated energy-efficiency in terms of $FOM_S = 168.8dB$ and $FOM_W = 0.71$ pJ/conv.step was found, which is improvement compared to the state-of-the-art of CBSC/ZCB $\Delta\Sigma$ ADCs and quite close to the state-of-the-art designs of OTA-based $\Delta\Sigma$ ADCs.

7-2 Suggestions for future work

The correct operation of the designed ADC has been verified using simulations and its layout has been designed and verified as well. But, since the new prototype has not been fabricated, it can be readily included in an MPW run. This will enable the experimental characterization of the improved self-timed ZCB I$\Delta\Sigma$ ADC, leading to improved understanding of its performance limiting factors. Also, there are some potential improvements and direct extensions of this work that are summarized below.

- Based on the designed single-ended ZCB I$\Delta\Sigma$ ADC, an extension to the pseudo-differential topology that was proposed in this thesis but was not implemented due to design time restrictions is possible. A pseudo-differential implementation is expected to demonstrate superior resolution and linearity at comparable energy-efficiency with the proposed single-ended ZCB I$\Delta\Sigma$ ADC.
- The noise balance of the individual contributors can be revisited in order to achieve higher energy efficiency. As mentioned previously, in this design the noise contributors of the charge-transfer phase of the ZCB integrator, including ZCD preamp noise, were

suppressed more aggressively compared to kT/C_S. This was done to provide extra design margin, because during the design time of this project the validity of the developed noise model was not proven, as the updated measurement results of the first prototype were not available. Thus, another iteration of the noise design is suggested, in which the noise of the ZCD preamp should dominate the total input-referred noise of the ZCB integrator. In this case, the current consumption of the preamplifier is expected to be lower, improving further the energy-efficiency of the ADC.

- Since it turned out that the major limiting factor of the linearity performance of the ADC is the off-transient behavior of the fine charging current source, an alternative implementation of the fine current source should be found. Possible candidates could be a source degenerated current source or a switched-resistor current source similar to [7]. The latter solution is expected to drastically reduce the off-transients at the expense of increased die area. Also, implementing the current source using switched resistors could potentially remove the off-transients mismatch problem and make the fully-differential implementation of the ZCB integrator possible.
- Finally, the designed ADC can be readily applied to the implementation of integrated sensor readout circuits of low-frequency signals, such as environmental signals.

Appendix A

Results of pre-layout and post-layout input sweeps

In this appendix, the results of the pre-layout and post-layout input sweeps of the designed ADC are attached. These results have been used to extract the INL of the ADC which is plotted in Figure 6-7 and Figure 6-9 respectively. Also, based on these findings the conversion time of the ADC was plotted in Figure 6-8 and Figure 6-10 respectively.

Table A-1: Simulation results of pre-layout input sweep

Input voltage (V_{in})	**Decimated output ($V_{dec,out}$)**	**Conversion time (T_{conv})**
0.1500033 V	0.14603355 V	1.0016 ms
0.2000033 V	0.19592756 V	0.9989 ms
0.2500033 V	0.24582146 V	0.9914 ms
0.3000033 V	0.29574511 V	0.9867 ms
0.3500033 V	0.34560931 V	0.9804 ms
0.4000033 V	0.39550321 V	0.9765 ms
0.4500033 V	0.44539742 V	0.9706 ms
0.5000033 V	0.49529133 V	0.9670 ms
0.5500033 V	0.54519136 V	0.9628 ms
0.6000033 V	0.59508607 V	0.9574 ms
0.6500033 V	0.69487378 V	0.9513 ms
0.7000033 V	0.69687377 V	0.9454 ms
0.7500033 V	0.74476780 V	0.9435 ms
0.8000033 V	0.79466139 V	0.9390 ms
0.8500033 V	0.84455542 V	0.9321 ms

Table A-2: Simulation results of post-layout input sweep

Input voltage (V_{in})	**Decimated output ($V_{dec,out}$)**	**Conversion time (T_{conv})**
0.2000033 V	0.19533799 V	1.0017 ms
0.3000033 V	0.29502029 V	0.9921 ms
0.4000033 V	0.39464400 V	0.9827 ms
0.5000033 V	0.49429681 V	0.9732 ms
0.6000033 V	0.59395695 V	0.9655 ms
0.7000033 V	0.69360929 V	0.9555 ms
0.8000033 V	0.79326194 V	0.9454 ms

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