A High Slew-Rate Push–Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement

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***Abstract*—A high slew-rate amplifier with push–pull output driving capability is proposed to enable an ultra-low quiescent current ($I_Q \sim 1\ \mu$A) low-dropout (LDO) regulator with improved transient responses. The proposed amplifier eliminates the tradeoff between small I_Q and large slew-rate that is imposed by the tail-current in conventional amplifier design. Push–pull output stage is introduced to enhance the output driving ability. Small dropout voltage ($V_{\rm DO}$) with large-size pass transistor and ultra-low I_Q can thus be used to minimize power loss of LDO regulator without transient-response degradation. The proposed amplifier helps to improve stability of LDO regulators without using any on-chip and off-chip compensation capacitors. This is beneficial to chip-level power management requiring high-area efficiency. An LDO regulator with the proposed amplifier has been implemented in a 0.18-μm standard CMOS process and occupies 0.09 mm^2. The LDO regulator can deliver 50-mA load current at 1-V input and $\sim$ 100-mV $V_{\rm DO}$. It only consumes 1.2 μA I_Q and is able to recover within $\sim$ 4 μs even under the worst case scenario.**

***Index Terms*—High slew rate, low-dropout (LDO) regulator, low-quiescent current, tail current.**

I. Introduction

LOW-DROPOUT (LDO) regulators are often used in battery-powered mobile systems requiring small size and clean supply voltage. To prolong the battery life, power efficiency of LDO regulators can be improved by reducing the quiescent current (I_Q) and dropout voltage ($V_{\rm DO}$). Fig. 1(a) shows the regulator efficiency as a function of load current ($I_{\rm LOAD}$) with different I_Q and under a particular output voltage ($V_{\rm OUT}$) and $V_{\rm DO}$. It shows that the use of ultra-low I_Q effectively improves the regulator efficiency at small $I_{\rm LOAD}$, which often happens when systems are operating in standby mode to extend the battery life. From the efficiency expression in Fig. 1(a), small $V_{\rm DO}$ also improves the regulator efficiency and this improvement is more significant in the small $V_{\rm OUT}$ case.

However, reduction of I_Q and $V_{\rm DO}$ unavoidably slows down the transient responses of an LDO regulator. This can be explained with a generic LDO regulator shown in Fig. 1(b). The tail-current of amplifier is equal to I_Q of the LDO regulator.

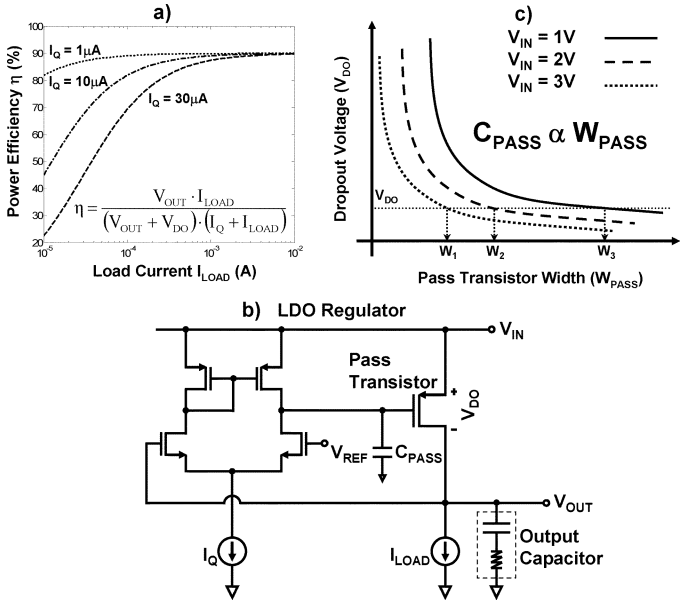

Fig. 1. (a) Plot of regulator efficiency. (b) Schematic of LDO regulator with conventional amplifier. (c) Plot of regulator dropout voltage.

Since this I_Q sets the maximum current to charge and discharge the gate capacitance ($C_{\rm PASS}$) of the pass transistor, requirement of ultra-low I_Q inevitably reduces the slew-rate ($I_Q/C_{\rm PASS}$) at the gate of the pass transistor. Transient responses are therefore degraded.

$V_{\rm DO}$ reduction also degrades transient responses of an LDO regulator. As shown in Fig. 1(c), $V_{\rm DO}$ can be reduced by enlarging the width of the pass transistor ($W_{\rm PASS}$). To achieve the same $V_{\rm DO}$ at smaller input voltage ($V_{\rm IN}$), $W_{\rm PASS}$ needs to be greatly enlarged to compensate for the limited gate-drive voltage. As $C_{\rm PASS}$ is proportional to $W_{\rm PASS}$, time required to charge or discharge $C_{\rm PASS}$ is greatly increased when both ultra-low I_Q and small $V_{\rm DO}$ at low $V_{\rm IN}$ are required. Transient responses of an LDO regulator are hence significantly degraded.

I_Q of existing LDO regulators [1]–[6] is normally ranged from several tens of to few hundreds of microamperes. For applications required ultra-fast responses [7], the I_Q is up to several thousands of microamperes. Efficiency of those LDO regulators at small $I_{\rm LOAD}$ is degraded.

In this work, a high slew-rate amplifier with push–pull output stage is thus proposed to enable an ultra-low I_Q LDO regulator

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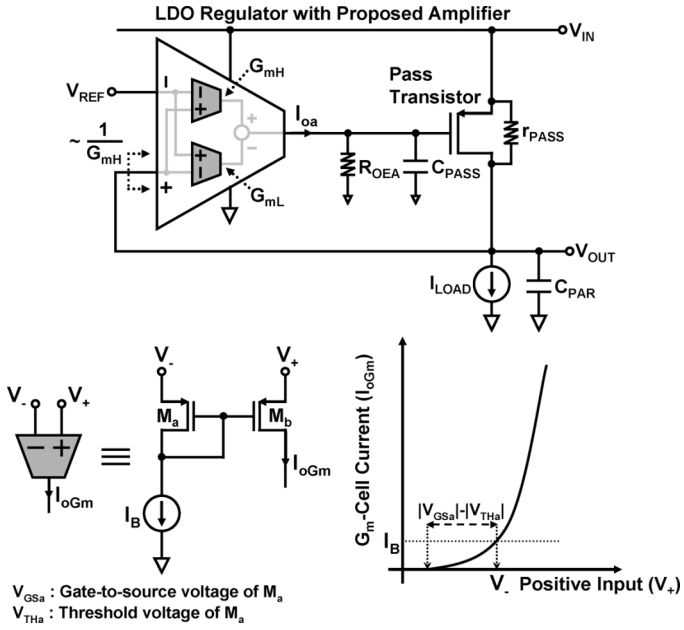

Fig. 2. Conceptual schematic of an LDO regulator with the proposed high slew-rate amplifier with push–pull output configuration.

with improved transient responses. Concept of the proposed amplifier is discussed in Section II. Circuit design and implementation are shown in Section III. Experimental results and conclusions are given in Sections IV and V, respectively.

II. Concept of Proposed Amplifier

Fig. 2 shows the conceptual schematic of an LDO regulator with the proposed amplifier, which is constructed by two common-gate differential-input transconductance (G_m) cells, G_{mH} and G_{mL}, and a current-summation circuit. Each G_m-cell is made by a constant current source (I_B) and a pair of matched transistors, M_a and M_b, in the form of current mirror.

The maximum output current of G_m-cell (I_{oGm}), and therefore the maximum amplifier-output current (I_{oa}), are no longer limited by the constant-current source I_B as in the case of conventional amplifier with a tail-current. As shown in Fig. 2, the common-gate configuration enables I_{oGm} depending on its input-voltage difference, which is the difference between the reference voltage ($V_{\rm REF}$) and the $V_{\rm OUT}$. Since all the transistors of the G_m-cell operate in saturation region I_{oGm} has a quadratic dependence on its input-voltage difference according to the square-law characteristic of MOS transistor [8]. Even if an ultra-low I_B is used, the amplifier-output current (I_{oa}) and also the amplifier slew-rate is no longer limited.

High slew-rate in both positive and negative direction is achieved with the current-summation circuit and the cross-coupled connection scheme. As shown in Fig. 2, the inputs of the two G_m-cells, G_{mH} and G_{mL}, are connected in a cross-coupled manner. The outputs of G_m-cells are connected by a current-summation circuit. Regardless of whether the $V_{\rm OUT}$ becomes larger or smaller than the $V_{\rm REF}$ during transient responses, the large I_{oGm} from either one of the G_m-cells is able to charge or discharge the gate capacitance $C_{\rm PASS}$ quickly. As a result, both positive and negative direction slew-rates can be successfully enhanced even if an ultra-low I_Q is used.

The small input-resistance of the G_m-cell helps to improve stability of LDO regulator without using any off-chip and on-chip compensation capacitors. As shown in Fig. 2, the source terminal of transistor M_b insider the G_m-cell, G_{mH}, is directly connected to the output of the LDO regulator. The open-loop output resistance of LDO regulator is now modified from its original value $\sim r_{\rm PASS}$ to $\sim r_{\rm PASS}//(1/G_{mH})$. This provides the regulator with a small open-loop output resistance under a wide range of $I_{\rm LOAD}$ from several tens of milliamperes to several μA. Even the output-parasitic capacitance ($C_{\rm PAR}$) due to the metal lines used to perform chip-level power distribution is as large as several hundreds of pF (e.g., ~ 100 pF), the regulator-output pole $\{\sim 1/C_{\rm PAR}[r_{\rm PASS}//(1/G_{mH})]\}$ is still located at high frequency and much far away from the low-frequency amplifier-output pole ($\sim\ 1/R_{\rm EOA}C_{\rm PASS}$). Stability of an LDO regulator with the proposed amplifier is greatly improved without using any on-chip and off-chip compensation capacitors. Area efficiency of such LDO regulator is highly improved. This is particular suitable for chip-level power management requiring multiple LDO regulators with high chip-area efficiency. In case a large off-chip output capacitor is used to improve transient responses under fast changing load current, stability of proposed LDO regulator can be achieved like conventional LDO regulators by the pole-zero cancellation [3], [5] where the zero is generated from the output capacitor and its equivalent-series resistor.

III. Circuit Design and Implementation

Fig. 3 shows the schematic of the proposed LDO regulator, which consists of a pMOS pass transistor ($M_{\rm PASS}$), the proposed high slew-rate push–pull output amplifier and a reference buffer. As mentioned before, the $V_{\rm DO}$ reduction, especially under a very-low $V_{\rm IN}$ (e.g., 1 V in our case), is very important to the efficiency improvement and is usually achieved by enlarging the pass transistor width $W_{\rm PASS}$. Hence, to provide 50-mA load current at 100-mV dropout under 1-V input, the aspect ratio of $M_{\rm PASS}$ ($W_{\rm PASS}/L_{\rm PASS}$), where $L_{\rm PASS}$ is the channel length of $M_{\rm PASS}$, is chosen to be 5940 μm/0.18 μm in a 0.18-μm standard CMOS process where the threshold voltage of $M_{\rm PASS}$ is $\sim |0.5\ V|$.

To ensure the proposed amplifier has fast-transient responses and large voltage-gain for input-offset reduction, the channel lengths of all transistors except the $M_{\rm PASS}$ are designed to be two and half times of the minimum feature size of 0.18-μm process, which balances the tradeoff between the need for small-gate capacitance and large-drain resistance.

To make sure the proposed regulator can be tested under several-μA I_Q (e.g., 1.2 μA in our case), gate-to-source voltage of M_{BH}, M_{BL}, and M_{Ba}, (e.g., V_B) is generated by injecting a well-defined DC current to the drain terminal of diode-connected transistor (not shown in Fig. 3) that has the same size as and is closely integrated on the same chip with, M_{BH}, M_{BL}, and M_{Ba}. Impact of process variation on the bias current (e.g., 100 nA in our case) generated by those transistors is greatly minimized. It is important to note that conventional supply-insensitive biasing circuits [8] can be used to define the V_B and be integrated with the proposed LDO regulator without any problems.

The proposed amplifier is constructed by two common-gate G_m-cells, G_{mH} and G_{mL}, and a current-summation circuit. As

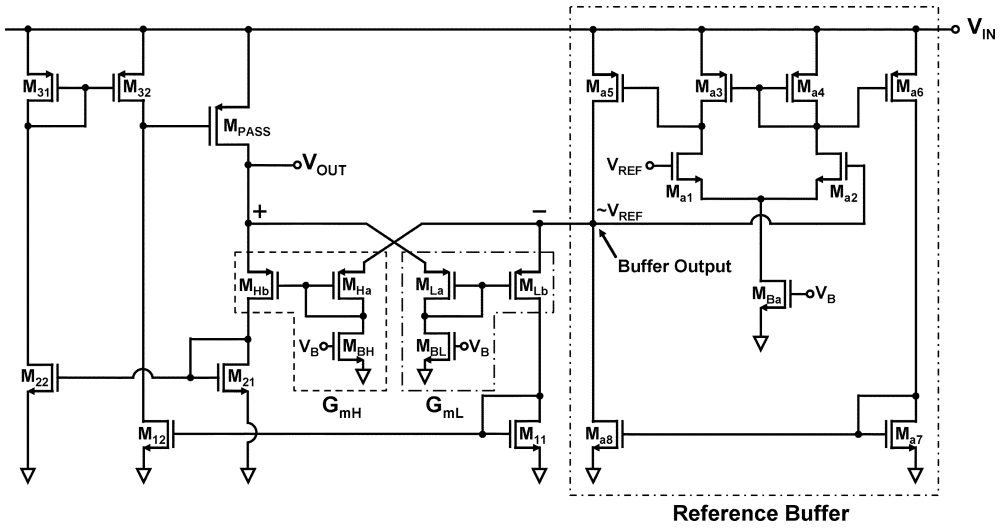

Fig. 3. Schematic of an LDO regulator with the proposed high slew-rate push–pull output amplifier and a reference buffer.

TABLE I
DIMENSIONS OF TRANSISTORS

Transistors	Ratio
M_{Ha}:M_{Hb}, M_{La}:M_{Lb}, M_{21}:M_{22} & M_{a1}:M_{a2}	1:1
M_{11}:M_{12} & M_{31}:M_{32}	1:3
M_{Ba}:M_{BH}:M_{BL}	1:1:1
M_{a3}:M_{a4}:M_{a5}:M_{a6}	1:1:6:2

shown in Fig. 3, the G_{mH} (G_{mL}) consists of two pMOS transistors, M_{Ha} and M_{Hb} (M_{La} and M_{Lb}), and one nMOS transistor, M_{BH} (M_{BL}), acting as a constant-current source. Mismatch between the input transistors (e.g., M_{Ha} and M_{Hb}) can be reduced with methods commonly used in conventional amplifier design such as placing these input transistors with common-centroid method and designing them in large width. The current-summation circuit is made by three current mirrors, M_{11} and M_{12}, M_{21} and M_{22}, and M_{31} and M_{32}, respectively.

To enable the proposed amplifier with sink and source output-driving ability, the three current mirrors are required to construct the push–pull output stage. As shown in Fig. 3, the current mirror constructed with transistors, M_{11} and M_{12}, redirects the output current of G_{mL} to the amplifier output. The large transient-output current of G_{mL} is now able to discharge the large gate capacitance of $M_{\rm PASS}$, from which sink ability is achieved. Source ability is achieved using current mirrors made by transistors, M_{21} and M_{22}, and M_{31} and M_{32}. The large transient-output current of G_{mH} is redirected to the output of amplifier and is now able to charge the large gate capacitance of $M_{\rm PASS}$. To further enhance this sink and source output-driving ability, the size of transistors, M_{12} and M_{32}, is set to three times of the size of transistors, M_{11} and M_{31}, respectively. Ratios of different transistors shown in Fig. 3 are summarized in Table I.

Moreover, the push–pull output stage constructed with transistors M_{12} and M_{32} enables the proposed amplifier with large output-voltage swing, which facilitates an LDO regulator using only moderate size $M_{\rm PASS}$ to provide a wide range of load currents under small $V_{\rm IN}$. The amplifier-output voltage is able to go from nearly zero to almost $V_{\rm IN}$ of the regulator when compared with the amplifiers using telescopic output stage. In other words, $M_{\rm PASS}$ can operate in cut-off region for small load current, or operate in saturation region or even linear region to handle heavy load current. Hence, very-large size $M_{\rm PASS}$ used to compensate the limited amplifier-output swing is no longer required in the proposed LDO regulator. The use of moderate size $M_{\rm PASS}$ also reduces its gate capacitance, and with the proposed slew-rate enhanced amplifier, the transient responses of an LDO regulator is further improved.

Since most of voltage reference circuits do not have output-current-driving ability, a reference buffer is introduced here to transfer the supply- and temperature-independent reference voltage $V_{\rm REF}$ to both the inverting input of G_{mH} and the non-inverting input of G_{mL}. As shown in Fig. 3, the reference buffer is a two-stage amplifier in unity-gain feedback. Since $V_{\rm REF}$ will not be changed quickly with time, high slew-rate is not required in the design of reference buffer. Therefore, a conventional common-source differential-input amplifier with small tail-current is chosen as the first gain stage, which is constructed with transistors, M_{a1}, M_{a2}, M_{a3} and M_{a4}, and M_{Ba} acted as a tail-current. Transistors, M_{a5}, M_{a6}, M_{a7} and M_{a8}, make up the second gain stage.

Moreover, it is important to note that the output of reference buffer is connected to a low-resistance node, which is the source terminal of transistor M_{Lb} inside G_{mL}. The pole at the output of reference buffer is therefore pushed to high frequency regime, where is much far away from the low-frequency pole at the output of first gain stage. Frequency compensation is hence not required in the reference buffer when compared with a stand-alone two-stage amplifier in unity-gain feedback.

IV. EXPERIMENTAL RESULTS

The proposed LDO regulator has been implemented in TSMC 0.18-μm CMOS process. The chip micrograph is shown in Fig. 4. Since the proposed regulator does not require any area-consuming on-chip compensation capacitors, the LDO regulator, including all the pads, only occupies 0.09 mm^2 only.

The total quiescent current I_Q of the proposed LDO regulator is 1.2 μA only. Even when the input voltage $V_{\rm IN}$ is changed from 1.8 V (the maximum voltage allowed in the 0.18-μm standard CMOS process) down to 1 V, the regulator is still able to provide a 50-mA load current $I_{\rm LOAD}$ and 0.9-V output voltage $V_{\rm OUT}$.

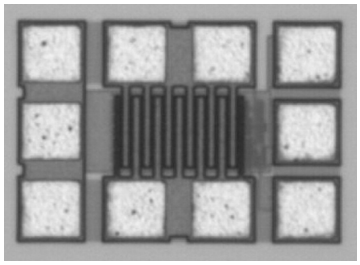

Fig. 4. Chip micrograph of the proposed LDO regulator.

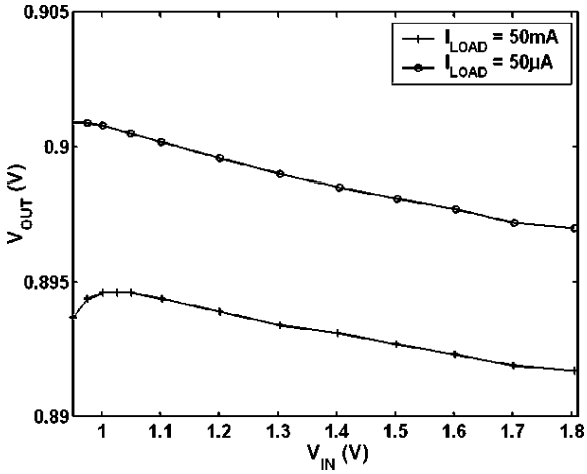

Fig. 5. Measured line regulation under 50 μA and 50-mA load current.

Fig. 5 shows the measured line regulation with different load-current levels (e.g., 50 μA and 50 mA). The line regulation is measured to be 4.75 mV/V at 50-μA $I_{\rm LOAD}$ and 3.625 mV/V at 50 mA $I_{\rm LOAD}$. The load regulation at 1.0 V $V_{\rm IN}$ is measured to be 148 μV/mA. From the measurement results, satisfactory line and load regulation are successfully achieved using only 1.2 μA I_Q.

In Fig. 5, it is found that the $V_{\rm OUT}$ is decreasing but not increasing with an increasing $V_{\rm IN}$. With extensive simulations and detailed analyses, the origin of this interesting phenomenon is found to be caused by the process-variation induced drain-resistance mismatch between M_{12} and M_{22}. Since the channel lengths of M_{12} and M_{22} are in deep sub-micron regime, channel length modulation (CLM) and short-channel effect such as drain-induced barrier lowering (DIBL) [9] make the drain resistance of these transistors to be very sensitive to the absolute value of channel length. Even though these transistors are matched in the layout using common-centroid method, any process variation induced channel-length mismatch still inevitably introduces mismatch between the drain resistance of transistors M_{12} and M_{22}.

Fig. 6 shows the simulated line regulation with different levels of channel-length mismatch between M_{12} and M_{22}. When the channel length of M_{22} (L_{22}) is smaller than that of M_{12} (L_{12}), the drain resistance of M_{22} becomes smaller than that of M_{12}. Once $V_{\rm IN}$ is increased, the drain current of M_{22} becomes larger than that of M_{12}. To match the drain currents of transistor M_{12} and M_{22}, $V_{\rm OUT}$ is forced to be decreased by the negative-feedback action of the amplifier. The negative slope of the measured line regulation (Fig. 5) is resulted from the channel-length mismatch between M_{12} and M_{22} (e.g., $L_{12} > L_{22}$).

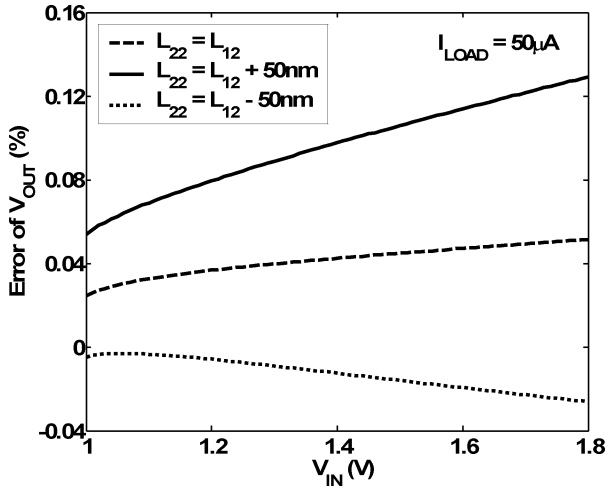

Fig. 6. Simulated line regulation with different levels of channel length mismatch between transistors M_{12} and M_{22}.

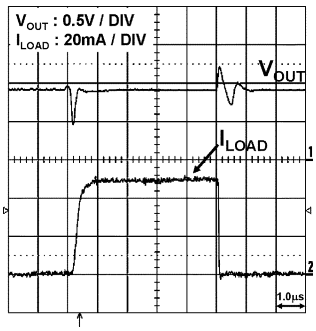

Fig. 7. Measured load-transient responses of the proposed LDO regulator without an off-chip output capacitor.

Load and line transient responses are measured to evaluate the transient performance of LDO regulator with the proposed amplifier. Fig. 7 shows the measured load-transient responses without an off-chip output capacitor. The $I_{\rm LOAD}$ varies from 50 μA to 50 mA, and $V_{\rm IN}$ is 1.2 V. Measurement result shows that the proposed LDO regulator responds within $\sim$ 200 ns and is fully recovered within $\sim$ 1 μs at 1.2 μA I_Q.

Fig. 8 shows the measured load-transient responses with a 100 pF off-chip output capacitor. It is used to model the regulator-output-parasitic capacitance from the metal lines used to implement chip-level power distribution. The $I_{\rm LOAD}$ again varies from 50 μA to 50 mA at 1.2 V $V_{\rm IN}$. Measurement result shows the proposed LDO regulator is fully recovered within 3 μs at 1.2 μA I_Q.

The measured line-transient responses without an off-chip output capacitor and with a 100 pF off-chip output capacitor are shown in Figs. 8 and 9, respectively. The $V_{\rm IN}$ varies from 1.2 to 1.7 V and the load current is 50 mA. Measurement results show that the output voltage of the LDO regulator can be recovered within $\sim$ 4 μs.

The measurement results shown in Figs. 7–10 confirm that stability of LDO regulator with the proposed amplifier is successfully achieved without using any on-chip and off-chip compensation capacitors. Even a parasitic capacitor with several hundreds of pF existed at the regulator output, stability is also guaranteed.

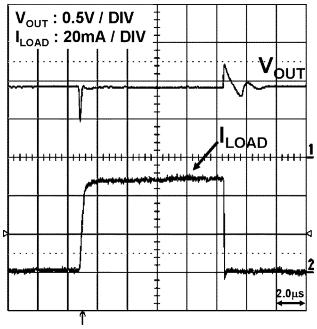

Fig. 8. Measured load-transient responses of the proposed LDO regulator with a 100 pF off-chip output capacitor.

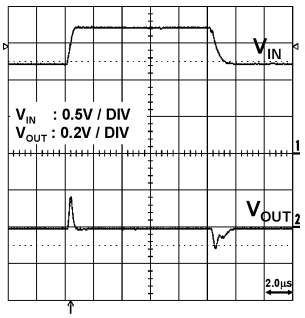

Fig. 9. Measured line-transient responses of the proposed LDO regulator without an off-chip output capacitor.

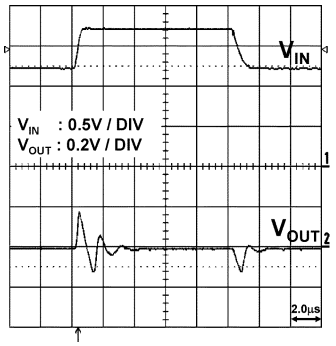

Fig. 10. Measured line-transient responses of the proposed LDO regulator with a 100 pF off-chip output capacitor.

Table II provides comparison between performance of the proposed LDO regulator and other published designs that are targeted for chip-level power management. A figure of merit ($\mathrm{FOM} = T_R \times I_Q / I_{\mathrm{LOAD\_MAX}}$) used in [7] is adopted here to evaluate the effect of I_Q to the load transient response time (T_R) in different designs. A lower FOM implies a better slewing performance. The proposed regulator has very comparable FOM (0.067 ns) to the design in [7]. However, the proposed regulator only requires 1.2 μA I_Q compared with 6 mA in [7]. It makes the proposed regulator with superior current efficiency at light-load condition. This feature is very important and attractive to any battery-powered mobile systems.

TABLE II
PERFORMANCE COMPARISON

	[5]	[7]	[4]	**This work**
Year	2003	2004	2007	**2007**
Tech. [µm]	0.6	0.09	0.35	**0.35**
V_{IN} [V]	1.5	1.2	1.2	**1.0**
V_{DO} [V]	0.2	0.3	0.2	**0.1**
$I_{LOAD\ MAX}$ [mA]	100	100	100	**50**
I_Q [mA]	0.038	6	0.1	**0.0012**
T_R [µs]	2	0.00054	50	**2.8**
FOM [ns]	0.76	0.032	50	**0.067**

V. CONCLUSION

A high slew-rate amplifier with push–pull output stage is introduced to improve transient responses of an LDO regulator which uses ultra-low I_Q to improve light-load efficiency and large-size pass transistor to reduce dropout loss. The proposed amplifier is able to provide a push–pull transient-output current, which is much larger than its quiescent current. Time required to charge or discharge the large pass transistor gate capacitance is greatly reduced. Both load and line transient responses of an LDO regulator are thus improved.

Experimental results show that the proposed LDO regulator with only 1.2 μA I_Q is able to recover within $\sim$ 4 μs under the worst case scenario. It also proves that the proposed unique structure enables a stable LDO regulator without using any on-chip and off-chip compensation capacitors. Chip-area efficiency is thus greatly improved and multiple proposed LDO regulators can be applied in chip-level power management.

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