A High-Speed, Low-Noise CMOS 16-Channel Charge-Sensitive Preamplifier ASIC for APD-Based PET Detectors

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***Abstract*--A high-speed, low-noise 16-channel amplifier IC has been fabricated in the HP 0.5 μm CMOS process. It is a prototype for use with a PET detector which uses a 4x4 avalanche photodiode (APD) array having 3 pF of capacitance and 75 nA of leakage current per pixel. The preamplifier must have a fast rise time (a few ns) in order to generate an accurate timing signal, low noise in order to accurately measure the energy of the incident gamma radiation, and high density in order to read out 2-D arrays of small (2 mm) pixels. A single channel consists of a charge-sensitive preamplifier followed by a pad-driving buffer. The preamplifier is reset by an NMOS transistor in the triode region which is controlled by an externally supplied current. The IC has 16 different gain settings which range from 2.085 mV/fC to 10.695 mV/fC. The gain is determined by four switched capacitors in the feedback loop. The switch state is set by two digital input lines which control a 64-bit shift register on the IC. A preamplifier 10-90% rise time as low as 2.7 ns with no external input load and 3.6 ns with a load of 5.8 pF was achieved. For the maximum gain setting and 5.8 pF of input load, the amplifier had 400 electrons of RMS noise at a peaking time of 0.7 μs. The IC is powered by a +3.3 V supply drawing 60 mA.**

I. Introduction

In positron emission tomography (PET), detection of 511 keV annihilation photons is accomplished by scintillator crystals coupled to transducers that convert the light into an electrical signal. The transducers must be fast (in order to accurately determine the time of interaction) and low noise (in order to measure the energy deposited by the interacting photon). Currently, most PET modules utilize photomultiplier tubes (PMTs) for this purpose. Although PMTs are very fast and have high gain, their size limits the spatial resolution of detectors. The PMTs are much larger than the individual scintillator crystals, so commercial PET detectors use optical encoding schemes [1], which leads to spatial blurring. Avalanche photodiodes (APDs) have the potential to address this issue, as they can be fabricated with pixel sizes that are matched to the few mm sizes of the individual scintillator crystals. Because they have internal gain (typically 50–500) and a fast rise time (~1 ns), the APD signal-to-noise is good both at the bandwidth necessary to generate an accurate timing signal (~1 GHz) and at the lower bandwidths (~1 MHz) necessary to measure energy accurately. Consequently, a number of PET detector concepts based on APD readout have been proposed [2-6]. However, most of these prototypes have used amplifiers using discrete components. Given the large number of pixels in a PET camera, a complete camera requires a multi-channel custom IC to amplify the signals from the APD array.

Several ICs designed for APD-based PET cameras have been designed [7-9], but all have drawbacks. The amplifier in [7] was designed for a 10 pF APD and uses a "super-regulated" cascode topology that further boosts the open-loop gain by increasing the loop gain of the local feedback, but the IC contains only a single channel. The amplifier in [8] uses a regulated, or "gain-boosted" cascode (this adds a local feedback loop which helps boost the open-loop gain of the op-amp) and was designed for a relatively high capacitance (30 pF) APD, but it too has only a single channel. The amplifier in [9] is a 16-channel array that uses a JFET as the input device, but has a relatively slow (20 ns) rise time.

We have fabricated an IC for amplifying the signals from the 16-channel (4x4 array of 2 mm x 2 mm pixels) APD array made by RMD Inc. [10]. APD signal in the HP 0.5 μm CMOS process. The capacitance is ~3 pF per pixel, and while both the APD gain and the leakage current depend on bias voltage, the gain ranges from 10^2-10^3 and the leakage current ranges from 10 nA-1 μA per pixel.

II. Circuit Design

A. Basic Specifications

The IC was fabricated with an HP 0.5 μm CMOS process with a 3.3V power supply. It has 16 analog inputs, 16 analog outputs, and 16 probe pads for probing the preamplifier outputs. It requires one external reference current of 350 μA and two other external reference currents which adjust rise and fall times. Finally, it has three digital inputs and two digital outputs which are used for controlling gain settings.

B. Concept

The basic concept of the amplifier is shown in Figure 1. Each channel consists of a charge-sensitive preamplifier

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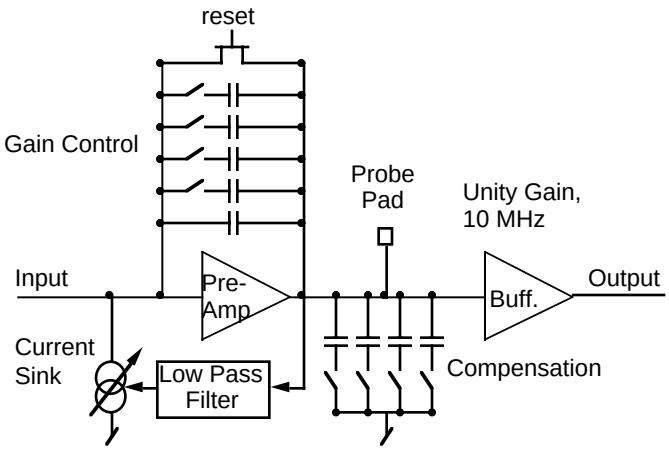

Figure 1: Block diagram of a single channel.

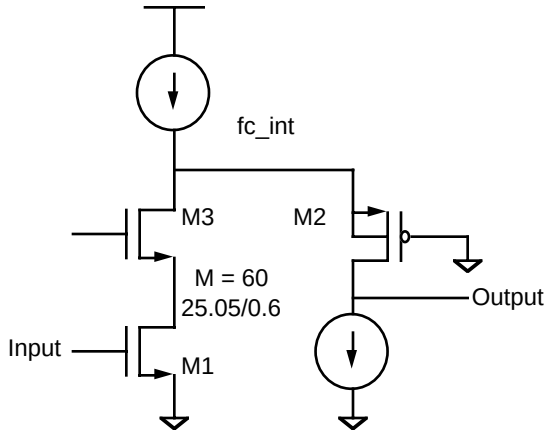

Figure 2: Schematic of a single channel.

followed by a simple output buffer for driving a pad. The IC contains 16 of these channels. A small pad for an on-chip probe has been placed at the output of each preamplifier. This output has a rise time on the order of nanoseconds and will hence be referred to as the "fast output." Because the preamplifier is not capable of driving the large capacitance associated with a bonding pad, an output buffer is inserted in between the preamplifier and the output pad. The output of the buffer has a rise time on the order of hundreds of nanoseconds to microseconds (controlled by an external capacitor) and will thus be referred to as the "slow output." In the future, the fast output can be connected to an on-chip constant-fraction discriminator (CFD), which will be used to generate the timing signal which is currently generated by PMTs in existing PET scanners. The buffer can be replaced by a true shaper with an adjustable shaping time.

The gain is determined by the value of the feedback capacitor. If Q_{inj} is the charge injected by the detector, the output voltage is equal to Q_{inj}/C_F. Therefore larger values of C_F lead to lower gain. The IC has 4-bit gain control, where more or less capacitance is switched in depending on the gain setting. The 64 bits of gain data are be clocked into the IC using a shift register consisting of standard-cell D flip-flops. Changing the gain also changes the compensation requirements of the channel, thus more or less compensation capacitance(C_L) is switched in depending on the gain setting.

The amplifier is reset by a single NMOS device (MR1) connected between the input and output and operated in the triode region. This device acts like a variable resistor, which means that the reset time is controlled by the RC delay of MR1 and the feedback capacitance C_F. Because C_F controls the gain, the effective "resistance" of MR1 needs to be adjusted according to the gain if the reset time is to remain the same. This "resistance" is controlled by an external input current mirrored to all channels. However, because a single input current controls all 16 channels, channels with different gains may experience varying reset times. This variation is only important when the event rate is extraordinarily high.

C. Core Amplifier

The core of the preamplifier circuit is shown in Figure 2. It is essentially a folded cascode of the large NMOS input transistor (M1) with a small PMOS (M2). To achieve high speed, a large current of 2.5 mA is run through M1, while the cascode device M2 carries a much smaller current of 270 μA. The input is also cascoded (M3) in order to minimize the Miller capacitance seen at the gate of M1. The dominant pole is designed to be at the output, while the first nondominant pole is at the source of M2 (labeled "fc_int"). This pole is therefore the critical pole when considering stability issues and its location limits the performance of this amplifier. The compensation capacitor on the output (C_L in Figure 1) is adjusted to make the amplifier stable in the presence of this nondominant pole.

D. Automatic Leakage Current Compensation

One of the IC requirements is that it be compatible with APD arrays from different vendors and in different biasing conditions. This requires the preamplifier to automatically accommodate a wide range of detector leakage current with little or no change in the output response. This feature is also necessary when pixels from the same array show a large leakage current dispersion. The automatic compensation scheme, shown in Figure 1, consists of a very low bandwidth transconductor connected between input and output [11]. The transconductor provides to the input the DC current necessary to keep the output node at a reference voltage. As long as the bandwidth of this stage is kept low enough (we used ~1 kHz), the fast signal response is not affected and it is still determined by the single transistor conductance described in Section IIB. The maximum current that can be compensated for is limited by the (externally provided) biasing of the transconductor. The dominant pole of this stage moves to higher frequency depending on the bias, so excessive bias results in ringing on the amplifier output signal. Our design can accommodate up to a few mA of leakage before the amplifier response is affected.

E. Pad Driver

Although the most interesting part of this IC is the fast output of the preamplifier, making noise measurements is greatly facilitated by having the output available off-chip. Therefore the fast output has been fed to a simple output buffer which drives a bonding pad. When the output buffer drives an RC load of 8 kΩ, 47 pF, it has a bandwidth of

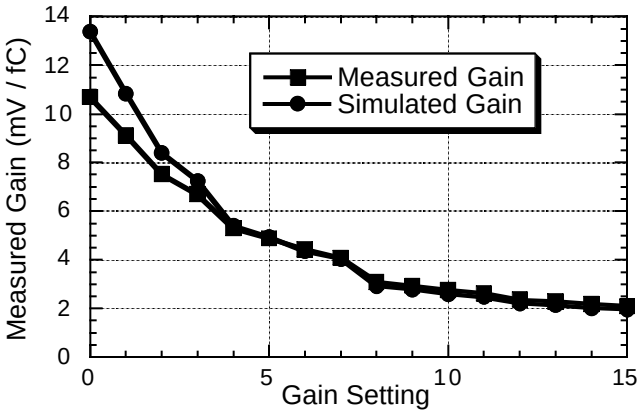

Figure 3: Gain vs. gain control setting.

approximately 1 MHz. This bandwidth can be adjusted by changing the value of the capacitor.

F. Simulation Results and Discussion

Prior to fabrication, the circuit was simulated with the HSPICE analog simulator. As mentioned previously, the IC has 16 different gain settings. Gain changes are accomplished by changing the feedback capacitance C_F and the compensation capacitance C_L.

DC characteristics are independent of the gain setting because only capacitances are changed. The core amplifier has a maximum gain of 786, and over the expected maximum signal swing (between 680 mV and 1.18 V), the gain remains greater than 600. At low frequencies, the capacitors have high impedance compared to the reset "resistor", so the loop gain is equal to the gain of the core amplifier. At medium frequencies, the core amplifier still acts as if it were at DC and the only poles and zeros occur through the feedback path.

There is a pole at frequency $1/[2\pi R_F(C_F + C_{in})]$ and a zero at frequency $1/[2\pi R_F C_F]$. The pole can logically be attributed to the amplifier's input node, which has a resistance R_F and capacitance $C_F + C_{in}$ attached to it. The zero can be attributed to feedforward across the feedback path and has a time constant of $R_F C_F$.

The bandwidth and phase margin of the amplifier are determined by the poles of the core amplifier. The dominant pole can be attributed to the output, while the first nondominant pole arises at the cascode node ("fc_int" in Figure 2). Another nondominant pole exists at the input cascode node (drain of M1), but it has a much smaller effect on the frequency response than the first nondominant pole. The nondominant poles limit the bandwidth of the amplifier because the dominant pole must be adjusted (by changing C_L) to keep the amplifier stable.

III. PERFORMANCE

A. Power Consumption

With one input and one output bonded, the IC consumed 60 mA of static current from the +3.3 V supply (198 mW). The power consumption is not expected to change significantly when all of the lines are bonded because current still runs through channels with the input open. The measured power consumption agrees closely with the simulation result of 63 mA.

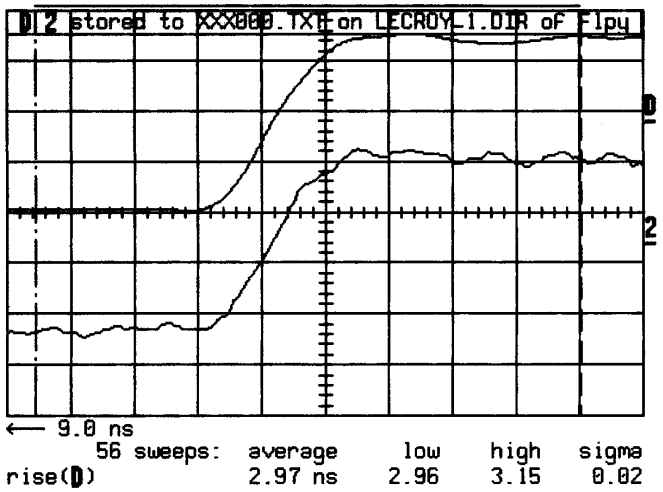

Figure 4: Scope trace showing preamplifier rise time, both as averaged (top trace) and single shot (bottom trace) signals.

B. Gain

The gains for each of the 16 settings are shown in Figure 3. They ranged from 2.1 mV/fC to 10.7 mV/fC. The gain was measured with a test pulse as an input. The input was bonded to a 2.6 pF trace plus a 3 pF capacitor to ground to simulate the APD. The gain was linear (within a few percent) for input charges between 20 fC and 45 fC at a gain setting of 0 (10.7 mV/fC).

C. Preamplifier Rise Time

The rise time of the preamplifier was measured with a square wave coupled to the input through a 0.5 pF injection capacitor. A Picoprobe Model 18B (350 MHz bandwidth) connected to a 1 GHz oscilloscope was used to probe the preamplifier output on-chip, and the oscilloscope's 10-90% rise time measurement was used on the averaged signal to determine the rise time. The rise times were measured both with no input trace bonded and with a load capacitance connected from the input to ground. A typical oscilloscope trace (gain setting=8 and 2.6 pF input load) is shown in Figure 4. This setup yielded a 1.6 ns rise time when directly probing the pulser signal (BNC cable: ~500 ps). The results are plotted with respect to gain setting and input load in

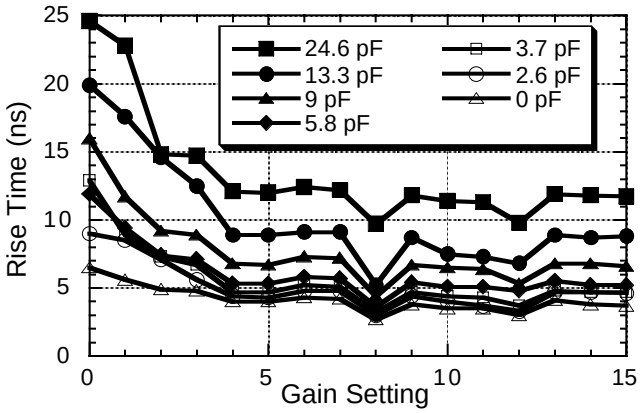

Figure 5: 10%-90% rise time vs. gain control setting.

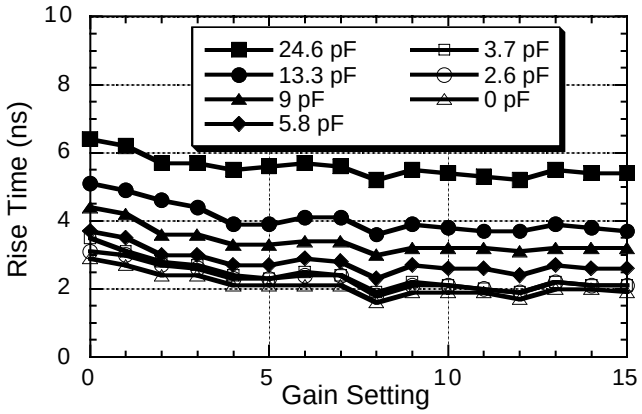

Figure 6: 5%-55% rise time vs. gain control setting.

Figure 5. The variance with the gain setting is expected. Four compensation settings were used to cover 16 gain (feedback capacitor) settings, and the result is that some gain settings are designed to be more aggressive than others. Reflections in the measurement apparatus distort the latter portion of the rising edge, giving 10-90% rise times that are exaggerated, especially with gains (settings 0-4). Therefore, the 5%-55% rise times are shown in Figure 6. In a real PET detector the fast output will be used to generate a timing pulse, and thus should trigger long before the 90% level is reached.

D. Noise/Energy Resolution

To measure noise, the preamplifier a test pulse is injected into the preamplifier and the output signal is shaped with a NIM module and sent to a LeCroy 3512 ADC, which converts it for readout through a computer running LabVIEW. Figure 7 shows measured RMS noise versus shaper peaking time and input capacitance for a maximum gain setting of 10.7 mV/fC. The measurements should be considered upper limits, as the noise corresponds to only a few mV, which is comparable to the width of an ADC bin. Even with a very large input capacitance, the noise is almost three orders of magnitude smaller than the signal. The results demonstrate that the total noise will be dominated by the parallel noise contributed by the APD leakage current, and therefore the amplifier should be operated at short shaping times to minimize this parallel noise.

To measure the effects of noise due to leakage current and the compensation circuit, an APD is connected to the amplifier input and bias voltage applied. While the leakage

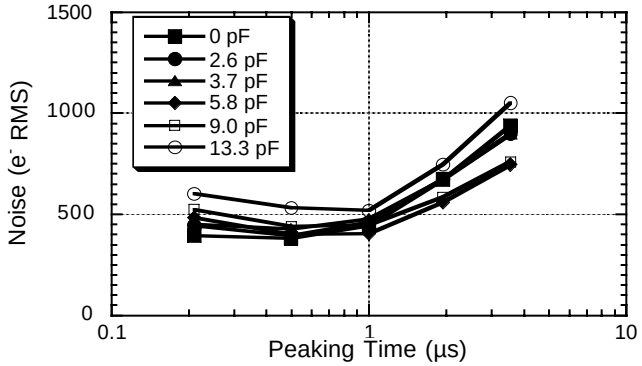

Figure 7: Noise vs. peaking time for several capacitive loads.

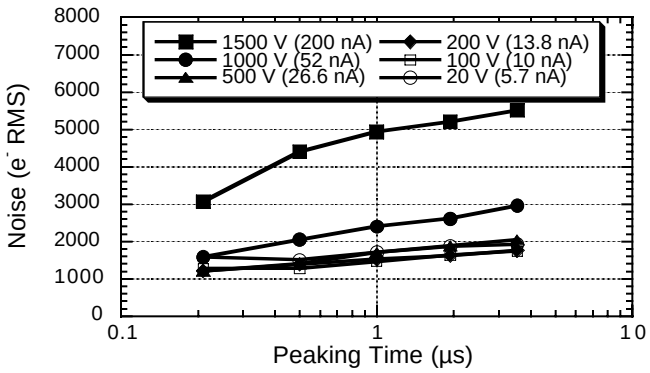

Figure 8: Noise vs. peaking time with an APD load.

current depends strongly on the bias voltage, the device fully depletes at a low voltage and so the capacitance is ~3 pF, independent of bias voltage. Thus, we can measure the noise versus leakage current (with a constant input capacitance). Figure 8 shows such data. It indicates that when the leakage current is ≤25 nA and for the range of peaking times measured (200 ns – 3.5 μs), the series noise is dominant. When the leakage current is >25 nA, the shot noise is dominant and the lowest noise is obtained at short shaping times. In fact, the noise minimum probably occurs at peaking times less than the lowest we used (200 ns), but our peak detect circuit and ADC prevented us from using shorter peaking times.

The energy resolution was measured by coupling a 3x3x22 mm^3 LSO crystal to an APD and exciting it with 511 keV photons from a ^{68}Ge positron source, and the resulting pulse height spectrum is shown in Figure 9. An energy resolution of 16% FWHM was measured for a peaking time of 300 ns. Figure 9 also shows a pulse height spectrum

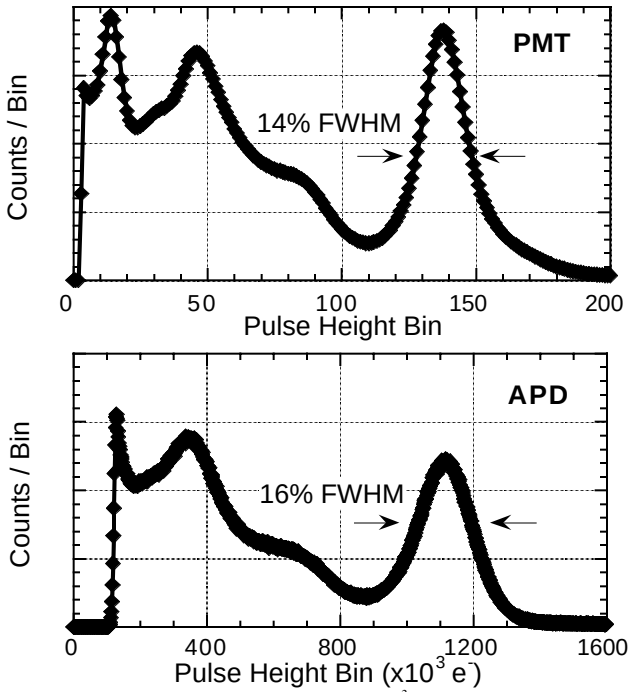

Figure 9: Pulse height spectrum of a 3x3x22 mm^3 LSO crystal excited with 511 keV photons. Top: read out with a PMT. Bottom: read out with an APD.

for the same crystal measured with a PMT (14% FWHM).

Several factors give sub-optimal noise performance with the APD setup. First, the shaper was not operated at the noise minimum. Because parallel noise is dominant, short shaping times are optimal, but the shaper and ADC used are not fast enough to reach the noise minimum. Second, the measured APD leakage current was ~200 nA, far above the specification of < 75 nA. As the dominant electronic noise source is the leakage current, improvements in APD fabrication technology should further improve the energy resolution. Finally, the electronic noise cannot account for the difference between energy resolutions seen by the PMT and the APD, and so it is presumed that the scintillator-photodetector coupling is worse for the APD. The results for the APD compare well with those obtained with a PMT and indicate that the APD is a viable replacement for the PMT in a PET detector.

IV. Conclusions

The high speed and density of avalanche photodiodes makes them possible replacements for photomultiplier tubes in high-resolution PET detectors. However, high density readout electronics (i.e., ASICs) must be developed before this can be realized. Therefore, this project fabricated a high-speed, low-noise 16-channel amplifier IC in the HP 0.5-µm CMOS process. Measurements with this IC demonstrate the potential of an APD-based detector module to fulfill the demanding timing and energy resolution requirements of PET.

Future directions for this research include on-chip integration of additional functionality required for eventual use in a complete PET detector module. A constant fraction discriminator circuit which takes the preamplifier output as its input will produce the timing signal normally generated by the PMT. A true shaper with rise and fall time controls will replace the simple output buffer. A more elaborate digital control scheme will enable the implementation of additional controls which can be set externally. The implementation of these functions will enable the construction of a detector module which replaces all photomultiplier tubes with APDs.

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