A high-voltage compliance, 32-channel digitally interfaced neuromodulation system-on-chip

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***Abstract*—This paper presents the integration of a 32-channel neuromodulation system on chip (SoC) which is developed for chronic implantation in humans. The ASIC offers low noise recording, a state-of-the-art (SotA) neurostimulator capable of both current and voltage controlled stimulation with high-voltage compliance, on-chip 16-bit data digitization as well as safety features like electrode impedance estimation and charge balancing. The chip communicates through two distinct SPI interfaces for independent command and data transfer. Thus, the developed system constitutes a fully digital, bidirectional 32-channel interface to the brain.**

***Index Terms*—ASIC, Brain-Machine-Interfaces, BMI, Neurostimulation, Neuromodulation, Biomedical Implant, Brain Implant**

I. Introduction

THE rapid progress in the field of brain-machine-interfaces (BMIs) is fueling neurophysiological research and the development of potential clinical applications [1], [2]. Modern implantable systems allow massively-parallel, ultra-low noise recording on dozens or even hundreds of channels [3], alongside sophisticated stimulation capabilities [4], [5]. Closed-loop neuromodulation is achieved by adapting the stimulation parameters and patterns to the biomarkers extracted from the recorded data. This is a powerful tool for both basic research as well as future treatment for diseases like Parkinson's Disease and Epilepsy [6], [7], [8]. Furthermore, the combination of biosignal extraction and feedback through electrical stimulation could result in a new generation of significantly improved neuro-controllable prosthetics [9], [10].

Many different architectures for neural recording applications have been presented and constitute the state-of-the-art, each with a specific set of advantages and disadvantages. AC-coupled front-ends solve the issue of large electrode DC offset (EDO) superposing the signal by capacitive coupling, thus preventing the saturation of the amplifier. However, the input capacitors are very costly area-wise and the noise performance is limited by flicker noise of the first amplifier's input pair [11]. This can be solved by using a chopped neural front-end which mitigates the flicker noise contribution of the LNA, but at the cost of an additional DC servo loop (DSL) for offset suppression and a significant decrease in input impedance which must be compensated [12], [13]. DC-coupled designs optimize the circuit area by omitting the input capacitor and employing mixed-signal feedback loops for input offset compensation, however with limitations to linearity and noise performance [14].

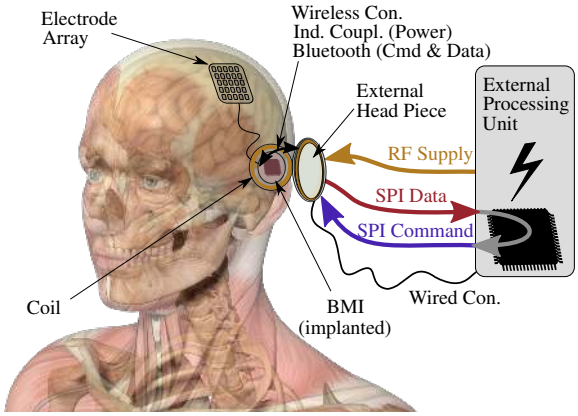

Fig. 1. Simplified setup for targeted neuromodulation system

The same holds true for implantable stimulators, which vary strongly depending on the targeted application. A large number of different electrodes are available to chose from, with severe differences in type (surface or penetrating/shaft electrodes), geometry/size and material, resulting in a vast range of potential electrode impedances. Desired stimulation currents can range from several µA for sub-retinal and intracortical stimulation to several mA for motor muscle and cortical stimulations [15], with the requirement of high precision timing for well-controlled charge delivery. Several modes have been published, amongst which are charge-controlled [16], current-controlled and voltage-controlled stimulations.

In this article, the system integration of a 32-channel neuromodulation system is shown, which is designed for chronic implantation in humans. Individual circuit components have been prototyped before and have now been integrated into a fully digital neural-interface on chip (NoC). This presented system provides an all-digital, bidirectional, multi-parallel interface to the brain. In contrast to several prior art publi-

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Special thanks for photographs and electrode arrays goes to CorTec GmbH in Freiburg, Germany.
We thank Dr. Dennis Kätzel and Gabriel Gschwend (Ulm University) for their support with in-vivo recordings.
This work was funded by the German Federal Ministry of Education and Research under research grant MR:Implant.
Manuscript received September 16, 2020; revised January 11, 2021.

Fig. 2. Photograph of the neural implant: *On the left* encapsulation of the electronics and *on the right* full system including various electrode array types. Courtesy of CorTec GmbH, www.cortec-neuro.com

cations that presented closed-loop neuromodulation with on-chip feature extraction for treatment of Epilepsy or Parkinson's Disease, this NoC relies on an external control unit to close the loop. This provides greater flexibility, as classification algorithms can easily be reprogrammed and adjusted, thereby allowing the developed hardware platform to be used in various applications. External out-of-body processing relaxes power constraints on the classification hardware, meaning that commercially available CPUs or FPGAs can be utilized to run more computationally expensive classifications with additional benefit in computation time. This is however bought at the cost of potentially much higher transmitter power and data rate. Also, additional latencies arise from data and command transmission, which can compensate the classification time benefits achieved by powerful external processing hardware and need to be small enough to not become the dominant delay contributor in the loop. The $2.4\,\mathrm{GHz}$ wireless transmission between implant and external unit can add latencies of several $10\,\mathrm{ms}$, with negligible additional delay introduced by the SPI-programming of the ASIC ($\leq 3.5\,\mathrm{ms}$). Therefore, event response times similar to state of the art internal classifiers (e.g. for epilepsy therapy), achieving latencies of $\leq 0.1\,\mathrm{s}$ [17] and $\leq 0.3\,\mathrm{s}$ [18], are possible.

The ASIC provides a 32-channel interface to the brain for any processing entity capable of SPI command and data transfer and is therefore easy to employ. To cover many different application scenarios, the NoC is capable of low noise neural recording in both LFP (local field potentials) and AP (action potentials) frequency bands with a large number of gain and bandwidth adjustments, as well as biphasic current- and voltage-controlled stimulation with $50\,\mathrm{dB}$ of dynamic range and high-voltage compliance. A larger channel count can be achieved by clustering, which allows controlling several NoCs from a single command SPI by assigning unique 3-bit IDs.

Fig. 1 shows the simplified application scenario for which this NoC was developed. The neural implant (see Fig. 2) contains the brain-machine-interface, a Bluetooth communication module, a microcontroller and a power management module. An external head piece provides the power via inductive link and handles the Bluetooth-based command and data transfer. An external processing unit is connected by cable. This component handles the extraction of biomarkers from the recorded data and can react with adapted stimulation commands if necessary. Finally, it contains the battery and an optional mass storage device for long-term monitoring.

This article is organized as follows: Section 2 presents the individual components of the neuromodulator ASIC. Measurement results are shown in Section 3, including in-vitro and in-vivo validation; Section 4 concludes the paper.

II. 32-Channel Neuromodulator ASIC

The presented neuromodulator ASIC is the result of several years of research in the field, where most individual circuit elements have been published earlier. Together with partial enhancements, the individual parts have been combined with a custom control and ADCs to form a state of the art digitally controlled neural interface.

Fig. 3 shows a circuit level overview of the ASIC. It consists of 32 channels of a high-voltage (HV) compliant, reconfigurable constant-voltage and constant-current (CVS/CCS) stimulator [19], an electrode impedance estimation [20], artifact reduction and a low-noise recorder for both local field potentials (LFPs) and spike data (action potentials, APs), followed by a switched capacitor biquad with adjustable frequency selection [11]; the channel is further illustrated in Section II. Each 16 channels are multiplexed onto one of two on-chip 16-bit incremental delta-sigma ADCs. Stimulation timing control is globally stored and executed [21], which allows almost arbitrary stimulation waveforms. Local stimulation and recorder settings are stored in the local control units. Programming data for global and local settings is received via a Command SPI, while the 16-bit data from the ADCs is provided by a Data SPI at a rate of $640\,\mathrm{kS/s}$. Thus, the overall neuromodulator can be digitally interfaced to a system μC or FPGA or be directly controlled via a (wireless) serial data stream. The ASIC occupies an area of $5.3\,\mathrm{mm} \times 4.7\,\mathrm{mm}$, consumes roughly $6.2\,\mathrm{mW}$ (recording) and was fabricated in $180\,\mathrm{nm}$ HV CMOS.

A. Recorder

The capacitively coupled recording frontend is shown in the green part of Fig. 3 [20]. The LNA is a simple telescopic amplifier with large input transistors scaled in weak inversion for low 1/f noise. The large bias current for low thermal noise increases the gain-bandwidth. Thus, an AAF filter is required to limit the signal bandwidth before the subsequent switched-capacitor (SC) filter. These filters are implemented as biquads and offer various gain and bandwidth settings.

Two frequency bands are typically of interest in neural recording. Local field potentials (LFPs) consist of the averaged potential of hundreds or even thousands of neurons in proximity of the electrode and correspond to the general level of activity in the observed brain region. The LFPs range from approximately $0.2\,\mathrm{Hz}$ to $200\,\mathrm{Hz}$ with expected amplitudes of up to $5\,\mathrm{mV}_{pp}$. Given the $3\,\mathrm{V}$ supply voltage of the LV-recorder, the maximum signal amplification is limited and a trade-off between linearity and input-referred noise is necessary. The LNA stage was thus given a gain of $40\,\mathrm{dB}$, while subsequent stages allow to increase this gain up to $58\,\mathrm{dB}$ for LFP signals. The action potentials (APs) or spikes are located in the frequency band of $200\,\mathrm{Hz}$ to $7.5\,\mathrm{kHz}$ and consist of the activation response of a single neuron. The AP signal

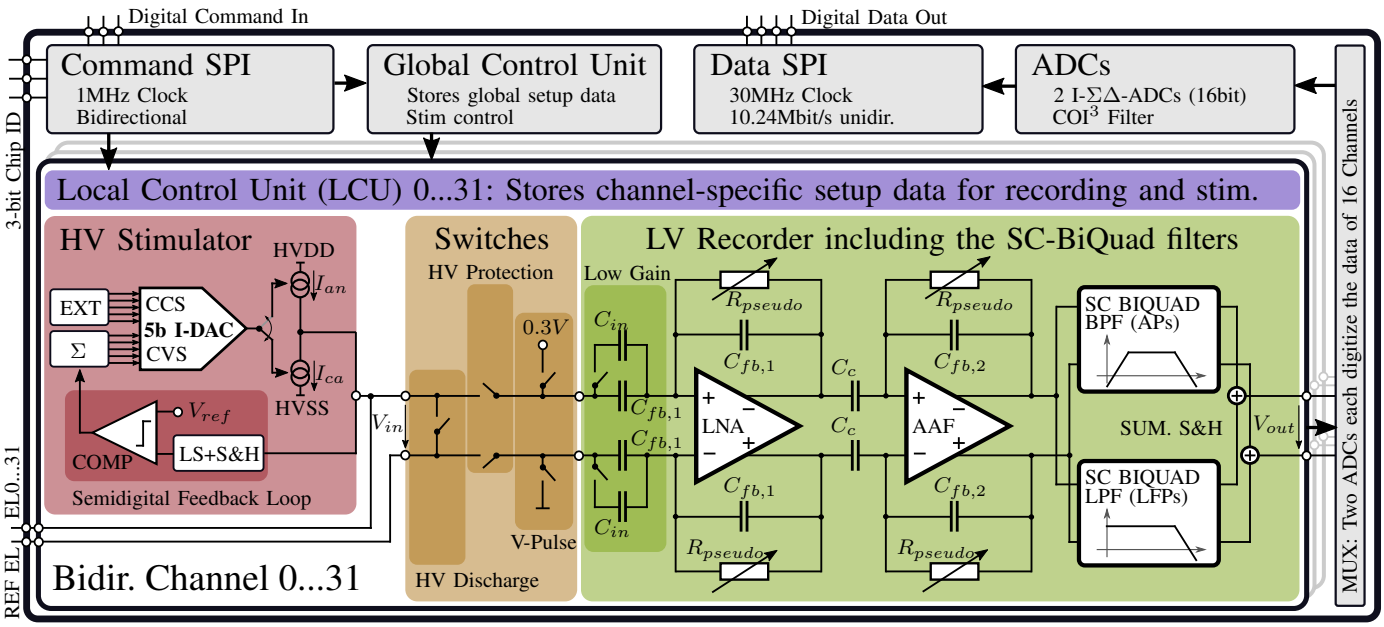

Fig. 3. Simplified ASIC architecture focusing i) on the digital interfacing and control as well as ii) on the circuit implementation of the 32 bidirectional channels. Shown *in red* is the CCS HV stimulator with feedback loop for CVS, *in orange* the switches used for blanking, passive charge balancing and electrode impedance estimation, and *in green* the recorder frontend including the subsequent filtering stages

amplitudes are typically at least an order of magnitude smaller than that of LFP biosignals, thus the respective gain options are larger (up to 70 dB). The input-referred noise was targeted to be $\leq 3.5\,\mu V_{rms}$ in both bands

The band-specific amplification allows to equalize both signal bands to approximately equal amplitude before digitization, thereby relaxing the ADC's dynamic range requirements [11], [20]. After the filtering and band-specific amplification, both signal bands are recombined in a summing S&H stage, with the option to deactivate either of the signal bands, allowing LFP only, AP only and equalized full-band recording modes. Due to the superposition of signal components from both filters in the intermediate frequency range between LFPs and APs (100 Hz to 400 Hz) in full-band recording mode, phase-shift induced signal distortion may occur. As the switched capacitor filter corners offer high precision, correction in post-processing is possible. Also, the effect can be minimized by equalizing the LFP and the AP corners or by suitable placement of the overlapped region. Limiting the bandwidth to the required signal band reduces in-band noise and is therefore a relevant application specific feature. Additionally, a 4-bit DAC allows to tune the resistance of the pseudo-resistors, thus resulting in an adaptable high-pass corner frequency of the recorder transfer function, which significantly improves the settling speed of the LNA and AAF stages e.g. during startup or after experiencing artifacts. This is especially useful if only APs are recorded, since the elevation of the low-frequency high-pass corner avoids sacrificing settling speed to preserve unused signal bandwidth. The available settings are summarized in Table I.

A comparison of the presented recorder to the state of the art (SotA) is illustrated in Fig. 4. The plot shows the Noise Efficiency Factor (NEF), which is frequently used as

	Block	LFP	AP
Gain	LNA	40dB	40dB
	AAF	0dB/6dB	0dB/6dB
	Biquad	0dB/6dB/12dB	6dB/12dB/18dB/24dB
	Σ	40dB – 58dB	46dB – 70dB
BW	Tune-DAC	HPC: 0.5-1000Hz	HPC: 0.5-1000Hz
	AAF	LPC: 8 kHz	LPC: 8 kHz
	Biquad	LPC: 100/200/400 Hz	HPC: 100/200/400 Hz

TABLE I
AVAILABLE GAIN AND BW SETTINGS OF IMPLEMENTED RECORDER, SORTED BY RESPONSIBLE FUNCTIONAL BLOCK

a figure of merit, as it combines the mutually contradicting design parameters *bandwidth*, *current consumption*, and *input referred noise*. Increasing the transistor area improves low-frequency noise performance. Since the area consumption is not included in the NEF, its influence is covered by plotting the NEF against area. The figure presents the performance of designs published in JSSC and TBioCAS starting from 2010. As NEF is defined for thermal noise, the AP domain NEF is used for all publications which specified it. Besides NEF and area, the absolute noise is included by color-coding, and the marker symbol indicates the usage of HV capable technology nodes. HV CMOS is generally not available in scaled CMOS technologies, and the available technologies are larger than 130 nm.

The plot shows that the herein presented front-end meets state-of-the-art (SotA) performance and is well comparable to prior art implemented in similar technology nodes ($\geq$ 180 nm) [3], [13], [22]–[25]. It is slightly outperformed by designs [26]–[28], which are all implemented in the smaller 130 nm CMOS node but also use very low analog supply voltages of typically 1.2 V. Superior performance both in area and

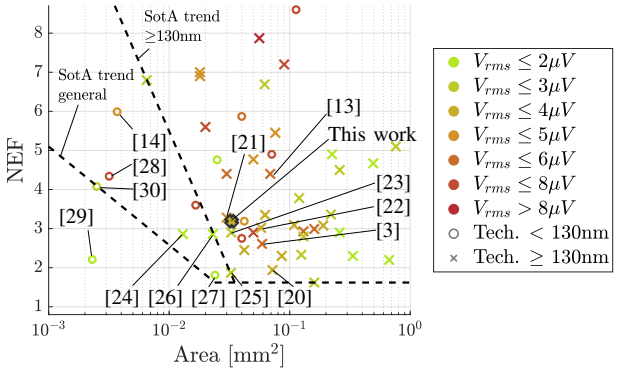

Fig. 4. The performance of the presented neural recorder compared to the state of the art (JSSC and TBioCAS, 2010 to present)

NEF can be achieved by further exploiting the merits of technology scaling like intrinsically lower flicker noise and increased integration density. For instance, several of the SotA designs use fine-line CMOS (65 nm) to improve noise and area e.g. by employing direct conversion front-ends and/or mixed-signal feedback loops [14], [29]–[31]. Furthermore, chopping or similar concepts can be used to mitigate the flicker-noise contribution without significant area increases, but at the cost of additional system level disadvantages like finite electrode DC offset compliance, chopping ripples and reduced input impedance that may require additional circuitry to compensate. These scaled technology nodes however do not offer HV transistors and thus typically prevent the chip-integration of a HV-compliant stimulator, which is a severe system level disadvantage for applications where bidirectional tissue-interfacing is required. This limits these designs to recorder-only implementations, while integrated neuromodulator SoCs require the usage of HV-capable technology nodes at the cost of a performance penalty in the recorder. One possible solution to this issue was published in [32], where a stimulation voltage compliance of ±11 V was achieved by using H-bridge stimulators. The issue of low voltage tolerance of individual devices (1.2 V, 65 nm process) was tackled by stacking LV-devices in the adaptive resonant HV charge pumps. Still, the lack of true HV-transistors results in system level drawbacks: since no HV-switches are available, the stimulator output needs dedicated electrodes that cannot reuse recording sites. Also, HV generation using charge pumps requires large area, thus partially compromising the benefits of using scaled technologies, especially if many stimulation channels are required; also, maximum currents are limited. Furthermore, device stacking generally comes with the risk of reliability e.g. during startup, which is of utmost importance for an implant. Thus, and despite of clear disadvantages in the recorder design, the usage of a natively HV-capable technology node is still beneficial when larger stimulation currents and many combined recording/stimulation channels are desired.

B. CVS and CCS Stimulator

The implemented neurostimulator provides both constant current stimulation (CCS) and constant voltage stimulation (CVS) with high voltage compliance ($\geq \pm 8$ V), which is reconfigurable with very low area overhead [19]. The implemented circuit is schematically illustrated in the red part of Fig. 3. CCS is more commonly used nowadays for stimulation, as it allows to precisely define the amount of charge transfered to the tissue [21]. However, vast clinical experience with CVS exists, and findings in [33] suggest that individual patients respond better to CVS than CCS. Combinations of CVS and CCS on different electrodes during a single stimulation event allow to define an electrode with a programmable preset potential (e.g. reference), which serves as a return path for the charge introduced by a simultaneous CCS executed on surrounding electrodes. Actively driving the electrode potential can also be used to compensate residual charge after CCS, thus active charge balancing is possible. Providing both modes is therefore an advantageous trade-off between significantly improved functionality and only minor additional area consumption, which is achieved due to the reconfiguration of existing blocks.

The stimulator can provide anodic and cathodic stimulation currents with 5-bit resolution and an LSB = 32 µA. The DAC current is generated in the LV domain, and is then mirrored into the HV domain in order to provide the required HV compliance [21]. A gain-boosted cascode and triode-mode mirror devices are used to improve both the HV compliance and the current mirror precision, which is crucial to minimize residual charge remaining on the electrode due to device mismatch even after nominally charge-neutral stimulation. An additional, programmable mirror gain allows to boost the resulting current 1-, 2-, 5- or 10-fold [34], resulting in an absolute maximum nominal stimulation current of $\pm$ 10.2 mA, thereby achieving a dynamic range of approximately 50 dB.

An on-chip state-machine allows almost arbitrary waveform generation with high temporal resolution. The timing for individual segments of the waveform is managed by a counter, which can postpone the execution of the next command by a 7-bit timestep, with an LSB programable between 1 µs to 8 µs. The resulting temporal range for the execution of commands is 0 µs to 1016 µs. The waveform segments are generated using commands like *LSB UP*, *DOUBLE*, *INVERT POLARITY*, etc. [21]. Once the execution of a stimulation command is triggered via the Command SPI in Fig. 1, the previously stored global waveform is executed on all stimulation-enabled channels, each having an individually programmable and locally stored magnitude and polarity. Stimulation waveforms in research often consist of a short-time, large-amplitude cathodic current pulse, which triggers neuron activity. After an optional waiting period an anodic compensation pulse is applied, which can be significantly smaller in amplitude [15]. The stimulation duration of the second pulse is determined such that the integral of the waveform is zero, resulting in nominal charge-neutrality. This principle can also be adapted to exponentially decaying pulses, which closer mimic the biological activation signals [11].

For the current controlled stimulation, the I-DAC is set by the user through a SPI-transmitted 5-bit word, thus the user directly controls the stimulation current. When configured for voltage controlled stimulation (VCS), the I-DAC is set through

an on-chip semidigital feedback loop [19], as is depicted in Fig. 3. The users SPI word is then internally redirected to program a binary-scaled capacitor array which is part of a capacitive voltage divider. The electrode voltage is level-shifted and scaled by a user-defined factor in this voltage divider, and the output is compared against a constant reference voltage $V_{ref} = 0.5\,\mathrm{V}$. The surrounding feedback loop then forces equality between the comparator inputs which is achieved by adjusting the I-DAC and thereby the electrode voltage. Thus, the CCS current sources are reused and internally regulated by the loop to produce a specific electrode voltage. The steady state is achieved once the electrode voltage is such that it scales to V_{ref} at the output of the programmable divider for the given divider setting, which allows to control V_{el} by adjusting the voltage divider ratio. In this way, the control loop operates like a voltage DAC, where a digital input word results in a specific HV output voltage at the electrode. Since a 2-level comparator was used, a toggle is seen at the electrode voltage as the loop continuously alternates between the two best fitting current DAC settings. The CVS system thus behaves like a single-bit delta-sigma DAC [19].

The electrode potential for a given setting of the binary-scaled capacitor array can be determined as follows:

$$\begin{aligned} V_{EL} &= n \cdot 250mV - 8V, n \in [0, 63] \\ &= [-8V, 7.75V] \end{aligned} \tag{1}$$

The asymmetric output range stems from the digital encoding, which is determined by the 5-bit I-DAC, with an additional polarity bit. Thus a total of $2^{5+1} = 64$ voltage levels are available, starting at $-8\,\mathrm{V}$ with a step size of $250\,\mathrm{mV}$. The stimulator circuit design and architecture, as well as a stability analysis of the control loop is found in [35].

C. I-Delta Sigma ADCs

The neuromodulator includes two incremental 16-bit $\Delta\Sigma$-ADCs, which digitize the data of all 32 channels and combine them into a single serial data stream operating on a $30\,\mathrm{MHz}$ clock, Data SPI Out, see Fig. 3. The incremental architecture allows multiplexing 16 channels per ADC, as it provides sample-to-sample conversion. The resulting data rate is $10.24\,\mathrm{Mbit/s}$, which results from a resolution per sample of 16-bit, a sampling rate of $20\,\mathrm{kSamples/s}$ on each channel, a total of 16 channels per ADC and 2 ADCs per ASIC. The implemented ADC is based on [36], but was modified to support a higher data rate at the cost of a slightly reduced ENoB = 14bit. To do so, the OSR was changed from 150 to 90, while keeping the power consumption of $1.65\,\mathrm{mW}$ per ADC unaltered. The full-scale range is $2.25\,\mathrm{V}$ and the (LNA) input-referred noise of the ADC is $\approx 100\,\mathrm{nV}_{rms}$. The quantization noise is negligible due to the sufficiently large ENoB = 12.1 and the large gain ($\geq$40 dB) in prior stages. Therefore, the ADCs total noise contribution is negligible.

D. Digital control and chip clustering by ID

The neuromodulator ASIC features two seperate interfaces which are based on the SPI protocol (Fig. 3). One, the Data SPI Out, manages the ADC data stream. The second, Command SPI In, handles command interactions e.g. during stimulation, see Section II-B, and allows to program the chip, e.g. with setup data like the individual channel recording settings, see Section II-A. In order to increase flexibility on the system level and allow more channels than are provided on a single neuromodulator, each ASIC has a 3-bit input that allows the assignment of a *CHIP ID*. These IDs allow clustering up to 8 ASICs (with a total of 256 recording and stimulation channels) such that they can be controlled from a single command SPI.

The programming interface, Command SPI In, has a sophisticated, package-based protocol, which is illustrated in Fig. 5. There are 5 implemented types of transmissions, which are *GLOBAL REC* (programming global recorder settings), *AMPL* (local gain and stimulation settings), *TIMING* (global stimulation waveform profile), *START STIM* (for the start of a programmed stimulation) and *RST LCU* (reset the channel-specific gain and stimulation registers).

Following the transmission of every 16-bit word, a mandatory waiting period of at least 8 clock cycles is required, which allows the ASICs on the bus to respond to the SPI Master if a protocol error has been detected. The waiting cycles are counted by every ASIC, with the option to seize the transmission channel and respond once the internal counter is equal to the chip's ID; this sequential procedure allows every clustered ASIC to respond while it prevents potential collisions on the SPI. The ASIC response after a transmission error contains a 16-bit error report; a reset is necessary, as the neuromodulator is set into an error mode to prevent unintended, potentially malicious states and harmful stimulation. Full configuration of the ASIC using a $1\,\mathrm{MHz}$ SPI clock is achieved in $\leq 3.5\,\mathrm{ms}$, which corresponds to 140 transmitted packages. Partial reconfiguration can be much faster, e.g. programming a two-pulse biphasic stimulation waveform is possible in $\leq$0.5 ms.

A command (CMD) transmission is always initiated by a 16-bit *HEADER* word, which specifies what type of command the ASIC is about to receive and passes additional arguments for some transmission types. Afterwards, a pre-specified number of CMD words can be transmitted. A programmable 3-bit clock prescaler is used to define the timing LSB for stimulation, which then becomes $1\mu s \cdot (1 + prescaler)$. The transmission always ends with a *FOOTER* package of the respective type.

Each package type then controls a specific functionality and is thus implemented for either a global (all ASICs and channels) or local (one channel on one ASIC) execution. *GLOBAL REC* sets the frequency band selection and bandwidth adaptation of all channels on all connected chips (i.e. global). The package types *START STIM* and *RST LCU* are used to globally trigger stimulation on all enabled channels simultaneously, and to globally reset the local control units to recording-only mode, respectively. Transmissions of type *TIMING* allow to globally set the stimulation waveform by filling an ASIC-internal storage table with delay and command specifiers. The CMD type *AMPL* is designed to individually address and program each channel on each connected ASIC, and defines channel-specific recorder gain, as well as local stimulation parameters (i.e. magnitude, polarity and mode).

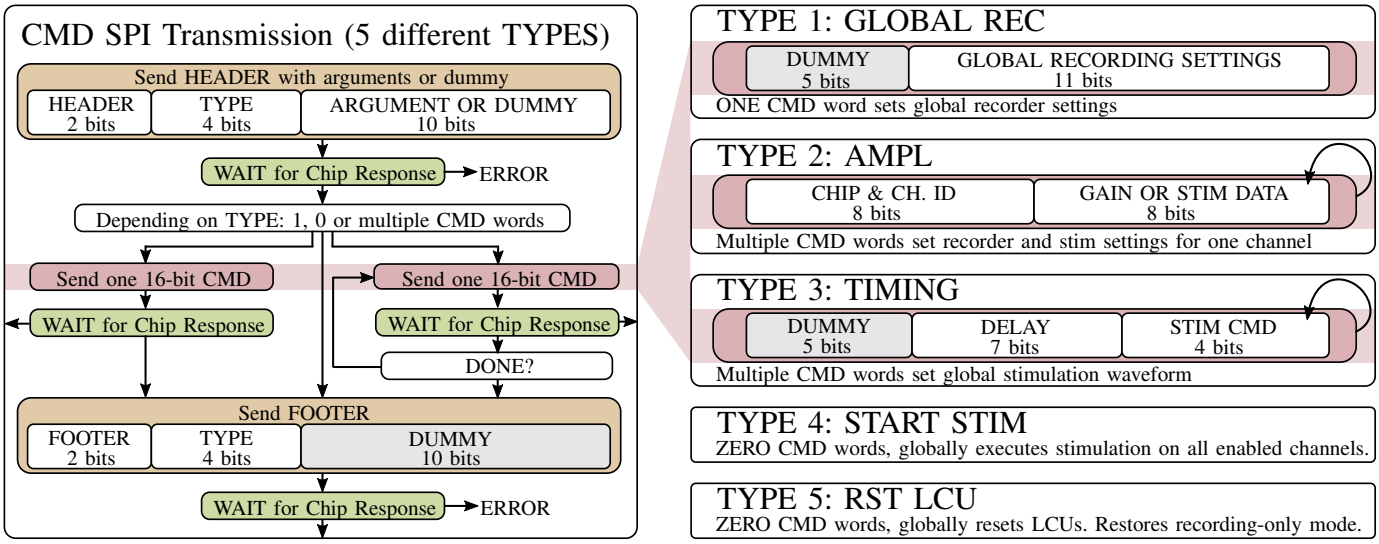

Fig. 5. Illustration of the implemented digital command interface featuring a simplified transmission protocol and command type description.

E. Electrode Impedance Estimation

Monitoring the electrode impedance improves both functionality and safety [20]. Tissue reactions and scaring can significantly alter the electrode-tissue-interface over time, resulting in changes in electrode impedance [37] which can affect the recording quality. Additionally, long-term stimulation can lead to electrode degeneration which also manifests in impedance changes [38]. Therefore, keeping track of the impedance allows to monitor the electrode condition. This information can then be used to adapt the stimulation parameters over time and to warn the controlling entity of looming electrode failures.

In order to estimate the electrode impedance while the system is chronically implanted, a low gain mode is used (see Fig. 3), which sets the gain of the recording front-end to $0\,\mathrm{dB}$, allowing the measurement of a voltage pulse of $V_{pulse} = 300\,\mathrm{mV}$ without saturating the LNA. During this pulse the electrode is disconnected, therefore the resulting response is purely a characterization of the transfer function of the individual recording channel ($H_{REC} = \frac{V_{out}}{V_{in}}$). In the next step the electrode is reconnected and a $100\,\mu\mathrm{s}$ current pulse with $I_{pulse} = 32\,\mu\mathrm{A}$ is applied by the CCS module. The measured response is then:

$$H_{comb} = \frac{V_{out}}{I_{pulse}} = \frac{V_{out}}{V_{in}} \cdot \frac{V_{in}}{I_{pulse}} = H_{REC} \cdot Z_{EL} \qquad (2)$$

After digitization of both responses, the electrode impedance Z_{EL} can be calculated off-chip and be mapped onto a simplified Randle's Cell Electrode model containing only the solution resistance R_S and the double-layer capacitance C_{DL}. Changes of R_S and C_{DL} can be monitored over time and improve patient safety as well as stimulation efficiency. A detailed circuit description can be found in [20].

The range of assessable electrode impedances with this approach is still limited by the current-to-voltage conversion over Z_{EL}. The resulting voltage V_{EL} must be sufficiently larger than the *low-gain*-mode input-referred noise for accuracy; for electrodes with small impedances, this can always be assured by prolonging the current pulse. At the same time, the electrode voltage may not cause the LNA output to approach the analog supply voltage in order to avoid saturation. This is a limitation for very large electrode impedances $|Z_{EL}(f)| \geq 40\,\mathrm{k\Omega}$ with $f \in$ AP domain. The final limitation is the recording bandwidth: An accurate estimation requires the *RC* corner frequency of the Randle's cell model to be within the observable range (AP domain), which is however given for a vast range of different electrodes.

F. Charge Balancing and Blanking

The neuromodulator frontend features a HV-switch capable of passive charge balancing. During the stimulation process, the recorder is disconnected from the electrode by a HV-protection switch. This is necessary, as the HV-compliant stimulator could otherwise damage the LV-recorder. When the recorder is reconnected and residual charge is still stored on the electrode, amplifier saturation can occur, which will blind the recording and persist for several seconds due to the small high-pass corner set by the pseudoresistor. This is avoided by temporarily closing a discharge switch between the affected electrode and the reference electrode right after the stimulation. Once the residual charge is canceled, the recording can commence without saturation (typically within less than $10\,\mathrm{ms}$).

III. Measurement Results

The neuromodulator was designed and fabricated in $180\,\mathrm{nm}$ HV CMOS. A chip photograph and a layout overlay marking the individual circuit components are given in Fig. 6. In the following, measurement results of selected features are shown, which highlight the performance of the presented ASIC.

The area and power breakdown is given in Fig. 7. The area consumption is dominated by the 32 bidirectional channels; as the system power consumption is currently dominated by

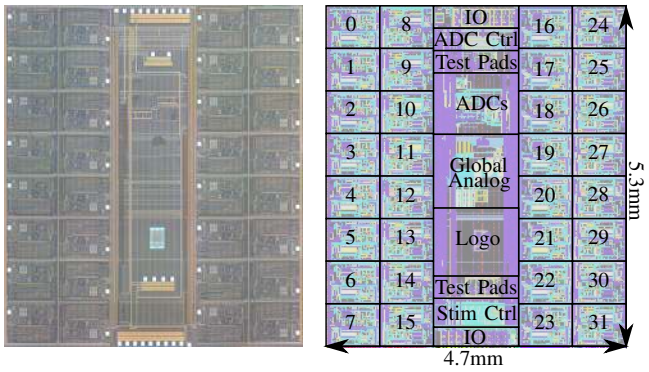

Fig. 6. Chip photograph with highlighted circuit elements

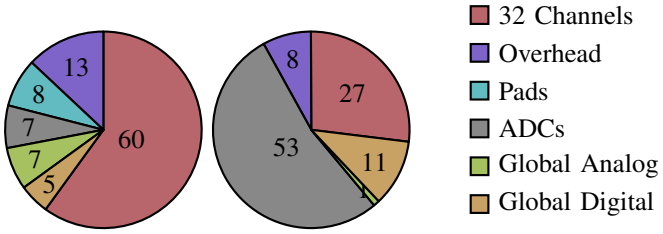

Fig. 7. *On the left:* Area consumption in % of total area $A \approx 25\,\mathrm{mm}^2$ and *on the right:* Simulated power consumption in % of total power $P \approx 6.2\,\mathrm{mW}$

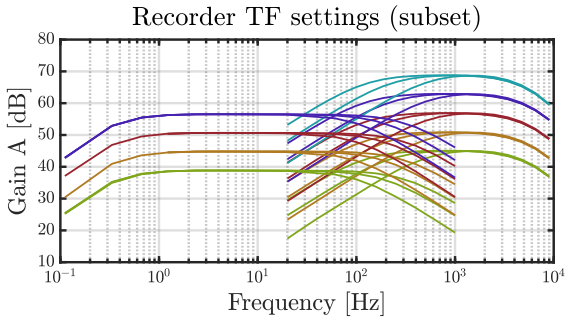

Fig. 8. Subset of available gain and bandwidth settings for AP-only and LFP-only recording modes

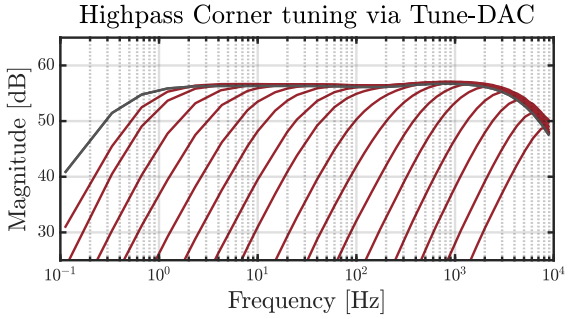

Fig. 9. Effect of the Tune-DAC on the system Transfer Function, exemplary for LFP+AP mode with 58 dB of gain

the uC and bluetooth transceiver, the ADC was reused from earlier work [36] with no optimization and thus most of the neuromodulator power is consumed in the ADCs. Power savings could be achieved by employing the slicing method for incremental $\Delta\Sigma$-ADCs [36], or redesigning the ADCs for a larger noise contribution, as they are currently negligible to the input referred SNR.

A. Electrical verification

Fig. 8 shows a subset of the adjustable transfer functions of the recorder, depicting AP and LFP modes with all achievable gain settings and only the bandwidth settings in the SC-filters. The given LFP and AP transfer functions can be combined to achieve full-band recording at individual gain levels for LFPs and APs. The effect of the tune-DAC is presented in Fig. 9. The recorder was set to LFP+AP recording, with $58\,\mathrm{dB}$ of gain in both bands. Shown are *in red* the 16 different tune-DAC settings (4-bit) as well as *in grey* the untuned (tune-DAC off) transfer function.

Fig. 10 shows the HV compliance of the implemented neurostimulator. As the LV recorder is reconnected following every stimulation event, a measurement of stimulation current over a full (HV) sweep of the electrode voltage was not possible in order to avoid harmful conditions. Instead, an alternating stimulation current was integrated on a $100\,\mathrm{nF}$ load capacitor, and a subsequent passive discharge was used to bring the electrode voltage back to a safe LV range within $0.5\,\mathrm{ms}$. The plotted trace shows that the electrode voltage settles at $\pm 8.9\,\mathrm{V}$. However, the slope of the electrode voltage, and thus the stimulation current according to $I_{stim} = C \cdot \frac{dV_{EL}}{dt}$, starts to saturate at $\pm 8.2\,\mathrm{V}$, which is therefore determined to be the HV compliance limit for the maximum stimulation current of $\pm 10.2\,\mathrm{mA}$. For smaller currents, the compliance range is obviously larger.

The use of pseudoresistors is often associated with poor linearity; still Fig. 11 shows that even for comparably large input-signals of $5\,\mathrm{mV}_{pp}$ a sufficient spurious free dynamic range of $\approx 65\,\mathrm{dB}$ in the AP domain and $\approx 55\,\mathrm{dB}$ in the LFP domain can be achieved. Besides, also power supply noise from the test setup, harmonic distortion as well as inter-modulated tones, which result from the mixing of input signal harmonics and the $50\,\mathrm{Hz}$ supply tone, are clearly visible. The two plotted traces were recorded in LFP-only and AP-only recording modes, with the minimum available gain, i.e. $40\,\mathrm{dB}$ (LFPs) and $46\,\mathrm{dB}$ (APs). Spectra from 10 measurements each were averaged to flatten the noise floor. The input-referred signal was calculated by dividing the recorded data by the measured midband gain for each range prior to DFT. A normalized first-order Hanning window was used to suppress spectral leakage. The larger AP gain results in better noise floor suppression in the respective signal domain.

The measured noise floors in the LFP and the AP band are depicted in Fig. 12. The measurement for LFP noise was conducted in LFP-only recording mode with maximum available gain, i.e. $58\,\mathrm{dB}$. The limiting influence of 1/f noise is evident. For the AP noise floor, the transfer function is noticeable, indicating that the in-band noise is white and thus of thermal origin. The total integrated input-referred noise is $3.8\,\mu\mathrm{V}_{\mathrm{rms}}$ in the LFP band ($1\,\mathrm{Hz}$ to $200\,\mathrm{Hz}$) and $3.3\,\mu\mathrm{V}_{\mathrm{rms}}$ in the AP band ($200\,\mathrm{Hz}$ to $7500\,\mathrm{Hz}$), which are the median values of 96 channel measurements on 3 individual samples. The total

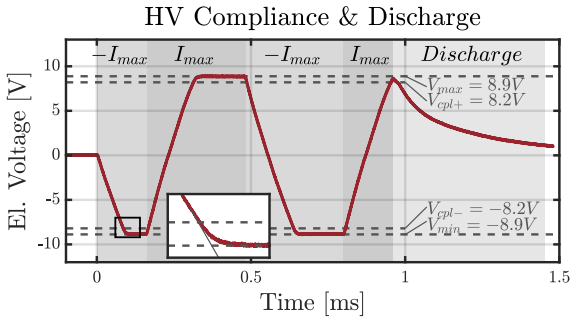

Fig. 10. HV Compliance Measurement. CCS into purely capacitive load ($C_{meas} = 100\,\mathrm{nF}$) with subsequent passive discharging

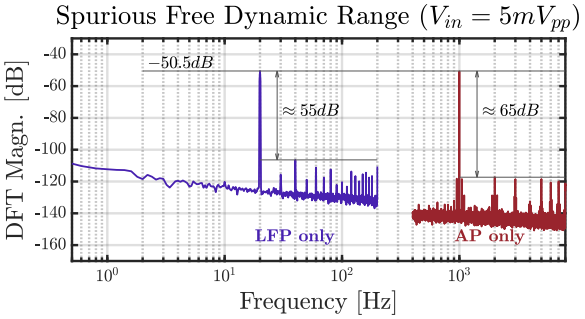

Fig. 11. Input-referred spurious free dynamic range for a $5\,\mathrm{mV_{pp}}$ input signal in LFP-only ($f_{in} = 20\,\mathrm{Hz}$, 40 dB gain) and AP-only ($f_{in} = 1\,\mathrm{kHz}$, 46 dB gain) recording mode (separate one-tone measurements). Each plotted trace is averaged from 10 individual spectra with normalized Hanning-window)

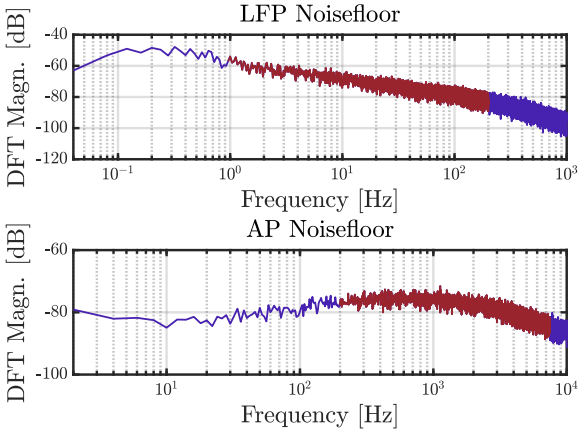

Fig. 12. LFP (1 Hz to 200 Hz) and AP (200 Hz to 7500 Hz) noise floors

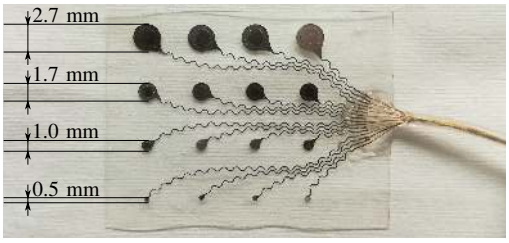

Fig. 13. PtIr-electrode array used for the in-vitro verification. Courtesy CorTec GmbH.

integrated noise is slightly higher as in the prototyped case, where 2.9 µV (LFP) and 3.2 µV (AP) were measured [20]. As the additional input referred noise from the ADC is negligible, this increase is attributed to the digital noise on the overall SoC, compared to the original all-analog prototypes.

B. In-vitro verification

In-vitro verification was done using a standard PtIr-electrode testing array with differently sized electrodes, which is depicted in Fig. 13. The diameters range from $0.5\,\mathrm{mm}$ to $2.7\,\mathrm{mm}$. For the test-setup these electrodes were placed in phosphate buffered saline (PBS) solution. To ensure a negligibly small counter electrode impedance, a much larger Pt electrode was used.

Fig. 14 shows the result of the in-vitro stimulation verification. Tests include both CCS and CVS on the largest ($2.7\,\mathrm{mm}$) and the smallest ($0.5\,\mathrm{mm}$) electrodes of the array. As a larger diameter translates into a smaller electrode impedance, a larger stimulation current mirror setting (5x) was used for the $2.7\,\mathrm{mm}$ electrode to ensure fast settling. For the smaller electrode, a mirror gain of 2x was used to minimize stimulation current saturation due to HV-compliance limits.

The plots in Fig. 14 show the electrode voltage (blue trace) and the stimulation current (red trace) over time for an exemplarily varying stimulation waveform. For CCS on the smaller electrode, voltage compliance is reached due to the relatively large current and the larger electrode impedance. This corresponds to the decline in the nominally constant stimulation current as soon as the electrode voltage approaches $>8\,\mathrm{V}$.

In the CVS case, the current mirror gain settings correspond to a trade-off between settling time and magnitude of the toggle which occurs due to the ongoing switching between the two best-fitting states of the current DAC (comparator in feedback loop). Here, smaller target voltages were used on the large electrode due to the fact that its impedance was so small not allowing more than $\pm 4\,\mathrm{V}$ for the used stimulation current of $\pm 5.1\,\mathrm{mA}$ (see also CCS for larger electrode). Additionally, settling limitations are visible. Both of these limitations can be addressed by increasing the current mirror gain, however at the cost of reduced current LSB (CCS) and larger toggle (CVS). For the smaller electrode the full $\pm 8\,\mathrm{V}$ range for CVS can be used. Even though the larger electrode is tested with larger current mirror gain, the toggling is suppressed by its large C_{DL}. The toggling around the two best fitting DAC values is though visible for the smaller electrode.

Fig. 15 presents the in-vitro electrode impedance estimation for the $2.7\,\mathrm{mm}$ and the $0.5\,\mathrm{mm}$ electrode from Fig. 13. The plot shows two traces for each electrode type: The blue curve shows the estimated electrode impedance that results from averaging 25 individual estimates. The red line corresponds to a reference measurement conducted with a commercial, desktop size VersaStat4 potentiostat. The accuracy of the individual measurements was $\leq 2\,\mathrm{dB}$ within the recording bandwidth (AP domain).

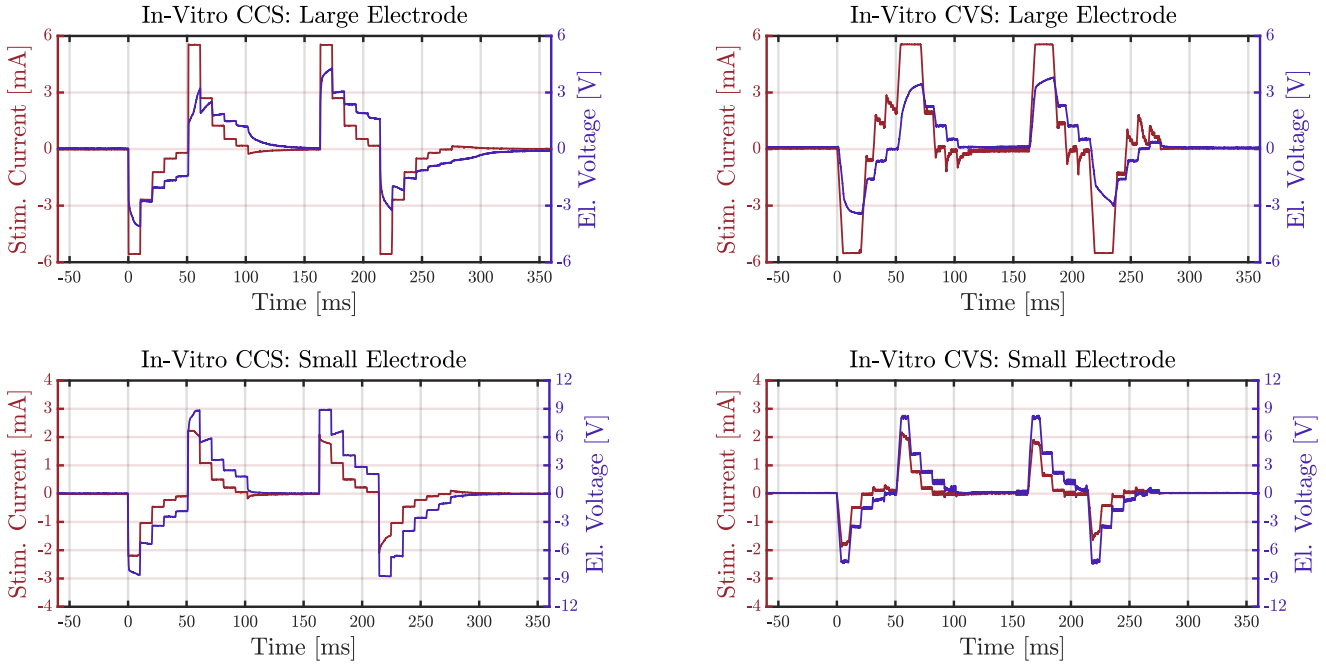

Fig. 14. In-vitro stimulation; shown are waveforms for CCS and CVS on different PtIr-electrodes (diameters: 2.7 mm and 0.5 mm, Fig. 13) in PBS

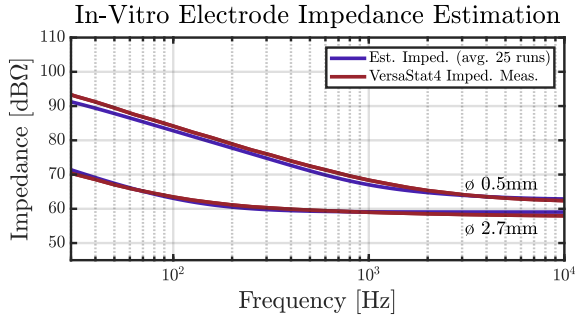

Fig. 15. In-vitro electrode impedance estimation alongside reference measurement, PtIr-electrodes (Fig. 13) in PBS

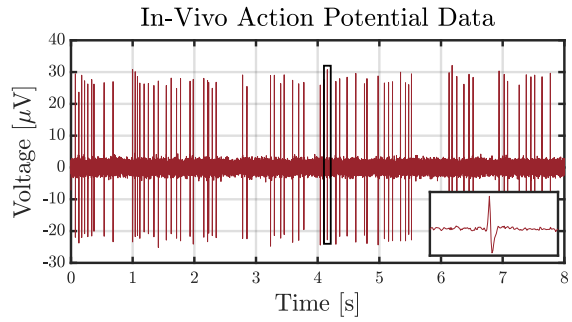

Fig. 16. Input-referred in-vivo spike data measured from the brain of an anesthetized laboratory mouse. Recorder was set to AP-only recording with 70 dB gain.

C. In-vivo verification

In order to verify the functionality of our neuromodulator in-vivo, a 4-shaft 32-channel silicon probe with 25 µm diameter iridium oxide electrodes (E32+R-50-S4-L6-200 NT, ATLAS Neuroengineering, Belgium) was inserted above the midbrain

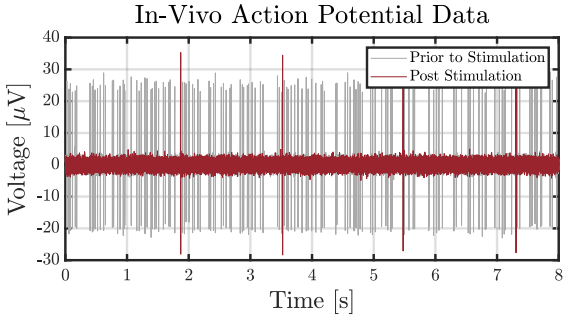

Fig. 17. Input-referred in-vivo spike data showing the effect of an applied stimulation of ±32 µA, for 2 µs pulse width each at 5 Hz. Recorder was set to AP-only recording with 70 dB gain. Reduced spike-rate was measured 10 s after the end of the stimulation.

region into a terminally anesthetized mouse, maintained under 0.8 % to 1.2 % isoflurane and stabilized within a motorized stereotaxic frame (Neurostar, Germany). Experiments conformed to the German Animal Rights Law 2013 and the European Union regulations for the use of laboratory animals (EU Directive 2010/63), and were approved by the Federal Ethical Review Committee. The recording was grounded and referenced through a scull screw above the contral-lateral cerebellum. Trains of spontaneous action potentials could be reproducibly recorded at multiple sites along the trajectory, including from the substantia nigra and the dorsal subiculum region above. Measurement results from substantia nigra are shown in Fig. 16 and reveal an input-referred magnitude of the neural spikes of ≈ 30 µV. The zoomed-in part of the figure reveals the expected spike pattern. The system was setup for AP-only recording with the maximum available gain of 70 dB, resulting in decent input-referred suppression of DC offsets, low-frequency potentials and out-of-band (e.g. 1/f) noise.

Figure 17 shows the result of a $2\,\mathrm{min}$ CCS with $5\,\mathrm{Hz}$ which was conducted using a biphasic waveform consisting of two current pulses with $2\,\mu\mathrm{s}$ each and with an amplitude of $\pm 32\,\mu\mathrm{A}$; for the shaft electrodes, this minimum stimulation charge was used. The effect of the stimulation is clearly visible, as the spike rate is significantly reduced post stimulation compared to the a priori reference measurement. The post-stimulation measurement was started $10\,\mathrm{s}$ after the end of the stimulation.

IV. State of the Art comparison

Table II shows a comparison of the presented neuromodulator ASIC to state-of-the-art designs. The listed designs are predominantly in $180\,\mathrm{nm}$ CMOS nodes, as the available HV transistors in these technologies are beneficial for efficient on-chip integration of the HV stimulator. The listed recorders differ vastly since different frequency ranges are covered. The NEF is typically worse for LFP-only recorders (and obviously NEF is in some cases even irrelevant then, as it concerns thermal noise only), due to the additional 1/f noise contribution in the low-frequency range. The table compares only HV-capable designs, thus most of the technology-scaled LV-implementations that outperform the $180\,\mathrm{nm}$-designs in Fig. 4 are not included. This more balanced comparison reveals that the herein presented recorder front-end matches state of the art performance. The comparably large area per channel stems from the very flexible implementation which provides an independent stimulator unit in every channel without multiplexing components. Uniquely, the proposed design allows CVS and CCS from the same stimulator. Each CCS/CVS stimulator is capable of providing a large maximum stimulation current with high voltage compliance. Shared electrodes for recording and stimulation can be arbitrarily selected. Chip-clustering allows systems with up to 256 recording and stimulation channels that can be controlled from a single command bus.

V. Conclusion

This article presents the system integration of a 32-channel neuromodulation ASIC forming a fully-digital, bidirectional interface to the brain. Priorly published circuit parts from low-channel-count prototypes were combined with a digital control mechanism and on-chip ADCs to form an easy-to-use bidirectional digital interface into the brain for any controlling hardware capable of handling the SPI data and command transfers. This ASIC can be employed in many application scenarios due to the systems versatility: The individual chip ID allows clustering up to 8 ASICs such that a total of 256 electrodes can be controlled from a single SPI-based command bus. The ASIC offers CCS and CVS with high voltage compliance, a large dynamic range for the stimulation currents, almost arbitrary stimulation patterns, as well as a high level of flexibility in the recording (e.g. individual gain settings for each channel). The included electrode impedance estimation and charge balancing features are relevant for clinical applications and enhances patient safety in chronic implantation. Results from in-vitro and in-vivo measurements are included to prove the functionality and the system's feasibility.

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	ISSCC'16 [39]	**VLSI'17** [40]	**TBioCAS'16** [41]	**JSSC'20** [32]	**TBioCAS'18** [42]	**This work**
No. Ch. (Rec/Stim)	16/160	64/4	4/4	64/4 †	16/16	32/32
Area/Ch. [mm^2]	—	—	0.18 ‡	—	0.6 *	0.46
Tech. [nm]	180	180	180	65	180	180
Stimulator						
Supply [V]	±6...12	12	5	±11	5	±9
Stim mode	CCS	CCS	CCS	CCS	CCS	CCS/CVS
$I_{Stim,max}$	0.5 mA	5.04 mA	0.25 mA	2 mA	4 mA	10.2 mA
Stim waveform	Square	Arbitrary	Arbitrary	Arbitrary	Square	Arbitrary
Recorder						
Power [µW/Ch.]	5.4 (LNA+LP)	8 (LNA+ADC)	5.5 (bioADC)	3.21 (mux'd Rec.)	9 (LNA)	11.8 (LNA)
Input noise [μV_{rms}]	7.68	1.6	1.0	2.9 (1 Hz-1 kHz)	4.57	3.8/3.3 (LFP/AP)
BW	5 Hz - 7 kHz	≤1 Hz - 500 Hz	0.25 Hz - 0.25 kHz	tunable (<32 kHz)	0.3 Hz - 7 kHz	0.2 Hz - 7.5 kHz
NEF	6.2 (LFP+AP)	7.8 (LFP)	4.67 (LFP)	4.08 (1 Hz-1 kHz)	4.77 (LFP+AP)	3.1 (AP) / 4.5 (LFP+AP)
f_S/Ch.	—	1 kS/s	0.5kS/s	≤16kS/s	—	20kS/s
ADC	10-b pipeline	15-b SAR	10-b ΔΣ	Nyquist Δ-Encode	10-b V-ADC	16-b I-ΔΣ
ENoB	8.5	10.2	9.4	14	9.1	12.1

‡ *estimated (Rec. + DSL + Stim.)* † *stacking of LV devices to achieve HV compliance. No shared electrodes possible* * *estimated*

TABLE II
COMPARISON TO STATE-OF-THE-ART NEUROMODULATOR DESIGNS

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