CERN/ECP 91–27
13 December 1991

A HIGHLY INTEGRATED TRIGGER AND READOUT SYSTEM FOR A SILICON MICRO-STRIP DETECTOR INSTALLED AT THE CERN OMEGA SPECTROMETER

A. Beer, A. Corre, Ph. Farthouat, B. French, L. Malferrari, V. Ryzhov, G. Schuler and M. Weymann

CERN, Geneva , Switzerland

G. Darbo, P. Martinengo, L. Rossi and C. Salvo

INFN and Dipartimento di Fisica, Genoa, Italy

C. Enz and F. Krummenacher

Smart Silicon System, Lausanne, Switzerland

ABSTRACT

This paper describes the readout electronics of a silicon micro-strip (μ-strip) vertex detector aimed at finding secondary vertices for beauty identification. High density and high speed have been achieved allowing the detector to take part in the trigger.

Presented at the 1991 IEEE Nuclear Science Symposium and Medical Imaging Conference, 5–9 November 1991, Santa Fe, USA

MacWord/9010F/PF/mnb

1. INTRODUCTION

The WA92 experiment installed at the Omega spectrometer at CERN, aims to study beauty physics. Although hadronic interactions are a strong source of beauty particles, the signal over noise ratio is small (10^{-6}) at fixed target energies. As a consequence the success of such an experiment depends on the strategy adopted for the triggering and the identification of beauty events. The WA92 experiment decided to use a trigger which selects events with evidence of high P_t tracks *coming from* secondary vertices, and to identify B decays, thanks to a high precision "decay detector". To fulfil these two functions, a new silicon μ-strip detector has been built.

2. THE SILICON MICROSTRIP DETECTOR

The silicon μ-strip detector consists of twelve 25 μm pitch planes (6 for the Z coordinate, 6 for the Y coordinate) of 5×5 cm^2 sensitive area. This gives a total number of 2048 channels per plane.The arrangement along the beam axis is shown in fig. 1.

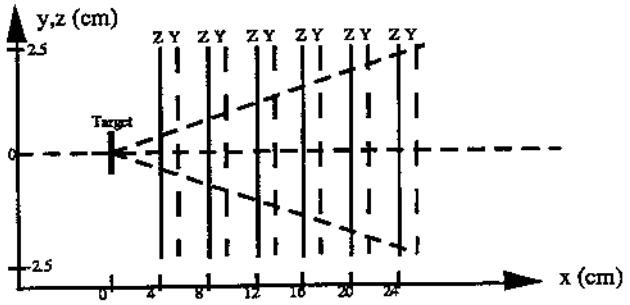

Fig. 1 View of the detector

This detector is used for tracking only, and the energy deposition is not measured. It will contribute to the trigger in two ways:

- by calculating the multiplicity within a preset window for each plane, and
- by using the Z coordinates.

A fast trigger processor will find the tracks that have an impact parameter [1, 2] (i.e. the distance between the primary vertex and the intersection of the extrapolation of the track into the target plane) higher than a preset value. Events with more than two tracks missing the primary vertex by more than 100 μm will be selected.

3. THE READOUT ARCHITECTURE

3.1 The constraints

The constraints come from the high number of channels (> 24 000) and the time available to evaluate the multiplicity in each plane, and to feed the trigger processor. To reduce efficiently the input rate, it is necessary to have the multiplicity count ~ 2 μs after the interaction has taken place, and the output of the trigger processor < 20 μs later. As the algorithm of the trigger processor needs ~ 10 μs to execute, the time available to process the analogue data and to give hit coordinates is < 10 μs, which excludes extensive multiplexing. To avoid huge amounts of cables from the experimental area to the counting room, it was decided to process the data as much as possible on the detector itself, and to transmit only the coordinates of the hit strips to both the trigger processor and the data acquisition system.

The mechanics of the detector demands that groups of 128 μ-strips are processed independently. This resulted in the placement of 16 printed boards, of 5 mm maximum thickness, around each detector plane. The limited available space strongly influenced the choice of the technology.

3.2 Overview of the system

An overview of the implementation is given in fig. 2. One detector plane is equipped with 16 front end (FE) boards, each of them processing the signals coming from 128 strips. Two kapton buses connect these boards, on one side to a POWER board which distributes the power supplies and on the other side to an INTERFACE board which distributes the timing signals and makes the interface to the FASTBUS readout board.

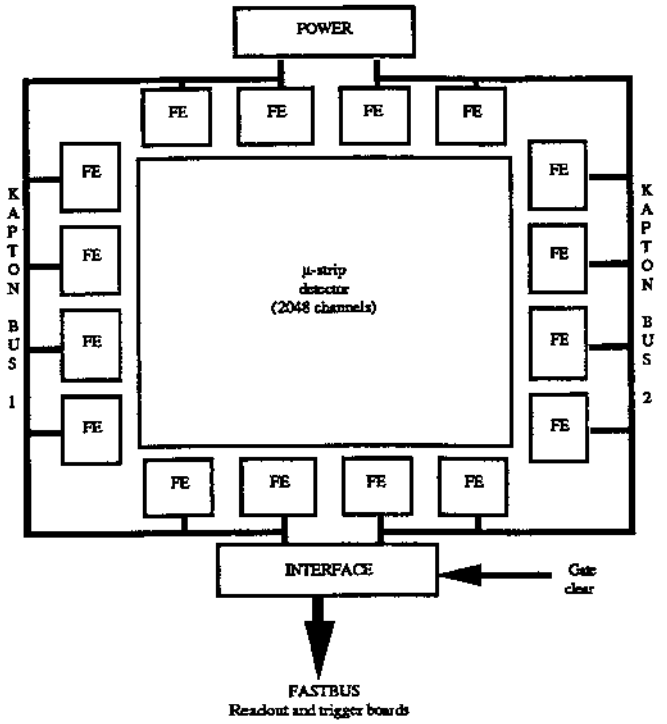

Fig. 2 Overview of the system

4. THE ELECTRONICS

4.1 The front-end board

Two CMOS chips were designed to process the data, one for the analogue part (ICAR) and one for the digital part (FEROS).

4.1.1 The front end chip: ICAR

A 16-channel CMOS monolithic chip has been designed by the firm Smart Silicon System(*) to process the strip signals. This chip is named ICAR and is a modified version of the AMPLEX chip [3]. The block diagram is shown in fig. 3, and its main characteristics are listed in table 1.

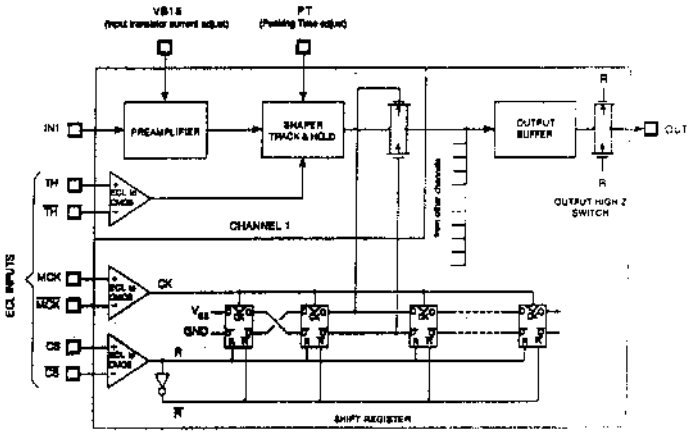

Fig. 3 The ICAR block diagram

Table 1 The ICAR characteristics

Parameters	
Number of inputs	16
Power consumption	67 mW
Gain	40 mV/fC
Peaking time	200 ns
Eq. input noise (C_{det} = 5 pF)	1000 e^-
Reset time	500 ns
Readout frequency	6 MHz min

The ICAR ship has, on each input, a low-noise preamplifier followed by a shaper. The peaking time of the shaper can be adjusted (between 150 and 300 ns) and we use it as a delay. When the signal track and hold (TH) occurs, the analogue value of each input is latched. A 16:1 multiplexer and an output buffer are used to read out the 16 analogue values. The chip select (CS) allows, if required, another level of multiplexing.

On each FE board, 8 of these chips are mounted; the output of each ICAR feeds an external comparator with a programmable threshold, as shown in fig. 4.

(*) Smart-Silicon System, 23 Av. de Chailly, CH–1012 Lausanne, Switzerland.

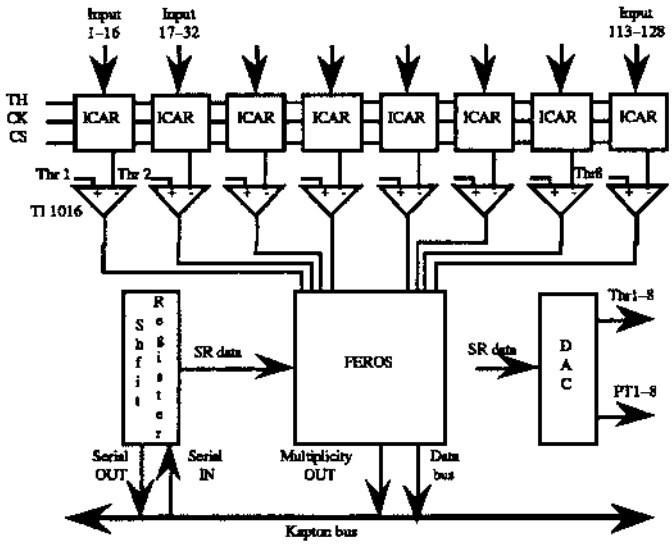

Fig. 4 board block diagram

Both thresholds (Thr 1–8) and peaking time adjustment (PT 1–8) are programmable through a serial shift register and DACs.

The outputs of these comparators feed another chip: the FEROS.

4.1.2 The read out chip: FEROS

This chip encodes in 10 bits the coordinates of the hit strips. It calculates the multiplicity within the group of 128 strips and sends it to the kapton bus. A distributed adder tree is used to calculate the overall multiplicity; each FEROS contains one adder. The total multiplicity is made available to the INTERFACE via the kapton bus.

The coordinates of the hit strips are stored for future readout, controlled by the INTERFACE board. For test purposes, the input of the FEROS chip can be driven through the shift register.

FEROS is implemented in a 1.2 µ, double-level metal HCMOS gate array from SGS Thomson Microelectronics (ref. ISB12011) and uses 4500 equivalent gates. The design has been done at CERN on a DAZIX(*) CAE workstation using the component library from SGS Thomson. Pre-layout and post-layout simulations were performed, first with the default parameters given by the library, and then with the actual parameters of the routed chip. The measurements made on the real chip completely agreed with the simulation results and no iteration was needed.

The main characteristics of FEROS are listed in table 2.

Table 2 The FEROS characteristics

Parameters	
Number of input strips	128
Encoding time	25 ns
Multiplicity calculation	25 ns

(*) DAISY Cadnetix Inc.

A photography of the FE board is given in fig. 5, and a view of the overall system is given in fig 6. One can see the 16 FE boards connected through the kapton bus to the POWER (on the left) and INTERFACE boards (on the right).

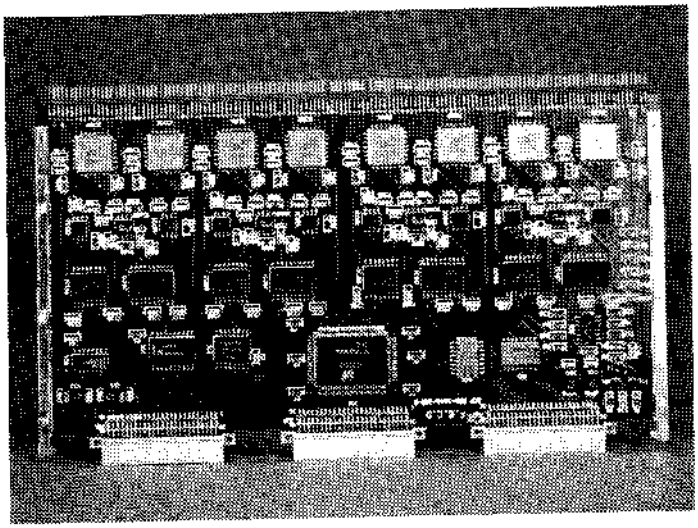

Fig. 5 View of the FE board. From top to bottom, one can see the connection to the detector, the 8 ICAR chips, the FEROS chip and the three connectors to the kapton bus.

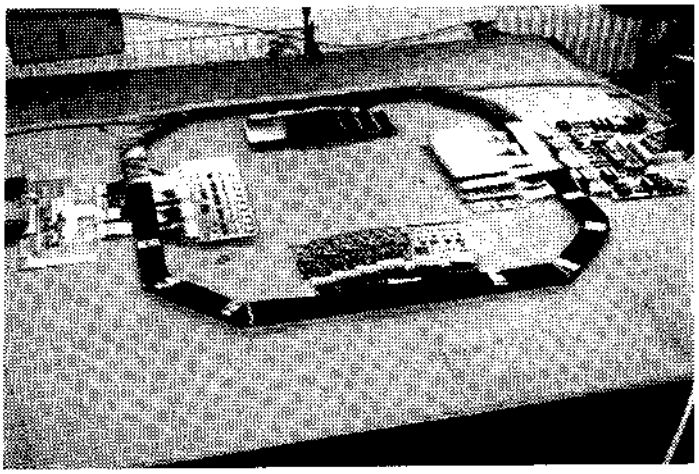

Fig. 6 View of the front-end system

4.2 The interface to the readout system

Two modules are used for this purpose: one board on the detector (INTERFACE) and one FASTBUS board (COROM) (fig. 7).

The INTERFACE is connected to the FE boards through the kapton bus and to the COROM module through a 30 m, 20 pairs differential bus (READOUT BUS). Both of them receive the GATE signal from the first-level trigger and the CLEAR from the second-level trigger. One COROM board is able to handle two detector planes so that only six FASTBUS modules are used for the full readout of the detector.

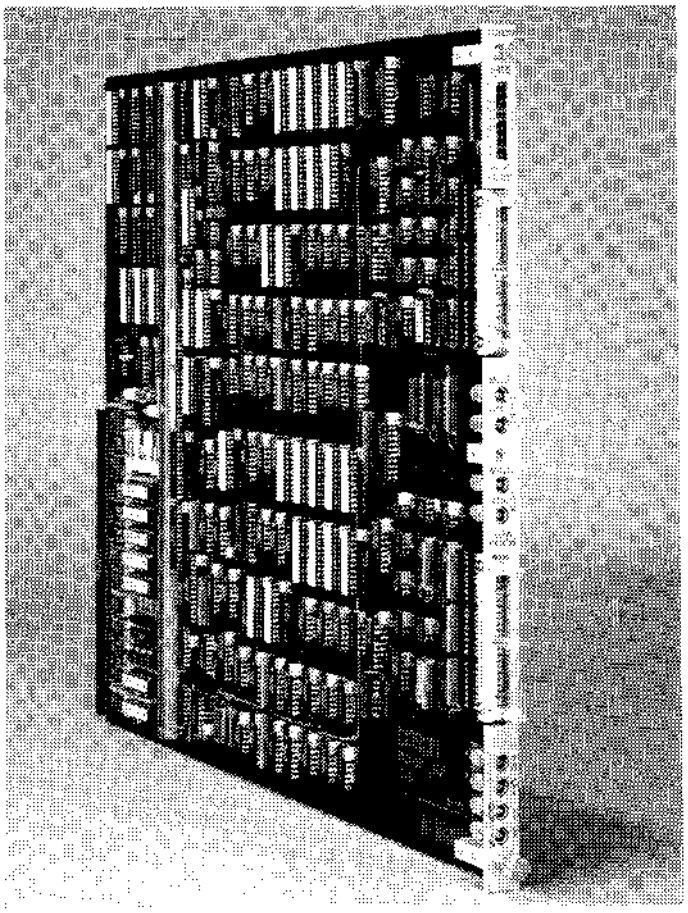

Fig. 7 Side view of COROM

The READOUT bus uses a simple protocol: first an instruction cycle defines the type of transaction which will be done, and then the data transactions take place, until the INTERFACE sends an end of transaction.

The INTERFACE/COROM has to manage four main tasks:

(a) Distribution of the timing signals. As soon as a GATE occurs, the INTERFACE proceeds with the analogue readout sequence allowing FEROS to start working. When a CLEAR occurs, the system is reset and able to accept a new event (after the 500 ns reset time of ICAR).

Special instruction cycles allow the simulation of GATE and CLEAR for test and calibration purposes.

(b) Readout of multiplicity and of the coordinates of hit strips is done in two steps: first a slave handshake phase which allows fast readout of the multiplicity (used by COROM to give a signal to the trigger logic if the multiplicity is inside a preset window) and of the coordinates to feed the track-trigger processor at high rate (programmable from 2.5 MHz to 10 MHz); next a full handshake phase is used by COROM to build the data buffer, including programmable clustering. Both phases can be interrupted by the CLEAR signal without introduction of dead time.

(c) Programming and control of the thresholds, peaking time values and test data.

(d) Monitoring of the power supplies.

The performance of the overall system in terms of speed is as follows:
- multiplicity is available in COROM 2.5 μs after the interaction;
- first coordinate is available to the track trigger 2.6 μs after the interaction and then is followed by one coordinate each 100 ns.

For an average event size of 10 tracks, the full event will have been transferred to the track trigger 3.6 μs after the interaction.

The readout of COROM is done by a VSB to FASTBUS interface (FVSBI(*)) in block transfer mode. To avoid software overheads, the FASTBUS slave port implements a daisy chain capability so that all the COROMS in the crate are seen as a single module. The FASTBUS readout speed is 10 MB/s (400 ns per word).

The design of these boards has been done at CERN, using a DAZIX CAE workstation. The first description and simulation of COROM has been made using a hardware description language (DABL from DAZIX). Then, it has been implemented in finite states machines in PLD and fully simulated again. No iteration was needed between the prototype phase and the production.

5. THE TRACK TRIGGER

5.1 Principle

An appropriate transformation of the Z coordinates of the tracks, has the feature of changing primary tracks into horizontal straight lines and secondary tracks into hyperbolas with characteristics depending on the impact parameter.

As a detector plane is made of 2048 strips, everything looks like a mesh array of 6×2048 pixels as shown in fig. 8.

A special Contiguity Trigger Processor based on the same principle as the one used in DELPHI [4] will process the data in the following way:
- suppression of primary tracks;
- for a given impact parameter (IP), an hyperbola is transformed into an horizontal track by adding to the Z coordinates of inner planes a value which is a function of the IP.

As we have a quantified measure of the Z coordinates (2048 pixels per plane), this corresponds in fact to a certain number of shifts along the Z axis. Using this algorithm, one can find and count the tracks which have a given IP.

(*) FVSBI, Creative Electronics System, 70, rte du Pont Butin, CH–1213 Petit Lancy 1, Geneva, Switzerland.

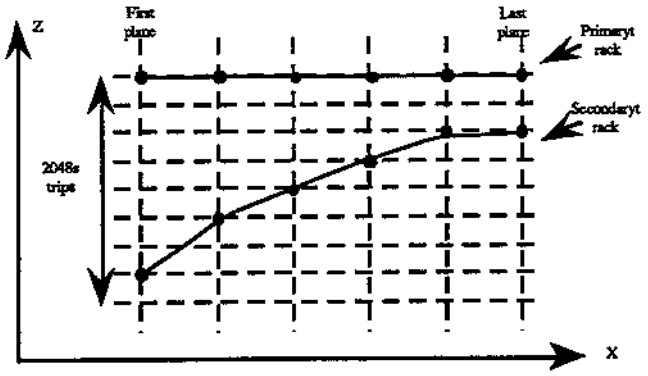

Fig. 8 Example of an event with one primary track and one secondary vertex track

5.2 Realization

The contiguity trigger is a single instruction multiple data (SIMD) machine. One simple processor element (PE) handles each pixel and can communicate with its four neighbours. All the PEs will execute the same instruction at the same time on different data. A so-called contiguity processors (CP) including 64 PEs, has been designed.

The CP has been implemented in a 1.2 μ, double-level metal HCMOS SGS Thomson Microelectronics gate array, using 15000 equivalent gates. The design has been done in Genoa using a DAZIX CAE workstation.

Six FASTBUS boards house the required 192 CPs. Two extra boards connected to the detector planes READOUT BUSEs, read the coordinates, transform them and send the result to the CPs through the auxiliary backplane.

5.3 Performances

After an interaction, the readout phase, as mentioned above, is < 5 μs for an average event size of 10 to 15 hits per plane. The time needed to erase the primary tracks is ~ 1 μs. Searching for impact parameters between 100 μm and 1 mm requires ~ 10 μs. Thus the overall time necessary for this system to take a decision is of the order of 16 μs.

6. FIRST RESULTS

6.1 Set-up

For the 1991 test, eight μ-strips planes were installed after the target and two before to monitor the beam. At that time the track trigger was not available, and a single muon trigger was used to start the readout. A view of the installation at the Omega experimental area is given on fig. 9.

The trigger rate was 1500 triggers/s. It is expected to reduce this rate to 500 Hz when the track trigger is installed for the next run (during the spring of 1992).

6.2 Results

The behaviour of the system has been excellent in both stability and data quality. In particular, the calculation of the multiplicity by the front-end electronics was always correct.

The spatial resolution of the detector has been found to be 8 μm, which was the expected value.

For the next run, it is planned to install these readout electronics on other parts of the decay detector.

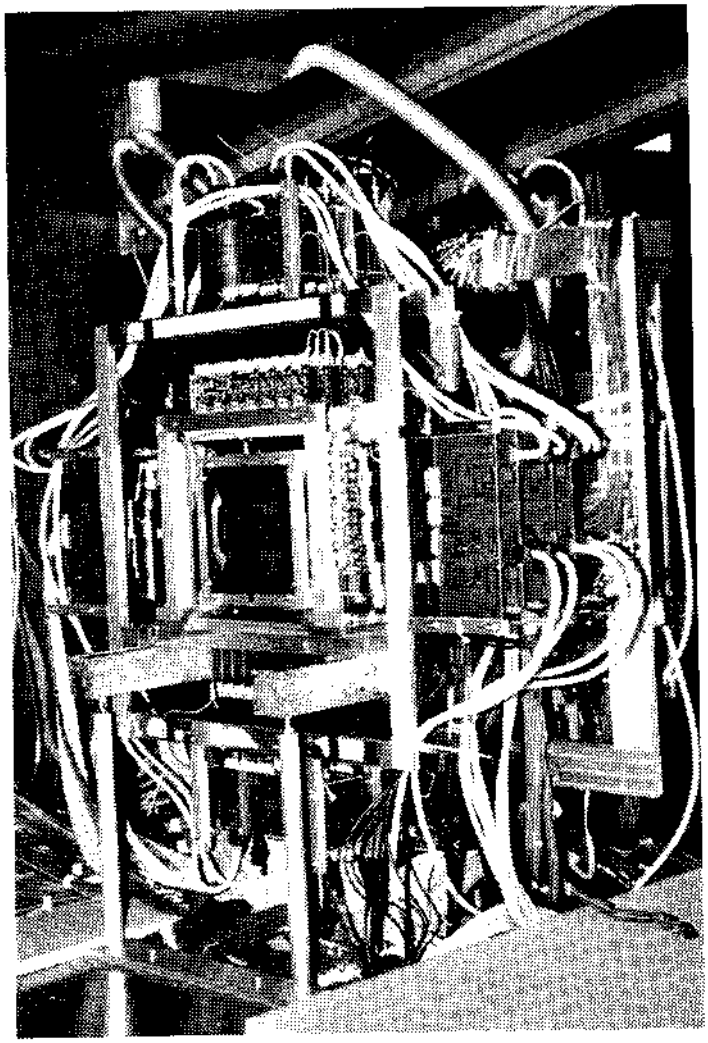

Fig. 9 View of the detector in the experimental area

7. CONCLUSIONS

A complete readout system has been designed, using high-level technologies to fulfil the requirements of a powerful silicon μ-strip detector. Despite the large number of channels and thanks to the use of ASICs, the amount of electronics needed for the readout is rather small, which increases the level of confidence and simplifies the maintenance and the cabling of the system.

The use of CAE tools allowed a very fast design (1.5 year), which was reliable and well documented.

REFERENCES

[1] J.F. Baland et al, Nucl. Phys. B (proc. suppl.) 1B (1988) 303.

[2] J.P. Dufey et al., Results on heavy quark selection through an impact parameter trigger, IEEE Trans. on Nucl. Sci., vol. 37 (1990).

[3] P. Jarron et. al., AMPLEX a low-noise, low-power analogue CMOS signal processor for multi-element silicon particle detectors, proc. of the 5th Europ. Symp. on Semiconductor Detectors, Munich, Germany (1989).

[4] G. Darbo et. al., The contiguity trigger processor, a SIMD architecture for a second-level track trigger, proc. of the Intern. Conf. on the Impact of Digital Microelectronics on Particle Physics, Trieste, Italy (1988).