A Highly Linear Low-Noise Amplifier

Sivakumar Ganesan, Edgar Sánchez-Sinencio, and Jose Silva-Martinez

***Abstract*—A low-noise amplifier (LNA) that achieves high third-order input intercept point (IIP3) at RF frequencies using a nonlinearity cancellation technique is proposed. The circuit tackles the problem of the effect of the second-order nonlinearity on IIP3 at RF frequencies. The circuit functionality is analyzed using Volterra series. The linear LNA was designed and fabricated in a TSMC 0.35-μm CMOS process. An IIP3 of $+21$ dBm was achieved with a gain of 11.5 dB, noise figure of 2.95 dB, and a power consumption of 9 mA at 2.5 V.**

***Index Terms*—Low-noise amplifier (LNA), nonlinearity, third-order input intercept point (IIP3), third-order intermodulation (IM3), Volterra series.**

I. Introduction

THE communication technology in the 21st Century has been predominantly wireless in nature and has resulted in numerous standards spanned over closely spaced frequencies governing different applications. Due to the possible large interference signals at the input of the low-noise amplifier (LNA), it has to provide high linearity, thus preventing the intermodulation tones created by the interference signal from corrupting the carrier signal. This linearity improvement should not be at the expense of gain or noise figure (NF). This demands the use of linearization techniques implemented with minimal current overhead.

Negative feedback techniques to obtain linearity cannot be easily used at RF frequencies due to stability reasons and, hence, demanding different linearization techniques. The LNA in [1] and [2] is linearized using the fact that the third-order derivative of dc transfer characteristics of a field-effect transistor (FET), which is responsible for third-order nonlinearity, changes from positive to negative in the moderate inversion region. Thus, a FET biased at the zero crossing point will be highly linear, but the region over which this linearity boost can be obtained is very narrow and the bias point is bound to change due to process variations leading to a very sensitive and limited improvement. The major drawback of this technique is that the transistor has to be biased at the "sweet spot," hence, limiting the transconductance of the input stage leading to reduced gain and increased NF.

The feed-forward technique has been used in different forms to achieve linearity in an LNA. In [3], the output is taken as the difference of outputs of two amplifiers whose inputs are scaled accordingly to obtain zero third-order distortion and, thus, high linearity is achieved, but this results in reduced gain, which further deteriorates the NF. The derivative superposition (DS) method [4]–[9], which falls under the category of feed forward, uses two transistors connected in parallel and biased in weak and strong inversions, respectively. The transistor widths and bias voltages are chosen such that the positive peak of third-order derivative of dc transfer characteristics of the weak inversion transistor is aligned with the negative peak of that of the strong inversion transistor. This results in extended linear range over which the third-order derivative is close to zero, but the improvement obtained at RF frequencies is not significant due to the effect of frequency-dependent second-order nonlinearity, which is explained in more detail in Section II. In [10]–[13], these second harmonic frequencies are trapped by terminating the input and output impedances accordingly, but this would require large values of inductance, thus forcing the use of off-chip inductors. In [14], a modified DS method is proposed, which takes into consideration the second-order nonlinearity effects. This method uses two inductors to tune the magnitude and phase of the second- and third-order nonlinearity contribution to intermodulation components [third-order intermodulation (IM3)] such that they are equal in magnitude and opposite in phase, resulting in zero IM3 components at the output, but all the feed-forward methods described above use additional components, which load the input, thus affecting the frequency of operation, as well as input match, which is not desired. Further, the weak inversion transistor connected to the input degrades the NF of the LNA [14].

This paper briefly explains the theory behind the DS method and modified DS method and their drawbacks. A novel circuit to achieve high third-order input intercept point (IIP3) in a regular cascode LNA at RF frequencies with a minimal effect on gain and NF and at the expense of minimal power is proposed. Theoretical analysis is done using Volterra series, and MATLAB plots are provided to prove the circuit functionality. The LNA has been designed and fabricated in TSMC 0.35-μm CMOS technology and the experimental results achieve $+21$ dBm of IIP3, thus corroborating the proposed concepts.

II. DS Linearization Method

The nonlinearity of a MOS transistor arises from its voltage-to-current (*V–I*) conversion. The drain current in a MOSFET can be modeled in terms of its gate–source voltage as follows:

$$i_d = g_{m1}v_{\rm gs} + g_{m2}v_{\rm gs}^2 + g_{m3}v_{\rm gs}^3 + \dots \quad (1)$$

where g_{m1} is the main transconductance, g_{m2} represents its second-order nonlinearity obtained by the second-order deriva-

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S. Ganesan is with Pulsewave RF Inc., Austin, TX 78746 USA (e-mail: sganesan@pulsewaverf.com).

E. Sánchez-Sinencio and J. Silva-Martinez are with the Analog and Mixed-Signal Center, Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843 USA (e-mail: sanchez@ece.tamu.edu; jsilva@ece.tamu.edu).

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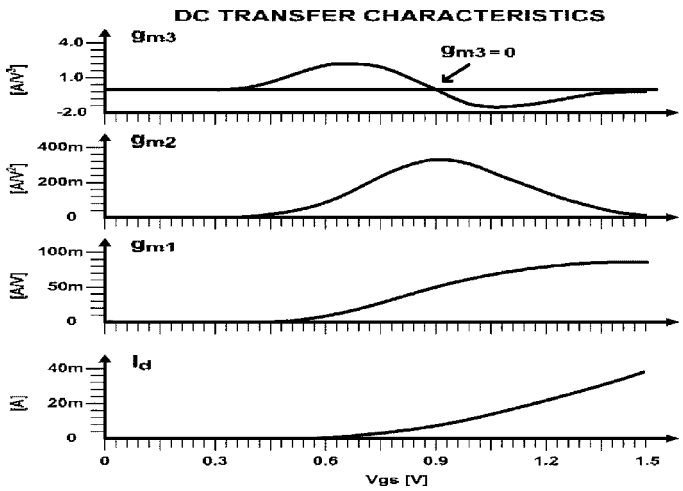

Fig. 1. MOSFET transfer characteristics.

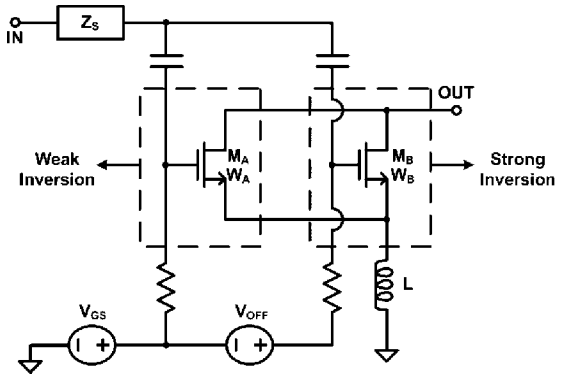

Fig. 2. DS method.

tive of MOSFET dc transfer characteristics (Fig. 1) (I_d–$V_{\rm gs}$) and g_{m3} is the third-order nonlinearity obtained by the third-order derivative of MOSFET dc transfer characteristics. The IIP3 in the above-mentioned terms is given as follows:

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{2}$$

The MOSFET dc transfer characteristics in Fig. 1 show that g_{m3} changes from positive to negative as the FET moves from weak inversion to strong inversion. In the DS method, g_{m3} is minimized by connecting two transistors in parallel, as shown in Fig. 2, with M_A biased in weak inversion and M_B biased in strong inversion. The bias voltages and the transistor widths are chosen such that the positive peak of g_{m3a} (M_A) and the negative peak of g_{m3b} (M_B) are aligned, resulting in composite transfer characteristics with minimum g_{m3} and, hence, high IIP3.

The drawback with the DS method is that it is valid only at low frequencies at which the effect of circuit reactance is negligible. At RF frequencies, the source degeneration inductance (L) creates a feedback path for the drain current i_d to the gate–source voltage $V_{\rm gs}$ of M_B through the gate–source capacitance $(C_{\rm gs})$. In a two-tone test, the second harmonics $(2\omega_1, 2\omega_2, \pm\omega_1 \pm \omega_2)$ generated due to second-order nonlinearity are fed back across the gate and source and get mixed with

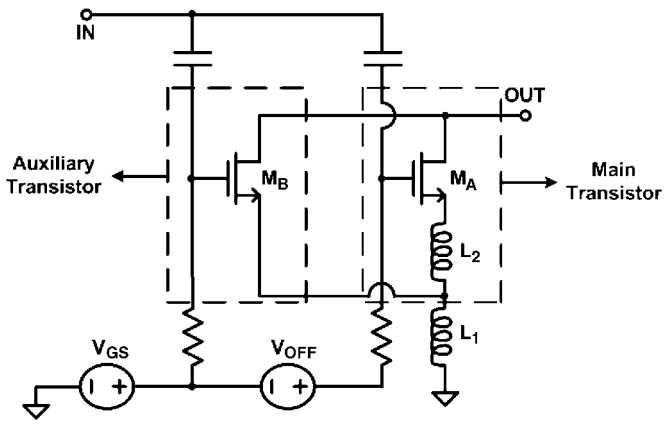

Fig. 3. Modified DS method.

the fundamental components. These spectral components are further subjected to second-order nonlinearity resulting in IM3 components at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. Thus, the second-order nonlinearity also contributes to IM3. An expression derived in [12] for the circuit shown in Fig. 2 with a source impedance of Z_s shows the effect of g_{m2} on IIP3 as follows:

$$\text{IIP3} = \frac{4g_{m1}^2\omega^2 LC_{\rm gs}}{3|\varepsilon|}$$

$$\varepsilon = g_{m3} - \frac{2g_{m2}^2/3}{g_{m1} + \dfrac{1}{2j\omega L} + 2j\omega C_{\rm gs} + Z_s(2\omega)\dfrac{C_{\rm gs}}{L}}. \tag{3}$$

As seen from (3), achieving zero g_{m3} as in the DS method does not necessarily result in high IIP3 at RF frequencies due to the nonzero g_{m2} term present.

III. Modified DS Linearization Method

The "modified DS method" proposed in [14] addresses the issue of feedback of second-order frequency components described in Section II. In this method, the magnitude and phase of second-order nonlinearity contribution to IM3 components is tuned to cancel the third-order nonlinearity contribution to IM3 components, thus resulting in an output current with a minimum IM3 component. As shown in Fig. 3, the transistor M_A is biased in the strong inversion region, while M_B is biased in weak inversion. The two source degeneration inductors L_1 and L_2 connected to the sources of the two transistors are used to tune the magnitude and phase of the IM3 components. The expression for IIP3 is given by (4). In the expression C_A and C_B are the gate–source capacitances of transistors M_A and M_B, respectively,

$$\text{IIP}_3 = \frac{4g_{1B}^2\omega^2\left[L_1(C_A + C_B) + L_2C_B\right]}{3|\varepsilon|};$$

$$\varepsilon = g_{3A}n(s)\,|n(s)|^2\left[1 + \frac{L_2C_B}{L_1(C_A + C_B) + L_2C_B}\right] + g_{3B} - \frac{2g_{2B}^2}{3g_{1B}}\frac{1}{1 + \dfrac{1}{j2\omega(L_1 + L_2)g_{1B}}}$$

$$n(s) = 1 + j\omega L_2 g_{1B}. \tag{4}$$

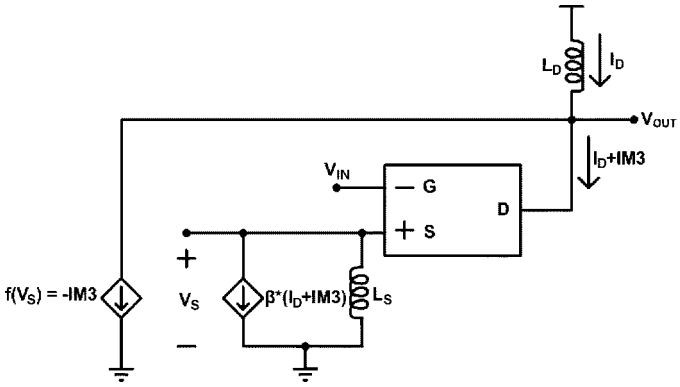

Fig. 4. Conceptual view of the proposed solution.

There are primarily two drawbacks involved in any of these methods using the feed-forward techniques. The first and the most important drawback is that the additional weak inversion transistor added to achieve linearity degrades the noise performance of an LNA due to its high gate induced current noise getting added to the input [14].

The other drawback with this technique is that the weak inversion transistor connected to the input loads the input node adding extra capacitance and, hence, changes the input impedance matching and reduces the frequency of operation. The increased capacitance would demand a larger source inductor to achieve 50-Ω input matching. Further, the number of iterations required for optimization (achieving good linearity and input match) would be large, as any changes to the weak inversion transistor to tune for linearity would result in the input match being affected and vice versa.

IV. Proposed Linear LNA

As described above, high linearity can be achieved at RF frequencies only if the contribution of second-order nonlinearity to IM3 components is taken into account. The proposed solution uses a nonlinearity cancellation technique in which the magnitude and phase of IM3 component currents in the main and auxiliary branch are tuned to be equal in magnitude and opposite in phase, thus resulting in very small IM3 current component at the output. The conceptual idea is illustrated in Fig. 4.

The first major step is to remove the auxiliary transistor connected to the gate of the main transistor (see Figs. 2 and 3). However, an auxiliary branch is unavoidable because of the need for additional processing to cancel the IM3 components. Hence, an alternate way of processing the currents using an auxiliary circuit to cancel the IM3 components is required.

The drain current of an LNA contains information about the IM3 components generated due to third order and feedback of second-order nonlinearity components. If an additional auxiliary branch were added to this LNA, which can process this information present in the drain current of the main branch to generate an output current with its IM3 components equal in magnitude and opposite in phase with that in the main branch, then the sum of these currents would result in a smaller IM3 component at the output of the LNA, as shown in Fig. 4. This is the main idea behind the proposed solution.

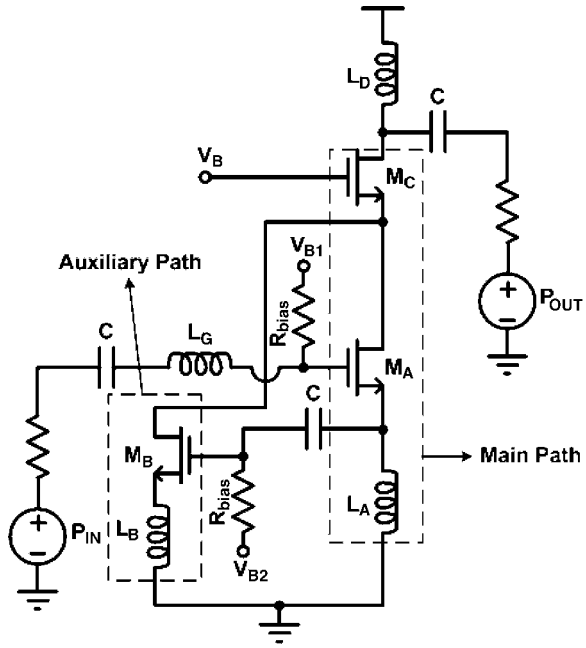

Fig. 5. Proposed solution.

The schematic of the realized circuit for the proposed idea is shown in Fig. 5. The transistors M_A and M_C form the basic cascode LNA with the inductors L_G and L_A for obtaining input impedance matching and the inductor L_D for resonating with the output capacitance to provide gain at the desired frequency. The transistor M_B is source degenerated with the inductor L_B and is used to tune the magnitude and phase of the IM3 components along with its bias voltage V_{B2}. The nonlinearity information present in the drain current of the main transistor is tapped as voltage at the source of the main transistor and forms the input to the auxiliary transistor. The transistor M_A is biased in strong inversion and the transistor M_B is biased in weak inversion. The aspect ratio, bias voltage, and the inductor value associated with the auxiliary transistor are varied to tune the magnitude and phase of its IM3 components to cancel the IM3 components generated by the main transistor.

To theoretically verify the functionality of the circuit, the equivalent small-signal model of the proposed solution shown in Fig. 6 is analyzed using Volterra series. The effect of all parasitic capacitances other than the gate–source capacitance is neglected. The capacitances C_A and C_B shown are the gate–source capacitances of main and auxiliary transistors, respectively. The impedance Z_s is the input source impedance. The currents i_a and i_b are the currents through main and auxiliary transistors, respectively. The expressions used for the above-mentioned currents are given below where v_a and v_b are the gate–source voltages of the main and auxiliary transistors, respectively,

$$\begin{aligned} i_a &= g_{1a}v_a + g_{2a}v_a^2 + g_{3a}v_a^3 \\ i_b &\cong g_{3b}v_b^3 \end{aligned} \tag{5}$$

g_{1b} and g_{2b}, which are the first- and second-order transconductance of the auxiliary transistor, are neglected in the analysis, as they have a very weak effect on the IM3 components since

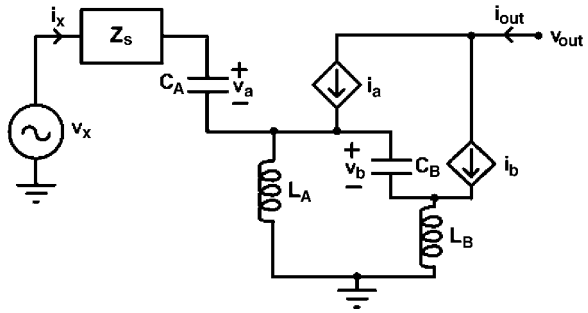

Fig. 6. Small-signal model of proposed solution.

the auxiliary transistor is operating in weak inversion. The harmonic input method in the Volterra series analysis is used to analyze the various coefficients of nonlinearity associated with the output current for an input signal of amplitude A and two tones of frequency ω_a and ω_b. The two tones are assumed to be closely spaced ($\omega_a \cong \omega_b$). The analysis results in the following expression for IIP3:

$$\begin{aligned} \mathrm{IIP}_3 &= \frac{1}{6\mathrm{Re}\left(Z_s(s)\right)\left|A_1(s)\right|^2}\left\{\frac{g_{1a}}{\varepsilon}\right\} \\ \varepsilon &= g_{3a} - \frac{g_{2a}^2}{3g_{1a}} + g_{3b}n(s)\left|n(s)\right|^2\frac{2+s^2L_BC_B}{2(1+s^2L_BC_B)} \\ n(s) &= \frac{sL_A(g_{1a}+sC_A)}{1+sC_B(sL_A+sL_B)} \\ A_1(s) &= \frac{1+s^2C_B(L_A+L_B)}{2s^2L_AC_A(1+s^2L_BC_B)}. \end{aligned} \tag{6}$$

It can be seen from (6) that the second-order nonlinearity coefficient (g_{2a}) appears in the expression due to the feedback effect discussed earlier. The effect of g_{2a} on IIP3 has become independent of any circuit components, thus resulting in a constant value. The value of g_{3b} can be tuned to obtain high IIP3 by choosing appropriate values for the inductors L_A and L_B. Fig. 7 shows the theoretical values of IIP3 obtained from a MATLAB simulation for given values of g_{1a}, g_{2a}, g_{3a}, g_{3b}, C_A, and C_B tabulated in Table I and different values of L_A and L_B.

As shown in Fig. 7, IIP3 peaks for certain values of inductors L_A and L_B at which the IM3 components in the main and auxiliary branches cancel each other, thus proving the theory of phase cancellation. It can be seen that large values of IIP3 can be obtained when the circuit is designed to be at the "sweet spot" at which the IM3 components in the main and auxiliary branches cancel each other. Biasing the LNA at this particular point is very difficult, as it is bound to change due to process variations, but as shown in Fig. 7, reasonable values of IIP3 in the order of 20–25 dBm can be obtained even with 10%–15% variation in the value of inductors, thus making the design reliable.

V. Effect of Auxiliary Circuit on Other Parameters

One of the major disadvantages in all of the feed-forward techniques is the inability to tune the circuit for good input match and good linearity independently due to the tuning element affecting the input match. The input impedance of the proposed linear LNA is calculated to find the effect of the additional

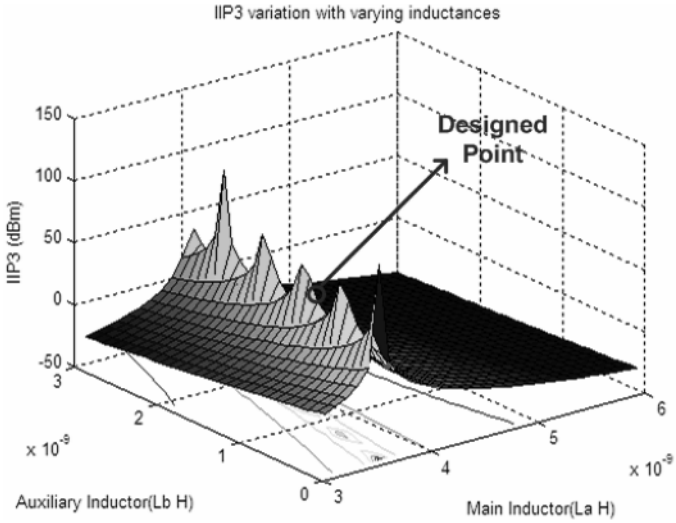

Fig. 7. Variation in IIP3 with source degeneration inductors at 950 MHz.

TABLE I
VALUES USED FOR MATLAB SIMULATION

Component	Value	Component	Value
g_{1a} (A/V)	34.95e-3	g_{2a} (A/V^2)	35.94e-3
g_{3a} (A/V^3)	-202.02e-3	g_{3b} (A/V^3)	1.41
C_A (fF)	476.8	C_B (fF)	786.7

circuitry on the input match. In the small-signal model shown in Fig. 6, the outputs are grounded and the input impedance given by $Z_{\mathrm{in}} = V_x/I_x$ is calculated with $Zs = sL_G$. The calculated value for input impedance is

$$\begin{aligned} Z_{\mathrm{in}} = sL_G + \frac{1}{sC_A} + (sL_B(sC_B + g_{1b}) + 1) \\ \cdot\frac{\left(sL_A + \dfrac{g_{1a}L_A}{C_A}\right)}{(s^2L_AC_B + sL_B(sC_B + g_{1b}) + 1)}. \end{aligned} \tag{7}$$

If $|s^2L_AC_B| \ll 1$ in (7), Z_{in} can be simplified as

$$Z_{\mathrm{in}} \cong sL_G + \frac{1}{sC_A} + sL_A + \frac{g_{1a}L_A}{C_A}. \tag{8}$$

It can be seen that the input impedance calculated in (8) is basically the same as the input impedance of a regular cascode LNA [15]. Thus, if the condition mentioned above is met (which, in our case, is $1.5e-3$), which is almost always the case at RF frequencies, the additional auxiliary circuit will not affect the input impedance, thus allowing independent tuning for input match and high linearity.

The effect on NF due to the additional auxiliary transistor is explained below. The drain current noise in a weak inversion transistor is negligible, as the drain current is small, while the gate noise of a weak inversion transistor is significant, as it is inversely proportional to the drain current [14]. In the case of the DS method, the weak inversion transistor degrades the noise performance, as the gate noise current directly gets added to the total noise at the input. In the proposed solution, as shown in Fig. 8, the gate noise of the auxiliary transistor gets added to the drain noise of the main transistor, which, when referred to the

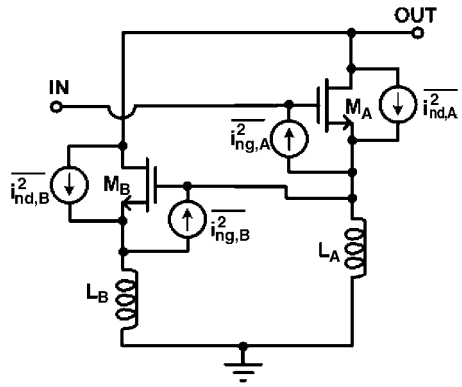

Fig. 8. Noise sources.

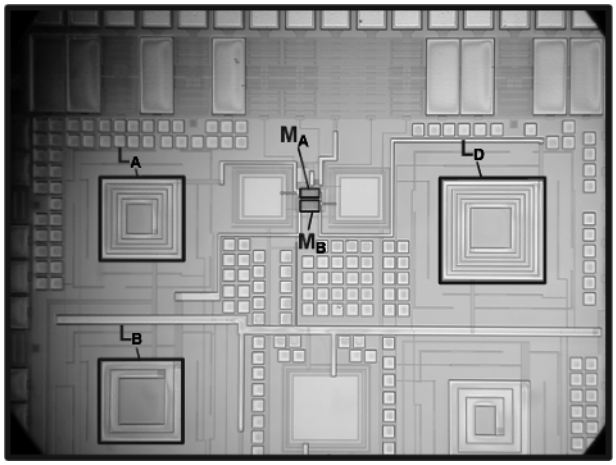

Fig. 9. Linear LNA chip microphotograph.

input, gets divided by the gain of the LNA, resulting in a small effect on the overall NF. The gain of the LNA is unaffected too as the transconductance of the weak inversion transistor is very less. Thus, the proposed solution achieves high linearity without seriously degrading any of the specifications of gain, NF, and at the expense of minimal additional power.

VI. LNA Design and Experimental Results

The LNA shown in Fig. 5 was fabricated in TSMC 0.35-μm CMOS technology through the MOSIS educational program. The die microphotograph is shown in Fig. 9. The layout of the inductors were drawn using ASITIC and were shielded with broken P- and N-well contacts. The transistors were drawn multifingered and inter-digitized for good matching. The initial values of the inductors were chosen from the MATLAB plot shown in Fig. 7 and later tuned for IM3 cancellation. The aspect ratios of different transistors and values of inductors of the designed LNA are listed in Table II.

The LNA was simulated and fabricated as a standalone device without a cascaded internal mixer or buffer or any external matching network at the output and, hence, it sees the 50-Ω impedance of the output port leading to limited gain. An external capacitor C_m was used to tune out the effect of bond-wire inductance on the frequency of operation. To measure the actual gain of the LNA, a resistance (R) is placed in series with the decoupling capacitor C_b and then connected to the output port, as

TABLE II
Component Design Values of LNA

Component	Value
M_A	24 μm/0.4 μm, m=16
M_C	24 μm/0.4 μm, m=16
M_B	24 μm/0.4 μm, m=36
L_G	30 nH
L_A	5 nH
L_B	1.05 nH
L_D	10 nH
V_B, V_{B1}, V_{B2}	840mV,610mV,2V
I_{DA}	4.68mA
I_{DB}	0.84mA

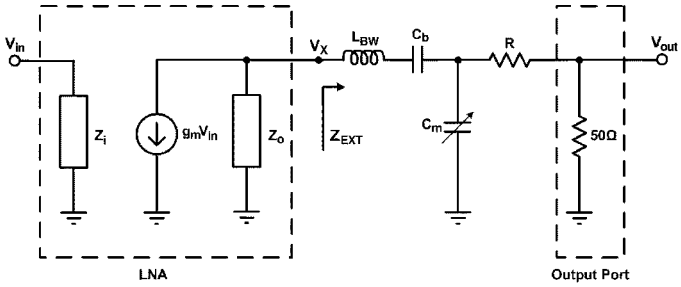

Fig. 10. LNA testing strategy.

shown in Fig. 10. Here, the LNA sees a total output impedance Z_{ext} of $(sL_{\text{BW}}+R+50)\,\Omega$, where sL_{BW} is the impedance due to the bond wire. By choosing a sufficiently high value of R, provided the S_{22} is good, the real case in which the LNA sees the high impedance of a mixer can be emulated, but the signal at the output port (V_{out}) would be attenuated by $50/|sL_{\text{BW}}+R+50|$ times the original signal at the output of LNA (Vx). Hence, the gain at the output of LNA can be calculated by adding the attenuation factor to the measured gain. The resistive divider stage being a linear element should not affect the measured linearity. Since the internal nodes of the LNA would see a large-signal swing, this would also prove to be a realistic test for linearity. The NF of the LNA can also be calculated from the measured results by deembedding the noise contribution of the resistors R and 50 Ω.

The test setup shown in Fig. 10 with $R = 100\ \Omega$ was used to measure the LNA performance at the node V_{out}. The corresponding gain measured at the output of LNA was found to be 11 dB for a power consumption of 9 mA at 2.5 V. The LNA was tested for linearity by the two-tone test for this case. The LNA had maximum gain at a frequency of 950 MHz. Hence, the two tones were chosen as 940 and 945 MHz so that one of the IM3 tones fall at 950 MHz. The input power was swept over a range of values such that the 1-dB compression point of LNA falls within this range. The input power was swept from -15 to $+5$ dBm and Fig. 11 shows the variation of power of the signal and IM3 components at the output. It can be seen that the linearity obtained is $+21$ dBm.

Different values of resistance R of 0, 75, 100, and 150 Ω were employed to see their effect on linearity, and the results are summarized in Table III.

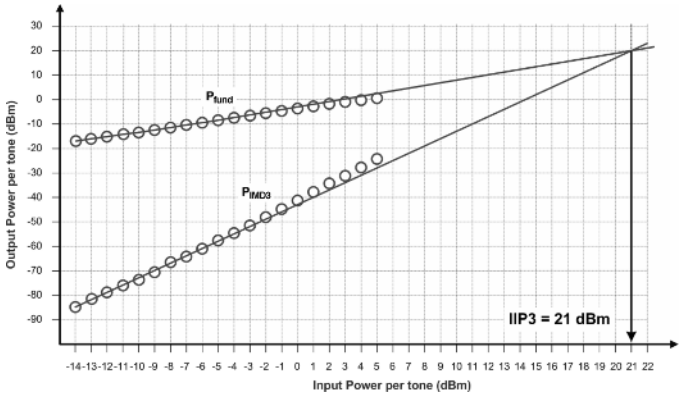

Fig. 11. IIP3 measurement.

TABLE III
EXPERIMENTAL RESULTS FOR DIFFERENT VALUES OF R

R(Ω)	S11 (dB)	Gain (dB)*	IIP3 (dBm)
0	-16	5	20
75	-10.5	10.5	20.9
100	-11.5	11	21
150	-9.5	11.5	20.5

* Gain measured (indirectly) at node V_x in Figure 10.

As shown in Table III, the IIP3 in all cases was measured to be in the range of 20–21 dBm, hence proving, as expected, that the loading does not have much effect on the linearity of the circuit. Further higher values of R have not been tried since the value of S_{22} degrades for further increase in the value of R resulting in reflection at the output. The NF is quite similar for all values of R, as well as there is no improvement in the NF despite increased gain because the series resistor at the output itself adds more noise to the output of LNA, which nullifies the improvement obtained due to increased gain.

The actual gain and NF of this LNA if cascaded with an internal high input impedance block (mixer or buffer) can be predicted from the results in Table III. It can be seen that the incremental gain obtained is small for further increase in the value of R beyond 75 Ω. This is because the resistance $R + 50\ \Omega$ is comparable to the resistance offered by the on-chip output *LC* resonator at this frequency. It can be seen that there is a 6-dB increment in gain when R is changed from 0 to 100 Ω from which the resistance offered by the on-chip *LC* resonator can be computed to be 150 Ω. Gain of the LNA $(V_x/V_{\rm in})$ with $Z_{\rm ext}$ acting as a load in parallel with Z_o yields 11 dB for $R = 100\ \Omega$ (from Table III), but the effective load impedance of the LNA at V_x for this measurement is 75 Ω, as both Z_o and $Z_{\rm ext}$ are 150 Ω. Therefore, if the LNA is loaded by a high input impedance stage, the effective load impedance at V_x will be Z_o (150 Ω) and, hence, the voltage gain will be 6 dB higher. On top of this, there is also some signal attenuation due to the bond-wire inductance $(L_{\rm BW})$. Taking all these effects into account, the actual gain of the LNA if cascaded with an internal mixer/buffer can be predicted to be $(11 + 6 + 1.5)$ dB or 18.5 dB, where 1.5 dB is an estimate of the loss contribution due to bond-wire inductance. The NF of the LNA after deembedding the noise contribution of termination resistors ($R = 100$- and 50-Ω port) is calculated to be 1.76 dB.

TABLE IV
COMPARISON OF RESULTS

Work	Technology	Freq GHz	S21 dB	NF dB	IIP3 dBm	P_{dc} mW	FOM
[2]	0.25μm CMOS	0.9	14.6	1.8	10.5	5.4	117
[3]	0.35μm CMOS	0.9	2.5	2.8	18	45	3
[6]	0.18μm CMOS	3	6.5	1.9	15	8.9	29
[7]	0.6μm GaAs	0.9	17	1.6	8.5	12.7	63
[8]	0.25μm CMOS	2.2	14.9	3	16.1	23.5	54
[9]	0.35μm CMOS	0.9	10	2.8	15.6	21.1	19
[12]	0.5μm SiGe	0.88	15.7	1.4	11.7	11.7	124
[14]	0.25μm CMOS	0.9	15.5	1.65	22	24.2	503
This Work	0.35μm CMOS	0.9	11	2.95	21	22.5	92
De-em bedded	0.35μm CMOS	0.9	18.5	1.76	21	22.5	793

The final experimental results and deembedded results obtained are summarized and compared with other existing solutions in Table IV. The linearity achieved in this study is greater than +21 dBm and is comparable to the best achieved thus far in literature [14] and with lesser power consumption. In the experimental results, the LNA has lesser gain and poorer NF, as it is terminated with a resistive load. It is, however, possible to achieve higher gain if the LNA is terminated with a high-impedance load like a buffer or a high input impedance mixer leading to a lesser NF, as demonstrated in the deembedded results; where the effects of the termination resistors are deembedded. The NF and $S21$ performances can be further improved using inductors with higher Q. In our case, $Q \approx 3$ was obtained. This study outperforms all other published work in the same 0.35-μm technology [3], [9]. As seen from the deembedded results, the overall performance [figure-of-merit (FOM)] of this LNA is superior to previously reported topologies. The FOM used is defined in (9) as follows:

$$\text{FOM} = \text{OIP3(mW)}/\left(P_{\rm dc}(\text{mW}) \cdot \{F - 1\}\right). \qquad (9)$$

VII. CONCLUSION

The effect of second-order nonlinearity at RF frequencies on the linearity of an LNA has been explained. The drawbacks with the existing DS method and modified DS method have been explained. A novel circuit using the phase cancellation technique has been proposed, which uses a source degenerated auxiliary transistor to tune the IM3 components in its branch to be equal in magnitude and opposite in phase to that in the main branch, thus canceling them effectively at the output. Volterra series analysis to theoretically prove the concept has been done. The proposed solution has been experimentally shown to achieve linearity of

+21 dBm. It has been shown that the additional circuit component does not degrade the NF and does not affect the input match. Hence, the auxiliary circuit provides the capability to be attached to any given LNA and designed for high linearity without changing the given LNA's parameters.

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Sivakumar Ganesan received the B.E. degree (Hons.) in electrical and electronics engineering from the Birla Institute of Technology and Science, Pilani, India, in 2003, and the M.S. degree in electrical and computer engineering from Texas A&M University, College Station, in 2005.

Since 2006, he has been a Full-Time Design Engineer with Pulsewave RF Inc., Austin, TX.

Edgar Sánchez-Sinencio (F'92) was born in Mexico City, Mexico. He received the Ph.D. degree from the University of Illinois at Urbana-Champaign, in 1973.

He is currently the TI J. Kilby Chair Professor and Director of the Analog and Mixed-Signal Center, Department of Electrical and Computer Engineering, Texas A&M University, College Station.

Dr. Sánchez-Sinencio is a former IEEE Circuits and Systems (CAS) Vice President–Publications. He was the IEEE CAS Society representative to the Solid-State Circuits Society (2000–2002). He was a member of the IEEE Solid-State Circuits Society Fellow Award Committee from 2002 to 2004. In November 1995, he was the recipient of an Honoris Causa Doctorate presented by the National Institute for Astrophysics, Optics and Electronics, Puebla, Mexico, which was the first honorary degree awarded for microelectronic circuit design contributions. He was a corecipient of the 1995 Guillemin–Cauer for his work on cellular networks. He was a corecipient of the 1997 Darlington Award for his work on high-frequency filters. He was also the recipient of the 1999 IEEE CAS Society Golden Jubilee Medal.

Jose Silva-Martinez (SM'98) was born in Tecamachalco, Puebla, México. He received the Ph.D. degree from the Katholieke Univesiteit Leuven, Leuven, Belgium, in 1992.

He is currently an Associate Professor with the Analog and Mixed-Signal Center, Department of Electrical and Computer Engineering, Texas A&M University, College Station. He is the inaugural holder of the TI Professorship-I in Analog Engineering, Texas A&M University.

Dr. Silva-Martinez was a corecipient of the 1990 European Solid-State Circuits Conference Best Paper Award. He was also the recipient of the 2005 Outstanding Professor Award presented by the Department of Electrical and Computer Engineering, Texas A&M University.