A Highly Reliable SEU Hardened Latch and High Performance SEU Hardened Flip-Flop

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Abstract

In this paper, we present a novel single event upset (SEU) hardened latch. The latch consists of a new 12 transistor (12T) SEU hardened storage cell and a C-element. It is insensitive to single event transient (SET) affecting it's internal and output nodes. The differential writing capability of the proposed storage cell is very attractive for designing flip-flops. In addition, we present a high performance SEU hardened D type edge triggered flip-flop, particularly attractive for low data switching activity. The flip-flop utilizes an output feedback connection to the input register stage, in order to reduce power consumption at low data switching activity and eliminate the hold time constraint from traditional clocked CMOS register. We have implemented the proposed latch and the flip-flop in a standard 65 nm CMOS technology. We have investigated power consumptions, propagation delay, SET sensitivity and the area penalty of the proposed latch and flip-flop comparing with the recently reported SEU hardened latches and flip-flops. The proposed latch exhibits as much as 17% lower power-delay product (PDP) compared to recently reported SEU hardened latch, and the proposed flip-flop exhibits lower or comparable PDP compared to recently reported SEU hardened flip-flop while offering more robustness to particle induced SET.

Keywords

Latch, D flip-flop, single event upset, soft error

1. Introduction

Due to the increasing number of memory circuits, aggressive scaling of device sizes, reduction of node capacitance and supply voltage, in nanoscale ASICs and system-on-chips (SOCs) makes circuits more susceptible to single event transients (SETs) or spurious voltage glitches [1]-[2]. The sources of these SETs are cosmic radiation induced high energy neutrons or alpha particles from packaging materials. Interacting with the silicon atoms in the substrate these particles can generate unwanted charge. When the unwanted charge comes close to a reverse-biased p-n junction, particularly if the junction is floating or weakly driven, an SET occurs. If the SET is large enough to collect sufficient amount of charge (critical charge, Q_{cri}) that can alter the stored logic in a memory cell or a flip-flop a single event upset or SEU occurs. While an SEU can cause system malfunctions, it does not permanently damage the device, and hence is often referred to as a soft error [3]. However, with technology scaling, the soft error rate (SER) in logic circuits is exponentially increasing. In fact, the exponential increase of memory element in a chip also increases the SER [4]. Therefore, limiting the SER is very crucial to ensure the reliability and power efficiency of ASICs and SOCs.

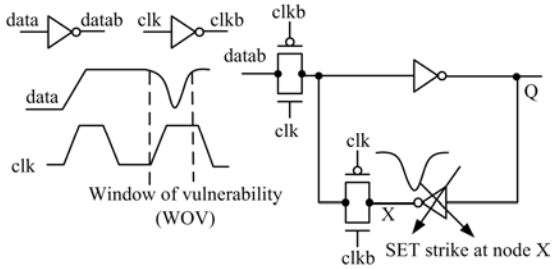

Figure 1. SEU mechanism in a traditional D latch.

The importance of soft error tolerance in current deep submicron technology and the technology trend makes it more attractive for microprocessor or SOC design. Critical applications require circuits to be soft error resilient without adversely affecting the other design parameters such as power, performance (e.g., delay), and area or cost. The protection of latches or flip-flops which are the part of combinational logic is the key to achieve soft error tolerance in the whole system with minimal design compromise. Therefore, many kind of SEU hardened latches and flip-flops are reported in the literature [5]-[17].

In this paper we propose a novel highly robust SEU hardened latch based on new 12T storage cell. In addition, we propose a high performance highly reliable D type edge-triggered SEU hardened flip-flop, designed particularly for low data switching activity. The flip-flop validates the proper operation and performance of the proposed 12T storage cell. The proposed latch shows better performance in terms of power than those in [6]-[7], [10], and better propagation delay than that in [7]. Proposed latch require slightly more silicon area than those in [6]-[7], [10]; however, exhibits better or comparable robustness to particle induced SETs. The proposed SEU hardened flip-flop shows better or comparable performance (in terms of power and delay) than those reported in [12]-[16], however, requires slightly more area than those in [13]-[16].

2. Soft error robust latch

Fig. 1 presents the SEU mechanisms in a traditional D latch. This latch is very sensitive to particle strike that causes an SET and consequently results in SEU. When clock (clk) = 0, a particle strike on node X or Q may upset the logic state of the latch, and the erroneous values are not corrected until a new value is written in the latch.

Fig. 2(a) presents the SEU hardened latch reported in [6]. The latch is based on dual interlocked cell (DICE) [5], which has four storage nodes and we refer this latch as DICE latch. Writing into the latch is done by utilizing two

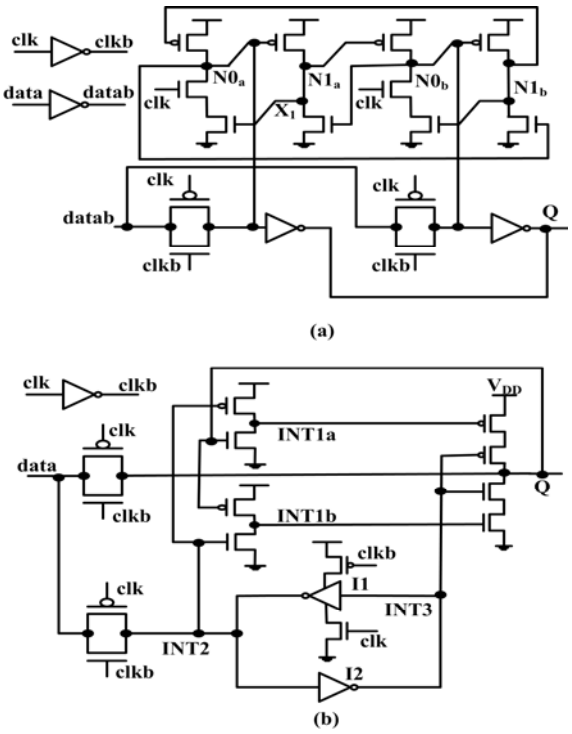

Figure 2. Schematic diagram of: (a) DICE latch in [6]; and (b) HiPeR latch in [10].

transmission gates driving the nodes $N0_a$ and $N0_b$. Two output inverters suppress an SET appearing at output node. The latch can tolerate any single node SET; however, it will produce glitches at the output.

Fig. 2(b) presents the SEU hardened latch reported in [10], named as HiPeR latch. HiPeR latch utilized five nodes including the output Q node to store the data. The storage cell requires 14T to store the data. The transmission gates pass the data directly to output and INT2 node at the clock low phase. Consequently, the node INT3 stores inverted data utilizing inverter I2 and the feedback from Q stables the inverted data at INT1a and INT1b nodes. When the clock is high the inverters I1 and I2 act as cross coupled inverter and help the output to be valid at this stage. Any SET at this phase at node INT2 or INT3 can easily flip that node; consequently produce wrong result at node INT1a or INT1b, depending on the amount of deposit charge, node driving transistor strength and node capacitance. However the problem associated with node INT2 or INT3 due to an SET will not propagate to the output thanks to 3-input output stage. The only problem with this design is the feedback from the output. When clock is low, an SET at output node can easily affect the upstream circuits through transmission gate and flip the data of storage cell. However, low clock phase is not a valid state of a latch and will only increase power consumption.

Nicolaidis *et. al.* proposed a highly robust hardened latch uses blocking feedback transistors to mitigate SEUs [7]. Another approach utilizes triple path dual interlocked configuration to mitigate SEUs [17]. These approaches are plagued with the disadvantages of consuming large power or

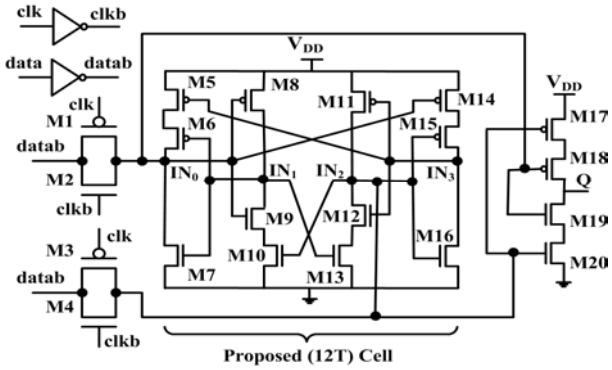

Figure 3. Proposed SEU hardened latch.

latch performance degradation. Thus a highly reliable SEU hardened latch with minimal power and performance degradation is of great interest.

3. Proposed SEU hardened latch

The proposed SEU hardened latch has transmission gates, 12T novel storage cell and a C-element as shown in Fig.3. Similar to DICE and HiPeR latch proposed 12T storage cell has four internal storage nodes IN_0, IN_1, IN_2, and IN_3. Each of these four nodes is connected to one NMOS and two PMOS (or two NMOS and one PMOS). The data are stored at each node as 1, 0, 1, 0, or 0, 1, 0, 1 in the nodes IN_0, IN_1, IN_2, IN_3, respectively. The writing into the cell can be done utilizing pair of nodes (IN_0, IN_2), (IN_1, IN_3) using similar potential at each pair of nodes. The major advantage of this cell is we can write differentially into the cell utilizing nodes IN_1 and IN_2. This special characteristic is also present in Quatro latch reported by Jahinuzzaman *et. al.* in [18]. However, a sufficiently large particle strike at any sensitive node of Quatro latch can flip the storage logic. The SEU tolerance of the proposed latch will be discussed in the subsequent sections. When the clk is in low position and data is high, M8, M14, and M15 are turned ON resulting high potential at nodes IN_1 and IN_3. Consequently, M7, M12, and M13 are turned ON, providing excellent feedback and help the cell to store the data. The C-element utilizes two similar potential nodes (IN_0 and IN_2) to write data at the output. When the clk is in low position and data is low, the operation is analogous to previous case.

4. Simulation results of proposed latch

We implemented our proposed latch considering a standard 65 nm CMOS technology with clock frequency of 5 GHz and 1V supply voltage. In order to perform all the simulations we have followed the following aspect ratio (*W/L*) for Fig. 3: *(W/L) = 2* for the transistors M5-M8, M11-M16, and M19. *(W/L) = 3* for the transistors M1, M3, and M18. *(W/L) = 4* for the transistors M9 and M10. *(W/L) = 5* for the transistors M17 and M20. *(W/L) = 10* for the transistors M2 and M4.

In order to have a fair comparison, we have also implemented a standard D latch (see Fig. 1), and recently reported latches in [6]-[7], [10], utilizing corresponding sizing techniques described in these articles. The layout area, propagation delay of the proposed latch and the competing latches are presented in Table 1. Here the term propagation

Table 1. Performance comparison of the latches.

Types of latches	Layout Area (μm^2)	Delay t_{D-Q} (ps)	Power (μw)	PDP (fJ)
Traditional D latch	5.70	26.0	18.4	0.48
Hiper latch [10]	12.15	36.5	33.0	1.21
Latch in [7]	8.46	52.0	27.8	1.45
DICE latch [6]	12.01	45.0	27	1.22
Proposed latch	12.73	49.5	24.4	1.21

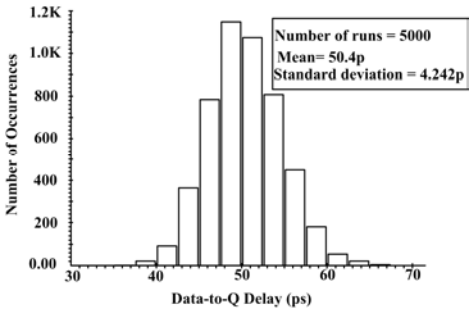

Figure 4. Monte-Carlo simulations of D-Q (t_{D-Q}) delay of the proposed latch.

delay (t_{D-Q}) is defined as the time interval between a transition of the latch input signal and its corresponding transition of the latch output, each of them measured at the 0.5 V_{DD} [10]. We considered the propagation delay of the latch as the average of the propagation delays of both input transitions low-to-high and high-to-low.

In order to measure the correct functionality and performance of the proposed latch, we considered 5000 sample of t_{D-Q}, utilizing Monte-Carlo simulation. In Monte-Carlo simulation, we considered process variation, and mismatch with fanout-of-4 (FO4) inverter as latch load. The result of this experiment is shown in Fig.4.

We determined the power consumption of each latch considering the clock driver power and latch internal power consumption. The total power consumption (at 25% data activity) and the power-delay (t_{D-Q})-product (PDP) of the each latch are presented in Table 1. We defined 100% data activity as, for each clock cycle, when a new data is written in the latch. The proposed latch outperforms the other latches. In particular, proposed latch consumes 26% less power than that of recently reported HiPeR latch [10] and 9.6% less power than that of DICE latch reported in [6]. However, the proposed latch consumes 4.6% higher area than that of HiPeR latch and 5.7% higher area than that of DICE latch.

5. SEU sensitivity of the proposed latch

We have verified the robustness of the proposed latch by introducing ideal current source to emulate a particle induced SET at different internal nodes of Fig. 3. Fig. 5 shows the result of this experiment with nominal sizing of the latch explained earlier. Fig. 5(a) presents an SET affecting at node IN_0 (1-to-0 and 0-to-1). When node IN_0 has an (0→ 1) SET, it has no affect to two nodes (IN_1 and IN_3) driven by IN_0. As on that instant IN_2 = 0, M10 OFF, holding the node IN_1 at high level. When node IN_0 has an (1→ 0) SET, it quickly

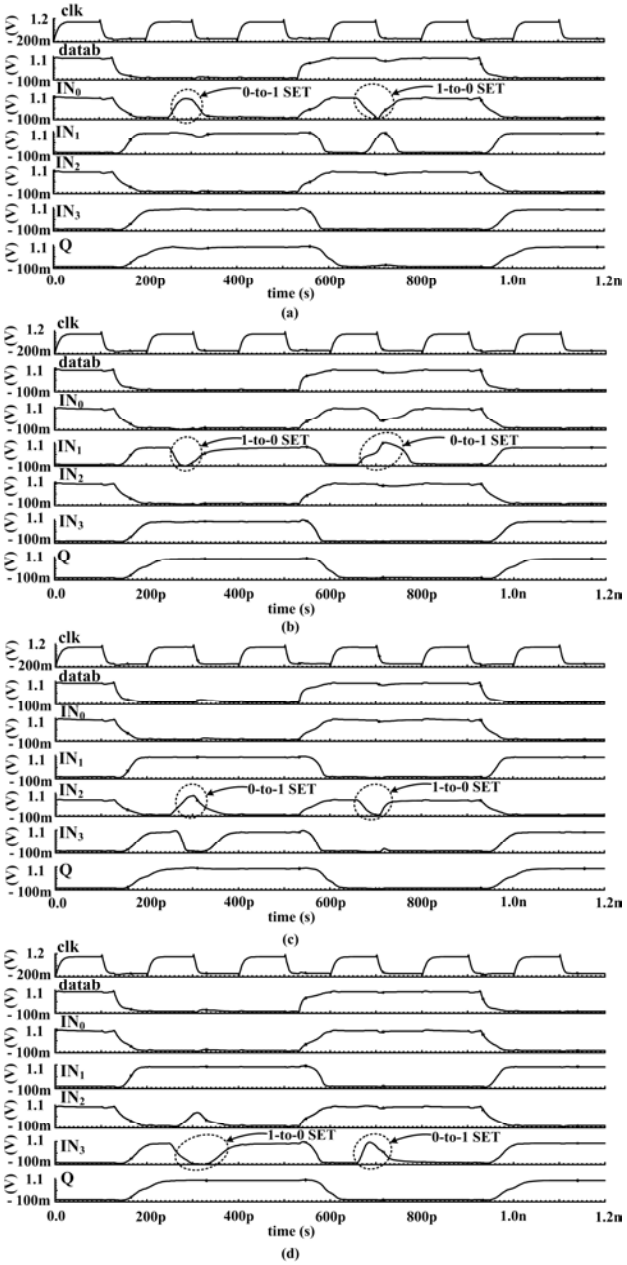

Figure 5. Simulation results obtained for SET affecting: (a) at node IN_0; (b) at node IN_1; (c) at node IN_2; (d) at node IN_3.

pulls-up node IN_1 by switching OFF M9 and turning ON M8. As on that instant IN_3 = 0, M12 OFF, holding the node IN_2 at high level. Consequently, it cannot alter the stored logic of the cell and recover after the SET period. Fig. 5(c) presents an SET affecting at node IN_2 (1-to-0 and 0-to-1); the recovery operation is analogous to node IN_0.

Fig. 5(b) presents an SET affecting at node IN_1 (1-to-0 and 0-to-1). When node IN_1 has an (1→ 0) SET, it has no effect to two nodes (IN_0 and IN_2) driven by IN_1. As on that instant IN_3 = 1, M5 OFF, holding the node IN_0 at low level. When node IN_1 has an (0→ 1) SET, it quickly pulls-down node IN_0 by switching OFF M6 and turning ON M7. However, it cannot alter the stored logic of the stored cell and

Table 2. Critical charges for multiple node SET of the latches.

	Proposed latch		DICE latch [6]		HiPeR latch [10]		
Critical node pairs	**(IN_0, IN_2), (IN_1, IN_3)**	**(IN_1, IN_2)**	**(N0a, N0b)**	**(N1a, N1b)**	**(INT1b, INT2)**	**(Q, INT2)**	**(Q, INT3)**
When Q=1, Q_{cri} (fC)	14	8.2	4.9	7.98	5.7	4.7	12.6
When Q=0, Q_{cri} (fC)	6.6	8.8	9.3	16.9	7.9	5.3	8.60

recover after the SET period. Fig. 5(d) presented an SET affecting at node IN_3 (1-to-0 and 0-to-1); the recovery operation is analogous to node IN_1. It is clear from this experiment that the proposed latch is insensitive to single node SET and the results are analogous to latches reported in [6], [10]. However, latch reported in [7] has two sensitive nodes, if a particle induced SET strikes at these nodes can easily flip the storage logic of the latch, which was also reported and explained in [10] by Omana *et. al.*.

Since in scaled sub-micron technology, the layout area is very small, the probability of charge sharing between two neighboring nodes is very high. A technique has been proposed in [6] to reduce SER when a particle strike alters multiple nodes at the same time. This technique identifies the critical nodes and utilizes the physical separation of those nodes on the layout implementation. In order to reduce SER, in our layout implementation of the proposed latch, we have also separated the potential critical nodes that may share charges.

In order to measure the sensitivity of the proposed latch to multiple node SET, we identify the critical nodes of the proposed latch and the latches reported in [6], [10]. However we eliminate the latch reported in [7] for this experiment, as only a single node SET has the potential to flip the stored data of this latch. The DICE latch reported in [6] has two pair of critical nodes can share charges and work in tandem to alter the stored logic. These pair of nodes are ($N0_a$, $N0_b$) and ($N1_a$, $N1_b$) in Fig. 2(a). In addition we identified the critical node pairs for HiPeR latch and these are (INT1b, INT2), (Q, INT2), and (Q, INT3) (see Fig. 2(b)). We considered the output node (Q) of HiPeR latch as the critical node as it is directly connected to the transistors driving the internal nodes. We have mimicked the scenario of multiple node SET by introducing two ideal exponential current sources to inject current at critical pair of nodes of Figs. 2-3. In order to have a fair comparison, we deactivated the clk and data signals for this experiment. Next, we utilized the parametric SPICE analysis to calculate the amount of charge (e.g., Q_{cri}) required to alter the stored logic by integrating the exponential ideal current. Actually, Q_{cri} of a node depends on the node driving transistor strength, node capacitance and the operating voltage [6]. Table 2 listed the Q_{cri} of the proposed latch comparing with the latches reported in [6], [10]. Clearly, proposed latch has comparable or higher critical charge than those of the latches reported in [6], [10], which directly translates to lower SER by following equation reported in [9]:

$$SER = \sum_{i=1}^{n} \frac{WOV_i}{T_{clk}} . K_i . \alpha . e^{-\beta Q_{cri(i)}} \qquad (1)$$

Where, n represents the number of nodes that might be affected by an SET, k_i is a constant proportional to the area of node i, WOV is the window of vulnerability (see Fig. 1), which is the time interval in which an SET can propagate to the output, T_{clk} is the clk interval, α and β are fitting parameters.

6. Proposed SEU hardened flip-flop

In order to validate the operation and the application of proposed 12T storage cell, we designed a D type SEU hardened edge-triggered flip-flop, sketched in Fig. 6.The feedback connection from the output to input register stage makes flip-flop more attractive, particularly, at low data switching activity. This structure also eliminates the hold time constraint from clocked CMOS input stage during the 1-1 overlap of clk and clkb signals. The transient response of the proposed flip-flop is depicted in Fig. 7. We used minimum length (60 nm) transistors and the width of each transistor is presented in Fig. 6 in μm.

When the clk is low, the input clocked stage will be active, if data ≠ output (Q). On the other hand if clk = 0, and data = Q, there is no internal node charging-discharging resulting significant power saving. If clk and Q are low, and if data is high, transistors M1-M3 are ON and charges node X to V_{DD}. With the rising edge of clk signal, nodes IN_0 and IN_2 discharge to low, resulting high Q. If clk = 0, Q stores a high logic, and if data is low, transistors M4-M6 are ON and discharge node X to ground. With the rising edge of clk signal nodes IN_0 and IN_2 charges to V_{DD}, resulting low logic at the output. Two similar potential nodes IN_0 and IN_2 drive the output C-element buffer. It is important to realize the importance of C-element at the output. It masks any single node SET propagating to the output. In contrary, it increases the flip-flop layout area and slightly degrade the performance; however, results show that it does not adversely affect the flip-flop overall performance.

7. Simulation results of the proposed flip-flop

We implemented our proposed flip-flop considering the clock frequency of 5 GHz and supply voltage of 1V. We have also implemented and SPICE analysis was performed consistently on the flip-flops reported in [12]-[16] and a standard master-slave D flip-flop (MSD FF). Here we consider the high-performance and low-power sense-amplifier transmission-gate soft-error tolerant flip-flop (SATG-SE) as flip-flop reported in [16]. Table 3 presents the layout area of the proposed flip-flop comparing with the recently reported SEU hardened flip-flops.

The setup time (t_s), hold time (t_h) were calculated via the method described in [13]. The t_s and t_h of the proposed flip-flop are 30 ps and -25 ps, respectively. The t_s of the proposed flip-flop is 30% higher than that of master-slave D flip-flop; however negative hold time makes it more attractive for utilizing in synchronous high frequency systems. The propagation delay, $t_{clk\text{-}Q}$, was measured from the 50% value of the rising edge of the clock to 50% value

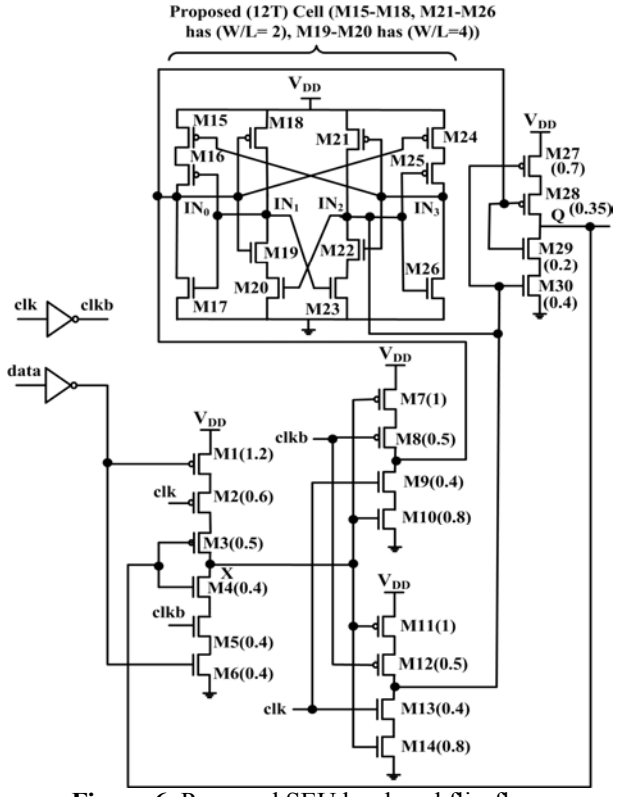

Figure 6. Proposed SEU hardened flip-flop.

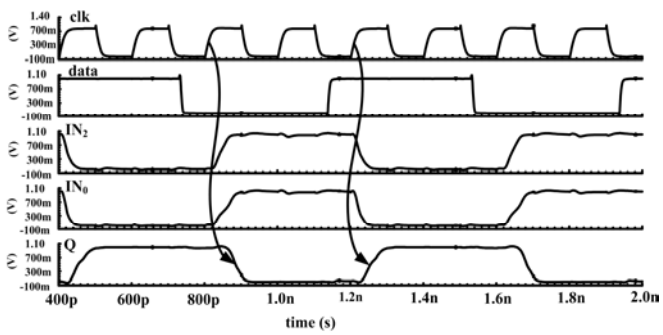

Figure 7. SPICE simulation waveforms of the proposed flip-flop.

of the flip-flop output. Table 3 also provides $t_{clk\text{-}Q}$ estimate by SPICE simulation under comparison. Clearly, proposed flip-flop exhibits lower or comparable $t_{clk\text{-}Q}$ than those of competing flip-flops.

We measured the power consumptions of the each flip-flop considering the clock and data driver powers, and flip-flop internal power. The total power consumption of the flip-flops then estimated by adding these three components from 100% to 0% data switching activity. We defined 100% data switching activity as, with each rising edge of clock signal, the flip-flop will latch a new data at the output. Table 4 provides normalized power consumption of each flip-flop estimated by SPICE simulation under comparison at 5 GHz clock frequency and V_{DD} = 1V. At 0% data switching activity the proposed flip-flop consumes 56% and 9% less power than those reported in [15] and [16], respectively. A

Table 3. Layout area and the delay ($t_{clk\text{-}Q}$) of the flip-flops.

Types of Flip-flop	Number of Transistors	Layout Area (μm^2)	Delay $t_{clk\text{-}Q}$ (ps)
MSD FF	22	12.8	36.8
Flip-flop in [12]	36	23.1	74.3
Flip-flop in [13]	28	18.2	52.0
Flip-flop in [14]	22	18.6	63.5
Flip-flop in [15]	32	18.8	63.7
Flip-flop in [16]	31	19.4	33.0
Proposed FF	34	21.4	39.3

Table 4. Normalized power consumption of the flip-flops.

Types of flip-flop	Data switching activity (%)				
	100	**50**	**25**	**12.5**	**0**
MSD FF	0.58	0.61	0.58	0.6	0.87
Flip-flop in [12]	1.75	1.51	1.13	1.03	1.16
Flip-flop in [13]	1.07	1.20	1.12	1.02	1.24
Flip-flop in [14]	1.08	1.19	1.17	1.24	1.85
Flip-flop in [15]	0.99	1.21	1.27	1.42	2.26
Flip-flop in [16]	1.17	1.12	0.94	0.91	1.10
Proposed FF	1	1	1	1	1

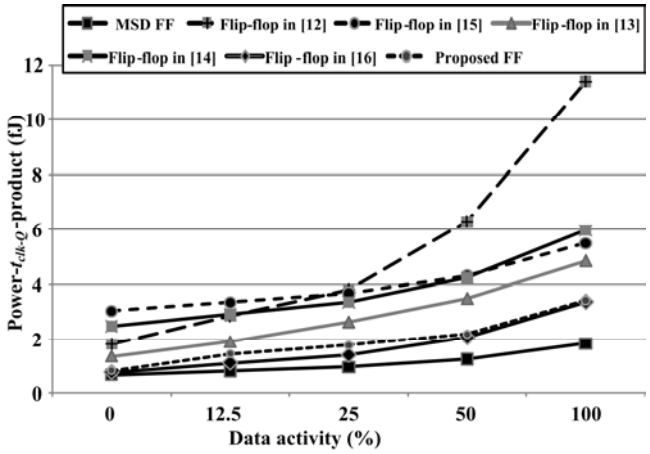

Figure 8. The power-$t_{clk\text{-}Q}$-product of the flip-flops at different data switching activity in (fJ).

careful observation of the Table 4 reflects that the rate of power reduction of proposed flip-flop is much higher than that of existing designs, thanks to the feedback connection from the output to input register stage (see Fig. 6). Then the power-$t_{clk\text{-}Q}$-product (PDP) of each flip-flop was estimated. Fig. 8 presents the PDP of the flip-flops at different data switching activity. At 25% data switching activity, the proposed flip-flop exhibits 51% lower PDP than that of flip-flop reported in [15], and 47% lower PDP than that of flip-flop reported in [14].

In order to ensure the reliability of the proposed flip-flop we considered 5000 sample of $t_{clk\text{-}Q}$, utilizing Monte-Carlo simulation. In Monte-Carlo simulation, we considered process variation and mismatch with fanout-of-4 (FO4) inverter as flip-flop load. The result of this experiment is shown in Fig. 9.

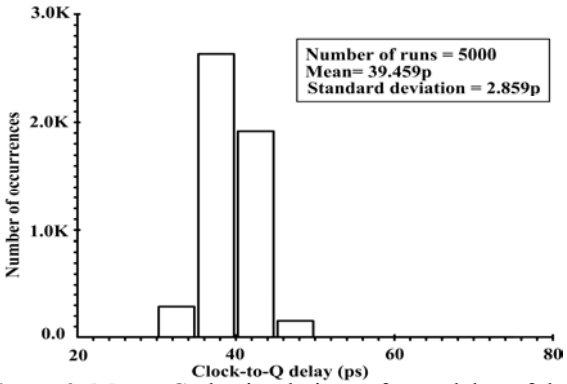

Figure 9. Monte-Carlo simulations of $t_{clk\text{-}Q}$ delay of the proposed latch.

8. Conclusion

In this paper, we have proposed a high performance, highly reliable SEU hardened latch. The latch is based on a novel 12T SEU hardened storage cell, which can tolerate any single node SET. The conventional C-element at the output, masks any single node SET propagation to output. Experimental results show that the proposed latch consumes less power than the recently reported latches with comparable propagation delay; however, consumes slightly higher area than the competing latches. We have demonstrated the robustness of proposed latch to multiple node SETs which is the growing concern in nanoscale technology, the results are better or comparable to reference latches. In addition, we have proposed a high performance SEU hardened D type flip-flop that consumes much lower power when compared to recently reported SEU hardened flip-flops, particularly at low data switching activity. Its input register structure eliminates the hold time constraint from the traditional clocked CMOS register. The PDP of the proposed flip-flop is much lower than those of recently reported flip-flop with slightly more silicon area. The differentially write ability of the 12T cell makes it more attractive for designing flip-flops or latches.

9. References

[1] R. C. Baumann, "Soft Errors in Advances Semiconductor Devices-Part I: The Three Radiation Sources", *IEEE Trans. on Device and Materials Reliability*, Vol. 1, No. 1, pp. 17 – 22, 2001.

[2] T. Karnik and P. Hazucha, "Characterization of soft errors caused by single event upsets in CMOS processes," *IEEE Trans. Depend. Secure Comput.*, vol. 1, no. 2, pp. 128–143, Apr./Jun. 2004.

[3] J. Benedetto, *et al.*, "Heavy ion-induced digital single-event transients in deep submicron processes," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3480–3485, Dec. 2004.

[4] R. C. Baumann, "Soft errors in advanced computer systems," *IEEE Des.Test. Comput.*, vol. 22, no. 3, pp. 258–266, May/Jun. 2005.

[5] T. Calin, M. Nicolaidis, and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology," *IEEE Trans. Nuclear Science*, vol. 43, no. 6, pp. 2874-2878, Dec. 1996.

[6] P. Hazucha, *et al.*, "Measurements and Analysis of SER-Tolerant Latch in a 90-nm Dual-VT CMOS Process," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1536-1543, Sept. 2004.

[7] M. Nicolaidis, R. Perez, and D. Alexandrescu, "Low-cost highly-robust hardened cells using blocking feedback transistors," in *Proc. 26th IEEE VLSI Test Symp.*, Apr. 27-May 1, 2008, pp. 371–376.

[8] R. Oliveira, A. Jagirdar, and T. J. Chakraborty, "A TMR scheme for SEU mitigation in scan flip-flops," in *Proc. 8th Int. Symp. Quality Electron. Design*, Mar. 26–28, 2007, pp. 905–910.

[9] M. Omana, D. Rossi, and C. Metra, "Latch Susceptibility to Transient Faults and New Hardening Approach," *IEEE Trans. Computers*, vol. 56, no. 9, pp. 1255-1268, Sept. 2007.

[10] M. Omana, D. Rossi, and C. Metra, "Novel High Speed Robust Latch," *in Proc. IEEE Int'l Symp. Defect and Fault Tolerance in Very Large Scale Integration (VLSI) Systems*, pp. 65-73, 2009.

[11] M. Omana, D. Rossi, and C. Metra, "High-Performance Robust Latches," *IEEE Trans. Computers*, vol. 59, no. 11, pp. 1455-1465, Nov. 2010.

[12] W. Wang and H. Gong, "Edge triggered pulse latch design with delayed latching edge for radiation hardened application," *IEEE Trans. Nucl. Sci.,* vol. 51, no. 6, pp. 3626-3630, Dec. 2004.

[13] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "Soft error robust impulse and TSPC flip-flops in 90nm CMOS," in *Proc. Microsystems and Nanoelectronics Research Conf.*, Ottawa, ON, 2009, pp. 45-48.

[14] S. M. Jahinuzzaman and R. Islam, "TSPC-DICE: a single phase clock high performance SEU hardened flip-flop," in *Proc. IEEE Int. Midwest Symp. on Circuits and Systems*, 2010, pp. 73-76.

[15] D. Krueger, E. Francom, and J. Langsdorf, "Circuit design for voltage scaling and SER immunity on a quad-core Itanium® processor," *ISSCC Dig. Tech. Papers*, pp. 94–95, 2008.

[16] D. Li, D. Rennie, P. Chuang, D. Nairn, and M. Sacdev, "Design and analysis of metastable-hardened and soft-error tolerant high-performance, low-power flip-flops," in *Proc. IEEE Int. Symp. on Quality Electronic Design (ISQED),* March 2011, pp. 1-8.

[17] D. R. Blum and J. G. Delgado-Frias, "Delay and energy analysis of SEU and SET-tolerant pipeline latches and flip-flops," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 3, pp. 1618–1628, Jun. 2009.

[18] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability*," IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3768 - 3773, Dec. 2009.