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A Hybrid Damping Method for *LLCL*-Filter Based Grid-tied Inverter with a Digital Filter and an *RC* Parallel Passive Damper

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***Abstract*—Grid-tied inverters have been widely used to inject the renewable energies into the distributed power generation systems. However, a large variation of the grid impedance challenges the stability of the high-order power filter based grid-tied inverter. Many passive and active damping methods have been proposed to overcome this issue. Recently, a composite passive damping method for a high-order power filter based grid-tied inverter with an *RC* parallel damper and an *RL* series damper was presented to eliminate this problem, but at the cost of more material and power losses. In this paper, a hybrid damping method with a digital filter and an *RC* parallel damper is proposed. The design of the digital filter is developed using a normalized method. The validity is verified through the simulations and the experiments on a 500 W, 110 V/50 Hz prototype, while the grid inductance varies from 0.15 mH to 5 mH.**

I. INTRODUCTION

High-order power filters, such as *LCL*-filters or *LLCL*-filters [1], [2], are increasingly being used as the connection between the grid-tied inverter and the distributed power grid, since they can provide better attenuation of the PWM switching harmonics with the less total inductance compared to the traditional *L*-filters [3]. However, the stability of the power electronics based power system has been challenged due to the possible resonance caused by the interactions between the higher-order based grid-tied inverters, the diode rectifier based loads, the parasitic capacitance, the line grid-impedance, and so on [4].

In order to resist the effect of the grid background harmonics, a Proportional Resonant regulator with Harmonic Compensation (*PR+HC* regulator) is often used for a grid-tied inverter. However, it is easy to trigger the resonance when the grid impedance varies [5], [6]. Two basic methods are adopted to stabilize the grid-tied inverter, where one is to estimate the on-line parameters of the grid [7]-[9] and the other is to use the passive or active damping solution to overcome this problem [4],[6],[10]-[18].

In theory, if the grid impedance can be detected precisely, it is possible to regulate the on-line gain of the controller to avoid the dangerous resonance. However, it is not easy to obtain the exact grid impedance. For example, [7] used try and error method to regulate the gain of the controller and estimate the grid impedance, but the result is unavoidable affected by the background harmonic voltages. Ref. [8] suggested using PQ variations to estimate the grid impedance, and obviously, this method depends on the power ratio between the inverter and the power system. Ref. [9] used the harmonic injection to estimate the grid impedance. However, if there are many inverters connected to the distribution power system, the error cannot be avoided. Till now, the on-line impedance detection is not an effective method to suppress the possible resonance for the power electronics based distribution power system.

The passive damping is an attractive method to enhance the stability for a high-order filter based grid-tied inverter. The simplest passive damping method is to insert a resistor in the loop of capacitor, but it will results in a large power losses, especially when the switching frequency is not so high [10]. An *RC* parallel damper is often adopted for a high-order filter based grid-tied inverter system due to the small additional power losses [4], [11]. In order to balance the damping effect and the power loss, the capacitance of the *RC* parallel damper has been suggested to be equal to the one of the *LCL*-filter [11]. But it has been proven that the damping effect depends on the grid inductance and an effective *RC* parallel damper cannot always be achieved, when the grid inductance varies in a wide range [4].

In contrast to the passive damping methods, the active damping solutions can eliminate the additional power loss. The plugged-in filter [12], [13] and the state feedback control [14], [15] are two attractive methods. However,

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when the grid inductance varies in a large range, they all meet their own problems. For instance, whether a notch digital filter or a lead-lag digital filter is used as plugged-in filter, it is difficult to tune the parameters when the grid impedance varies widely. Similarly, when the current of the capacitor is used as a feedback to dampen the system, the right gain for the stiff grid may cause a poor bandwidth under the weak grid condition.

Recently, the analysis on the regions of active damping control is an active research issue [16], [17], which may reveal that it is difficult to use a single damping method to stabilize a high-order power filter based grid-tied inverter in the distribution power system [6], [18]. Ref. [6] proposed a composite passive damping method for the *LLCL*-filter based inverter, but at the cost of more material and power losses.

In this paper, a hybrid damping method which combines a digital filter with an *RC* parallel damper is proposed, which ensures the stability of the high-order filter based inverter while the grid inductance varies widely. The main focus of this paper is to design a reasonable digital filter to realize the same function of *RL* series damper in [6]. The design of the digital filter is developed in details. Simulations and experimental results on a 500 W, 110 V/50 Hz single-phase prototype are carried out to verify the theoretical analysis.

II. *LLCL*-FILTER BASED INVERTER SYSTEM WITH *RC* PARALLEL PASSIVE DAMPER

A. Configuration

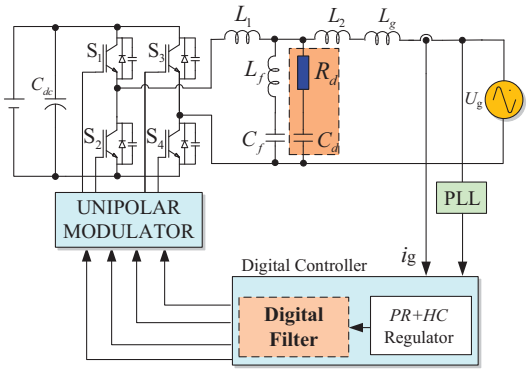


Fig. 1. Single phase grid-tied inverter with an *RC* parallel passive damper and a digital filter.

Fig. 1 shows a single phase grid-tied inverter with an *RC* parallel passive damped *LLCL*-filter, where *PR+HC* regulator is adopted. The grid current is used as the feedback and the transfer function of the grid current versus the output voltage of the inverter is then derived as

$$G_{u_i \to i_g}(s) = \frac{Z_c(s)}{Z_1(s)Z_2(s) + Z_1(s)Z_c(s) + Z_2(s)Z_c(s)} \quad (1)$$

$$Z_1(s) = L_1 s, Z_2(s) = (L_2 + L_g)s$$

$$Z_c(s) = \frac{(R_d C_d s + 1)(L_f C_f s^2 + 1)}{L_f C_f C_d s^3 + R_d C_d C_f s^2 + (C_d + C_f)s} \quad (2)$$

The open-loop transfer function of the system without considering the digital filter can be written as

$$G_{open-loop}(s) = G_c(s)G_{u_i \to i_g}(s)G_{inv}(s)H(s)delay(s) \quad (3)$$

where $G_c(s)$ is the gain of the *PR+HC* regulator, $G_{inv}(s)$ is the gain of the PWM inverter and $H(s)$ is the sensor gain of the grid-injected current, $delay(s)$ is the transfer function of the control delay, which includes the PWM delay and the sampling delay.

The gain and the phase characteristics of the above plant can be explored with (4) and (5) respectively,

$$\left|G_{plant}(s)\right| = 20\log\left|G_{u_i \to i_g}(s)G_{inv}(s)H(s)\right| \quad (4)$$

$$\varphi_{plant}(j\omega) = \varphi_{u_i \to i_g}(j\omega) + \varphi_{inv}(j\omega) + \varphi_H(j\omega) - \omega T_d \quad (5)$$

where $\varphi_{u_i \to i_g}(j\omega)$, $\varphi_{inv}(j\omega)$, and $\varphi_H(j\omega)$ are the phase of $G_{u_i \to i_g}(s)$, $G_{inv}(s)$, and $H(s)$ respectively, the ω is the frequency in rad, and T_d is total delay of system.

In order to achieve a high control bandwidth to insert the harmonic compensators, the control delay is always wanted to be as small as possible. Considering the easy realization with the DSP digital controller, all the design is based on that the delay of $T_d = 0.75\ T_s$ [19], where T_s is the switching period. Since the grid inductance and the crossover frequency of system may vary in a wide range, the effect on the stability of system caused by the control delay can be ignored when conservatively selecting the proportionality coefficient of the *PR* regulator.

B. Gain of the PR+HC regulator and the RC parallel damper

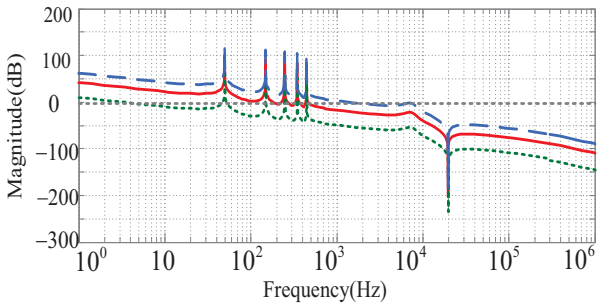


Fig. 2. Bode diagrams of $G_{open-loop}(s)$ with three different gains of *PR+HC* regulator.

Fig. 2 shows the Bode diagrams of $G_{open-loop}(s)$ with three different proportionality coefficients of *PR+HC* regulator. With the different gains, the cross-over frequency falls into different frequency ranges. If the cross-over frequency is within the frequency range of the harmonic compensators, the resonance may be triggered due to that the phase margin cannot always be satisfied [17]. If the cross-over frequency is lower than the fundamental frequency in the stiffest grid state, in theory, the system can also be kept stable [20], but the ability to resist the

background harmonic voltage is unavoidable limited, especially when the grid turns weak.

In the application, it is reasonable to ensure the minimum crossover frequency of the system is higher than that of highest order harmonic compensator under the weakest grid condition, so the proportionality coefficient of the *PR+HC* regulator should be limited in the range as the following,

$$k_{p\_\min} \le k_p < \min\left(k_{p\_\max\_1}, k_{p\_\max\_2}\right) \tag{6}$$

where $k_{\text{p\_min}}$ should satisfy that the crossover frequency is larger than a set value of $f_{\text{Min-B}}$ under the weakest grid condition [5] and it can be derived as,

$$k_{p\_\min} = \frac{2\pi f_{\min\_B}(L_1 + L_2 + L_g)}{|G_{inv}(j2\pi f_{\min\_B})H(j2\pi f_{\min\_cross})|} \tag{7},$$

while the $k_{\text{p\_max\_1}}$ and $k_{\text{p\_max\_2}}$ are the controller gains which are determined of the phase margin and gain margin respectively, and the detail derivations are explained in [6].

C. Parameter design of the RC parallel passive damper[4]

The aim of the *RC* parallel passive damper is to reduce the *Q*-factor of the open-loop transfer function of the system at the dominant characteristic frequency. Generally, the larger capacitance, the better damping effect is achieved, but more additional reactive power is consumed and more power losses are introduced. In order to balance the damping effect and the additional power loss, C_{d} is often set the same as C_{f} as also shown in Fig. 1.

The damping resistor of the *RC* parallel damper is chosen based on the following equation,

$$\frac{\sqrt{\varepsilon+1}}{\varepsilon}\sqrt{\frac{L_p + L_f}{C_f}} \le R_d \le \frac{\varepsilon+1}{\varepsilon}\sqrt{\frac{L_p + L_f}{C_f}} \tag{8}$$

where, $\varepsilon = \frac{C_d}{C_f}$, $L_p = \frac{L_1 \cdot (L_2 + L_g)}{L_1 + L_2 + L_g}$. When $C_{\text{d}} = C_{\text{f}}$, the optimal value of the damping resistor can be calculated as,

$$R_d = \frac{2+\sqrt{2}}{2}\sqrt{\frac{L_p + L_f}{C_f}} \tag{9}$$

D. Critical grid inductance

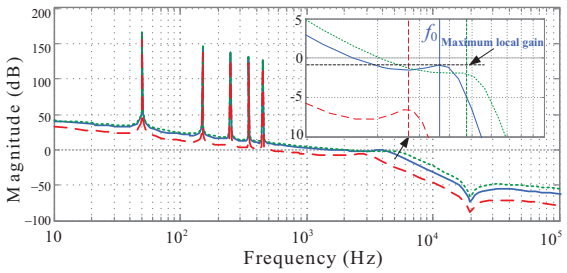


Fig. 3. Characteristics of $G_{open-loop}(s)$ at the dominant frequencies under different grid conditions.

For the *RC* parallel passive damped system, the *Q*-factor at the dominant frequency varies with the grid inductance. As shown in Fig. 3, a maximum value of the local gain around the dominant frequency will appear for a certain grid inductance, which is named as the critical grid inductance of L_0.

For a conservative design, the maximum gain of the *PR+HC* regulator should be chosen to ensure enough gain margin of the system under the most critical grid inductance condition. This critical grid inductance only depends on the parameters of the *LLCL*-filter and the *RC* parallel passive damper.

The first-order partial derivative and the Hessian matrix of the gain of plant can be derived in (10) and (11) respectively,

$$\begin{aligned} \frac{\partial|G_{plant}(j\omega, L_g)|}{\partial\omega} &= 0 \\ \frac{\partial|G_{plant}(j\omega, L_g)|}{\partial L_g} &= 0 \end{aligned} \tag{10}$$

$$H_f = \begin{vmatrix} \frac{\partial^2|G_{plant}(j\omega, L_g)|}{\partial\omega^2} & \frac{\partial^2|G_{plant}(j\omega, L_g)|}{\partial L_g \partial\omega} \\ \frac{\partial^2|G_{plant}(j\omega, L_g)|}{\partial\omega \partial L_g} & \frac{\partial^2|G_{plant}(j\omega, L_g)|}{\partial {L_g}^2} \end{vmatrix} \tag{11}$$

With (10) and (11), the critical grid inductance L_0 and the related frequency f_0 can be calculated. Then, they can be used to design the digital filter.

III. Digital Filter Design

From [6] it is known that for the *LLCL*-filter based inverter connected to a grid with a large variation of the inductance, a robust passive damping can be achieved with a composite passive damper, where its *RC* parallel part is designed under the weakest grid condition, while its *RL* series part is designed under the stiffest grid condition, but at the cost of more materials and power losses. In this section, a digital filter will be introduced instead of the function of the *RL* series damper presented in [6].

A. Identification on the requirement of the digital filter

A normalization method is used for the design and the base values are defined as,

$$\begin{aligned} Z_b &= \frac{(U_g)^2}{P_b} = R_b,\ R_b = \sqrt{\frac{L_b}{C_b}} \\ C_b &= \frac{1}{\omega_0 Z_b},\ L_b = \frac{Z_b}{\omega_0}, \lambda = \frac{L_g}{L_b}, \lambda_0 = \frac{L_0}{L_b} \\ K_o &= U_{dc} \cdot \frac{1}{V_{tri}} \cdot K_{sensor} \cdot K_P \cdot \frac{P}{P_b} \end{aligned} \tag{8}$$

where U_g is the RMS value of the grid, P_b is the basement rated output power of the inverter, U_{dc} is the DC side voltage, V_{tri} is the peak value of the triangle carrier in the modulation, K_{sensor} is the feedback index of the sensor, K_p is the gain of the *PR* controller, P is the rated power of the inverter, λ_0 is the normalized critical grid inductance, and K_o is defined as the normalized gain of the open-loop system.

When discontinuous unipolar modulation scheme is adopted, the current ripple ratio of inverter side inductor is 30%, the total reactive power is typical set to 3 %, the DC voltage is 175 V, the switching frequency is 20 kHz, the base rated output power of the inverter is 500 W, the delay is set to 0.75 T_s, the rated voltage is 110 V/50 Hz, and C_d is the same as C_f to balance the damping effect and the power loss, then the parameters in Fig. 1 can be derived as, $L_1 = 0.0156L_b$, $L_2 = 0.002855L_b$, $C_f = C_d = 0.015C_b$.

Fig. 4 shows the relationship of the gain margin and the grid impedance for an *RC* parallel damped *LLCL*-filter based system under the condition that the *PR* regulator is adopted and the digital filter is not inserted. When the normalized gain of the open-loop system K_o varies from 10.2 to 35.7, the minimum cross-over frequency of $f_{Min\text{-}B}$ changes from 288 Hz to 1050 Hz under the weakest grid inductance of λ = 0.065. [λ_l, λ_μ] is the unstable grid inductance area when K_0 = 21.2.

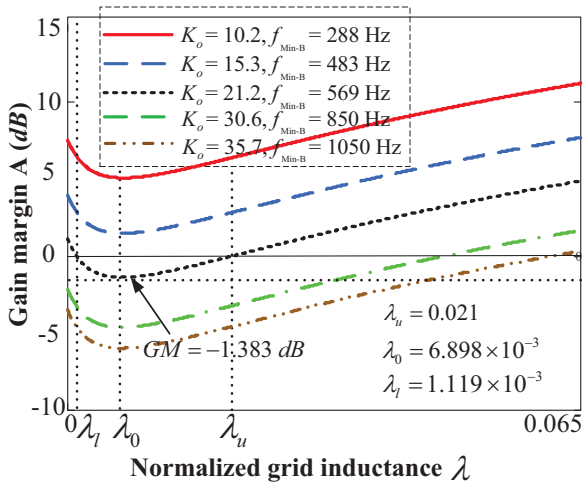


Fig. 4. Relationship of the gain margin and the grid impedance when the normalized gain of K_o is changing.

The minimum control bandwidths with the different K_o under the weakest grid condition are also shown in Fig. 4. It can be seen that the larger K_o, the larger bandwidth is achieved, but also a worse stability. When K_o is larger than a set value, the system cannot always keep stable under the condition of the grid with a large variation of the inductance. Note that a small K_o may help for the stability of system, but it will result in a poor total harmonic distortion of the grid-injected current and a poor dynamic response, especially in the weak grid state with the strong background harmonic voltages. It can also be seen that, at the critical grid inductance of λ_0, the minimum gain margin will always appear. Further, as shown in Fig. 4, if the minimum bandwidth of the system under the weakest grid condition is expected to be 569 Hz to insert the 11th order harmonic compensator, then a digital filter should be designed to offer a enough gain attenuation when grid inductance varies between the area of [λ_l, λ_μ], and at least 1.383 *dB* gain attenuation at the critical grid inductance λ_0.

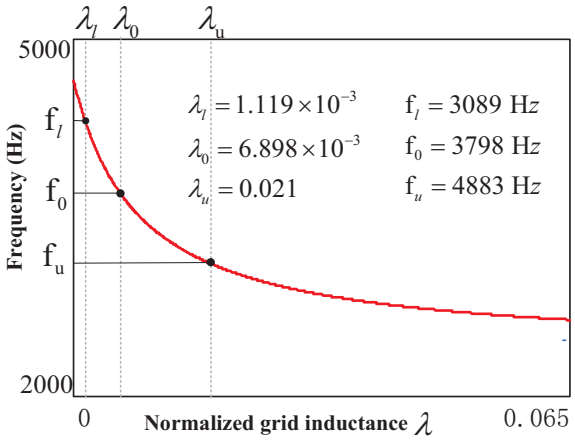


Fig. 5. The frequency versus the grid inductance when K_o is 21.2 and the phase of the system without the digital filter is -180°.

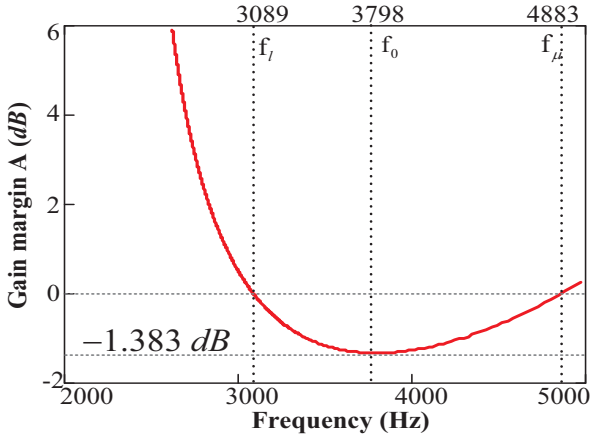


Fig. 6. Gain margin versus the frequency, where K_o is 21.2 and effect of the digital filter is not considered.

For the same target system, when the open loop gain is 21.2 and the phase of the open-loop transfer function (without the segment of the digital filter) is -180 degree, the relationship of the frequency and the grid inductance is shown in Fig. 5. It can be seen that when the grid inductance varies in the range of [λ_l, λ_μ], the corresponding frequency will fall into the range of [3089 Hz, 4883 Hz]. Fig. 6 shows the relationship of the gain margin and the frequency, where K_o is 21.2 and the effect of the digital filter is not considered. It can be seen that the system has not enough phase margin within the frequency of [3089 Hz, 4883 Hz].

From Fig. 4 to Fig. 6, it can be seen that for an *RC* parallel passive damped *LLCL*-filter based single-phase grid-tied inverter system, if the grid-inductance varies in a large range and the system still keeps stable with a set minimum control bandwidth, a digital filter should be adopted to obtain a enough gain attenuation in the frequency range of [3089 Hz, 4883 Hz].

B. Design procedure of the proposed hybrid damper

The design procedure of the proposed hybrid damper can be summarized as following:

1. The *LLCL*-filter and the *RC* parallel damper are designed in accordance to the design introduced in paper [2] and [6] respectively. It should be pointed out that the weakest grid condition should be considered when selecting the parameters for the *RC* parallel damper.
2. As shown in Fig. 4, the relationship of the gain margin and the grid inductance is used to select the desired minimum bandwidth and determine the unstable grid inductance area of [λ_l, λ_μ] together with the critical grid inductance of λ_0.
3. As shown in Fig. 5, the relationship of the gain margin and the grid inductance is used to determine the important frequency range of [f_l, f_μ], which corresponds to the unstable grid inductance area of [λ_l, λ_μ].
4. Design a digital filter by means of the information of [f_l, f_μ] and the desired gain attenuation at the frequency of f_0 which corresponds to the critical grid inductance value as shown in Fig. 6.
5. After the parameters of the digital filter are chosen, the gain margin and the phase margin of the whole system should be verified before the final design, since they are both affected by the character of the digital filter itself.

C. Design example for a 500 W, 110 V and 50 Hz system

In order to illustrate how to design a reasonable digital filter for a *RC* parallel damped *LLCL*-filter based single-phase grid-tied system, an example of a 500 W, 110V/50 Hz system is given. The parameters of the *RC* parallel damped *LLCL*-filter are listed in Table 1 under the condition that the current ripple ratio of inverter side inductor is 30 %, the total reactive power is set to 3 %, the DC voltage is 175 V, the switching frequency is 20 kHz, the delay is set 0.75 T_S, and the minimum cross over frequency is 569 Hz in order to insert 11th harmonic compensator under the weakest grid inductance of 5 mH.

TABLE I. PARAMETERS OF THE *RC* DAMPED *LLCL*-FILTER

Para.	L_1	R_1	L_2	R_2	L_f	R_f	C_f	C_d	R_d
Value	1.2 mH	0.1 Ω	0.22 mH	0.01 Ω	32 μH	0.2 Ω	2 μF	2 μF	35 Ω

The current sensor gain and the gain of PWM inverter are 0.0182 and 1400 respectively for all cases, a *PR+HC* (from 3rd to 11th) regulator is selected for grid-current feedback controller. The transfer function of *PR+HC* regulator is,

$$G_{PR}(s) = K_p + \sum_{h=1,3,5,7,9,11} \frac{K_{ih} s}{s^2 + (\omega_0 (2h-1))^2} \qquad (9),$$

where K_{ih} is set 100.

When a bandwidth of 569 Hz under the weakest grid condition of 5 mH is expected, K_p can be calculated to 0.83 and the normalized loop gain K_0 is 21.2. The critical region of the grid inductance range is [0.15 mH, 1.61 mH] and the corresponding frequency is [3089 Hz, 4883 Hz]. The critical grid inductance is 0.54 mH and the expected gain attenuation is at least 1.383 *dB*.

According to the Fig. 4, there are many kinds of digital filter that can meet the requirement. In order to achieve a good phase margin, the bi-quadratic filter [21] is adopted in this paper. The SISO tool in the MATLAB is used to design the filter and the transfer function of the filter can be obtained as

$$H(s) = \frac{1.21\times10^{-8} s^2 + 1.6\times10^{-4} s + 1}{1.96\times10^{-8} s^2 + 2\times10^{-4} s + 1} \qquad (10).$$

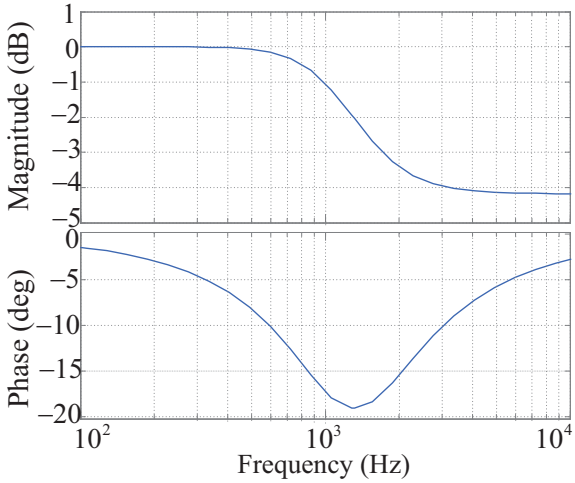
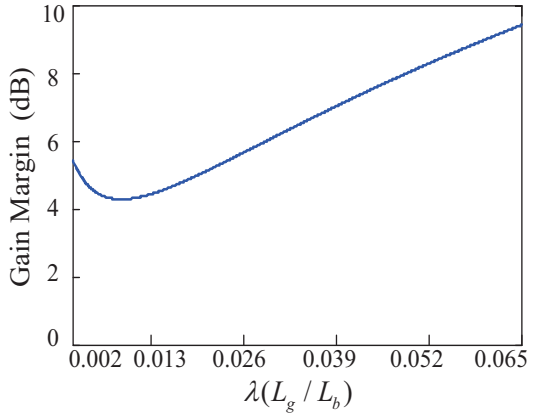


Fig. 7. Bode diagram of the designed digital filter.

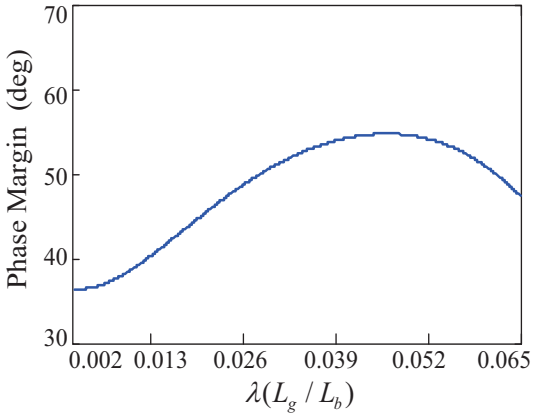
The Bode diagram of the digital filter is plotted in Fig. 5 and it can be seen that in the frequency range of [3089 Hz, 4883 Hz], the attenuation of -4 *dB* can be achieved, which can meet the requirement as described in Fig. 6.

Based on the bilinear transformation, when the sampling frequency is 20 kHz, the transfer function of the discrete digital filter can be derived as,

$$H(z) = \frac{0.6119 z^2 - 0.7091 z + 0.2525}{z^2 - 1.3590 z + 0.5144} \qquad (11).$$



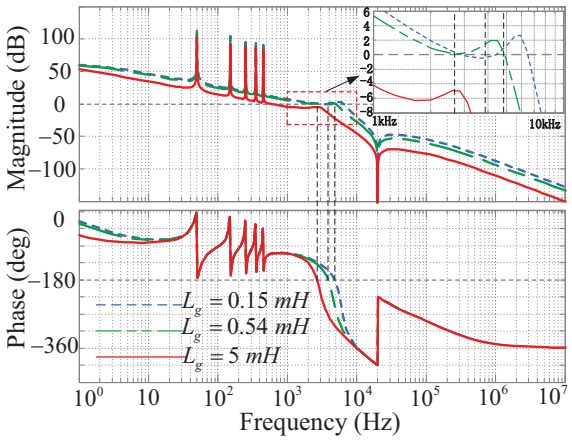
(a)



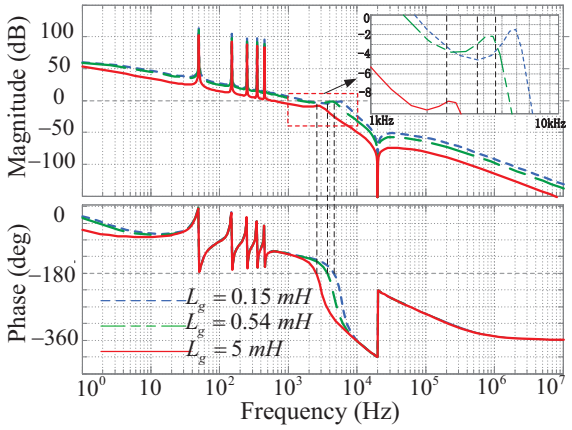
(b)

Fig. 8. Margin of whole system with *RC* parallel damper and the digital filter (a) Gain margin, (b) Phase margin.

Fig. 8 shows the gain margin and the phase margin for the whole system with the proposed hybrid damper. It can be seen that the minimum gain margin is larger than 4 *dB* and the minimum phase margin is larger than 35 degree, which can meet the requirement for the engineering design method.



(a)



(b)

Fig. 9. Bode diagram of the two damping methods based system (a) with an *RC* parallel damper (b) with a proposed hybrid damper.

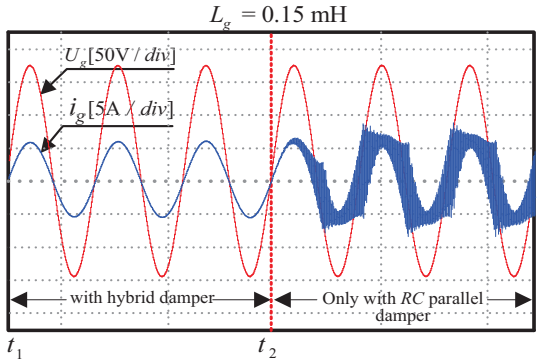
D. Comparison between the RC parallel damped LLCL-filter based system and the LLCL-filter based system with the hybrid damper

The Bode diagrams of the traditional *RC* parallel damped *LLCL*-filter based system and the *LLCL*-filter based system with the proposed hybrid damper are shown in Fig. 9 respectively. It can be seen that the system with the proposed damping method can be kept stable when the grid inductance varies in a wide range. However, the *RC* parallel damped *LLCL*-filter based system cannot and can only be kept stable under the weak grid condition.

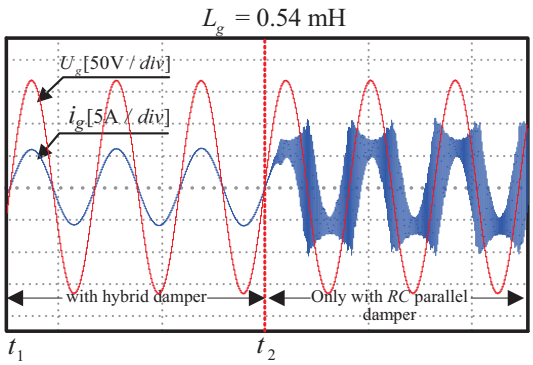
Note that the introduced design for the digital filter is a kind of normalized method. For different power ratings, the designed digital filter are the same, only if the modulation method, the current ratio, the switching frequency, the selection method for the *RC* parallel damper, the total delay and the normalized gain of the open-loop system of K_0 are the same. The grid-tied inverter system can always be kept stable while the grid-inductance varies in the range of $[0.002L_b, 0.065L_b]$. Certainly the proportionality coefficient of the *PR* regulator should be changed to keep the normalized gain of the open-loop system of K_0 to be a constant value.

IV. SIMULATIONS AND EXPERIMENTS

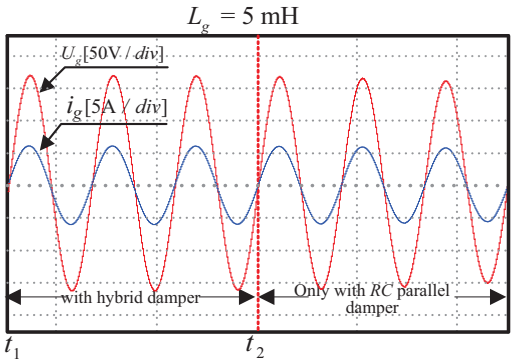
Simulations using PSIM software are carried out. All the parameters are the same as those for the theoretical analysis as listed in Table I. Based on the theoretical analysis and the simulations, a prototype of the single-phase full-bridge grid-tied inverter with the DSP (TMS320LF2812A) controller is constructed. The experiments are evaluated and investigated under the given conditions of f_s = 20 kHz, U_{dc} = 175 V, U_g =110 V/50 Hz, P = 500 W, the total delay is 0.75 T_s and the discontinuous unipolar PWM modulation method is adopted. The simulated and the measured grid voltages and currents of the *LLCL*-filter based inverter system are shown in Fig. 10 and Fig. 11 respectively.



(a)

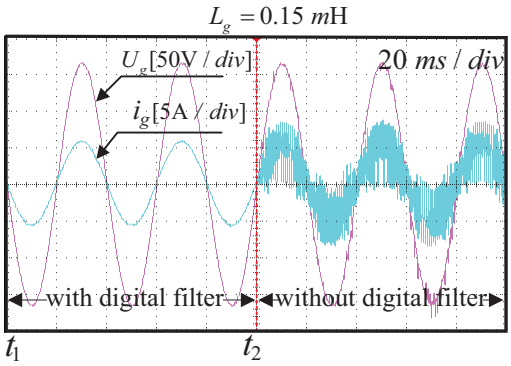


(b)

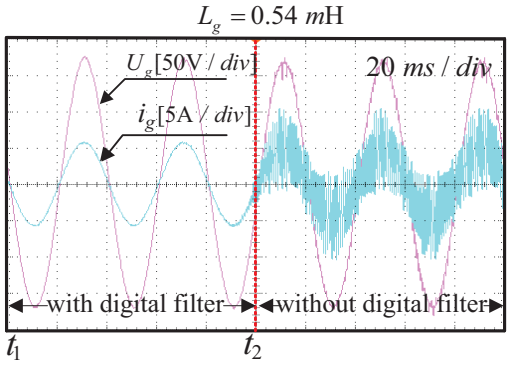


(c)

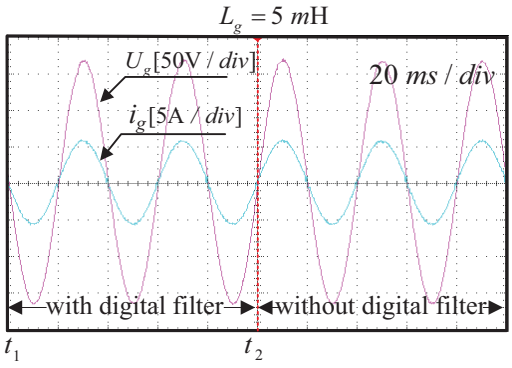
Fig. 10. Simulated grid voltages and currents of the *LLCL*-filter based system with the digital filter and the *RC* parallel damper when the digital filter is cut off at t_2 under (a) the stiff grid (L_g = 0.15 mH), (b) under the critical grid (L_g = 0. 54 mH), (c) under the weakest grid (L_g = 5 mH).



(a)



(b)



(c)

Fig. 11. Measured grid voltages and currents of the *LLCL*-filter based system with the digital filter and the *RC* parallel damper when the digital filter is cut off at t_2 (a) under the stiff grid (L_g = 0.15 mH), (b) under the critical grid (L_g = 0. 54 mH), (c) under the weakest grid (L_g = 5 mH).

As shown in Fig. 10 (c) and Fig. 11(c), it can be seen that in the weak grid state, both the conventional *RC* passive parallel damping and the proposed hybrid damping methods can keep the *LLCL*-filter based grid-tied inverter system stable. However, as shown in Fig. 10 (a), Fig. 10 (b), Fig. 11 (a) and Fig. 11 (b), under the stiff grid state and the critical grid condition, only the proposed hybrid damper based system can be kept stable, while the traditional *RC* passive parallel damped system cannot. Simulation and experimental results are in good agreement with the theoretical analysis.

V. CONCLUSION

In a power electronics based distribution power system, the stability of the grid-tied inverter system has been challenged due to the large variation of the grid inductance, especially when the *PR+HC* controller is adopted for a high-order filter based grid-tied inverter to resist the effect of the grid background harmonic voltages.

In order to overcome this problem, a new hybrid damping method employing a digital filter and an *RC* parallel damper has been proposed. The design of the proposed hybrid damper has been developed in details. The design is a normalized method and it is very convenient for future engineering design.

Compared with traditional composite passive damping method, the proposed hybrid damping method can save the total material, the cost and the power losses, certainly at the cost of more computing time. The simulations and experimental results on a 500 W, 110 V/ 50 Hz *LLCL*-filter based single-phase grid-tied inverter prototype with a wide variation of the grid inductance are in good agreement with the theoretical analysis.

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