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# A hybrid reference pulse width modulation technique for binary source multilevel inverter

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**ABSTRACT**

The article presents a seven-level reduced switch asymmetrical multilevel inverter with two different methods of pulse width modulation (PWM) techniques. Phase disposition (PD) PWM and hybrid variable-frequency phase disposition PWM (HVFPD-PWM) are the two different PWM methods for making the quality of output voltage waveform. In the first method, the unipolar sine reference with triangular carriers is used. In the second method, the hybrid unipolar reference (sinusoidal with trapezoidal) is proposed with variable frequency carriers to generate the switching pulses for asymmetric multilevel inverter (MLI). The main objective of this proposed method is to reduce the total harmonic distortion in the output voltage waveforms. A comprehensive comparison of the proposed HVFPD-PWM and the conventional PD-PWM with asymmetrical seven-level inverter is presented to show the enriched performances of the proposed method. The performance and viability of the suggested PWM are evaluated through simulation and experimental results using an asymmetrical seven-level inverter. The total harmonic distortion for the proposed PWM method (16.95%) is significantly reduced as compared with the conventional PWM method (18.01%) at the modulation index of one.



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## 1. INTRODUCTION

In latest past years, multilevel inverters (MLIs) are greatest key solutions for medium voltage and high-power energy conversion fields. A MLI with reverse voltage topology has been presented in [1] with fewer switching components. Moreover, the presented MLI utilize phase disposition-pulse width modulation (PD-PWM) scheme to obtain corresponding output voltage levels. However, the significance of PWM scheme is not discussed against performance factors. A seven-level hybrid inverter configuration with fundamental harmonic elimination switching scheme have been presented in [2]. However, the drawback of proposed topology is quite complex for higher number of voltage levels. The reduced flying capacitor MLI configuration has been presented in [3]. It has also introduced new phase shifted carrier PD-PWM technique. However, the proposed carrier based PWM technique requires (level-1) carriers and comparators for switching signal generation.

A new configuration of MLI has been presented in [4]–[6] with less number of power electronic components. The control signals for the switch are generated using bipolar sinusoidal PD-PWM scheme. However, harmonic distortions are analyzed only for fixed modulation index. Synchronous optimal PWM scheme has been presented with modular multilevel converter in [7]. However, the drawback of presented

scheme is low switching frequency, which leads higher harmonic distortion. Modulation scheme of any kind of MLI is quite challenging. The harmonic distortion of line-to-line output voltage is lowered by PD-PWM strategy. However, wide side band harmonics are presented in this technique [8], [9].

A detailed literature of various multicarrier PWM technique is presented in [10]. Moreover, modified reference and carrier signals are used to obtain the gating pulses. The modulation switching scheme is presented in [11]. However, the presented scheme is implemented only for cascaded MLI structure and harmonic performance alone studied for cascaded MLI. Sequential switching hybrid modulation scheme have been presented in [12]. However, the presented scheme is implemented only for cascaded MLI structure and harmonic performance are studied for cascaded MLI. The presents a new modulation strategy with modified reference signal to reduce the switching losses in [13], [14]. However, discontinuous PWM scheme have higher harmonic content in output voltage. A new hybrid modulation technique is proposed for cascaded H-bridge inverter and it can be stretched to any quantity of carriers for higher quantity of output stages in [15]. The seven-level modified inverter with level shifted and phase shifted PWM schemes has been presented in [16]. However (level-1) triangular carriers required to generate gating pulses. Level shifted techniques are often used to regulate and control the inverter [17]. Saw tooth carrier-based phase disposition PWM technique are presented in [14]. Moreover, this modified carrier signal reduces the switching loss due to removal of continuous switching transients. A new PWM techniques based on different carrier are presented in [18]. However, this new carrier based PWM techniques are not effective in terms of root mean square (RMS) voltage and harmonic distortion. The reduced switch asymmetrical multilevel inverter with different classical PWM techniques has presented in [19]–[21]. Modular seven level inverter configurations are proposed for grid connected photovoltaic (PV) system in [22], [23]. However, the proposed topology presented with conventional switching techniques. The reduced switch and source multilevel inverter for renewable power applications are proposed in [24]. However, the presented topology utilizes more number of switches and sources. Modified hybrid multilevel PWM are presented in [25]. However, it necessitates special setup to develop the PWM signal. The modified configuration inverters are presented in literature with conventional and modified PWM technique. Though, the inverter performance can be further enhanced in terms of total harmonic distortion (THD) and RMS voltage. Therefore, in this paper, hybrid carrier unipolar pulse width modulation named as hybrid variable frequency PD-PWM (HVFPD-PWM) is proposed to improve the performance over conventional methods. Hence, a comprehensive comparative analysis of VFPD-PWM and the classical PD-PWM is presented to show the superiority of suggested PWM technique.

## 2. SINGLE PHASE ASYMMETRICAL SEVEN LEVEL INVERTER

A circuit topology of seven level asymmetrical inverter [16] is depicted in Figure 1. The MLI comprises of two series connected sub-multilevel inverters with active power switches and direct current (DC) source as shown in Figure 1 to get positive polarity of output levels and a H-bridge cell is used to get output in both the polarity. The H-bridge is design in such a way that it should carry high voltage.

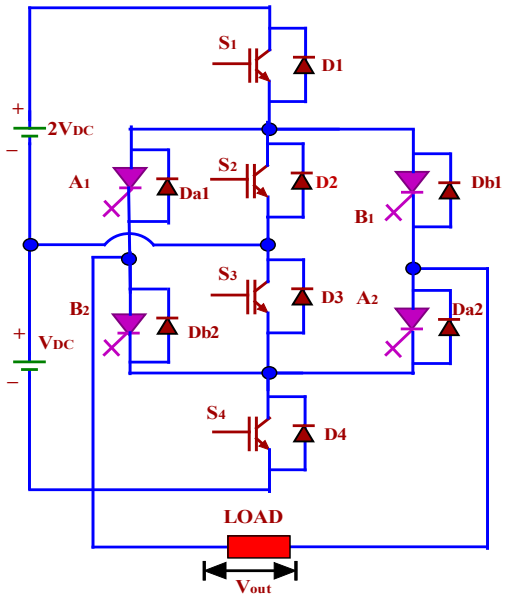



Figure 1. Single phase asymmetrical seven level inverter

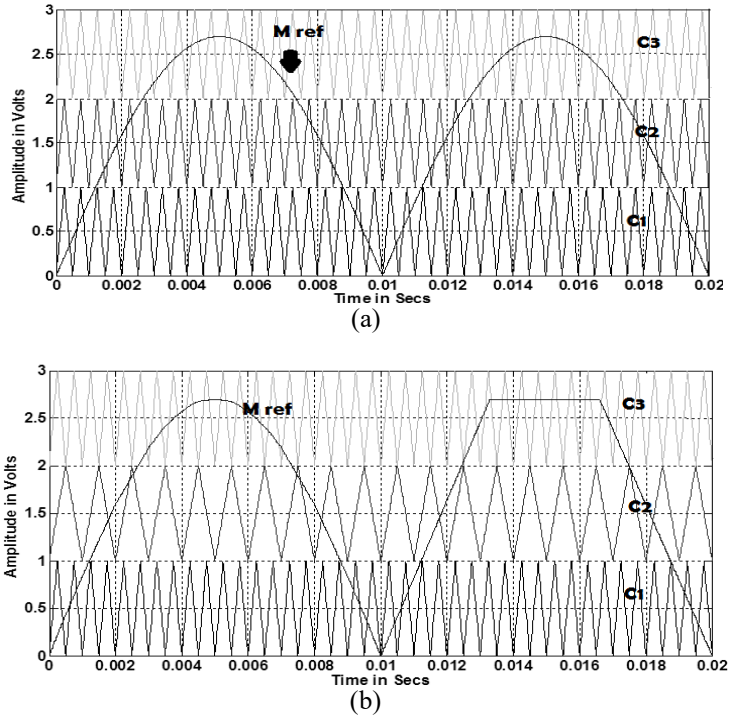
When the output voltage $V_{out}$ is $+V_{DC}$, the pair ($S_2$, $S_4$) and ($A_1$, $A_2$) are ON. When the output voltage Vout is $+2V_{DC}$, the pair ($S_1$, $S_3$) and (A1, A2) are ON. When the output voltage Vout is $+3V_{DC}$, the pair ($S_1$, $S_4$) and ($A_1$, $A_2$) are ON. The zero-output voltage is obtained when ($S_1$, $S_4$) and ($A_1$, $A_2$) are ON. In the same approach, the other levels $-V_{DC}$, $-2V_{DC}$, and $-3V_{DC}$ are generated. Table 1 shows the switching scheme with corresponding levels.

Table 1. Switching schemes with level of output

| S1 | S2 | S3 | S4 | A1 | A2 | B1 | B2 | Level of Output ($V_{DC}$) |
|---|---|---|---|---|---|---|---|---|
| ON | OFF | OFF | ON | ON | ON | OFF | OFF | +3 |
| ON | OFF | ON | OFF | ON | ON | OFF | OFF | +2 |
| OFF | ON | OFF | ON | ON | ON | OFF | OFF | +1 |
| OFF | ON | ON | OFF | ON | ON | OFF | OFF | 0 |
| OFF | ON | OFF | ON | OFF | OFF | ON | ON | -1 |
| ON | OFF | ON | OFF | OFF | OFF | ON | ON | -2 |
| ON | OFF | OFF | ON | OFF | OFF | ON | ON | -3 |

## 3. PD PWM AND HYBRID VFPD PWM STRATEGY

Figure 2(a) and Figure 2(b) depicts PD PWM and hybrid VFPD-PWM for seven level reduced switch inverter with unipolar PWM strategy. The unipolar PWM strategy requires half of the carrier signals compares with bipolar PWM strategy. In both PD PWM and VFPD-PWM cases, the modulating waveform has the amplitude of $M_{ref}$ and frequency is $F_{ref}$ but the carrier signal frequency $C_{freq}$ is chosen with respect to the slop of reference signal in respective band in HVFPD-PWM.




(a)

(b)

Figure 2. Carrier pattern for seven level inverter (a) PD-PWM and (b) HVFPD-PWM strategy

In PD-PWM, a rectified sinusoidal reference wave and three triangular carrier signals (C1-C3), with same frequency and same amplitude are disposed so that the bands they occupy are contiguous as shown in Figure 2(a). In the case of HVFPD-PWM strategy, combination of rectified sinusoidal and trapezoidal reference wave is used and three triangular carrier signals (C1-C3) with same amplitude is used. The carrier signal frequency is based on the slop of modulating wave in each band as shown in Figure 2(b).

The initial driving pulses are obtained by comparing modulating wave with carrier signals. Thereafter, switching pulses of the switches are executed from proper combination of logical gates. From Figure 3. It is observed that the comparator outputs are represented by $PW_1$ to $PW_3$. The switches S1 and S2

are alternatively driving by $PW_2$ and $\overline{PW}_2$, which is obtained by comparing carrier signal C2 and the reference signal $M_{ref}$. The switches S3 and S4 are driven by $PW_1$, $PW_2$, and $PW_3$ developed by comparing $M_{ref}$ with carriers C1 to C3 and using logical expression. The (A1, A2) and (B1, B2) switches are activated the based on the threshold comparison with reference wave Figure 3 shows pulse generation circuit built with logical gates.

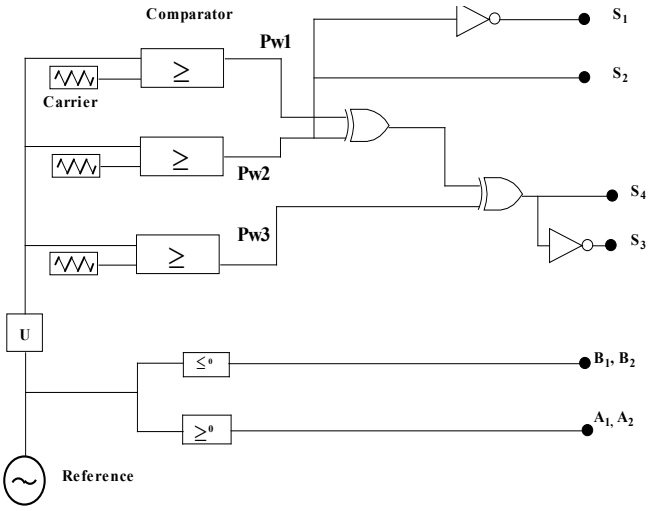



Figure 3. PWM generation circuit

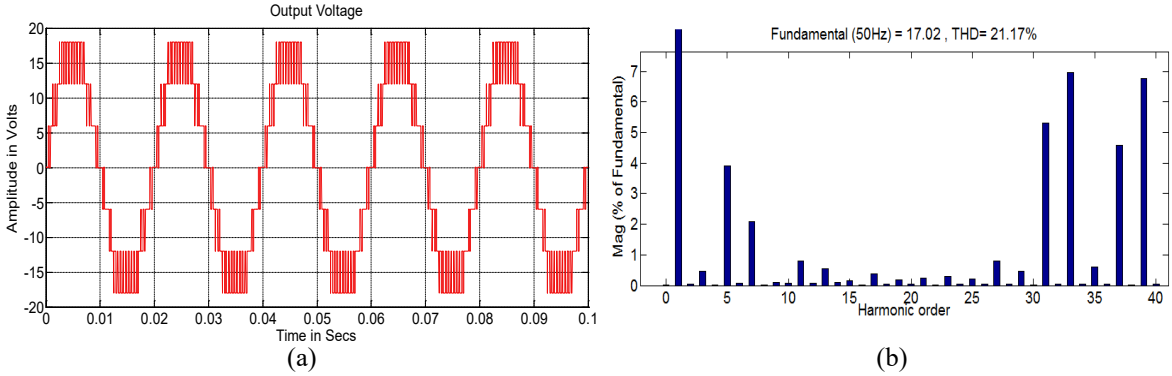
## 4. RESULTS AND DISCUSSION

This segment presents the simulation and experimental results for seven-level inverter [16] with PD-PWM and HVF-PWM. The simulation work has been done through the aid of MATLAB/Simulink. The experimental systems have been established to verify results with the aid of dSPACE RT110. The results present in the section are based on the parameters specified in Table 2.

The Figure 4(a) and Figure 4(b) depicts the feasibility of seven level output voltage waveform and corresponding % THD is 21.17 with modulation index of 0.9 using PD-PWM strategy using simulation results. Thus, the Figure 5(a) and Figure 5(b) shows resulting experimental seven level output voltage waveform and corresponding % THD is 21.3 respectively using PDPWM strategy. Moreover, the proposed HVFPD-PWM for seven level inverter is also confirmed with simulation and experimental results.

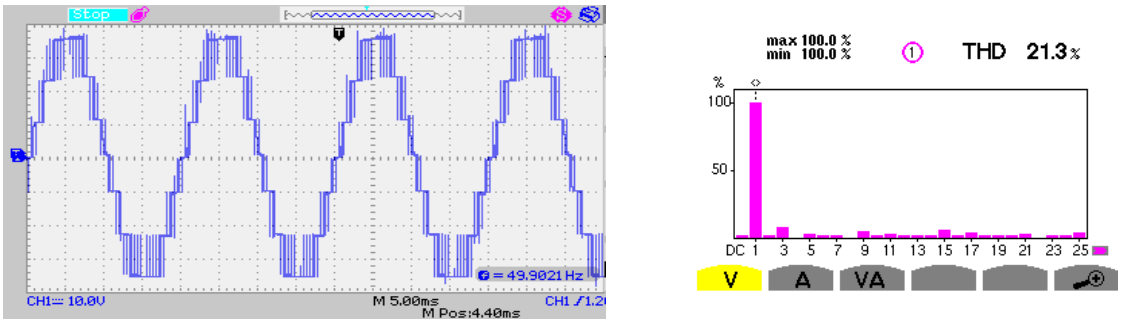
Table 2. Different parameters used for simulation and prototype

| Parameters | |
|---|---|
| Input Voltage Vin | 12 V |
| Modulation Frequency Fm | 50 Hz |
| Carier frequency Fc1 | 2000 Hz |
| Carier frequency Fc2 | 1000 Hz |
| Load | R=100 ohms and L=10 mH |




(a) (b)

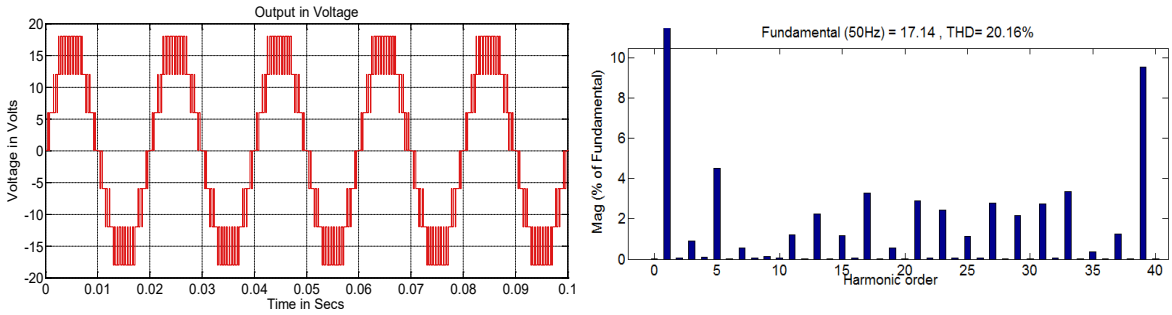
Figure 4. Simulated results with PD-PWM strategy (a) seven level output voltage waveform and (b) FFT




(a) (b)

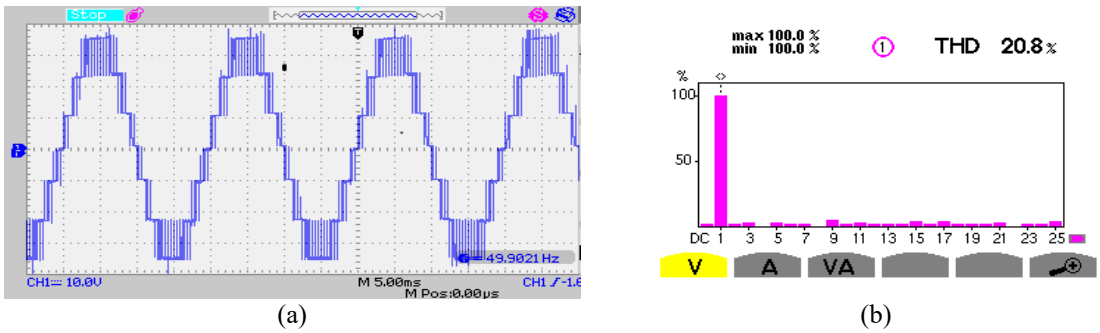
Figure 5. Experimental results with PD-PWM strategy (a) seven level output voltage waveform and (b) FFT

Simulation and experimental results for HVFPD-PWM are presented in Figures 6 and 7. The Figures 6(a) and 6(b) depicts the feasibility of seven level output voltage waveform and corresponding % THD is 20.16 with modulation index of 0.9 using HVFPD-PWM strategy using simulation results. Thus, the Figures 7(a) and 7(b) shows resulting experimental seven level output voltage waveform and corresponding % THD is 20.85 using HVFPD-PWM strategy. Table 3 and Figure 8(a) displays the harmonic content of the voltage with PD-PWM and HVFPD-PWM, it is observed that HVFPD-PWM provide lower THD than PD-PWM strategy. From Figure 8(b) and Table 4 it is noticed that RMS output voltage is higher in HVFPD-PWM strategy. Figure 8(c) shows % distortion magnitude for $m_a$=0.9, the following observations were made from Figure 8(c): 1) Lower and upper side bands (mf±1) appear in HVFPD-PWM strategies; 2) Lower and upper side bands (2 mf ± 1) appear very less in all strategies; 3) Harmonics present in center frequency mf, is slightly higher in PD-PWM strategy; and 4) 3rd order harmonics is not dominant both the strategies.




(a) (b)

Figure 6. Simulated results with HVFPD-PWM strategy (a) seven level output voltage waveform and (b) FFT




(a) (b)

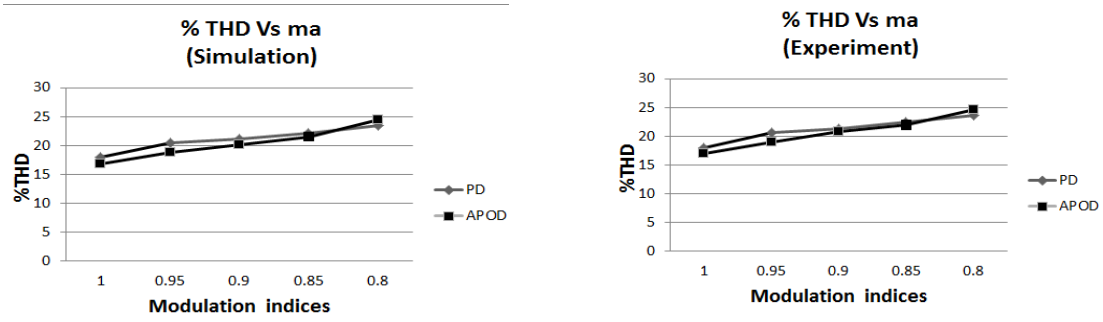
Figure 7. Experimental results with HVFPD-PWM strategy (a) seven level output voltage waveform and (b) FFT

Table 3. % Total harmonic distortion

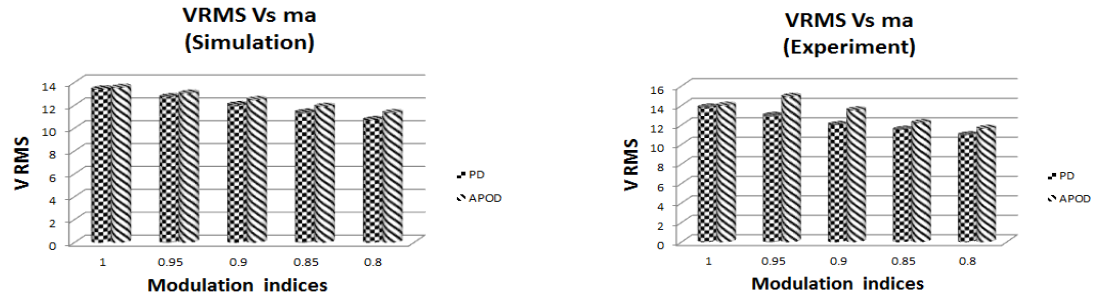
| $m_a$ | Simulation | | Experimentation | |
|---|---|---|---|---|
| | PD PWM | HVFPD PWM | PD PWM | VF PWM |
| 1 | 17.95 | 16.81 | 18.01 | 16.95 |
| 0.95 | 20.40 | 18.84 | 20.60 | 18.91 |
| 0.9 | 21.17 | 20.16 | 21.31 | 20.85 |
| 0.85 | 22.13 | 21.53 | 22.45 | 21.96 |
| 0.8 | 23.44 | 24.51 | 23.65 | 24.65 |

Table 4. VRMS (fundamental) for different modulation indices

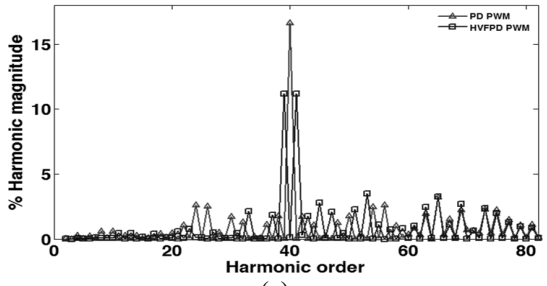
| $m_a$ | Simulation | | Experimentation | |
|---|---|---|---|---|
| | PD PWM | HVFPD PWM | PD PWM | HVFPD PWM |
| 1 | 13.4 | 13.54 | 13.81 | 14 |
| 0.95 | 12.72 | 13.03 | 12.96 | 14.9 |
| 0.9 | 12.03 | 12.47 | 12.01 | 13.52 |
| 0.85 | 11.37 | 11.88 | 11.52 | 12.2 |
| 0.8 | 10.72 | 11.32 | 10.95 | 11.62 |




(a)




(b)




(c)

Figure 8. Various parameters for different modulation indices by simulation results as well as experimental (a) % total harmonic distortion, (b) fundamental RMS voltage, and (c) % distortion magnitude

## 5. CONCLUSION

The operation of the asymmetric seven-level MLI has verified with two different PWM methods such as unipolar sine reference with phase disposition carriers PWM and proposed PWM. The proposed PWM has the hybrid unipolar reference (sinusoidal with trapezoidal) with variable frequency carriers. The performance of the asymmetric MLI has verified by using the simulation results and it has verified by the experimental results. The proposed PWM method has provided better results as compared with the convention PWM method in both simulation and experimental results. The comparison of simulation and experimental results has made to check the feasibility of the proposed PWM method. The proposed PWM provides the quality of output voltage with lower harmonic distortion and higher RMS voltage. From the results, it has evident that the total harmonic distortion for the proposed PWM method (16.95%) has significantly reduced as compared with the conventional PWM method (18.01%) at the modulation index of one.

## REFERENCES


[1] E. Najafi and A. H. M. Yatim, "Design and Implementation of a New Multilevel Inverter Topology," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 11, pp. 4148–4154, November 2012, doi: 10.1109/TIE.2011.2176691.

[2] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter," in *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 25–33, January 2009, doi: 10.1109/TPEL.2008.2006678.

[3] Z. Lim, A. I. Maswood, and G. H. P. Ooi, "Modular-Cell Inverter Employing Reduced Flying Capacitors with Hybrid Phase-Shifted Carrier Phase-Disposition PWM," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4086–4095, July 2015, doi: 10.1109/TIE.2014.2378753.

[4] C. -H. Hsieh, T. -J. Liang, S. -M. Chen, and S. -W. Tsai, "Design and Implementation of a Novel Multilevel DC–AC Inverter," in *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2436–2443, May–June 2016, doi: 10.1109/TIA.2016.2527622.

[5] V. Arun and N. Prabaharan, "Induction Motor Drive with Trinary DC Source Asymmetrical Inverter," *International Journal of Recent Technology and Engineering*, vol. 8, no. 2, pp. 5484–5490, July 2019, doi: 10.35940/ijrte.B2527.078219.

[6] A. Iqbal, M. D. Siddique, B. P. Reddy, and P. K. Maroti, "Quadruple Boost Multilevel Inverter (QB-MLI) Topology with Reduced Switch Count," in *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7372–7377, July 2021, doi: 10.1109/TPEL.2020.3044628.

[7] A. Edpuganti and A. K. Rathore, "Optimal Pulsewidth Modulation of Medium-Voltage Modular Multilevel Converter," in *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3435–3442, July-August 2016, doi: 10.1109/TIA.2016.2536585.

[8] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858–867, August 2002, doi: 10.1109/TIE.2002.801073.

[9] N. Prabaharan, V. Arun, T. Chinnadurai, K. Arulkumar, A. R. A. Jerin, and K. Palanisamy, "Analysis Of Symmetric Multilevel Inverter Using Unipolar Pulse Width Modulation For Photovoltaic Application," *Comptes rendus de l'Acad´emie bulgare des Science*s, vol. 71, no. 2, pp. 252–260, 2018, doi: 10.7546/CRABS.2018.02.13.

[10] C. Rech and J. R. Pinheiro, "Impact of Hybrid Multilevel Modulation Strategies on Input and Output Harmonic Performances," in *IEEE Transactions on Power Electronics*, vol. 22, no. 3, pp. 967–977, May 2007, doi: 10.1109/TPEL.2006.890010.

[11] S. Kouro, P. Lezana, M. Angulo, and J. Rodriguez, "Multicarrier PWM With DC-Link Ripple Feedforward Compensation for Multilevel Inverters," in *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 52–59, January 2008, doi: 10.1109/TPEL.2007.911834.

[12] C. Govindaraju and K. Baskaran, "Efficient Sequential Switching Hybrid-Modulation Techniques for Cascaded Multilevel Inverters," in *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1639-1648, June 2011, doi: 10.1109/TPEL.2010.2089064.

[13] K. P. Panda, P. R. Bana, and G. Panda, "A Reduced Device Count Single DC Hybrid Switched-Capacitor Self-Balanced Inverter," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 978–982, March 2021, doi: 10.1109/TCSII.2020.3018333.

[14] Z. Zhang, O. C. Thomsen, and M. A. E. Andersen, "Discontinuous PWM Modulation Strategy with Circuit-Level Decoupling Concept of Three-Level Neutral-Point-Clamped (NPC) Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1897–1906, May 2013, doi: 10.1109/TIE.2012.2227901.

[15] A. Ghazanfari, H. Mokhtari, and M. Firouzi, "Simple Voltage Balancing Approach for CHB Multilevel Inverter Considering Low Harmonic Content Based on a Hybrid Optimal Modulation Strategy," in *IEEE Transactions on Power Delivery*, vol. 27, no. 4, pp. 2150–2158, October 2012, doi: 10.1109/TPWRD.2012.2205277.

[16] A. Tsunoda, Y. Hinago, and H. Koizumi, "Level- and Phase-Shifted PWM for Seven-Level Switched-Capacitor Inverter Using Series/Parallel Conversion," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 4011–4021, August 2014, doi: 10.1109/TIE.2013.2286559.

[17] M. Narimani, B. Wu, and N. R. Zargari, "A Novel Five-Level Voltage Source Inverter with Sinusoidal Pulse Width Modulator for Medium-Voltage Applications," in *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1959–1967, March 2016, doi: 10.1109/TPEL.2015.2440656.

[18] Z. Lim, A. I. Maswood, and G. H. P. Ooi, "Common-Mode Reduction for ANPC With Enhanced Harmonic Profile Using Interleaved Sawtooth Carrier Phase-Disposition PWM," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7887–7897, December 2016, doi: 10.1109/TIE.2016.2592459.

[19] M. Aly, E. M. Ahmed, and M. Shoyama, "Thermal Stresses Relief Carrier-Based PWM Strategy for Single-Phase Multilevel Inverters," in *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9376–9388, December 2017, doi: 10.1109/TPEL.2017.2654490.

[20] N. Prabaharan, V. Arun, P. Sanjeevikumar, L. Mihet-Popa, and F. Blaabjerg, "Reconfiguration of a Multilevel Inverter with Trapezoidal Pulse Width Modulation," *Energies*, vol. 11, no. 8, p. 2148, 2018, doi: 10.3390/en11082148.

[21] V. Arun, B. Shanthi, and M. Arumugam, "Analysis of binary DC source reduced switch 7-level inverter," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 6, no. 1, pp. 70–76, March 2015, doi: 10.11591/ijpeds.v6.i1.pp70-76.

[22] R. Kumar, P. Kant and B. Singh, "Modified PWM Technique for a Multi-Pulse Converter Fed Multilevel Inverter Based IM Drive," in *IEEE Transactions on Industry Applications*, vol. 57, no. 6, pp. 6592–6602, November–December 2021, doi: 10.1109/TIA.2021.3111147.

[23] N. Sujitha, P. S. Subudhi, S. Krithiga, S. Angalaeswari, T. Deepa, and D. Subbulekshmi, "Grid tied PV system using modular multilevel inverter," *International Journal of Power Electronics and Drive System (IJPEDS),* vol. 10, no. 4, pp. 2013–20, December 2019, doi: 10.11591/ijpeds.v10.i4.pp2013-2020.

[24] V. Arun and N. Prabaharan, "Micro controller based asymmetrical multilevel inverter," *International Journal of Robotics and Automation (IJRA)*, vol. 8, no. 1, pp. 18–25, March 2019, doi: 10.11591/ijra.v8i1.pp18-25.

[25] Seong-Cheol Kim, S. Narasimha, and S. R. Salkuti, "A new multilevel inverter with reduced switch count for renewable power applications," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 11, no. 4, pp. 2145–2153, December 2020, doi: 10.11591/ijpeds.v11.i4.pp2145-2153.

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