A HYBRID THERMOELECTRIC COOLER THERMAL MANAGEMENT SYSTEM FOR ELECTRONIC PACKAGING

A HYBRID THERMOELECTRIC COOLER THERMAL MANAGEMENT SYSTEM FOR ELECTRONIC PACKAGING

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ABSTRACT

Conventional cooling techniques, such as the use of heat pipes and forced convective cooling can be inadequate for many high performance electronic chips or when the operating ambient temperature is high. In such cases, there is a need for active cooling of the chip to keep its operating temperature below the design point. Thermo-Electric coolers (TEC) provide an attractive option in such instances and have been developed and used for thermal management in electronic packaging systems. Such systems, however, can have a low overall coefficient of performance since the TEC needs to be kept on even at low heat load conditions. In this thesis a hybrid thermal management system is considered that incorporates a TEC based active path in parallel with a conventional heat pipe based passive path. A thermal resistance network model is developed for the hybrid system that takes into account the governing thermo-physical equations for the TEC. The advantage of this hybrid system is that the passive path can transport the heat from the chip at moderate thermal conditions keeping the TEC electrically off while the TEC modules can be turned on when the conditions become adverse. A higher overall system coefficient of performance can be achieved compared to a system consisting of only TEC module(s). One important design parameter is the fraction of the total heat sink area dedicated to each path, which will depend on the rated heat dissipation from the chip, thermal resistance of the entire heat sink and the operational ambient temperature. Controlled experiments were performed to validate the hybrid thermal management model for an example case of electronic package. The experimental facility consisted of a flexible heater to simulate the chip. The heat sink in the experiments was a cooling loop and the ambient temperature was

controlled by changing the temperature of the water flowing through the cooling loop. The thermal resistance of the heat sink was simulated by acrylic glass. Experiments were performed for different fraction of the heat sink area dedicated to the heat transfer paths for a range of ambient temperatures. An operating envelope was presented to compare different hybrid thermal management configurations with a heat pipe based passive system and an only TEC system. The model predictions were in good agreement with the experimental results. Parametric studies were performed to analyze the effect of different variables on the system performance. The hybrid model can be used for other thermal management systems involving TEC modules.

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NOMENCLATURE

Symbols

A	Cross-sectional area, surface area (m^2)
C_p	Specific heat of water ($JKg^{-1}K^{-1}$)
COP	Coefficient of performance
g	Direction of gravity force
G	Geometric factor (m)
h	Heat transfer coefficient ($Wm^{-2}K^{-1}$)
I	Applied electric current (A)
k	Thermal conductivity ($Wm^{-1}K^{-1}$)
K	Thermal conductance (WK^{-1})
L	Length (m)
$\dot{m}$	Mass flow rate of water (Kg/s)
n	Number of TEC modules
N	Number of thermo-couples in a TEC module
P_{in}	Input power to TEC (W)
Q	Heat load, transfer, flow (W)
r_C	Fraction of heat sink area dedicated to conventional passive path
R	Thermal resistance (°C/W)
R_{el}	Electric resistance of one thermo-couple (Ω)
t	Thickness, length (m)
T	Temperature (°C, K)
u'''	Energy generation per unit volume (W/m^3)
V	Voltage (V)
x	Spatial co-ordinate
Δ	Difference

Greek Symbols

α	Seebeck coefficient of one thermo-couple (V/K)
η	Charge carrier concentration (cm^{-3})
π	Peltier constant of one thermo-couple (V)
ρ	Electrical resistivity of n or p-type thermo-element (Ω.m)
σ	Electrical conductivity ($Sm^{-1} = \Omega^{-1}m^{-1}$)
τ	Thomson constant (V/K)

Subscripts

amb	Ambient
c	Cold side

chip	Chip
C	Conventional passive path
design	Design value of chip
fin	Finned heat sink
h	Hot side
HP	Heat pipe
i	Inlet, iteration number
in	Inside, input
max	Maximum
mean	Mean, average
min	Minimum
n	n-type semiconductor
o	Outlet
opt	Optimum
out	Outside, output
p	p-type semiconductor
P	Peltier effect
sub	Substrate
sys	System
tot	Total
T	TEC based active path, Thomson effect
TE	Thermo-element
TEC	Thermo-electric cooler
∞	Ambient, infinity

Chapter 1 INTRODUCTION

Since the advent of the Integrated Circuit (IC) by Kilby at Texas Instruments and Noyce at Fairchild Semiconductors in 1959 (Hanson, 1982), the packaging density of electronics has continued to increase. Over the last decade electronic circuitry has significantly been improved in terms of miniaturization. This is particularly evident in microprocessors where the number of micro transistors on a single die has increased from 10^6 to 10^9. As a result, more electrical energy is required to make them functional with a resultant increase in heat dissipation. Multi-core microprocessors are projected to dissipate a heat flux ranging from 10 to 50 W/cm^2 while power electronics or laser semiconductors are projected to dissipate over 100 W/cm^2 of heat flux (DTI report, 2006). For example, heat dissipation from a high performance single chip is predicted to be 183 W by 2014 (Phelan et al., 2002). Processors must operate below its safe design temperature which is typically 100 °C (DTI report, 2006), beyond which permanent failure may occur. The safe design temperature of the chip is not expected to increase in the electronics industry to keep pace with the increasing trend of the chip rated power (Krueger and Bar-Cohen, 2004). Over-heating of the chip can drastically deteriorate the chip performance and

shorten its lifetime (Kock and Visser, 2004). The reliability of the chip was found to decrease by 10% for every 2 °C increase above its safe design temperature (Bar-Cohen et al., 1983).

Thermal management of the electronic packages at elevated ambient temperature is becoming a challenge for thermal designers. Several cooling techniques have been developed to dissipate more heat from a chip and to maintain the functionality of the electronic packages. These cooling methods are usually limited by several factors such as size, shape and form factor of the packaging. One commonly used cooling method for electronic packaging is forced convection air cooling with extended surface heat sinks. In typical computers, fans are used to force air past a finned heat sink to remove heat from the chip and other fans to move cool air into and hot air out of the case (Saini and Webb, 2003). Such solutions, however, can be inadequate when the electronic packaging is operated in a high temperature ambient environment or if high performance chips are used in the packaging. Liquid cooling has been proposed for high heat dissipation rates from the chip. Zhang et al. (2003) reported a heat dissipation of 140 to 170 W using liquid cooling through a miniaturized aluminum heat sink with micro channels.

There are other applications such as sealed computers (Figure 1.1) where fans cannot be used to move fresh air in or hot air out of the case because of the nature of the casing. The cooling system in this computer typically consists of a heat pipe unit that transports the heat from the heat generating components to the finned case wall. The fins on the outside of the case allow the heat to be dissipated to the surroundings via natural convection. Sealed computers are used for specific purposes such as in industrial

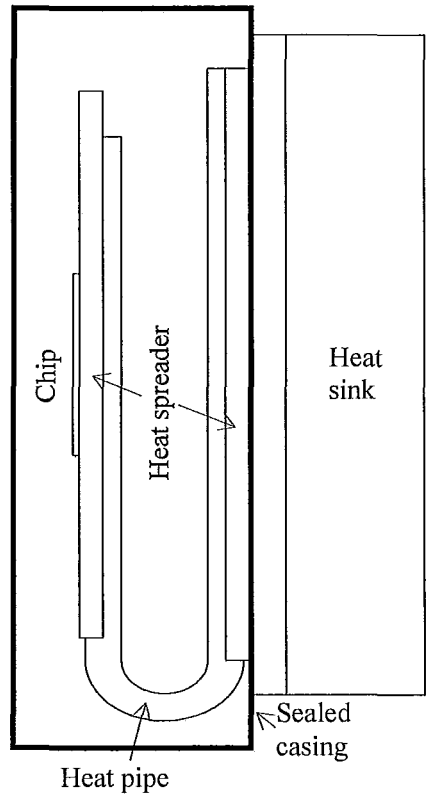


Figure 1.1: Schematic of a sealed computer.

environments where contaminant particles can accumulate on sensitive electronic components, in special vehicles such as police cars, military vehicles and coast guard ships. In such applications, refrigeration cooling using thermoelectric coolers (TEC) have been adopted to keep the chip temperature below its design point. Thermoelectric coolers (TEC) are an attractive option in such instances, and have been developed and used for thermal management in electronic packaging systems for years. B eing a solid state device, it overcomes the orientation effect of heat pipes (Loh et al., 2005, Russel el al., 2011) and provides high reliability (Riffat and Ma, 2003) and control in cooling the chip. Its smaller size and weight, noise free operation, absence of any moving parts make it advantageous over other cooling methods.

Typically, the cold side of the thermoelectric cooler (TEC) is in contact with the chip to maintain the chip temperature below its design temperature with natural or forced convection at the hot side of the TEC to transport the heat from the chip and the applied power to the TEC module to the ambient. The heat load from the processor will typically fluctuate over time and will depend on its operation. At moderate processor heat load and moderate ambient temperatures, a passive thermal management system such as use of heat pipes would be sufficient to transport the heat from the chip to the ambient. However, at high ambient temperatures or high heat load, such a system may fail to maintain the chip below its safe operating temperature. If only a TEC based system is used in this circumstance, the TEC module will have to be kept electrically on even at moderate operating conditions because of its high thermal resistance at the electrically off mode which would result in a low system coefficient of performance (COP_{sys}).

The objective of this research is to develop a hybrid thermal management system that incorporates a TEC based active path in parallel with a conventional heat pipe based passive path (Figure 1.2). The passive path consists of a heat pipe unit and a finned heat sink where the TEC based active path consists of TEC module(s), a heat pipe unit and a second finned heat sink. The two heat sinks associated with the two parallel paths are thermally isolated from each other. The proposed hybrid system utilizes the passive path at moderate heat loads at moderate ambient conditions while at higher ambient temperatures or high processor heat loads, the thermoelectric cooler will be electrically turned on with the necessary amount of current to keep the chip temperature below its safe operating temperature. Use of this hybrid system will improve the performance of the system in two

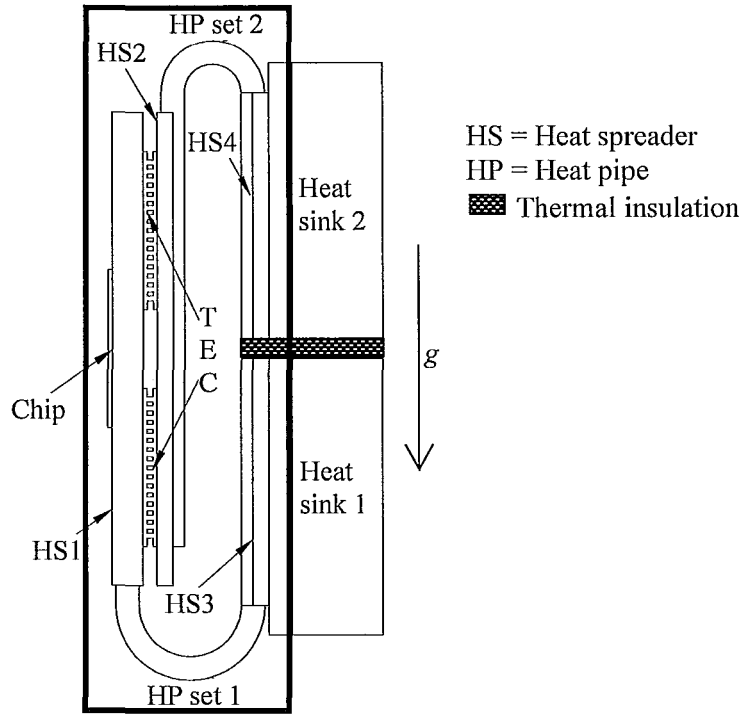


Figure 1.2: Schematic of the hybrid thermal management system.

ways: (a) the operating envelope will be extended at higher ambient temperature and (b) the COP_{sys} will be improved compared to an only TEC based thermal management system. A thermal resistance network model is developed for the hybrid system that takes into account the governing equations of the TEC modules. An experimental facility was developed to simulate different practical conditions for the hybrid system and to validate the predictions of the thermo-physical model.

This thesis is divided into six chapters. Chapter 2 provides background on thermoelectric cooler (TEC) modules, their operating principles, different studies performed previously on TEC systems and finally natural and forced convection at the heat sink. The modeling of the proposed hybrid system is presented in Chapter 3. Chapter 4

outlines the experimental set up and methodology used for the experiments. The results of the experimental findings are presented and discussed in Chapter 5. The model predictions are compared with the experimental results. Chapter 6 summarizes the work and provides recommendations for continuation of this project. The appendix of the thesis contains information on the thermo-physical properties of the TEC material and different parametric studies.

Chapter 2 LITERATURE REVIEW

There are several methods of cooling electronic packaging depending on the application. The cooling techniques can be classified broadly into two classes: (i) Passive and (ii) Active techniques. Passive techniques can be defined as those where no external power is required for cooling the electronic packages where active techniques require external power to cool the electronics (Baily, 2008). There are three scales of cooling for computer products: (i) Module level cooling, (ii) System Cooling and (iii) Data centre cooling (Chu et al., 2004). Module level cooling refers to cooling the chip, system level cooling refers to the entire electronic package and data centre cooling refers to cooling the rooms where computers and telecommunications equipment are stored. The research in this project will focus on the system level cooling using a hybrid thermal management system which involves thermoelectric cooler (TEC) modules, heat pipes and an air cooled heat sink. The components of the hybrid system along with other cooling techniques, both active and passive, adopted in electronics cooling are reviewed in the following sections.

2.1. THERMOELECTRIC COOLER (TEC)

A typical thermoelectric module consists of a number of thermocouples sandwiched between two layers of ceramic substrates. The ceramic substrates should ideally have a very high thermal conductivity so that there is minimal temperature drop across the layer of the substrate but very low electrical conductivity to avoid any leakage current flow through the substrate. A schematic of the construction of a typical TEC module is shown in Figure 2.1. Detailed descriptions of thermoelectric module operation and applications can be found in Ioffe (1957), Gray (1961), Goldsmid (1961). Thermoelectric cooling is achieved with the penalty of DC current supply through one or a series of thermocouples electrically connected in series but thermally in parallel. The schematic of a single thermocouple which consists of one n and one p-type semiconductor material, also known as a thermo-element with its operating principle is shown in Figure 2.2. In the n and p type semiconductors there exist excess electrons and holes respectively. With the electric polarity shown in Figure 2.2, electrons in p and n-type material flow from bottom to top and from top to bottom respectively, thus resulting in a clockwise electron flow or counter clockwise current flow through this circuit. Heat is absorbed at the top and released at the bottom of the schematic shown in Figure 2.2. If the polarity is changed, the hot and cold junction as well as the heat absorption and rejection will interchange. There are three important thermoelectric effects that have been known since the nineteenth century: (i) Seebeck effect, (ii) Peltier effect and (iii) Thomson effect.

Seebeck in 1821 discovered that, when a temperature difference is maintained at the two junctions of a thermocouple composed of two dissimilar conductors, a voltage is

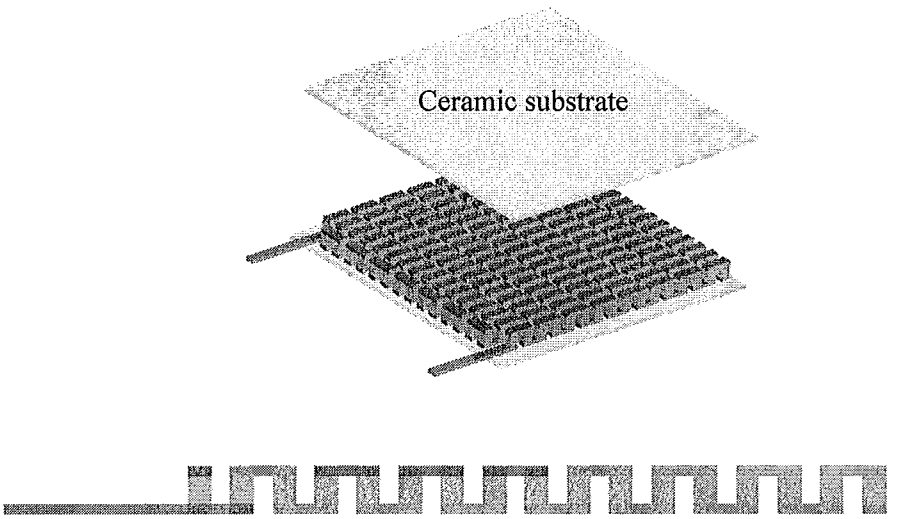


Figure 2.1: Schematic of a typical thermoelectric module.

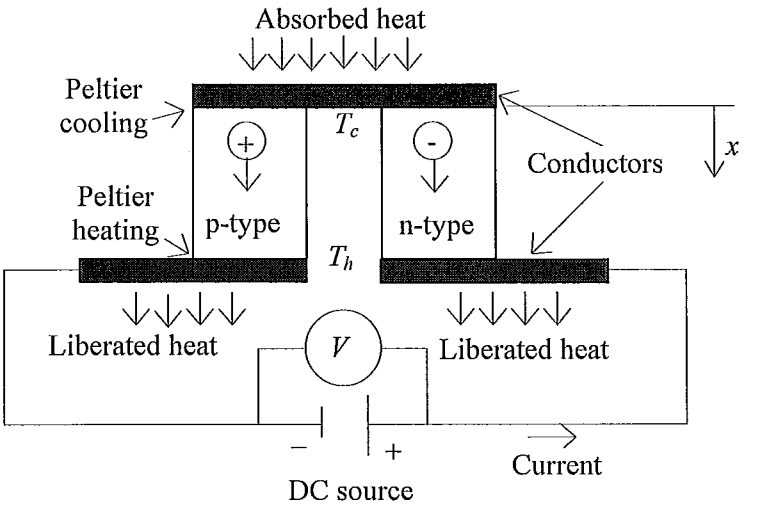


Figure 2.2: Schematic of thermoelectric module operation.

generated at the two terminals of the thermocouple as shown in Figure 2.3. The generated voltage is proportional to the temperature difference between the junctions and leads to the definition of the Seebeck coefficient, α_{AB} as

$$\alpha_{AB}(T) = \frac{\Delta V}{\Delta T} \qquad 2.1$$

The Seebeck coefficient depends on the materials A and B. A couple in a thermoelectric module is made of one n and one p-type semiconductor where the Seebeck coefficient α_{pn} is expressed as $\alpha_{pn} = \alpha = \alpha_p - \alpha_n$. Here α_p and α_n are the absolute Seebeck coefficient of p and n-type semiconductor respectively with respect to a superconductor (having zero Seebeck coefficient). Goldsmid (1961) presented Seebeck coefficients of n and p type bismuth telluride (Bi_2Te_3) at room temperature as a function of electrical conductivity which is reproduced in Figure 2.4.

The concentration of the charge carriers (electrons in n and holes or protons in p type semiconductors) depends upon the temperature. When there is a temperature gradient, negative charge carriers or electrons in n and positive charge carriers or holes in p-type semiconductors flow from the hot junction to the cold junction and thus produces an electron flow through the circuit when shorted and a voltage at open circuit condition.

Peltier in 1834 observed that, when an electric current flows through a junction composed of two dissimilar materials heat is either absorbed from the surrounding or dissipated to the surrounding at the junction as shown in Figure 2.5. The amount of heat absorbed or liberated at the junction is directly proportional to the electric current, I and related as

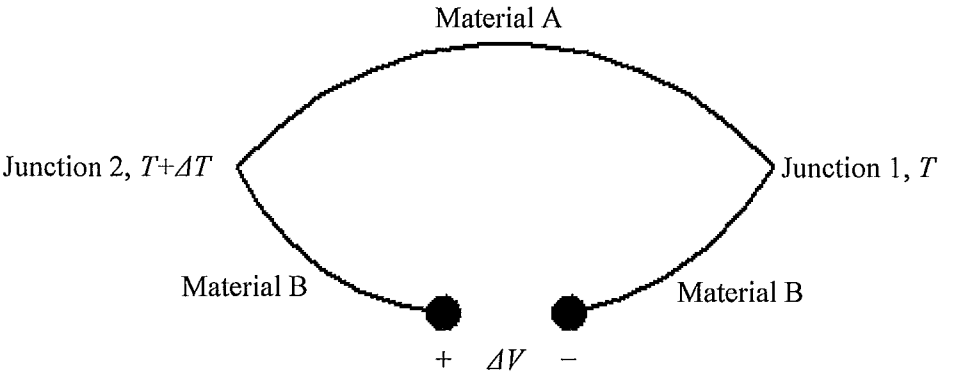


Figure 2.3: Schematic of basic thermocouple demonstrating Seebect effect (Gray, 1961).

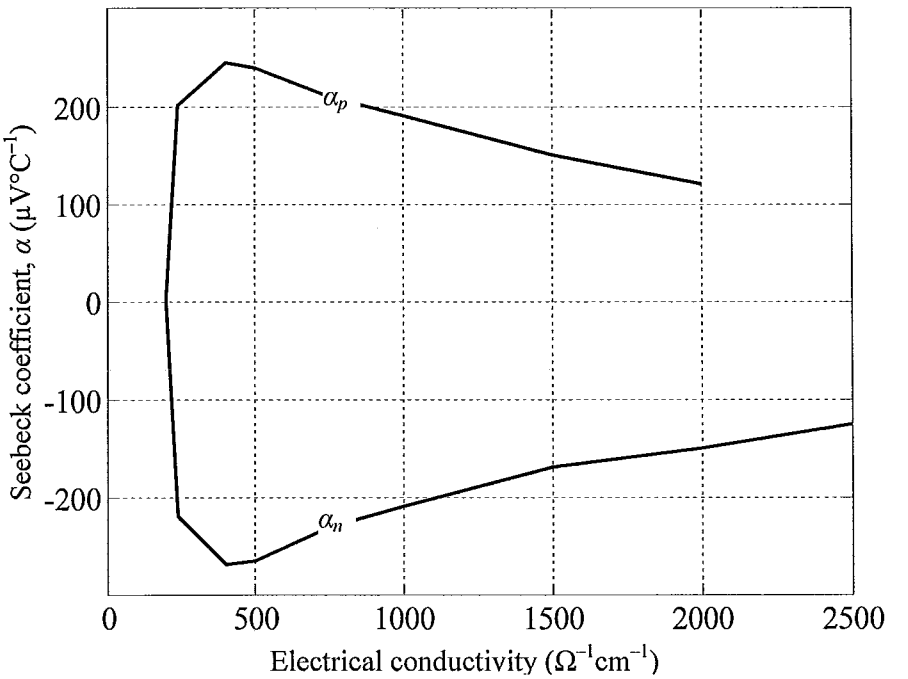


Figure 2.4: Seebeck coefficient of Bi_2Te_3 at room temperature (Goldsmid, 1961).

$$Q = \pi_{AB}(T) I \qquad 2.2$$

where $\pi_{AB}(T)$ is the temperature dependent proportionality constant and known as Peltier constant. The Peltier constant is related to the Seebeck coefficient as

$$\alpha_{AB} = \frac{\pi_{AB}}{T} \qquad 2.3$$

where T is the absolute temperature of the junction.

The potential energy of the charge carriers in different materials is different. The Peltier effect occurs at the junctions due to the difference in the energy levels in two dissimilar materials. For the polarity shown in Figure 2.2, at the cold junction heat is absorbed by the electrons as they move from a low energy level in the p-type to a high energy level in the n-type semiconductor. This consequently causes the holes in the p-type semiconductor to move in the opposite direction of the electron flow, i.e. toward the hot end. The electrons in the n-type semiconductor also move toward the hot end. Both the electrons and the holes carry thermal energy. So, the result is a net flow of heat from the cold end to the hot end where the heat is rejected due to the difference in energy levels.

Thomson in 1857 observed that when an electric current flows through a single homogeneous conductor in the presence of a temperature gradient in that conductor, the conductor exchanges energy with the surrounding. This phenomenon is illustrated in Figure 2.6. The direction of energy interchange between the conductor and the surrounding will depend on the direction of the temperature gradient and the direction of charge carrier in the conductor. The amount of heat absorbed or dissipated per unit length of the conductor is proportional to the current and the temperature gradient and is expressed as

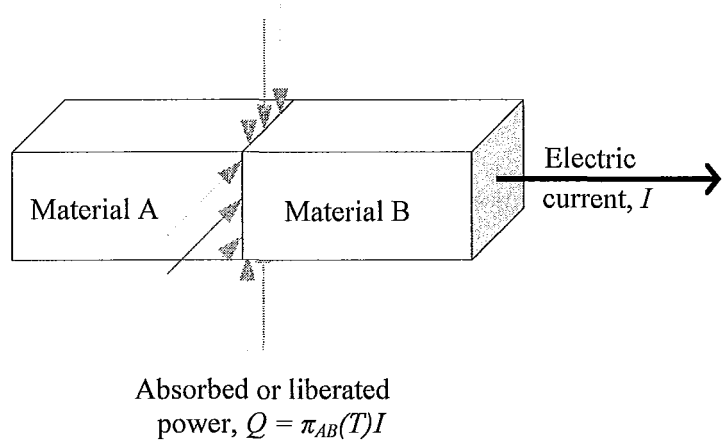


Figure 2.5: Schematic of a thermocouple demonstrating Peltier effect (Gray, 1961).

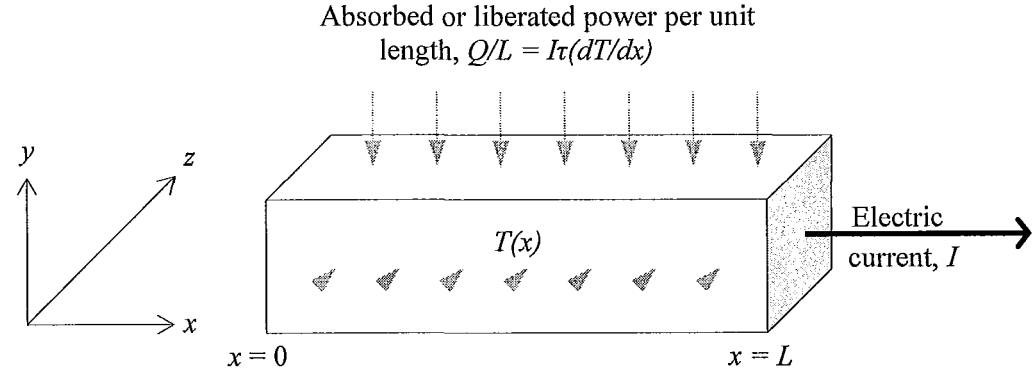


Figure 2.6: Schematic illustrating Thomson effect (Gray, 1961).

$$\frac{Q}{L} = I\tau\frac{dT}{dx} \qquad 2.4$$

where τ is the Thomson coefficient which is related to the Seebeck coefficient as

$$\frac{d\alpha}{dT} = \frac{\tau}{T} \qquad 2.5$$

The Thompson effect is reported as a second order effect in thermoelectric cooling as the heat flow due to this effect depends upon the product of the current and the temperature gradient (Gray, 1961). The Thomson effect has also been reported to be small (Ioffe, 1957, Goldsmid, 1961, Soo, 1968) and thus usually neglected in thermoelectric cooling or heating. The manufacture's specification (Melcor) of the thermo-element was used to determine the importance of the Thomson effect and is described in APPENDIX A. It was found that the heat transfer due to the Thomson effect is an order of magnitude smaller than the Peltier cooling effect and thus neglected in this study.

There are three major phenomena in a thermocouple shown in Figure 2.2 when the Thompson effect is neglected. They are:

(i) Reversible Peltier cooling and heating at the cold and hot junction respectively.

(ii) Irreversible thermal conduction along the temperature gradient.

(iii) Irreversible Joule heating.

The thermal conduction and the Joule heating oppose the cooling due to the Peltier effect in a thermo-couple. To achieve a higher cooling performance at the cold junction, a higher Seebeck coefficient (α), lower thermal conductance (K) or conductivity (k) and lower electrical resistance (ρ) or higher electrical conductivity ($\sigma = 1/\rho$) of the thermo-element is

favorable. Combining these parameters, a figure of merit which describes the quality of the thermocouple is expressed as (Ioffe, 1957)

$$z = \frac{\alpha^2 \sigma}{k} \qquad 2.6$$

The three parameters, Seebeck coefficient α, thermal conductivity k and electrical conductivity σ are all functions of charge carrier concentration (free electrons or holes), η. The relationship between the charge carrier concentration and these three properties of thermo-element is shown qualitatively by Ioffe (1957) and reproduced in Figure 2.7. The thermal and electrical conductivity is proportional to the carrier concentration, η while the Seebeck coefficient decreases nonlinearly with an increase in carrier concentration. The value of $\alpha^2\sigma$ approaches a maximum for a carrier concentration of the order of 10^{19} cm^{-3}, which is approximately 1000 times smaller than the free electron concentration in metals (Ioffe, 1957). The value of z is small for insulators due to their very low electric conductivity (σ) and for metals due to a very low Seebeck coefficient (α). This explains why thermoelectric modules were not feasible until the discovery of semiconductors.

The figure of merit of a thermocouple limits the maximum achievable temperature difference (ΔT_{max}) between the hot and the cold junctions whereas the cross sectional area to the length ratio of the n or p-type thermo-element, which is generally known as geometric factor, $G = A_{TE} / t_{TE}$ defines the heat pumping capacity. The most widely used thermoelectric material for refrigeration is a binary alloy, $(Bi,Sb)_2(Te,Se)_3$, commonly known as bismuth telluride (Guyer, 1988).

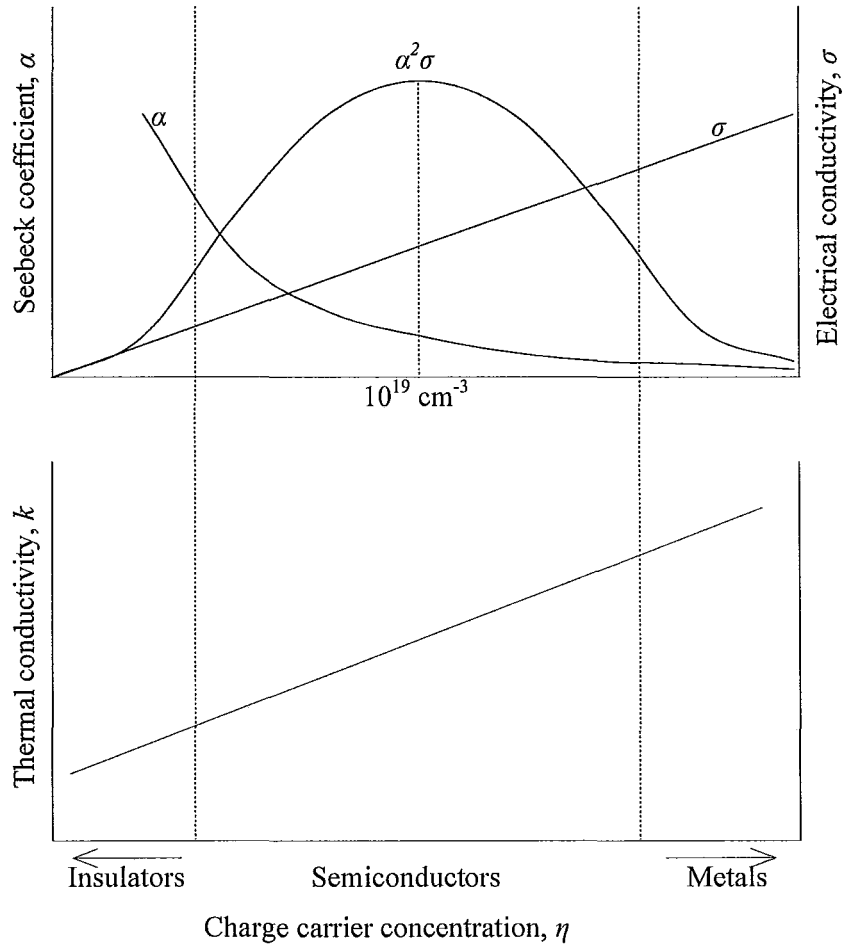


Figure 2.7: Effect of charge carrier concentration on the components of figure of merit (Ioffe, 1957).

Conventional thermoelectric modules can have various specifications in terms of their geometry, number of thermocouples and power rating for various applications. These devices can be cascaded to achieve a higher temperature differential across the entire thickness. Different applications of thermo-electric modules for (i) cooling, ranging from consumer products to military or aerospace applications, (ii) power generation, e.g. waste heat recovery (iii) sensors such as cryogenic heat flux sensor, ultrasonic intensity sensor, fluid flow sensor, infrared sensor are reviewed by Riffat and Ma (2003).

A number of investigations have been performed for geometric optimization of thermo-elements in a TEC to achieve better cooling capacity and coefficient of performance (Cheng and Lin, 2005, Fukutani and Shakouri, 2006, Hodes, 2007). The maximum cooling capacity improved for an increment in the cross sectional area of the thermo-element or a decrement in the length. The maximum achievable *COP*, irrelevant of the maximum cooling capacity, remained constant for any change in the area or the length of the thermo-element. To develop better thermo-element materials to achieve a higher figure of merit, several studies were performed by Venkatasubramanian et al. (2001) and Polvani et al. (2001). Venkatasubramanian et al. (2001) demonstrated a doubling in the thermoelectric figure of merit for super-lattice materials.

The physical modeling of thermoelectric devices has been considered in a number of studies e.g., one dimensional differential control volume approach by Hodes (2005) and finite element modeling by Seifert (2001) for the module alone and equivalent electric circuit model by Fukutani and Shakouri (2006), thermal resistance network model by Taylor and Solbrekken (2008), energy balance approach by Zhang et al. (2009) and

Yamanashi (1996) for a system consisting TEC module(s). Yamanashi (1996) adopted an entropy balance approach to analyze the system and presented both dimensional and non dimensional energy and entropy flow equations. The typical system considered is an only TEC system which consists of a heat source or chip, a cold side thermal resistor (from the chip to the cold side of the module), TEC module(s) and a hot side thermal resistor (from the hot side of the thermoelectric module to the ambient) as shown in Figure 2.8. The performance of TEC based thermal management systems in practical cooling applications has been considered for both forced air (Phelan et al., 2002, Zhang et al., 2009) and liquid (Zhang et al., 2009) cooling applications at the hot side of the system for fixed ambient temperature. The results showed that the chip temperature can be reduced or the heat dissipation from the chip can be improved by using TEC module(s). The hot side thermal resistance had a more significant effect on the performance of a TEC based thermal management system than the cold side thermal resistance at fixed ambient temperature (Phelan et al., 2002, Fukutani and Shakouri, 2006, Yamanashi, 1996). In particular, an increase in the hot side thermal resistance appeared to have an exponential effect on the chip temperature due to the non-linearity caused by the TEC module, while the cold side thermal resistance had a linear effect on the chip temperature. The optimized current and geometry factor used in the model proposed by Fukutani and Shakouri (2006) showed a minimum of 10 °C reduction in chip temperature compared to the model proposed by Phelan et al. (2002) for a range of heat load from the chip. An increase in hot side thermal resistance reduced the range of operating current where the TEC was effective

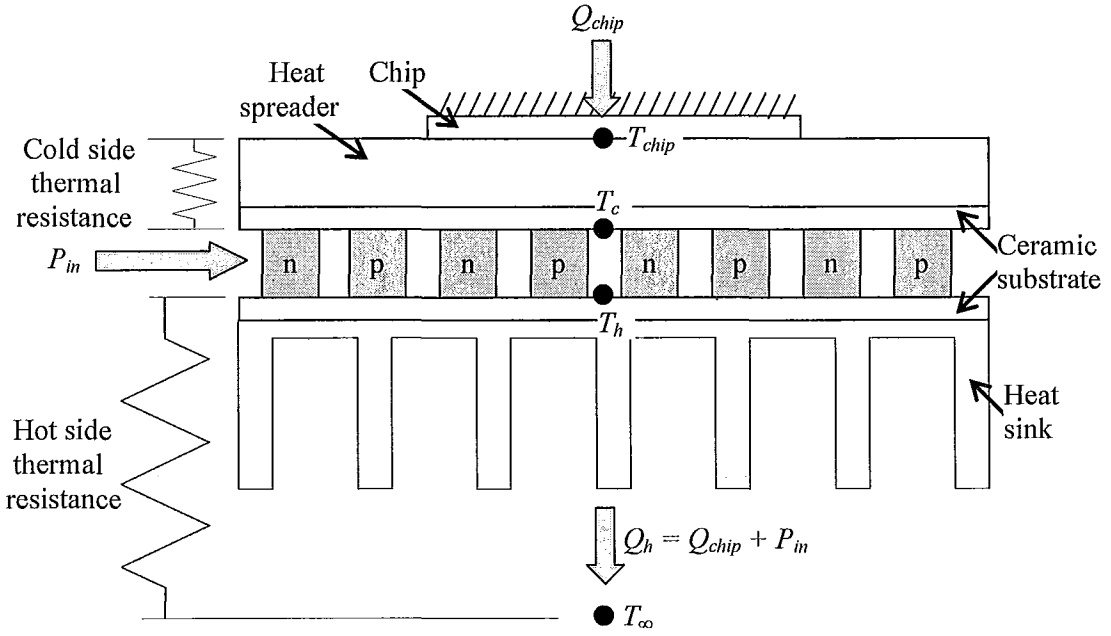


Figure 2.8: Schematic of a typical thermal management system incorporating TEC module.

(Yamanashi, 1996). This indicates the importance of considering all thermal resistances at the hot side including the hot side ceramic substrate which was ignored by Zhang et al. (2009). An empirical expression was proposed by Huang et al. (2000) for optimizing the performance of a TEC using its bulk properties and to obtain the required hot side thermal resistance. The empirical relation, however, was specific to the TEC module considered and was obtained from the curve fit to the experimental data. The prediction of performance of a TEC based system by Taylor and Solbrekken (2008) and Zhang et al. (2009) was found to be in reasonable agreement with experiments. Taylor and Solbrekken (2008) used temperature dependent thermo-element material properties in their model to predict chip temperature at a fixed heat load with a fixed hot side thermal resistance while Zhang et al. (2009) considered temperature independent properties to minimize chip temperature at fixed heat load and to maximize heat dissipation from chip at fixed chip temperature both at a fixed ambient temperature. Use of temperature dependent properties resulted in better agreement compared to the temperature independent properties (Taylor and Solbrekken, 2008). Thomson effect was neglected in these studies considering its small effect.

The aforementioned TEC based systems were studied to meet the most extreme condition that a thermal management system might experience. In many practical applications, the chip would experience a range of heat loads and/or a wide range of ambient temperatures. One disadvantage of an only TEC based system is that the TEC has a relatively high thermal resistance when it is off. Thus, it would have to be operational

even for operating conditions where a conventional thermal management system would be sufficient, which results in a lower overall *COP* (Phelan et al., 2002).

The heat dissipated at the hot side of the TEC module(s) in a TEC based thermal management system are typically cooled by natural or forced air convection. The sealed computer shown in Figure 1.1 has air cooling at the hot side. Air cooled heat sinks are thus further reviewed in the following section.

2.2. Air Cooled Heat Sinks

Heat sinks with natural or forced convection air cooling has been used for many years to transport heat from the chip or a TEC module to the ambient. A schematic of typical air cooled heat sink is shown in Figure 2.9. The base plate of the heat sink is in thermal contact with the chip or the hot side of the TEC module and the fins act as extended surface to transport heat to the ambient. Rectangular flat or pin fins (Figure 2.10) are commonly used in cooling electronics. Air flow can either be lateral (duct flow) or can impinge from the top through the passages between the fins (Figure 2.11). The thermal performance of the heat sink depends on many parameters: geometric parameters such as base plate thickness, height, thickness and spacing between the fins; material properties and the number of fins. The orientation of the flat fin heat sink at natural convection also has an effect on thermal performance. Several studies have been performed to optimize a heat sink. Yüncü and Anbar (1998) studied the performance of rectangular fins on a horizontal base plate for natural convection and found that natural convection heat transfer rate improves with increasing fin height for fixed fin spacing and fixed number of fins. A

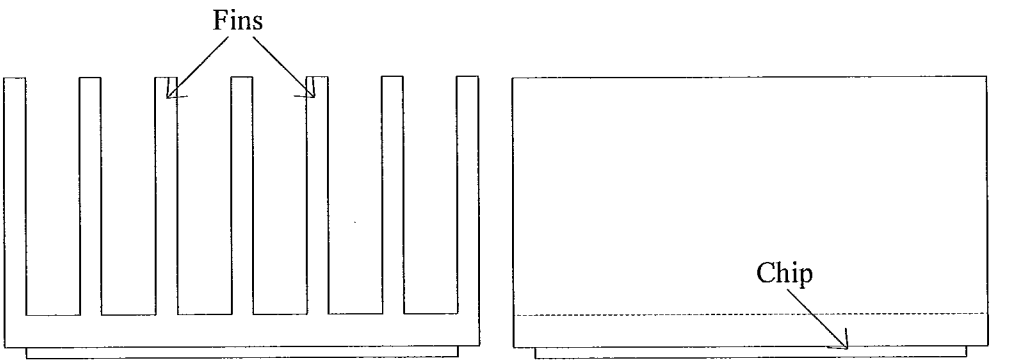


Figure 2.9: Typical air cooled heat sink.

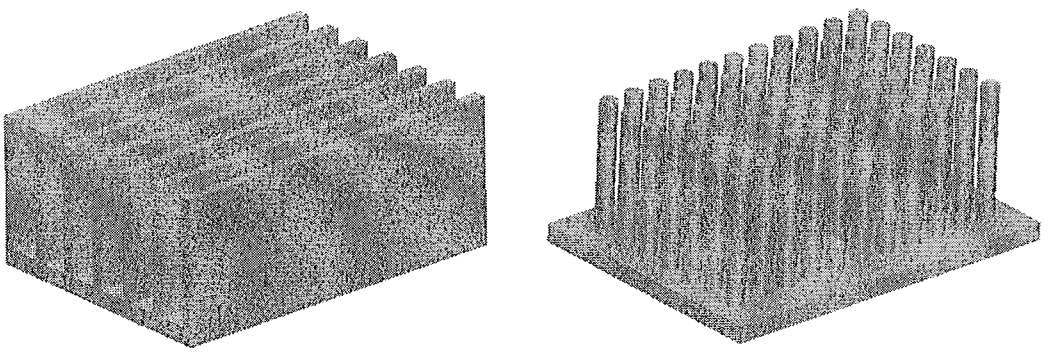


Figure 2.10: Typical (a) rectangular straight/flat and (b) pin fin heat sink.

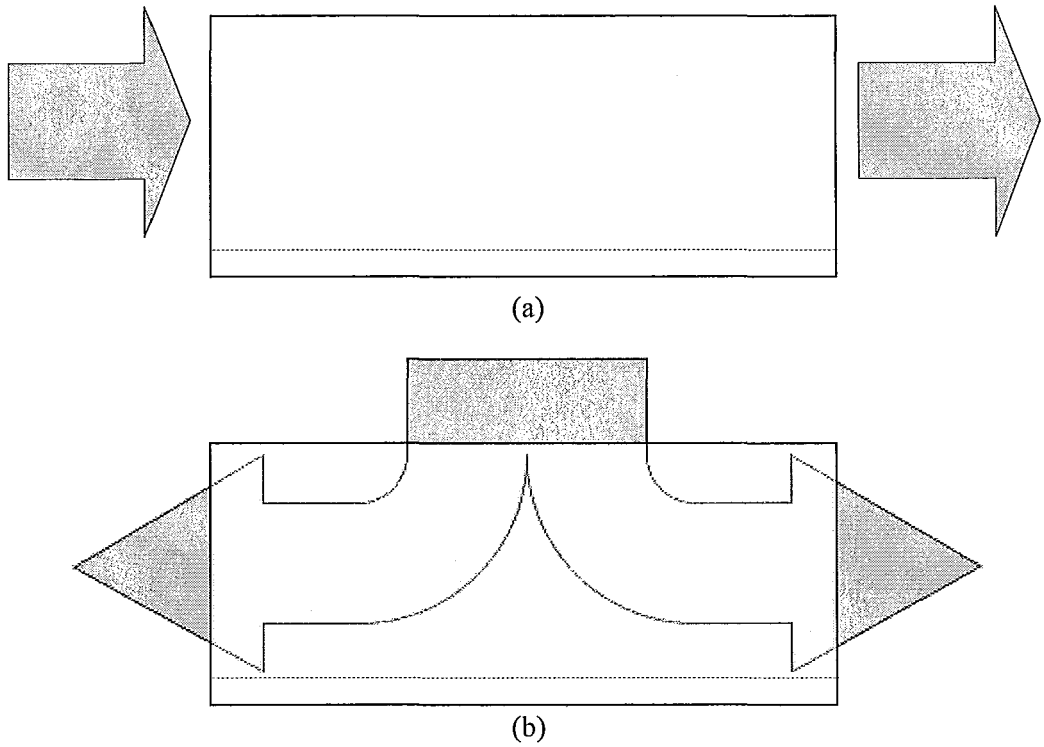


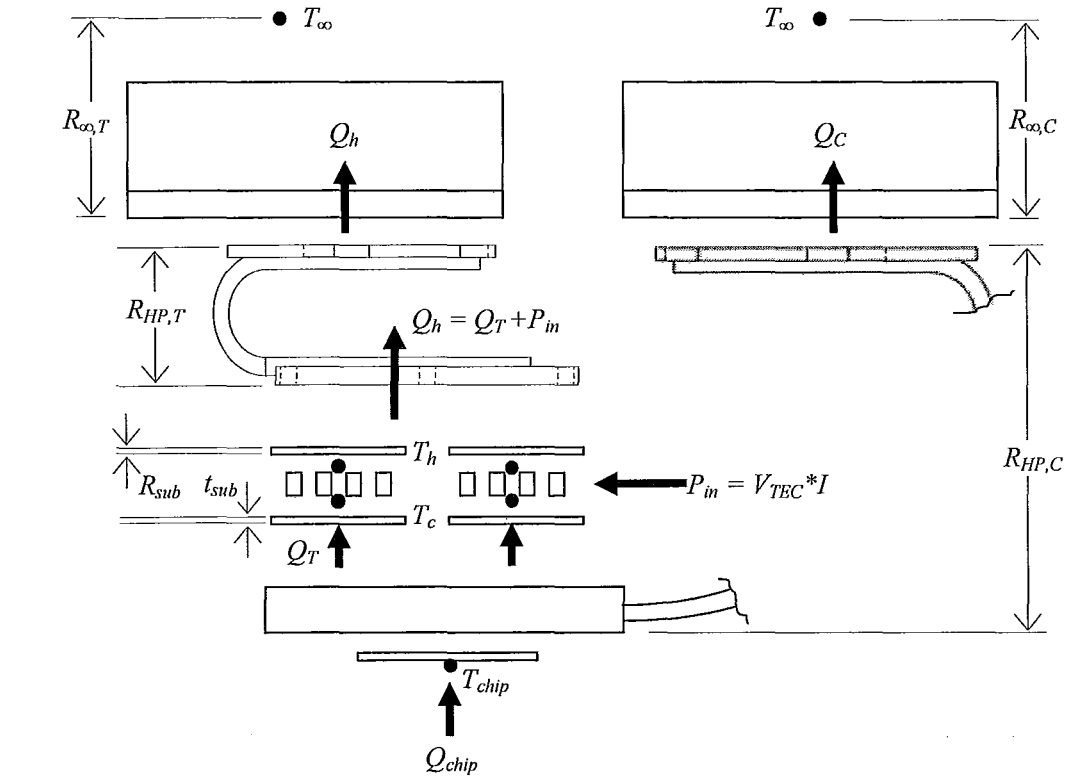
Figure 2.11: Air flow through the heat sink (a) duct flow and (b) impingement flow.

dimensionless empirical expression to correlate the natural convection heat transfer as a function of number of fins, fin height and fin spacing was developed. Güvenç and Yüncü (2001) investigated the performance of fins on a vertical base plate for natural convection. The natural convection heat transfer was improved by increasing the fin height and the fin base to ambient temperature difference. Fin spacing was found to have an optimum value at different fin base to ambient temperature differences. A better heat transfer enhancement was obtained with vertically oriented fin arrays than with horizontally oriented ones for the same fin geometry. Yazicioğlu and Yüncü (2007) studied the optimization of rectangular fins on a vertical base plate for natural convection and developed empirical expressions for optimum fin spacing as a function of fin length and Rayleigh number and for the ratio of maximum convection heat transfer rate at vertical orientation with rectangular fin to that of a flat plate with equal base area as a function of Rayleigh number, base to ambient temperature difference, base plate width and fin length. Teertstra et al. (1999) developed a model to predict the heat transfer from fin arrays with forced convection for a plate fin heat sink at duct flow with and without considering the fin efficiency. They experimentally showed that the effect of fin efficiency is an important parameter to be considered in case of high aspect ratio heat sinks (i.e. fin spacing << fin height) which are used for electronic package cooling. Experimental results were in good agreement with the predictions from model. Saini and Webb (2002) developed models for air cooled plane fin heat sinks both for duct and impinging flow to predict convection resistance of the heat sink. Kock and Visser (2004) considered trading-off between heat sink mass and thermal resistance to optimize the heat sink geometry for base plate thickness, fin thickness, height and number

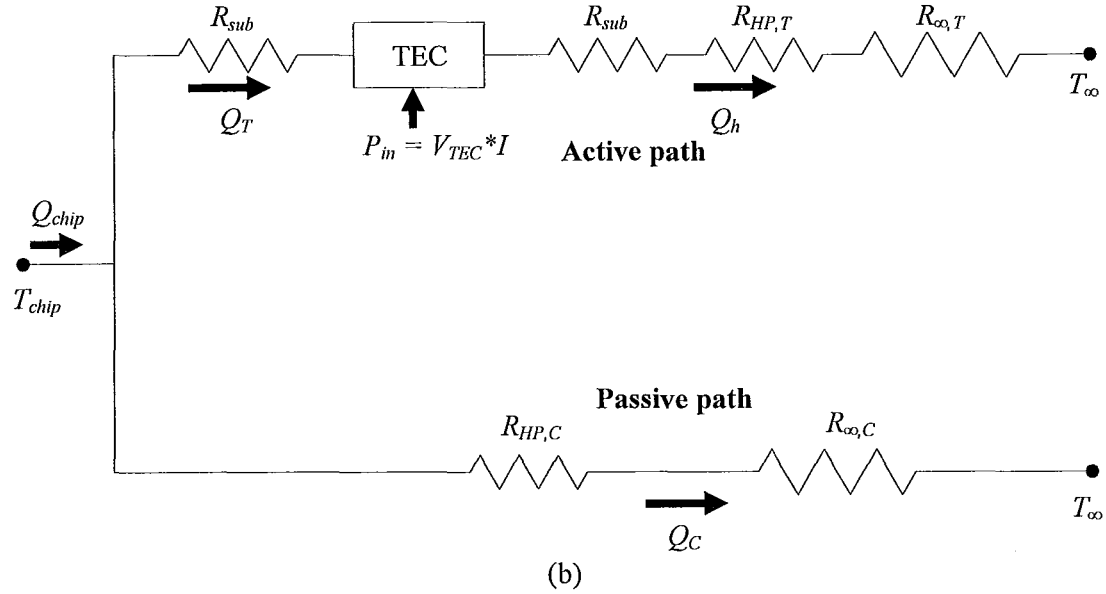
of fins at a fixed heat load from the chip for both natural and forced convections for straight fin heat sink. The heat sink thermal resistance decreased with an increase in fin thickness, base plate thickness, number of fins and thus mass of the fin. Maveety and Hendricks (1999) studied the effect of heat sink geometry, material, nozzle to heat sink vertical distance and Reynolds number based on nozzle diameter for air impingement cooling. Ledezma et al. (1996) optimized the pin fin spacing for impingement flow and found that the optimized fin height to base plate length ratio was 0.53 and the optimum fin width to base plate length ratio was 0.1 for a square pin fin. Maveety and Jung (2000) performed a numerical and experimental study to optimize square pin fins with turbulent air impingement.

Chapter 3 SYSTEM MODELING

The hybrid thermal management system considered here consists of two thermally parallel paths: (i) a conventional heat pipe based passive path and (ii) a TEC based active path. The passive path consists of heat pipes and heat spreaders with a finned heat sink and the TEC path consists of two TEC modules with a second set of heat pipes and heat sink as shown in Figure 1.2. An exploded view with the heat transfer through the different elements is shown in Figure 3.1 (a). The TEC modules in the active TEC path are electrically in series but thermally in parallel when more than one module is used. The case considered here is a natural convection cooling system to the ambient through a finned plate. The total finned area is fixed thus the thermal resistance of the total heat sink has a nominal fixed value over a range of operating ambient temperatures. The performance of the thermal management system will thus depend on the portion of the total heat sink area dedicated to each path. This is characterized by r_C, the fraction of heat sink area dedicated to the conventional passive path. When $r_C = 0$, the system is completely active, while when $r_C = 1$, the system is completely passive which means, in practice the TEC based active path is absent. When $0 < r_C < 1$, the system is a hybrid with a portion of the heat transferred



(a)



(b)

Figure 3.1: Hybrid thermal management system (a) exploded view (b) thermal resistance network.

through each path depending on the thermal resistance of the heat sink, operating condition of the chip and ambient, r_C and the number and operating conditions of the TEC modules.

3.1. MODELING THE HYBRID SYSTEM

The performance of the hybrid thermal management system is modeled using a thermal resistance network as shown in Figure 3.1 (b). When the TEC is off (i.e. no current supplied to the TEC modules), the mode of heat transfer from the chip to the finned heat sink is through the heat pipes and from the fin plate to the ambient by natural convection.

The governing equations at the TEC off mode are

$$Q_{chip} = Q_C + Q_T \tag{3.1}$$

where

$$Q_C = \frac{T_{chip} - T_\infty}{R_C} \tag{3.2}$$

and

$$Q_T = Q_h = \frac{T_{chip} - T_\infty}{R_T} \tag{3.3}$$

Here, Q_{chip} is the total heat load from the chip to the thermal management system, Q_C is the heat transported through the conventional path and Q_T is the heat flow through the TEC based active path. In this case the heat exiting from the TEC (Q_h) is the same as Q_T since the TEC is off.

The thermal resistance of the passive path can be expressed as

$$R_C = R_{HP,C} + R_{\infty,C} \tag{3.4}$$

where

$$R_{\infty,C} = \frac{R_{\infty,tot}}{r_C} \tag{3.5}$$

$R_{HP,C}$ is the thermal resistance of the heat pipe unit in the conventional passive path, $R_{\infty,C}$ is the thermal resistance of the associated heat sink, $R_{\infty,tot}$ is the thermal resistance of the entire heat sink and r_C is the fraction of the heat sink area dedicated to the conventional path. The thermal resistance of the interface material between the evaporator heat spreader and chip and between the condenser heat spreader and the associated heat sink is incorporated into the thermal resistance of the heat pipe unit. The thermal resistance of the entire heat sink is given by

$$R_{\infty,tot} = \frac{1}{hA_{fin,tot}} \tag{3.6}$$

where h is the heat transfer coefficient and $A_{fin,tot}$ is the surface area of the finned heat sink.

The thermal resistance of the TEC path when no current is applied to the TEC is given by

$$R_T = R_{in} + R_{TEC} + R_{out} \tag{3.7}$$

where R_{in} is the thermal resistance between chip and cold side and is given by

$$R_{in} = \frac{R_{sub}}{n} = \frac{1}{n}\frac{t_{sub}}{k_{sub}A_{sub}} \tag{3.8}$$

where t_{sub} is the thickness of the substrate (Figure 3.1 (a)), k_{sub} is the thermal conductivity of the substrate material and A_{sub} is the cross sectional area of the substrate in one module. The thermal resistance of the interface material associated with the cold side ceramic substrate layer is incorporated into R_{in}. Here and throughout, the relations are developed

for n modules electrically in series but thermally in parallel. When the interconnect material between n and p-type thermo-element is assumed to be ideal the thermal resistance of n modules when they are electrically turned off, each having N thermocouples is approximated as

$$R_{TEC} = \frac{t_{TE}}{k_{TE}(2nNA_{TE})} \tag{3.9}$$

Here, t_{TE} and A_{TE} are the length and the cross sectional area of n or p-type elements respectively that are assumed to be equal; and k_{TE} is the thermal conductivity of n or p-type elements (that are assumed to be equal here (Simons and Chu, 2000)). Nolas et al. (2001) noted that the electric resistivity ρ and thermal conductivity k_{TE} for both n and p-type conventional thermo-elements are almost the same. The thermal resistance from the hot side of TEC to the ambient is given by

$$R_{out} = \frac{R_{sub}}{n} + R_{HP,T} + R_{\infty,T} = \frac{1}{n}\frac{t_{sub}}{k_{sub}A_{sub}} + R_{HP,T} + R_{\infty,T} \tag{3.10}$$

where

$$R_{\infty,T} = \frac{R_{\infty,tot}}{1 - r_C} \tag{3.11}$$

and $R_{HP,T}$ is the thermal resistance of the heat pipe unit in the TEC path and $R_{\infty,T}$ is the thermal resistance of the associated heat sink. The thermal resistance of the interface material between the evaporator heat spreader and hot side ceramic substrate layer and between the condenser heat spreader and the associated heat sink is incorporated into the thermal resistance of the heat pipe unit, $R_{HP,T}$.

These equations can be solved to determine the heat load from the chip and the ratio of heat transfer through each path when the TEC is off. Thus,

$$Q_{chip} = \left(T_{chip} - T_{\infty}\right) \frac{R_C + R_{in} + R_{TEC} + R_{out}}{R_C \left(R_{in} + R_{TEC} + R_{out}\right)} \qquad 3.12$$

and

$$\frac{Q_T}{Q_C} = \frac{R_C}{R_T} \qquad 3.13$$

The thermal resistance model is more complex when the TEC is on as performance of the system depends on the applied DC current. The total heat load from the chip is still given by Eqn. 3.1, but the heat exiting at the hot side of the TEC modules Q_h when they are on is given by

$$Q_h = Q_T + P_{in} \qquad 3.14$$

where

$$P_{in} = V_{TEC}\, I \qquad 3.15$$

P_{in} is the electric power required by the TEC modules to transport Q_T, the amount of heat at the cold side of the TEC. The analysis of the conventional path is the same as when the TEC is off and is thus given by Eqn. 3.2 and Eqn. 3.4. The relationship between the portion of the heat dissipation from chip that is transported through the TEC path, Q_T, and the temperature difference between the chip and cold side of the TEC, T_c is given by

$$Q_T = \frac{T_{chip} - T_c}{R_{in}} \qquad 3.16$$

where R_{in} is the thermal resistance between the chip and the cold side of the TEC and is given by Eqn. 3.8. The relationship between the heat exiting the hot side of the TEC, Q_h

and the temperature difference between the hot side of the TEC, T_h and the ambient is given by

$$Q_h = \frac{T_h - T_\infty}{R_{out}} \qquad 3.17$$

where R_{out} is given by Eqn. 3.10.

The governing differential equation at steady state for one thermo-couple shown in Figure 2.2 when the thermo-elements are isotropic is expressed as (Arpaci, 1966)

$$k_{TE}\frac{d^2T}{dx^2} + u''' = 0 \qquad 3.18$$

where u''' is the energy generation per unit volume in one thermo-couple, which in this case is Joule heating, as the Thomson effect is neglected (APPENDIX A) and is expressed as

$$u''' = \frac{I^2 R_{el}}{2A_{TE}t_{TE}} \qquad 3.19$$

Here I is the applied current and R_{el} is the electric resistance of one couple and is expressed as

$$R_{el} = \frac{2t_{TE}\rho}{A_{TE}} \qquad 3.20$$

Here, ρ is the electric resistivity of n or p-type elements (that are assumed to be equal for this analysis (Simons and Chu, 2000)).Combining Eqn. 3.18, 3.19, 3.20 the governing equation is expressed as (Hodes, 2005)

$$\frac{d^2T}{dx^2} + \frac{I^2\rho}{k_{TE}A_{TE}^2} = 0 \qquad 3.21$$

The boundary conditions are

$$T(0)=T_c \tag{3.22}$$

$$T(t_{TE})=T_h \tag{3.23}$$

Solving Eqn 3.21 for these boundary conditions, the temperature distribution is expressed as (Hodes, 2005)

$$T(x)=\frac{-I^2\rho}{2k_{TE}A_{TE}^2}x^2+\left(\frac{I^2\rho t_{TE}}{2k_{TE}A_{TE}^2}+\frac{T_h-T_c}{t_{TE}}\right)x+T_c \tag{3.24}$$

The heat transfer at the cold and hot junction is obtained from the surface energy balance at these junctions. The heat transferred at any junction is the energy absorbed or released due to the Peltier effect plus the conduction heat transfer. Hence

$$Q(x)=I\alpha T(x)-2k_{TE}\left.\frac{dT}{dx}\right|_x \tag{3.25}$$

The heat transfer at the cold and hot junction can be obtained using Eqn. 3.25 for the boundary conditions expressed in Eqn. 3.22 and Eqn. 3.23 respectively and are expressed for one couple as

$$Q_{c1}=I\alpha T_c-K(T_h-T_c)-0.5I^2R_{el} \tag{3.26}$$

$$Q_{h1}=I\alpha T_h-K(T_h-T_c)+0.5I^2R_{el} \tag{3.27}$$

where K, the thermal conductance of one couple is given by

$$K=\frac{2k_{TE}A_{TE}}{t_{TE}} \tag{3.28}$$

The relationship between the heat into and out of the TEC module(s) is typically approximated assuming that, the interconnect material between the n and p-type thermo-

elements are ideal and the material properties of the n and p-type thermo-elements are identical (Simons and Chu, 2000) with opposite polarity for the Seebeck coefficient, α. The interconnect material between the n and p-type semiconductor is assumed to have no effect on the performance of the thermocouple, which is true if the interconnect material has a zero Seebeck coefficient. Typically a good conductor is used as the interconnect material as it possesses a low Seebeck coefficient and so that there is no temperature gradient. The interconnect thermal and electrical contact resistances for a typical TEC module are 10^{-8} to 10^{-7} $KW^{-1}m^{-2}$ and 10^{-9} to 10^{-8} Ωm^2 respectively (Silva and Kaviany, 2004) which leads to a contact thermal and electrical resistances of 1.74 X 10^{-13} °C/W and 1.74 X10^{-14} Ω respectively for a CP 1.4-127-06L thermoelectric cooler module from Melcor.

The expressions for Q_T and Q_h for n modules each containing N thermocouples (Figure 3.1 (b)) are thus expressed as

$$Q_T = nN\left[I\alpha T_c - K(T_h - T_c) - 0.5I^2R_{el}\right] \qquad 3.29$$

and

$$Q_h = nN\left[I\alpha T_h - K(T_h - T_c) + 0.5I^2R_{el}\right] \qquad 3.30$$

The Peltier cooling is linearly proportional to the applied current while the Joule heating is proportional to the current squared making it a more dominant factor. Thus, if the applied current exceeds a certain value the net cooling will start decreasing with a further increase in applied current.

The above set of equations can be solved to determine an expression for the heat load from the chip for the Hybrid system when the TEC is on as

$$Q_{chip} = \frac{\left[\begin{array}{l} \left\{\begin{array}{c} 1+nNI\alpha\left(R_{in}-R_{out}\right)+nNK\left(R_{in}+R_{out}\right) \\ -\left(nNI\alpha\right)^2 R_{in}R_{out}+nNR_c^{\,*} \\ \left(I\alpha+K-nNI^2\alpha^2 R_{out}\right) \end{array}\right\} T_{chip} \\ -\left\{\begin{array}{c} 1+nNI\alpha\left(R_{in}-R_{out}\right)+nNK^{\,*} \\ \left(R_C+R_{in}+R_{out}\right)-\left(nNI\alpha\right)^2 R_{in}R_{out} \end{array}\right\} T_{\infty} \\ -0.5nNI^2 R_{el}R_C\left(1-nNI\alpha R_{out}+2nNKR_{out}\right) \end{array}\right]}{R_C\left[\begin{array}{c} 1+nNI\alpha\left(R_{in}-R_{out}\right)+nNK\left(R_{in}+R_{out}\right) \\ -\left(nNI\alpha\right)^2 R_{in}R_{out} \end{array}\right]} \qquad 3.31$$

This expression is similar to those in Yamanashi (1996) and Zhang (2009) in the limit when r_C approaches zero (i.e. when only a TEC system is used in the on mode). The optimum current, I_{opt} to achieve the maximum amount of heat the system can dissipate, Q_{max} is obtained by solving the equation of the first derivative of Q_{chip} with respect to I.

The input voltage to the TEC depends on the applied current to the TEC module(s) and the hot and cold side temperatures. An expression for this voltage is obtained as

$$V_{TEC} = \frac{nN\left[\begin{array}{c} \alpha\left(nNI\alpha R_{out}-1\right)T_{chip}+\alpha\left(nNI\alpha R_{in}+1\right)T_{\infty} \\ +IR_{el}\left\{1+0.5nNI\alpha\left(R_{in}-R_{out}\right)+nNK\left(R_{in}+R_{out}\right)\right\} \end{array}\right]}{1+nNI\alpha\left(R_{in}-R_{out}\right)+nNK\left(R_{in}+R_{out}\right)-\left(nNI\alpha\right)^2 R_{in}R_{out}} \qquad 3.32$$

The input power to the TEC module(s) is expressed as Eqn. 3.15. The system coefficient of performance, COP_{sys} is given as

$$COP_{sys} = \frac{Q_{chip}}{P_{in}} \qquad 3.33$$

3.2. LIMITING CASES OF THE HYBRID MODEL

The two limiting cases are when $r_C = 0$ and $r_C = 1$ representing the only TEC and the only passive systems respectively. For the only TEC system ($r_C = 0$) the conventional passive path does not exist. Thus Q_{chip} approaches Q_T and

$$\frac{1}{R_C}=0 \qquad 3.34$$

When the numerator and the denominator of Eqn. 3.31 is divided by R_C, the expression reduces to

$$Q_T = \frac{\left[\begin{array}{l} \left\{\begin{array}{l} \dfrac{1+nNI\alpha(R_{in}-R_{out})+nNK(R_{in}+R_{out})}{R_C} \\ -\dfrac{(nNI\alpha)^2 R_{in}R_{out}}{R_C}+nN\left(I\alpha+K-nNI^2\alpha^2 R_{out}\right) \end{array}\right\} T_{chip} \\ -\left\{\begin{array}{l} \dfrac{1+nNI\alpha(R_{in}-R_{out})+nNK(R_{in}+R_{out})}{R_C} \\ -\dfrac{(nNI\alpha)^2 R_{in}R_{out}}{R_C}+nNK \end{array}\right\} T_\infty \\ -0.5nNI^2R_{el}\left(1-nNI\alpha R_{out}+2nNKR_{out}\right) \end{array}\right]}{1+nNI\alpha(R_{in}-R_{out})+nNK(R_{in}+R_{out})-(nNI\alpha)^2 R_{in}R_{out}} \qquad 3.35$$

Substituting 0 for $1/R_C$ from Eqn. 3.34 in Eqn. 3.35, the expression for Q_{chip} for only TEC system in the on mode is

$$Q_T = \frac{\left[\begin{array}{l} nN\left(I\alpha+K-nNI^2\alpha^2R_{out}\right)T_{chip}-nNKT_\infty \\ -0.5nNI^2R_{el}\left(1-nNI\alpha R_{out}+2nNKR_{out}\right) \end{array}\right]}{1+nNI\alpha(R_{in}-R_{out})+nNK(R_{in}+R_{out})-(nNI\alpha)^2R_{in}R_{out}} \qquad 3.36$$

This expression is similar to those in Yamanashi (1996) and Zhang et al. (2009). Consider the case where the thermoelectric has no substrate layers on either side of the modules and no external thermal resistance at the cold or the hot side of the modules. Then the chip temperature approaches the cold side temperature and the ambient temperature approaches the hot side temperature of the TEC modules. These conditions can be expressed as

$$\left.\begin{array}{l} R_{in}, R_{out} = 0 \\ T_{chip} = T_c \\ T_{\infty} = T_h \end{array}\right\} \qquad 3.37$$

When the conditions represented by Eqn. 3.37 are applied to Eqn.3.36 it reduces to Eqn. 3.26 or to Eqn. 3.29 for one couple (i.e., $n = 1$ and $N = 1$) which is the governing equation for the heat being absorbed at the cold side.

For the only TEC system ($r_C = 0$) with the modules electrically off, substituting $I = 0$ in Eqn. 3.36 results in

$$Q_T = \frac{nNKT_{chip} - nNKT_{\infty}}{1 + nNK(R_{in} + R_{out})}$$

$$Q_T = \frac{nNK(T_{chip} - T_{\infty})}{1 + nNK(R_{in} + R_{out})}$$

$$Q_T = (T_{chip} - T_{\infty})\frac{1}{\frac{1}{nNK} + R_{in} + R_{out}} \qquad 3.38$$

From Eqn. 3.9 and 3.28

$$R_{TEC} = \frac{1}{nNK} \qquad 3.39$$

Substituting R_{TEC} from Eqn. 3.39 in Eqn. 3.38 yields

$$Q_T = \frac{T_{chip} - T_\infty}{R_T} \tag{3.40}$$

Eqn. 3.40 is the same as Eqn. 3.12 for the only TEC system ($r_C = 0$).

For the only conventional passive system ($r_C = 1$) the TEC based active path does not exist. Thus Q_{chip} approaches Q_C and

$$\frac{1}{R_{out}} = 0 \tag{3.41}$$

Dividing the numerator and the denominator of Eqn. 3.31 by R_{out} results in

$$Q_C = \frac{\left[\begin{array}{l} \left\{\begin{array}{l} \dfrac{1}{R_{out}} + nNI\alpha\left(\dfrac{R_{in}}{R_{out}} - 1\right) + nNK\left(\dfrac{R_{in}}{R_{out}} + 1\right) \\ -(nNI\alpha)^2 R_{in} + nNR_c\left(\dfrac{I\alpha + K}{R_{out}} - nNI^2\alpha^2\right) \end{array}\right\} T_{chip} \\ -\left\{\begin{array}{l} \dfrac{1}{R_{out}} + nNI\alpha\left(\dfrac{R_{in}}{R_{out}} - 1\right) \\ +nNK\left(\dfrac{R_C + R_{in}}{R_{out}} + 1\right) - (nNI\alpha)^2 R_{in} \end{array}\right\} T_\infty \\ -0.5nNI^2 R_{el} R_C\left(\dfrac{1}{R_{out}} - nNI\alpha + 2nNK\right) \end{array}\right]}{R_C\left[\dfrac{1}{R_{out}} + nNI\alpha\left(\dfrac{R_{in}}{R_{out}} - 1\right) + nNK\left(\dfrac{R_{in}}{R_{out}} + 1\right) - (nNI\alpha)^2 R_{in}\right]} \tag{3.42}$$

Substituting 0 for $1/R_{out}$ and $I = 0$, the expression for Q_{chip} for the conventional passive system is

$$Q_C = \frac{T_{chip} - T_\infty}{R_C} \tag{3.43}$$

Eqn. 3.43 is the same as Eqn. 3.12 for the only conventional system ($r_C = 0$) for $I = 0$.

3.3. CONVERGENCE OF THE MODEL

The predictions from the model are performed using temperature dependent thermo-element material properties. The flowcharts to calculate the chip temperature are shown in Figure 3.2, Figure 3.3 and Figure 3.4 while for the heat dissipation from chip and the corresponding system *COP* at $T_{chip} = T_{design}$ are shown in Figure 3.5, Figure 3.6 and Figure 3.7 respectively. The iteration starts with an initial value of 300 K as the mean temperature (T_{mean}) of the hot and the cold side of the thermo-elements in the TEC modules. The predicted mean temperature (T_{mean}) for an applied current of 0.625 A at an ambient temperature of 40 °C and heat load from chip of 30 W is shown in Figure 3.8 for different number of iterations. The iteration stops when $[T_{mean}\ (i) - T_{mean}\ (i\text{-}1)] \leq 10^{-10}$. After third iteration the error in this particular example becomes less than 5.7 X 10^{-4} % with respect to the value in the second iteration. The number of iterations never exceeded 10 for any model prediction.

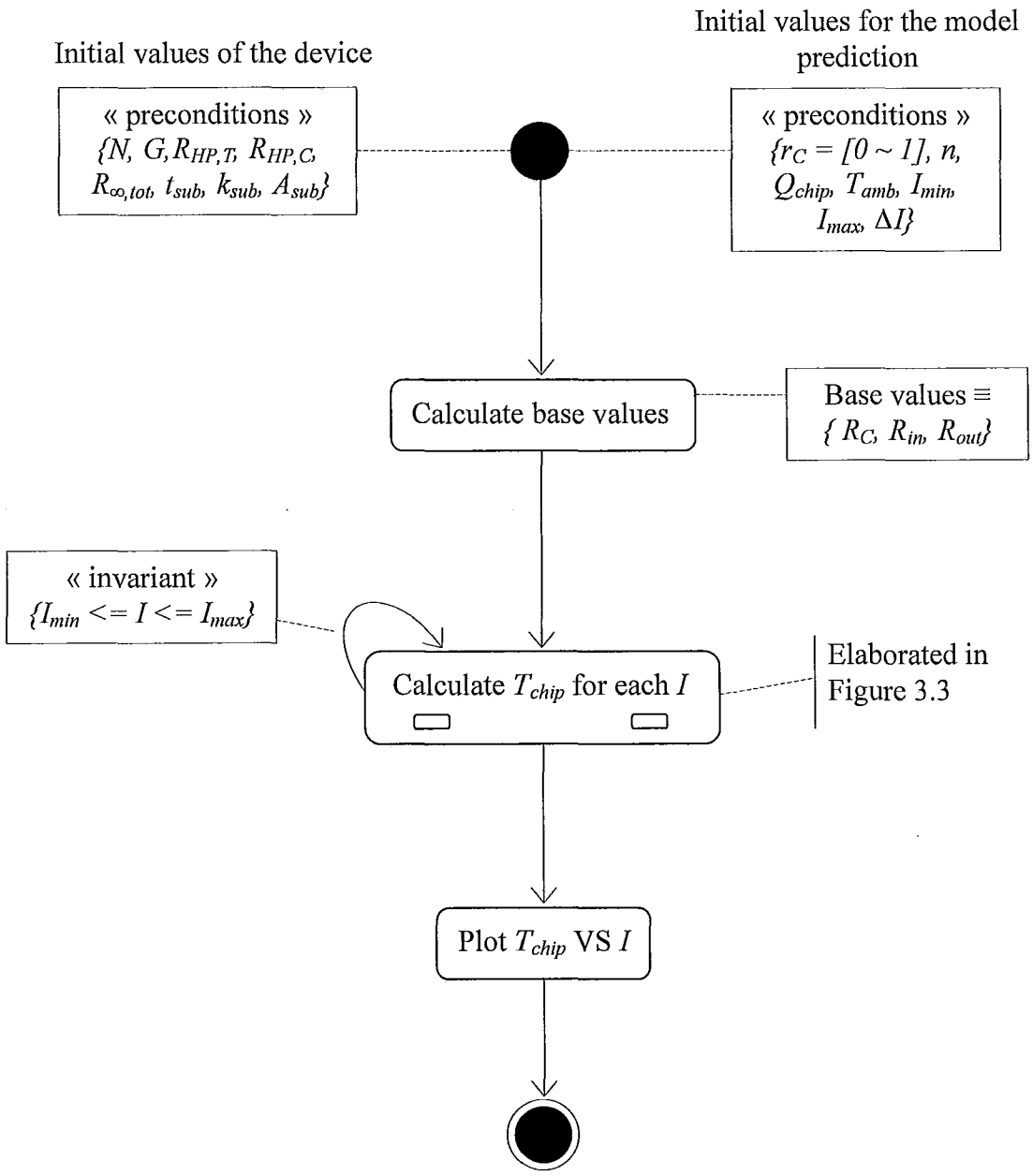


Figure 3.2: Flowchart (T_{chip} VS I): Top level state diagram for chip temperature at different applied current.

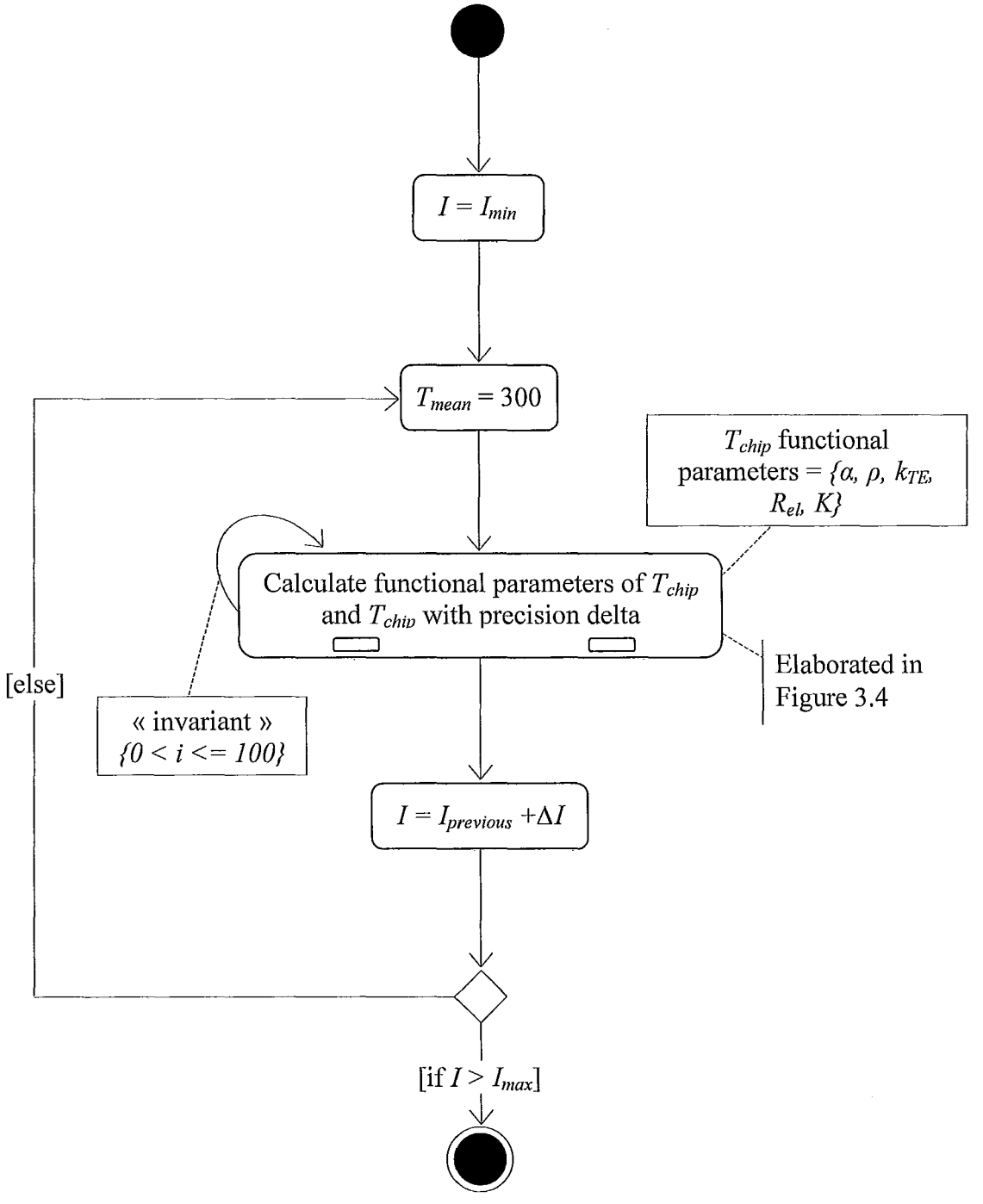


Figure 3.3: Flowchart (T_{chip} VS I contd.): Elaboration of calculating chip temperature for each applied current.

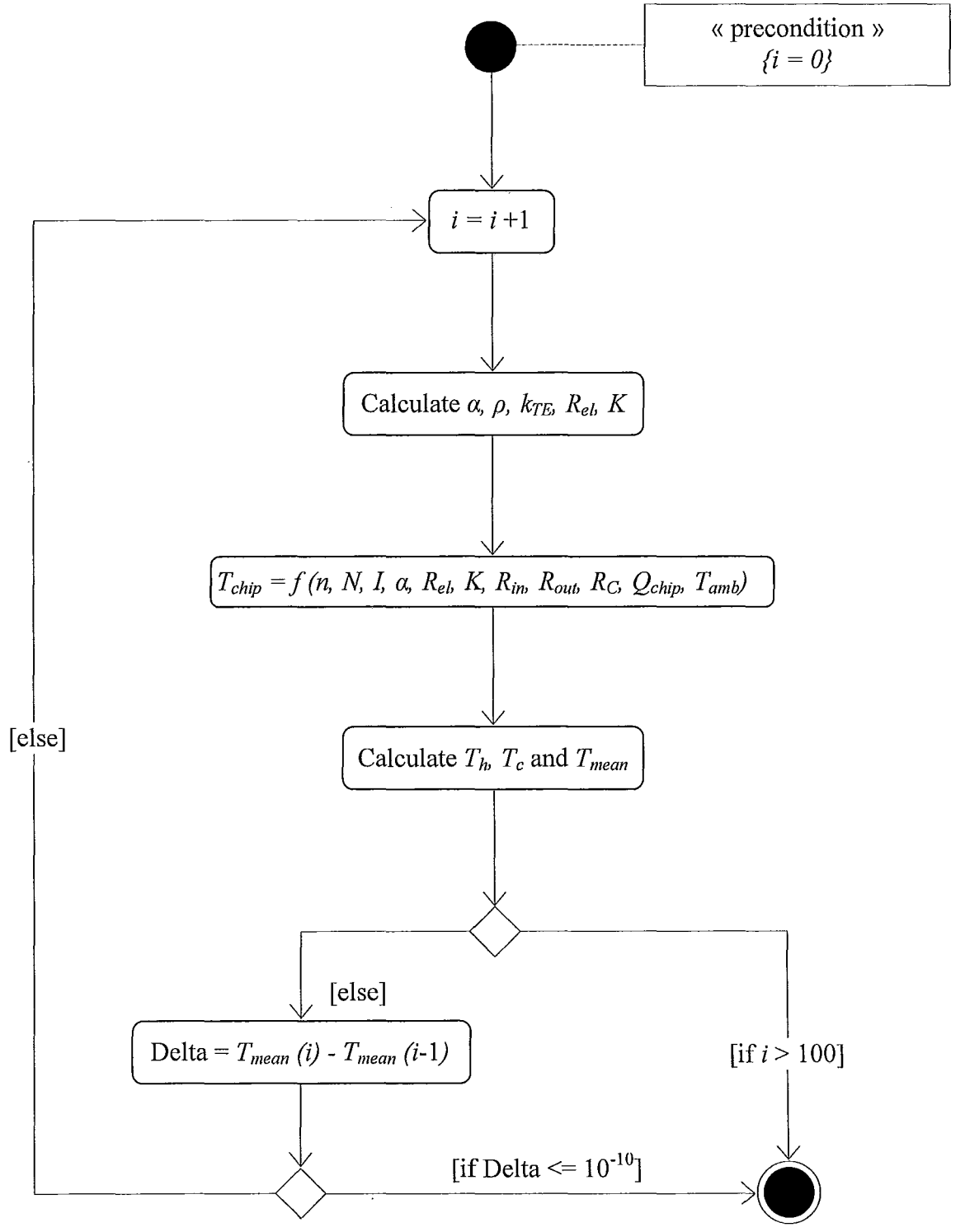


Figure 3.4: Flowchart (T_{chip} VS I contd.): Elaboration of calculating chip temperature with precision delta.

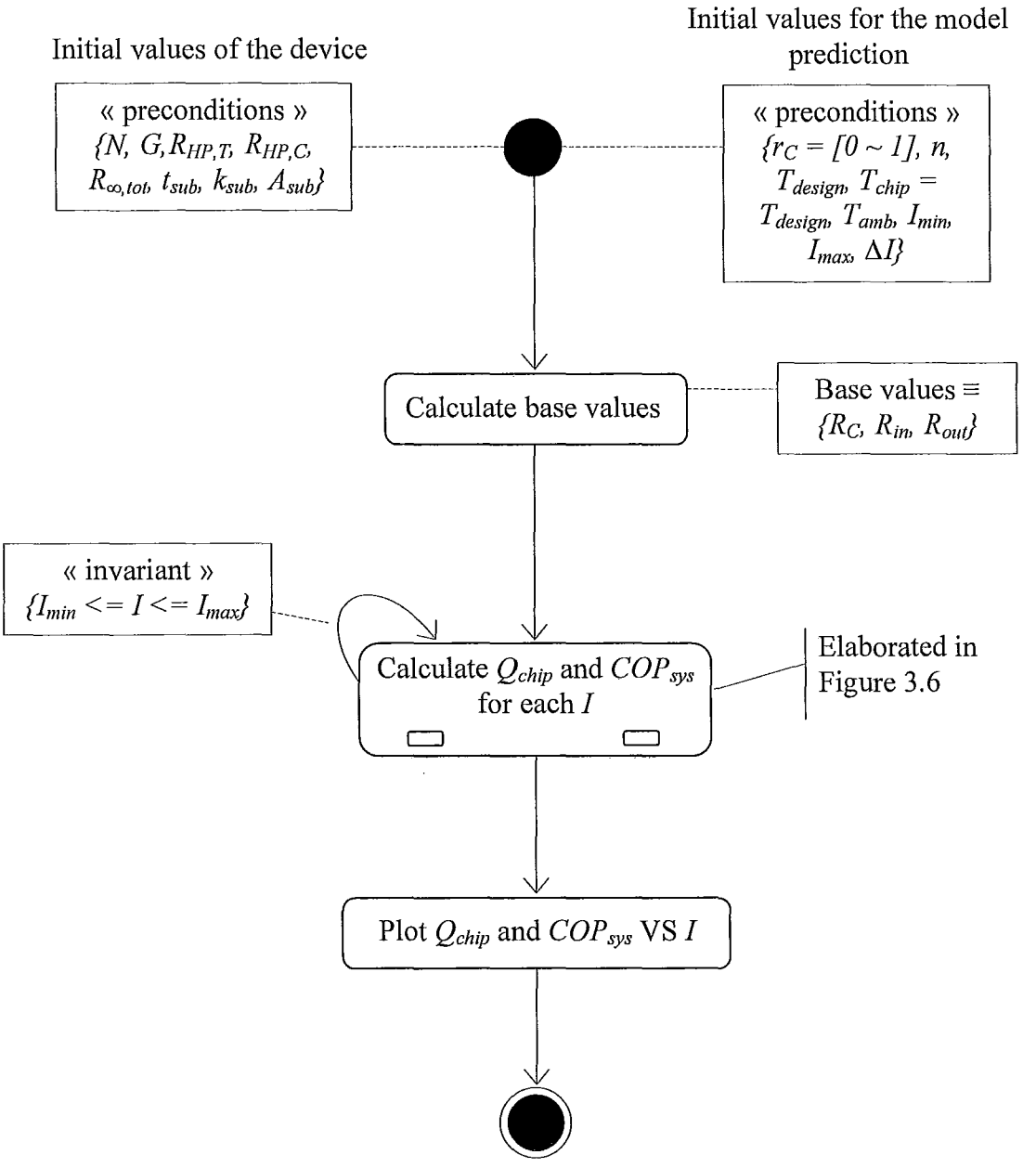


Figure 3.5: Flowchart (Q_{chip} VS I at $T_{chip} = T_{design}$): Top level state diagram for heat dissipation from the chip at different applied current.

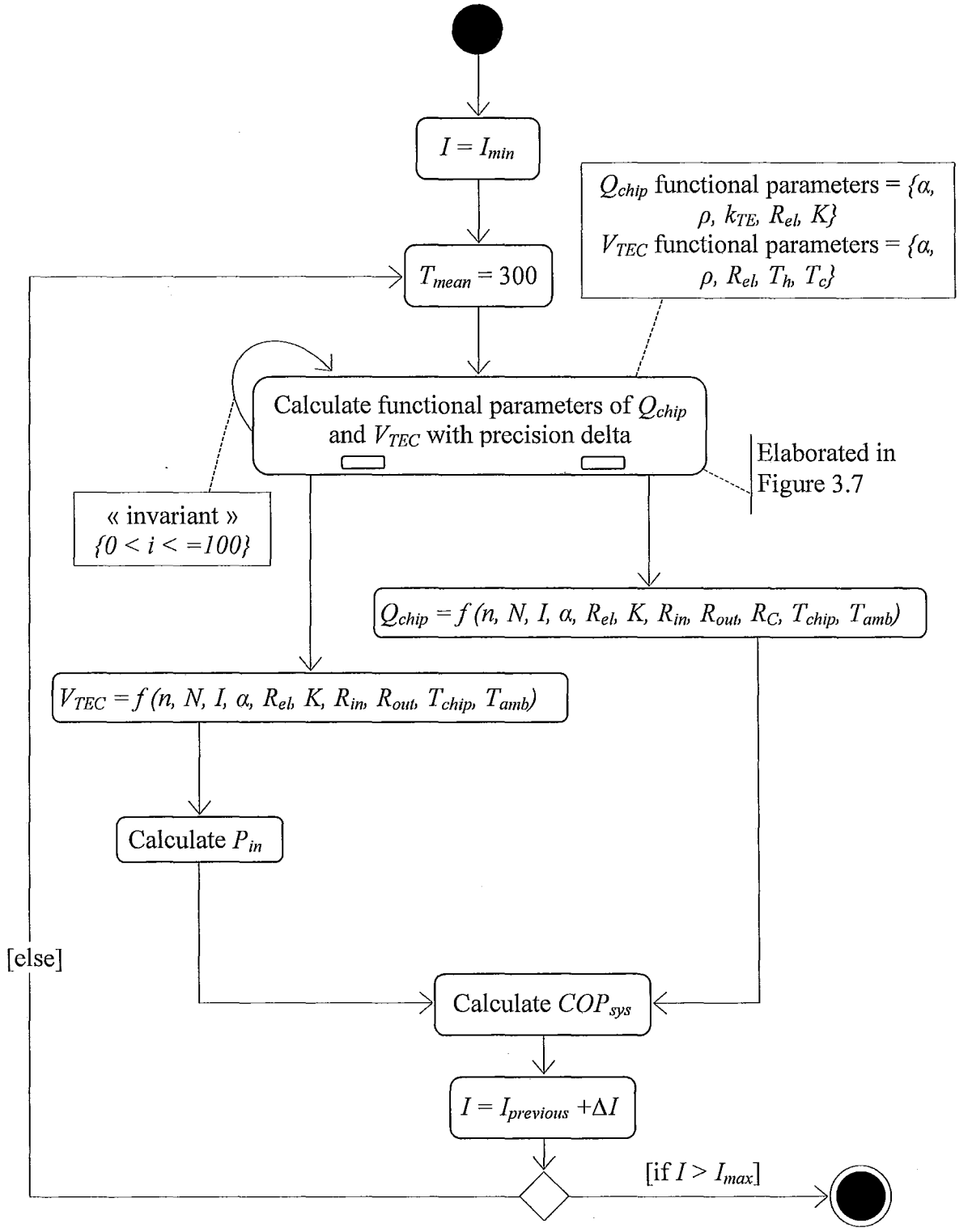


Figure 3.6: Flowchart (Q_{chip} VS I at $T_{chip} = T_{design}$ contd.): Elaboration of calculating heat dissipation from the chip and system COP for each applied current.

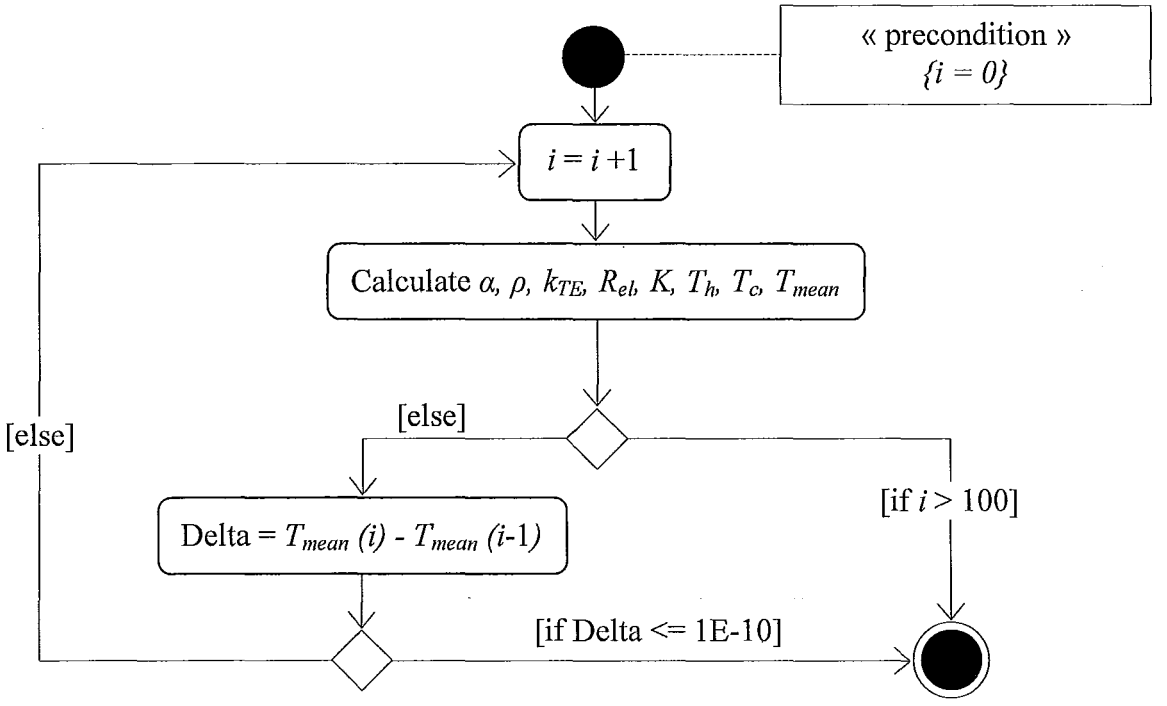


Figure 3.7: Flowchart (Q_{chip} VS I at $T_{chip} = T_{design}$ contd.): Elaboration of calculating the functional parameters of heat dissipation from the chip and voltage with precision delta.

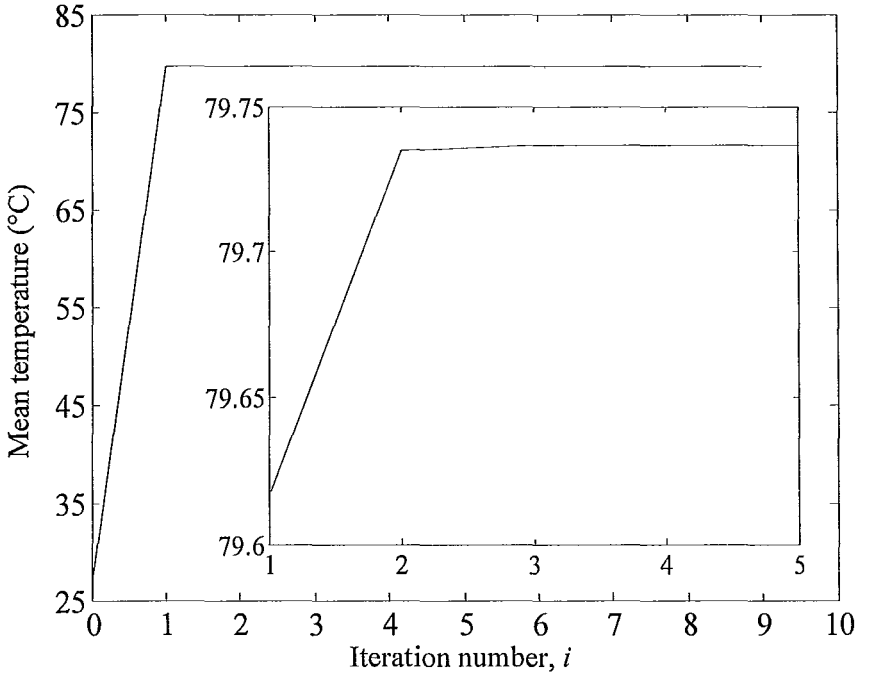


Figure 3.8: Predicted mean temperature of the hot and cold side of the thermoelectric modules at different iterations ($n = 2$, $r_C = 0$, I=0.625 A).

Chapter 4 EXPERIMENTAL FACILITY

Experiments were performed to validate the key model predictions for the only passive ($r_C = 1$), only thermoelectric ($r_C = 0$) and hybrid ($0 < r_C < 1$) systems. The model can be used as an engineering design tool to optimize the operating conditions such as operating current and corresponding system coefficient of performance. An important parameter in the design of the hybrid system is the fraction of heat sink area dedicated to the conventional passive and the active TEC paths. This would depend on the rated heat dissipation from the chip, the ambient temperature and the thermal resistance of the entire heat sink in the system. The heat dissipation from the chip in the experiments was simulated using a flexible heater and the amount of heat generated by the chip, Q_{chip} was controlled using a variable transformer. The temperature of the heater was recorded which represents the chip temperature. A heat sink with a cooling water loop was used to dissipate the heat from the heater and the TEC modules.

The sealed computer under study (Figure 1.1) has a vertical flat fin heat sink. The thermal resistance of the heat sink, R_{∞}, will depend on the base thickness, fin geometry, fin orientation with respect to gravity, mode of convective heat transfer (natural or forced

convection). The heat sink of the current system had a base plate of 252 mm X 190 mm X 3 mm with 15 equally spaced rectangular fins each of 252 mm X 22 mm X 1.5 mm. Heat transfer from the fin to the ambient was by natural convection. A correlation proposed by Churchill and Chu (Yunchu and Kakac, 1999) was used to estimate the natural convection heat transfer coefficient for the heat sink considered in this study. The estimated thermal resistance of the heat sink was approximately from 0.7 to 1.5 °C/W for a range of fin base to ambient temperature difference of 10 to 100 °C. To perform controlled experiments, a layer of acrylic glass was used to simulate the thermal resistance of the entire heat sink due to natural convection. A nominal thermal resistance of 0.77 °C/W was obtained experimentally for one layer (1.5 mm thick) of acrylic glass and was used in the model to predict the performance. The design temperature of the chip was assumed to be 85 °C as this would be safe for most recent processors used in computers. Experiments were performed for ambient temperatures in the range 30 to 60 °C. The ambient temperature was simulated in the experiments by controlling the average temperature of the water flowing through the cooling loop. The experimental facility and the instrumentation are described in detail followed by a description of the experimental procedure and an uncertainty analysis of the measurements.

4.1. TEST FACILITY

A schematic of the experimental facility is shown in Figure 4.1. A Neslab RTE 10 refrigerated bath chiller circulator (maximum cooling capacity of 500W) was used to supply the required cooling water. The temperature range of the unit is -25 °C to 150 °C

with temperature stability of ±0.01°C. An external centrifugal pump was used to supply a continuous water flow to the loops. Two separate cold plates, one for the TEC path and the other for the conventional passive path were fabricated in-house. The flow through each path was controlled by using the piping system shown in Figure 4.1. This includes a bypass loop to have a fine control of the flow rate. The water flow rate on the loop for the conventional passive path was measured using an Exact Flow dual-rotor turbine flow meter (with an uncertainty of 0.19% of the reading) connected to an Omron K3NR rate meter. The flow rate on the loop for TEC path was measured using an Omega FTB601B turbine flow meter (with an uncertainty of 1% of the reading) connected to an Omega DPF700 rate meter. The inlet and outlet water temperatures of the cooling loop on the conventional passive path were measured using two 4-wire Platinum RTD probes (6mm diameter) with an Omega DP251 precision thermometer reader while the temperatures on the cooling loop on the TEC path were measured using two 4-wire Platinum RTD probes (6mm diameter) with a Paperless Recorder VG06 reader. The piping system was well insulated using Rubatex Insul-Tube (nominal thermal conductivity of 0.038 $Wm^{-1}K^{-1}$) to minimize extraneous heat losses to the surrounding.

The schematic of the practical cases are shown in Figure 4.2 and the detailed schematic of the experimental set up for the different configurations are shown in Figure 4.3. The experimental set up of the only passive system (r_C = 1) is shown in Figure 4.3 (a) and consists of a flexible heater, a heat pipe unit, an external resistor and the cooling loop. The heat dissipation from the chip is simulated by an Omega flexible heater (KH 303/10, 3" X 3", nominal maximum capacity of 90 W) with a variable transformer. An Extech True

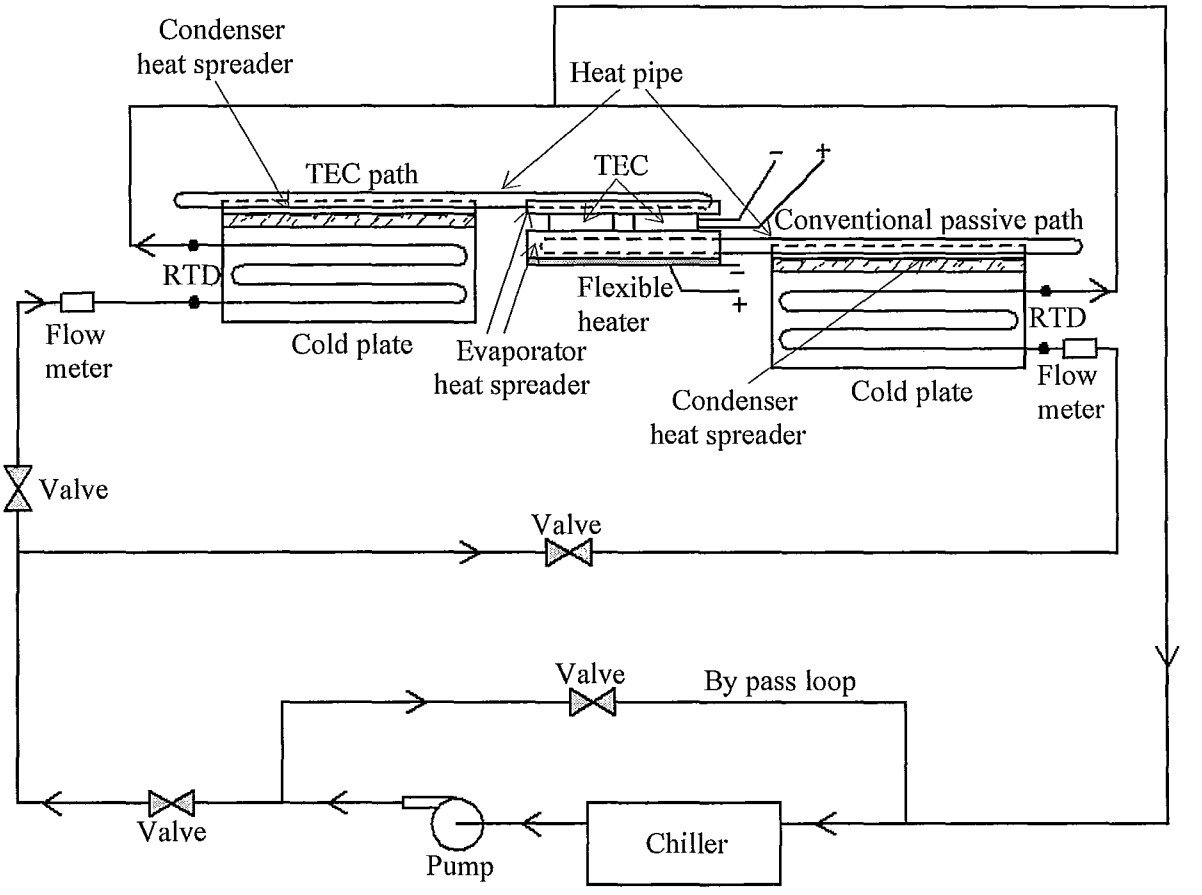


Figure 4.1: Schematic of the experimental test facility.

Power Multimeter was used to read the power input to the flexible heater. The heat is transported using a pair of heat pipes connected between two heat spreaders. The thermal resistance of the heat pipe units were measured separately and will be described later in this chapter. The thermal resistance of the fin plate at natural convection was estimated using correlations for a vertical flat fin plate in natural convection (Yuncu and Kakac, 1999). The external resistor is simulated using a layer of acrylic glass (PMMA, polymethyl methacrylic) of the same cross sectional area of the associated condenser heat spreader and the thickness of acrylic layer was calculated from the estimated thermal resistance value of the fin plate. The thermal conductivity of the acrylic layer was obtained from separate experiment which agrees well with previous studies (Miller and Kotlar, 1993) and is further described in section 4.4.3. The operating ambient temperature was simulated by the average temperature of the inlet and outlet water temperature of the cooling water loop. The experimental set up of the only thermoelectric cooler system ($r_C = 0$) shown in Figure 4.3 (b) consists of the same heat pipe unit and flexible heater with same external resistor. In this case, two TEC modules electrically in series but thermally in parallel are used with a flat aluminum sheet. The aluminum sheet was used to hold the TEC modules and to facilitate instrumentation of thermocouples in between the aluminum sheet and the cold side ceramic substrate of the TEC modules. The hybrid system ($0 < r_C < 1$) will depend on the fraction of heat sink area dedicated to the conventional passive path, r_C. The hybrid systems with r_C = 0.33 and 0.5 are shown schematically in Figure 4.2 (c) and (d). A generic schematic of the experimental set up for the hybrid system ($0 < r_C < 1$) is shown in Figure 4.3 (c). The change in r_C is directly related to the heat sink area, i.e., associated

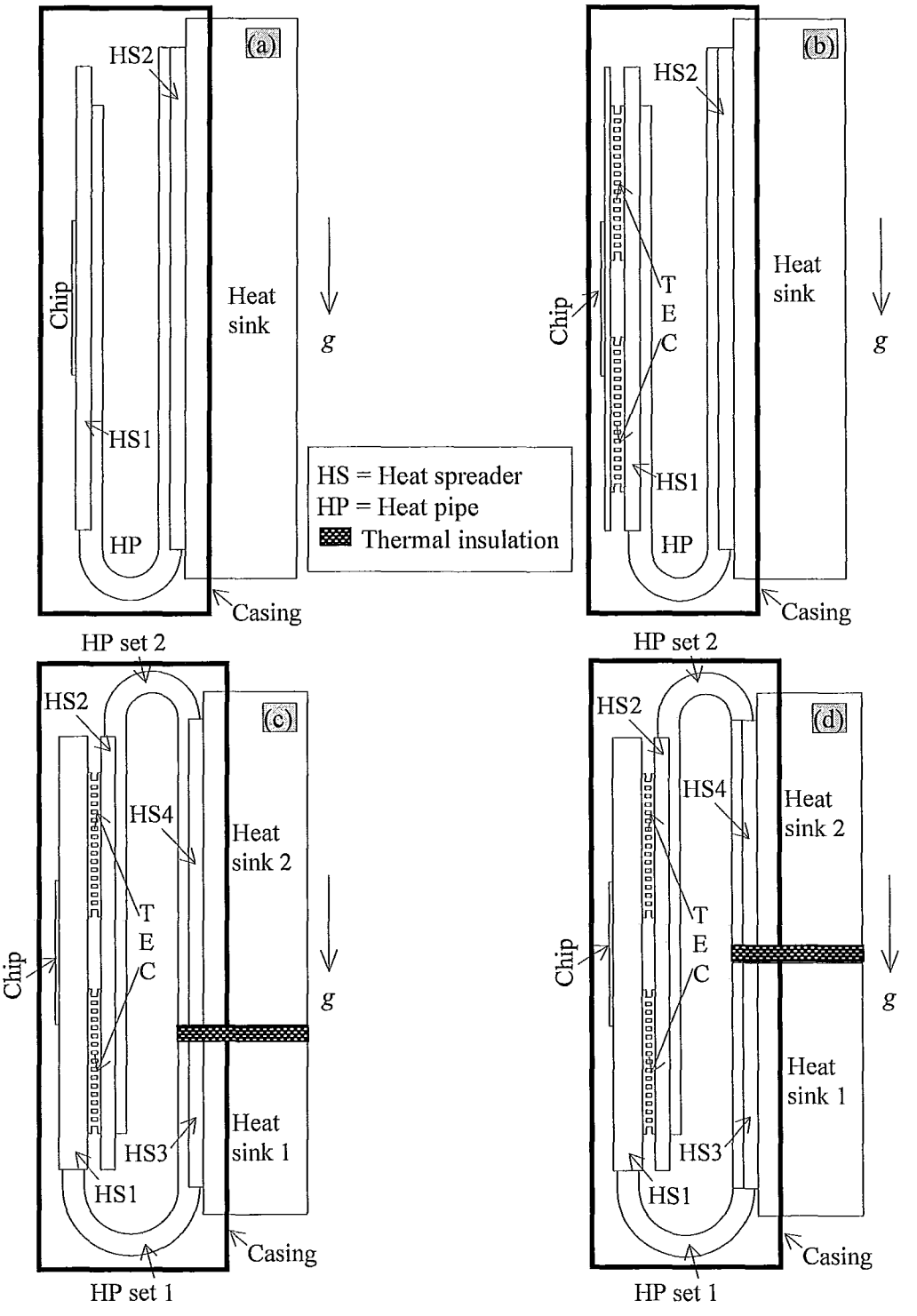


Figure 4.2: Schematic of different hybrid configurations (a) only passive system ($r_C = 1$), (b) only thermoelectric cooler system ($r_C = 0$) and hybrid system with (c) $r_C = 0.33$, (d) $r_C = 0.5$.

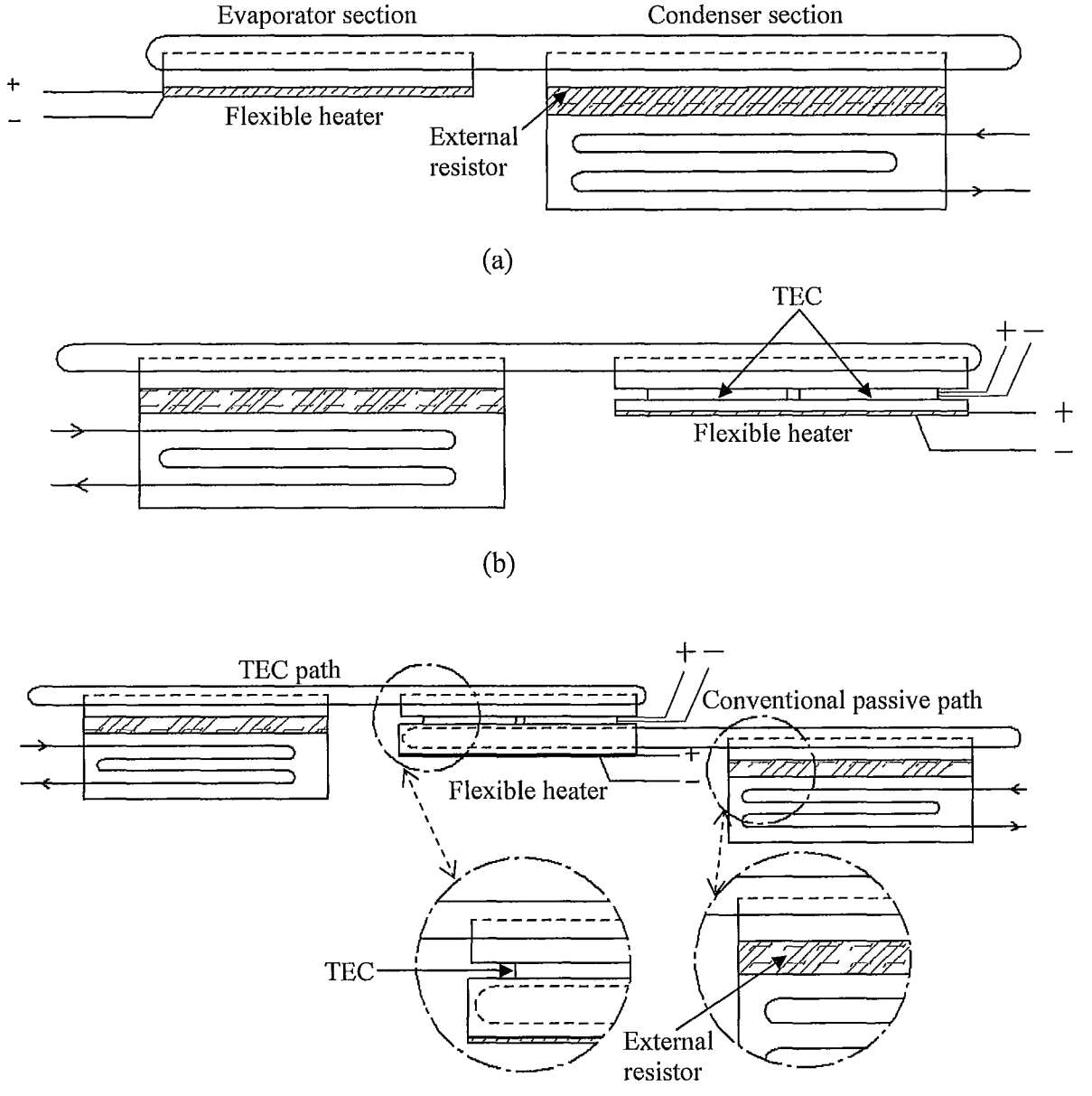


Figure 4.3: Schematic of different configurations experimented (a) only passive system (r_C = 1) (b) only thermoelectric cooler system (r_C = 0) and (c) hybrid system ($0 < r_C < 1$).

thermal resistance of the heat sinks in the conventional passive or TEC path. These resistances can be obtained from Eqn. 3.5 and 3.11. The TEC modules were powered by an Agilent 6655A 500 Watt System DC Power Supply (0~120 V, 0~4 A). The two cold plates used in the experiments were identical and fabricated in house out of Aluminum blocks. A schematic of the cold plate is shown in Figure 4.4. Each cold plate had a six pass serpentine loop, with a gasket between the body of the cold plate and the top aluminum lid for proper sealing. The bottom surface of the cold plate had two grooves (120 mm X 0.75 mm X 0.75 mm), to accommodate thermocouples. The grooves were located at 8 mm from the left and right edges in Figure 4.4 (b).

The heat pipe unit shown in Figure 4.5 (a) consists of two heat pipes connected at one end to the evaporator heat spreader (80 mm X 75 mm X 6 mm, aluminum) and the other end to the condenser heat spreader (120 mm X 75 mm X 6 mm). The same heat pipe unit is used for the only passive ($r_C = 1$), only TEC ($r_C = 0$) and for the TEC path in the hybrid system ($0 < r_C < 1$). T-type thermocouples were embedded along two 0.75 mm X 0.75 mm grooves on the flat surfaces on the evaporator and condenser heat spreaders. The heat pipe unit used as the conventional passive path in the hybrid system ($0 < r_C < 1$) shown in Figure 4.5 (b) consists of two heat pipes, one evaporator heat spreader (80 mm X 75 mm X 14 mm) and one condenser spreader (120 mm X 75 mm X 6 mm). The evaporator heat spreader thickness in this case was 14mm and had flat surfaces on both sides to attach the heater on one side and thermoelectric modules on the other side. This heat pipe unit has a total of six groves on its three flat surfaces (two flat surfaces on the evaporator heat spreader and one on the condenser heat spreader (Figure 4.5 (b)) where the

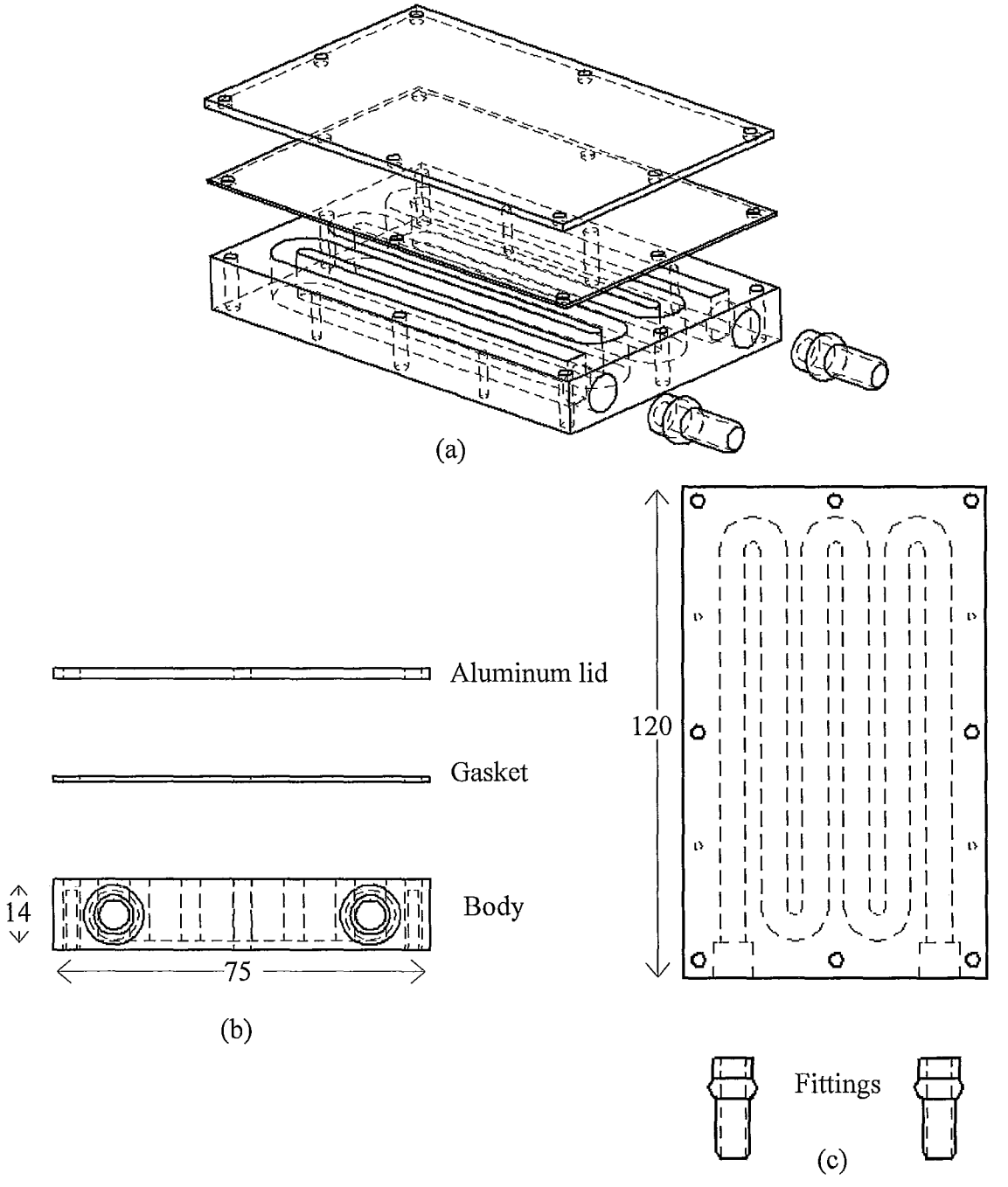


Figure 4.4: Schematic of the cold plate (a) isometric view, (b) front view and (c) top view. (all units are in mm).

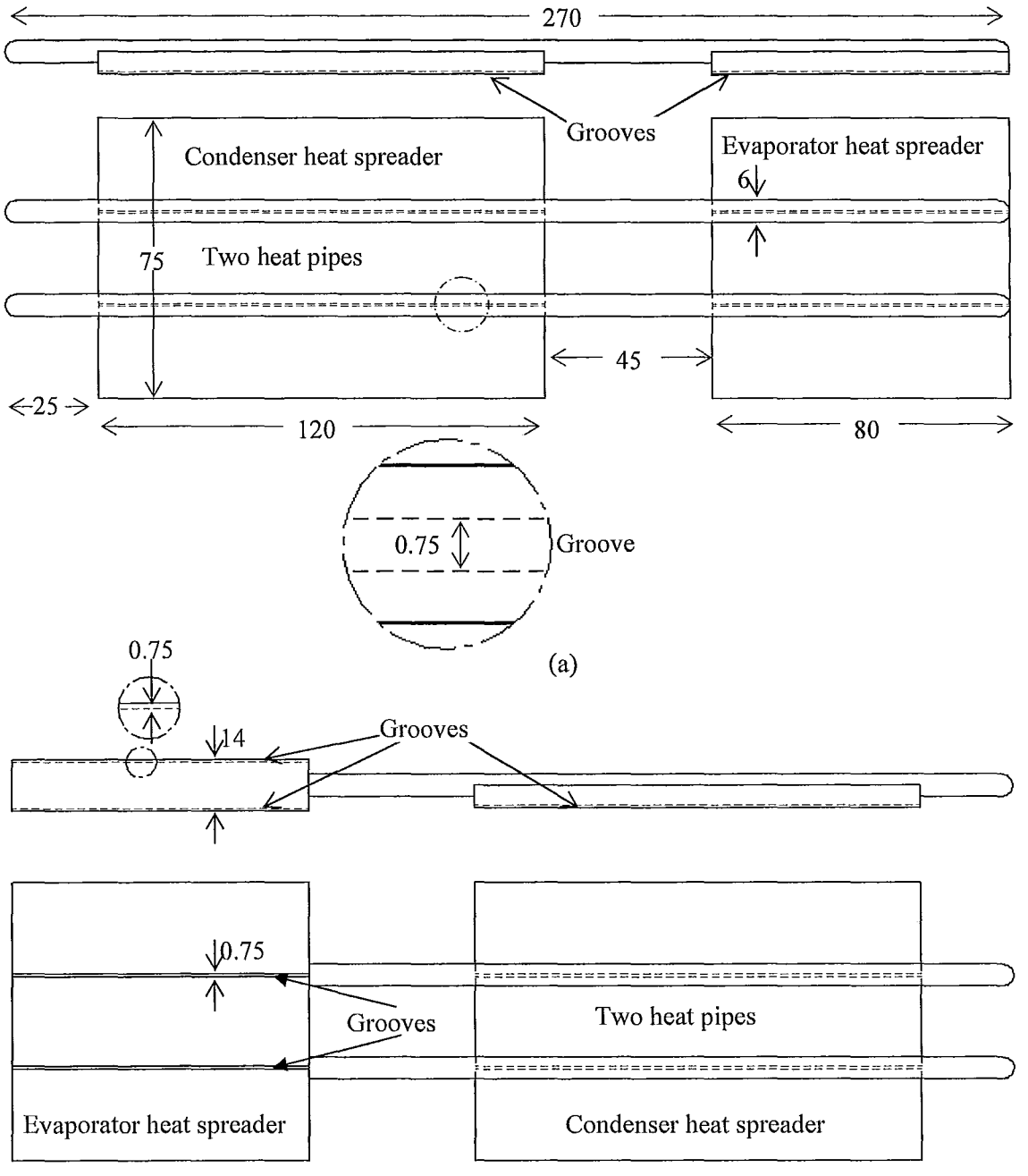


Figure 4.5: Schematic of heat pipe units (a) for only passive system ($r_C = 1$) or only thermoelectric cooler system ($r_C = 0$) or the TEC based active path in the hybrid system ($0 < r_C < 1$) and (b) for the conventional passive path in the hybrid system ($0 < r_C < 1$). (all units are in mm).

other one has four grooves on the two flat surfaces (Figure 4.5 (a)) to accommodate T-type thermocouples. Each heat pipe on both the heat pipe units is extended by 25 mm at the condenser heat spreader to compensate for any non-condensable gas. The 270 mm long copper-water heat pipes have a sintered wick with an outside diameter of 6 mm. The cross sectional view of the heat pipes is shown in Figure 4.6.

The thermoelectric cooler modules used were Melcor CP1.4-127-06L (39.9 mm X 39.9 mm X 3.81 mm) with 127 thermocouples and 0.7 mm thick ceramic substrate layers on both sides (Figure 4.7). The n and p-type semiconductors are Bismuth-Telluride (Bi_2Te_3) alloy. The manufacturer's specifications are presented in Table 4.1 and APPENDIX A.

The hybrid system was instrumented with a total of thirty six T-type thermocouples as shown schematically in Figure 4.8. Two thermocouples were located between the heater and the evaporator heat spreader on the conventional passive path, two between the other flat surface of the evaporator heat spreader of the conventional passive path and the cold side ceramic of the thermoelectric modules, two between the hot side ceramic of the thermoelectric modules and the evaporator heat spreader of the TEC path. Two thermocouples were located between the condenser heat spreader and the external resistor and between the external resistor and the cold plate on both the conventional passive and the TEC paths. Three thermocouples were installed on the surface of each heat pipe of the conventional passive path and four on each heat pipe of the TEC path. One thermocouple was used on the insulation of the heater and cold plates used for both conventional passive and TEC paths. Two thermocouples were placed on the insulation of the inlet and outlet water flow. The last thermocouple was used to measure room ambient temperature.

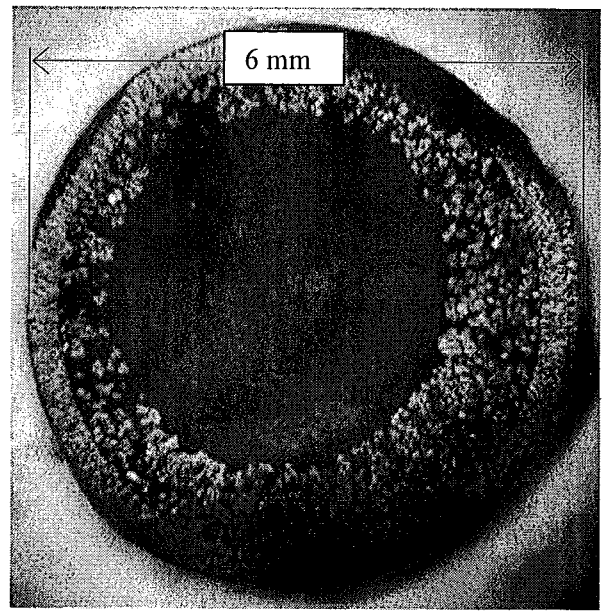


Figure 4.6: Cross sectional view of the heat pipes.

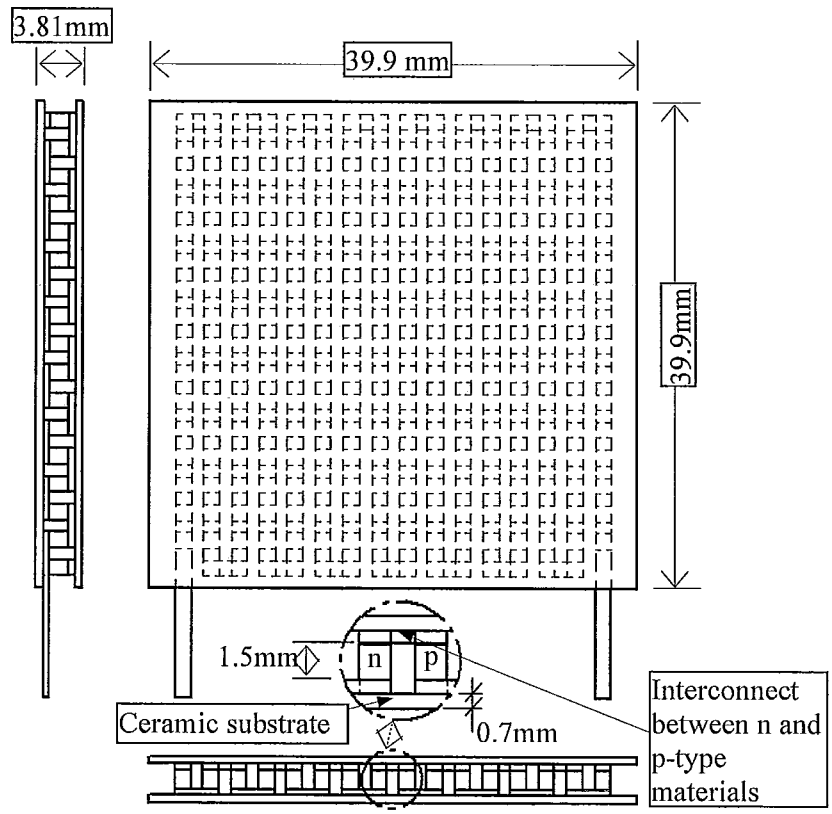


Figure 4.7: Schematic of thermoelectric module (CP 1.4-127-06L).

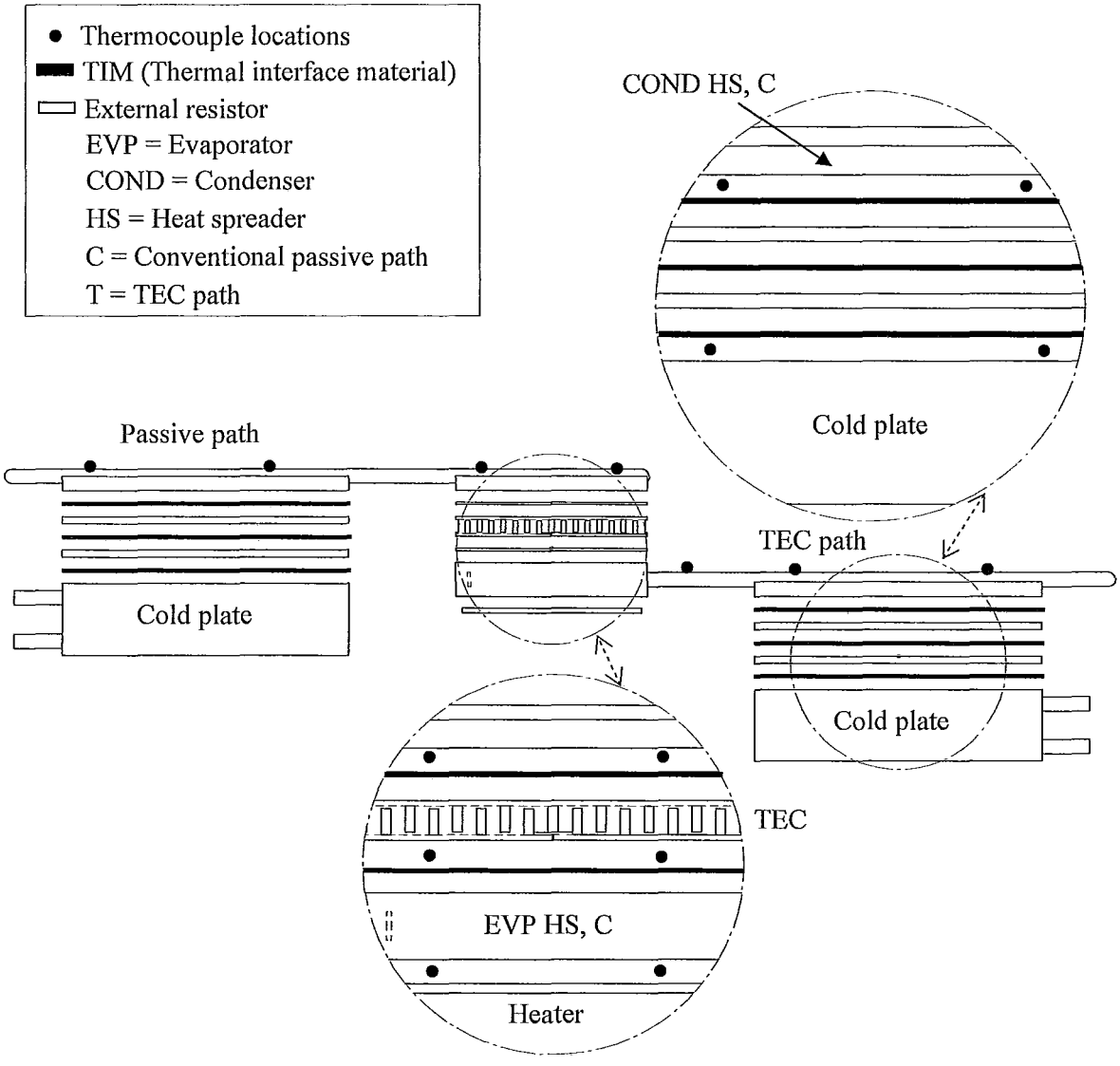


Figure 4.8: Location of the T-type thermocouples in the hybrid system.

Table 4.1: Specification data for thermoelectric module (CP 1.4-127-06L)

Parameter	Values
G (m)	0.00118
N	127
I_{max} (A)	6
V_{max} (V)	15.4
Bulk size (mm^3)	39.9 X 39.9 X 3.81

4.2. EXPERIMENTAL METHODOLOGY

Experiments were performed for the conventional passive (r_C = 1), only TEC (r_C = 0) and hybrid systems with r_C = 0.33 and 0.5. For all experiments, the chiller was first started and water temperature was set to the desired simulated ambient temperature. Once the water temperature reached steady state, the water was circulated through the cold plate(s). The heater was turned on and the heat load to the heater was set to the desired value using the variable transformer. For the only passive system (r_C = 1), experiments were performed at ambient temperatures of 30, 40, 50, 60 and 70 °C while for the only TEC system (r_C = 0) or hybrid systems with r_C = 0.33 and 0.5 experiments were performed at ambient temperatures of 30, 40, 50 and 60°C. The safe design temperature of the chip was assumed to be 85°C as this is a conservative value for most of the recent computer processors. The simulated chip temperatures were measured for different heat loads into the flexible heater. In case of only TEC system (r_C = 0) or the hybrid systems ($0 < r_C < 1$), experiments were performed for a range of DC current to the TEC modules. The appropriate current ranges for the different systems were obtained using the model. The

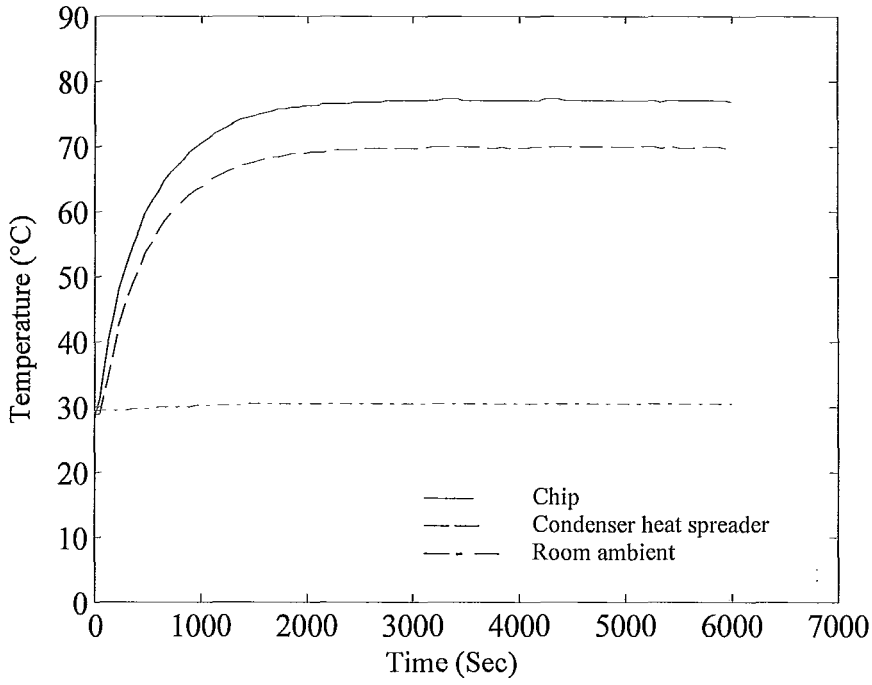


Figure 4.9: Transient analysis of the system.

heat dissipation from the chip at a given applied current to the TEC modules can be estimated from the model for a simulated ambient temperature when $T_{chip} = T_{design}$. The simulated heat dissipation capacity of the system at that simulated ambient temperature and applied current to the TEC modules was obtained from the curve fit of the experimental data when $T_{chip} = T_{design}$.

All readings were recorded once the entire system reached steady state. Steady state was determined by recording the temperatures over time. Typical temperature profile of different components with respect to time is presented in Figure 4.9. It was found that all the components in the system reached steady state after 60 minutes as the slope of the temperature profile of any component in the system after 60 minutes was less than 5%.

4.3. DATA ANALYSIS

The heat transfer into the evaporator heat spreader for any configuration is determined from an energy balance of the electrical heater. The electric power into the flexible heater would primarily be transferred into the heat spreader with a small loss through the insulation by natural convection. Thus the heat input into the evaporator section is given by

$$Q_{in} = Q_{heater} - Q_{nat\_heater} \tag{4.1}$$

where Q_{heater} is the input electrical power to the heater and is given by

$$Q_{heater} = V_{heater} I_{heater} \tag{4.2}$$

and V_{heater} and I_{heater} are the voltage drop across and current passing through the flexible heater, respectively. Natural convection heat loss to the surrounding through the insulation of the heater is given by

$$Q_{nat\_heater} = hA_{ins\_heater}\left(T_{ins\_heater} - T_{room\_amb}\right) \tag{4.3}$$

The heat transfer coefficient, h, was estimated using a correlation for heat transfer from a flat, horizontal surface (Kreith and Bohn, 2001). A_{ins_heater} is the surface area of the heater insulation exposed to the room ambient and T_{ins_heater} is the surface temperature of the insulation. The natural convection heat loss from the heater insulation was never more than 7% of the measured electrical power.

The heat removed from the system, Q_{out}, was estimated by

$$Q_{out} = Q_{water} - Q_{nat} \tag{4.4}$$

where Q_{water} is the heat transfer to the circulating water through the cold plates and is given by

$$Q_{water} = \dot{m}_C C_p (T_o - T_i)_C + \dot{m}_T C_p (T_o - T_i)_T \qquad 4.5$$

where $\dot{m}$ is the mass flow rate of the circulating water in the cold plate, C_p is the specific heat of water, T_o is the outlet water temperature of the cold plate, T_i is the inlet water temperature of the cold plate and the suffix C and T stands for conventional passive path and TEC path respectively.

The natural convection heat loss or gain through the insulation of the condenser section(s) and the ambient is estimated as,

$$Q_{nat} = hA(T_{ins} - T_{room\_amb}) \qquad 4.6$$

where A is the surface area of the insulation of the condenser section and T_{ins} is the surface temperature of corresponding condenser section.

An energy balance was performed for the hybrid systems with r_C = 0.5 at a simulated ambient temperature of 30 °C and is shown in Figure 4.10. The energy balance agreed to within ±10%. Similar energy balances were obtained for other cases.

To determine the heat dissipation from the heater at a particular simulated ambient temperature at T_{chip} = 85°C, a number of different heat loads were applied to the heater and the corresponding simulated chip temperatures were recorded. Chip temperature increased linearly with increased heat load applied and the linear fit of the experimental data agrees quite well with the model prediction. The comparison between model prediction and linear fit of the experimental data is shown in Figure 4.11 for the hybrid systems with r_C = 0.5 at

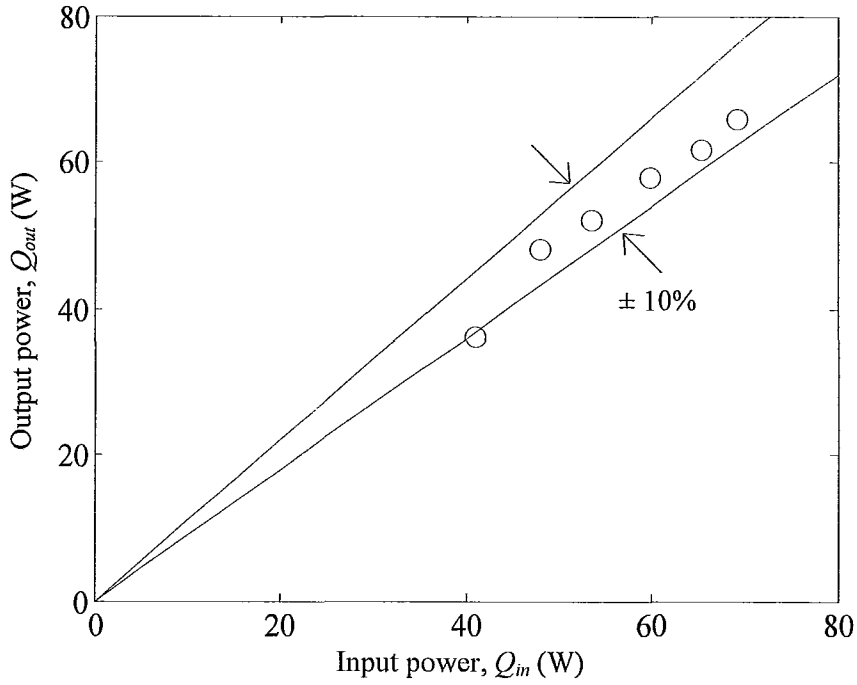


Figure 4.10: Corrected energy balance.

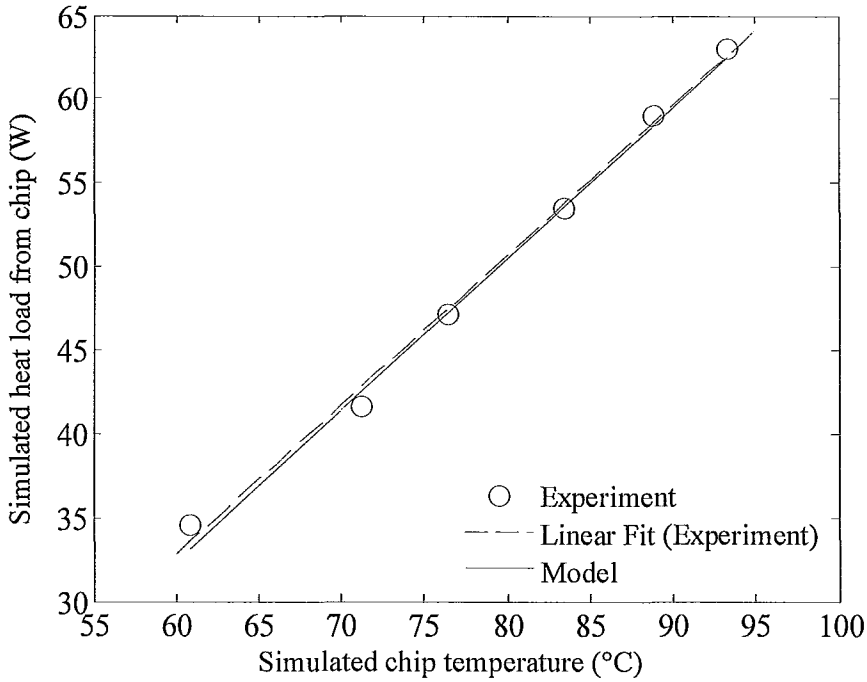


Figure 4.11: Variation of chip temperature with applied heat load to the chip.

a simulated ambient temperature of 30°C. Similar agreements were observed for only TEC (r_C = 0), only passive (r_C = 1) or the hybrid system with r_C = 0.33. As the agreement is very good, for other experiments only three data points were taken and from there the heat dissipation from the heater at T_{chip} = 85 of a system was obtained.

4.4. Determination of Component Properties

Parameters such as the thermal conductivity of the ceramic substrate and thermal resistance of the heat pipe unit(s) and the acrylic glass were unknown. Hence, independent experiments were performed to determine these parameters.

4.4.1. Thermal Conductivity of Ceramic Substrate (Alumina, Al_2O_3)

The ceramic substrate was taken off the thermoelectric module. The inter-connect metal traces between n and p-type materials were cleaned using different grades of sand papers. The thermal conductivity of the ceramic substrate was determined using the experimental setup shown in Figure 4.12. The ceramic substrate of the TEC module was sandwiched between two aluminum blocks (40 mm X 40 mm X 25 mm) with a thermal interface material (thermal conductivity of 8.7 $Wm^{-1}K^{-1}$) applied between the two sides of the substrate and the aluminum blocks to reduce the contact resistances. Each block had five embedded thermocouples. Three of them were located 10mm apart in the vertical direction to measure the temperature gradient along the heat flow and two others were

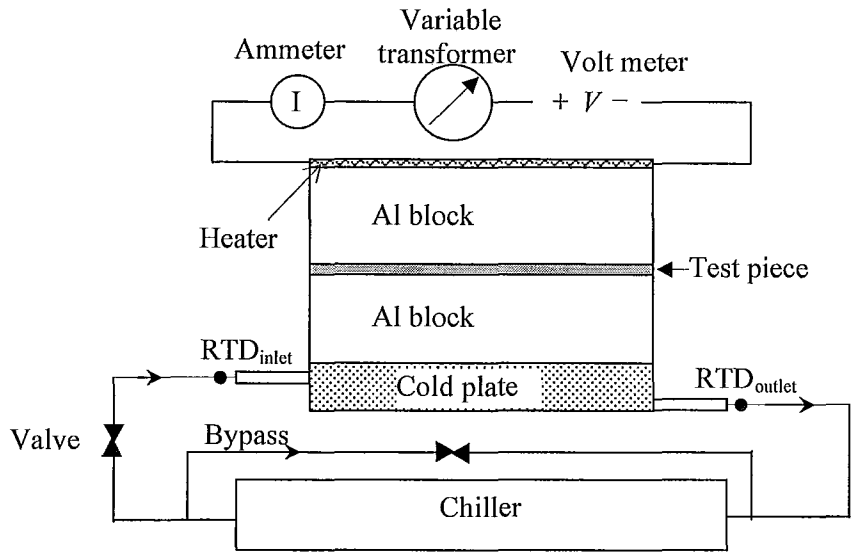
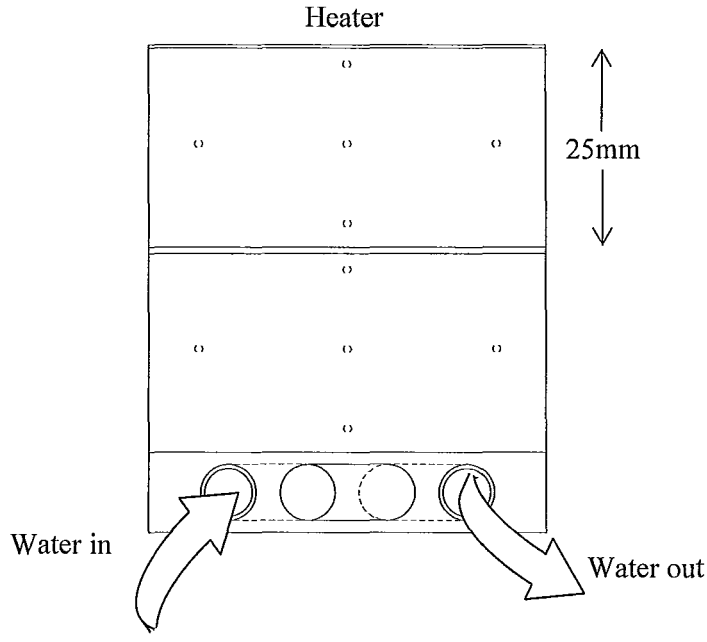


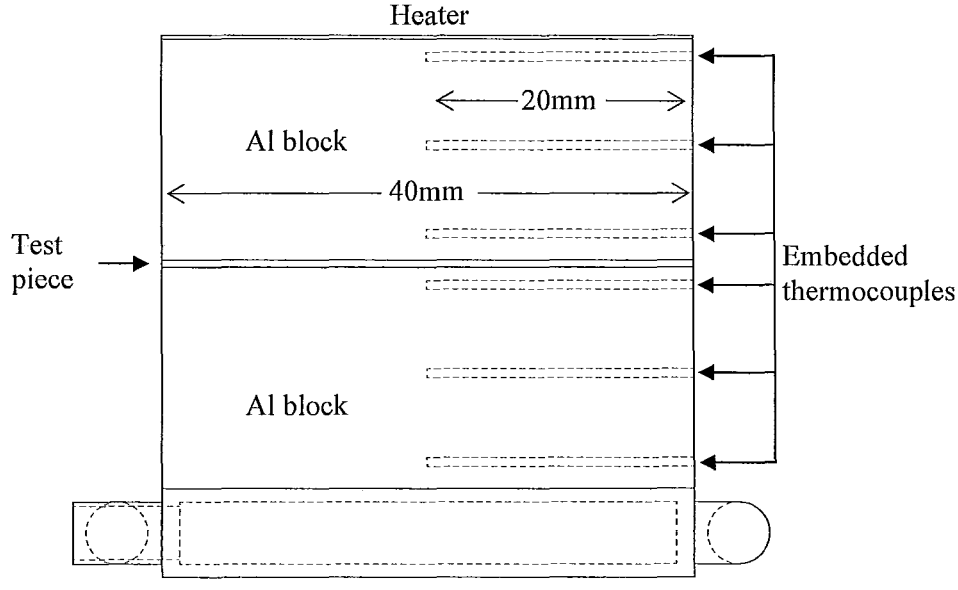
Figure 4.12: Schematic of the experimental setup to measure thermal conductivity of ceramic substrate.

located 15 mm apart from the location of the centre thermocouple in the horizontal direction to check the uniformity of the temperature in the cross stream direction. A flexible heater was placed over the top aluminum block as the heat source and a cold plate was used under the bottom aluminum block to remove the heat. The power to the heater was controlled using a variable transformer. The heat removed at the cold plate was controlled by varying the water temperature and the flow rate using a bypass valve. The entire setup was well insulated with fibre glass. The detailed schematic of the set up and location of the embedded thermocouples are shown in Figure 4.13. The surface temperature of the two sides of the ceramic substrate incorporating the thermal interface material was obtained by linear extrapolation of the experimental data to the substrate surfaces. The temperature difference across the thickness of the substrate incorporating the thermal interface material was used to estimate the composite conductivity of the ceramic

substrate and thermal interface material. The linear extrapolation of the experimental data is shown in Figure 4.14 for an applied heat load of 37 W. The thermal conductivity of ceramic substrate at different operating temperatures is shown in Figure 4.15. The experimental result shows that there is a slight temperature dependence of the thermal conductivity with operating temperature. For the model, the thermal conductivity was assumed to be temperature independent with a nominal value of 3.66 $Wm^{-1}K^{-1}$.



(a)



(b)

Figure 4.13: Schematic of the experimental facility showing the locations of the embedded thermocouples in the aluminum blocks (a) front view and (b) side view.

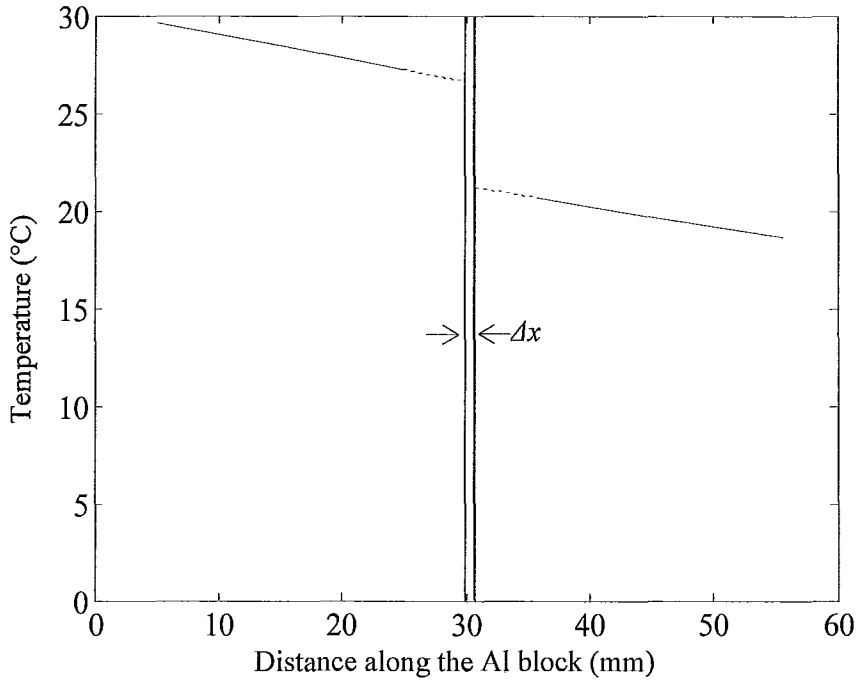


Figure 4.14: Temperature distribution along the aluminum blocks to obtain the surface temperatures of the ceramic substrate.

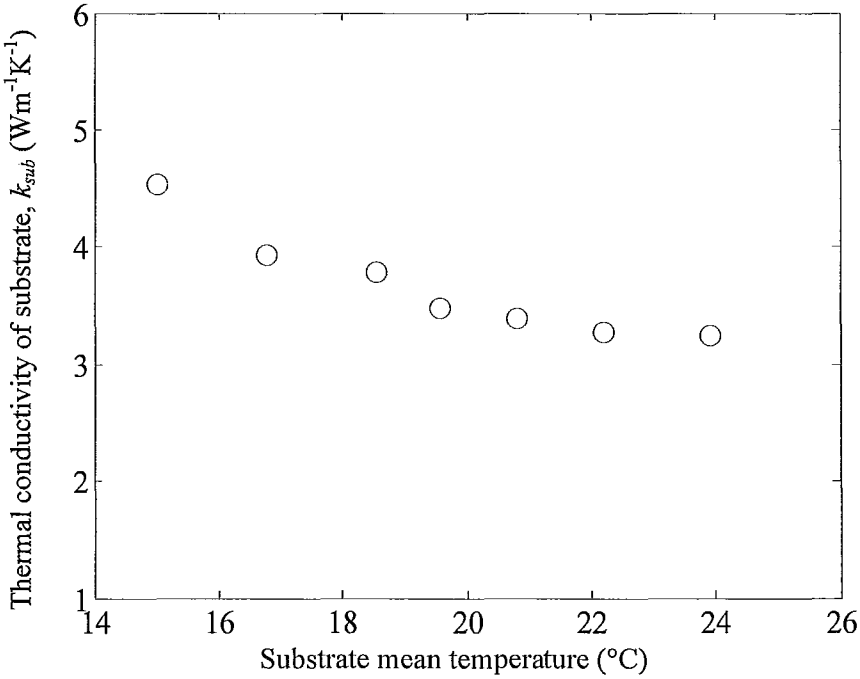


Figure 4.15: Thermal conductivity of the ceramic substrate at different mean temperatures.

4.4.2. Thermal Resistance of the Heat Pipe Units

The thermal resistances of the heat pipe units shown in Figure 4.5 were determined independently. For this experiment, a flexible heater with a variable transformer was placed in contact with the evaporator heat spreader to provide the thermal load to the heat spreader. The heater was connected through a power meter to measure the power input to the system. The condenser heat spreader was attached to the cold plate. Two T-type thermocouples were attached on the evaporator heat spreader and two on the condenser heat spreader. All sides were insulated using fiber glass insulation to reduce extraneous heat losses. The temperatures and the heat input to the heater were recorded once the system reached steady state. The thermal resistances of the heat pipe units are shown in Figure 4.16 and Figure 4.17 respectively.

At low heat loads the non- condensable gases in the heat pipe occupies a significant portion of the condenser due to the low vapor pressure and thus result in high thermal resistance (Dube at el., 2004). At moderate heat loads the thermal resistance remains almost constant (which is its working zone) and increases sharply when the maximum heat transportation capacity of the heat pipe is reached. This is because the evaporator temperature increases due to dry-out at the evaporator beyond maximum heat transportation capacity of the heat pipe. Nominal values of 0.3 °C/W and 0.2 °C/W were used in the model for the corresponding heat pipe units.

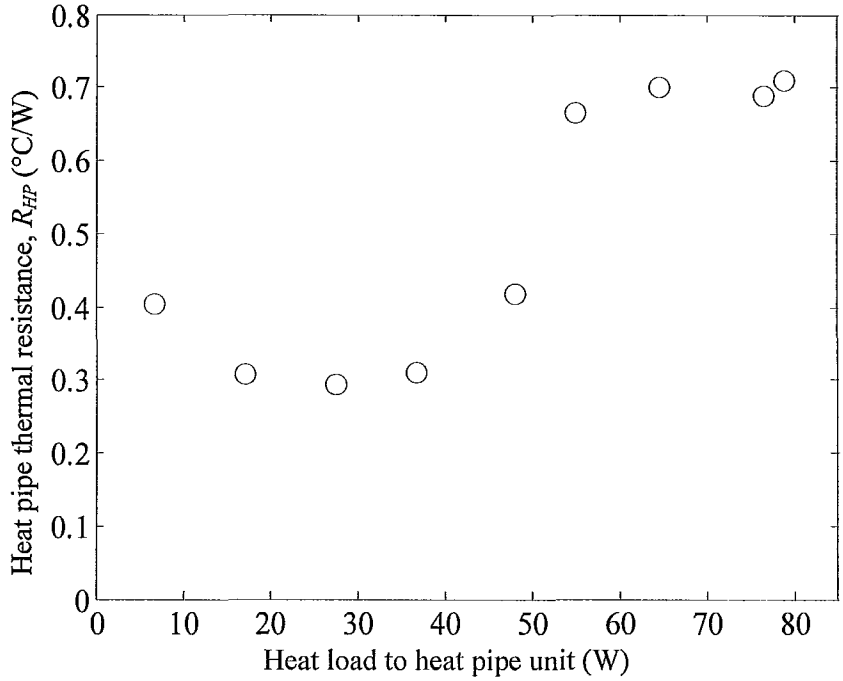


Figure 4.16: Thermal resistance of heat pipe unit shown in Figure 4.5 (b).

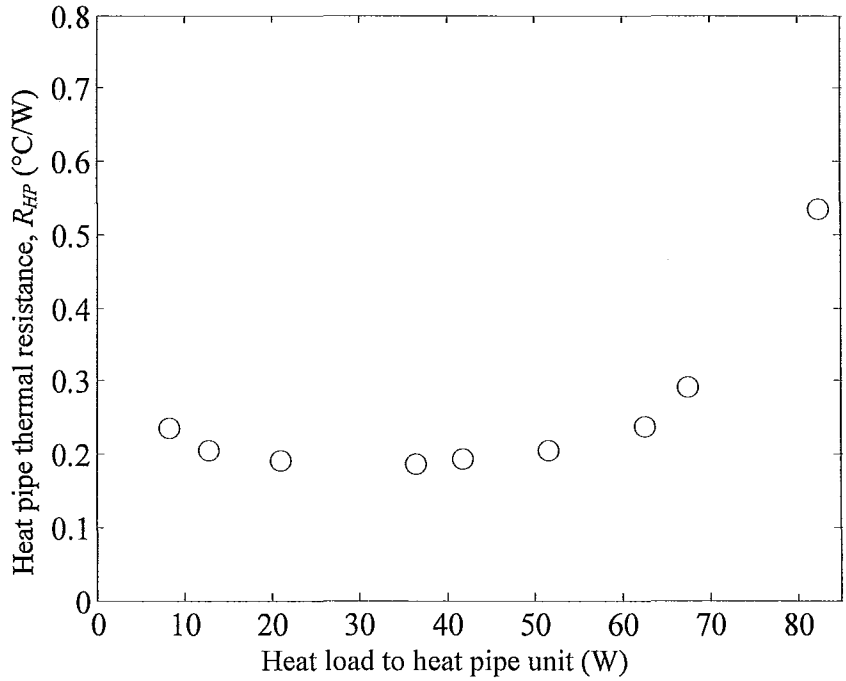


Figure 4.17: Thermal resistance of heat pipe unit shown in Figure 4.5 (a).

4.4.3. Thermal Resistance of Acrylic

For the conventional passive system (r_C = 1) and only TEC system (r_C = 0), one layer of acrylic glass was used to simulate the natural convection thermal resistance of the fin plate. The acrylic layer was 120 mm X 75 mm X 1.5 mm thick. In case of the hybrid system with r_C = 0.5, two layers of the acrylic glass were used in each path and when r_C = 0.33, three layers were used in the conventional passive path and 1.5 layer in the TEC path. The acrylic layers were sandwiched between the condenser heat spreader of the heat pipe unit and the cold plate (Figure 4.3 (a)). The same thermal interface material was used between the acrylic layer(s) and the condenser heat spreader or the cold plate. Two T-type thermocouples were embedded in the grooves on the condenser heat spreader and two others in the grooves on the cold plate. A flexible heater with a variable transformer was used on the evaporator heat spreader as the heat source and the supplied heat was dissipated by the cooling water. Temperature difference across the layer(s) of acrylic glass was recorded for a range of applied heat loads and the corresponding thermal resistance of the acrylic layer(s) was determined. Thermal resistance of one, two and three layers of acrylic glasses is shown in Figure 4.18. A nominal mean value of 0.77 °C/W was used in the model for one layer of acrylic which simulates the thermal resistance of the entire heat sink at natural convection. Experimental thermal conductivity of the acrylic glass for a range of temperature is shown in Figure 4.19 and results from previous studies are presented in Table 4.2. Though the results from previous studies were at lower temperatures than the ones in this study they were within the same approximate range.

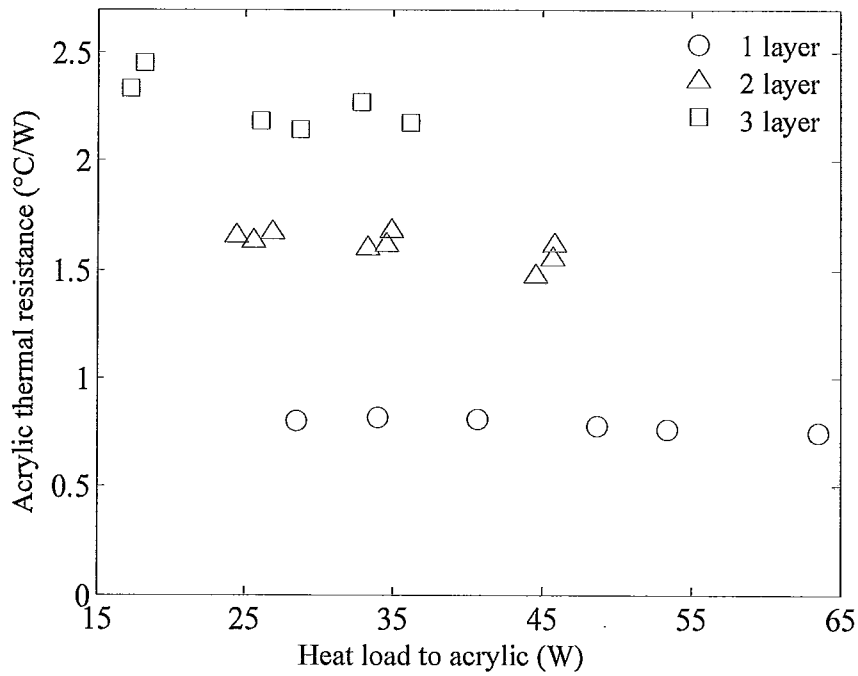


Figure 4.18: Thermal resistance of different layers of acrylic glass.

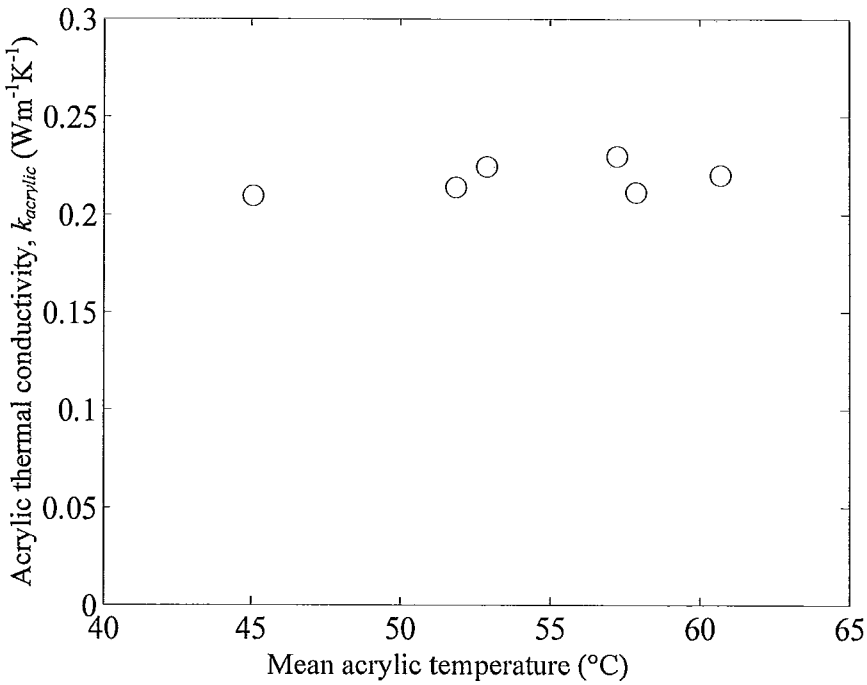


Figure 4.19: Thermal conductivity of acrylic glass at different mean temperatures.

Table 4.2: Thermal conductivity of acrylic from previous studies (Miller and Kotler, 1993)

Mean Temperature (°C)	Thermal Conductivity ($Wm^{-1}K^{-1}$)	Reference
23	0.179	Miller and Kotler, 1993
25	0.192	Krischer and Esdorn, 1955
23	0.152	Lucks et al., 1952
40	0.193	Brown and Otten, 1988
20	0.189	Eiermann, 1961

4.5. UNCERTAINTY ANALYSIS

The uncertainty associated with the calculated parameters were quantified using the method outlined by Kline and McClintock (1953). The uncertainty of a parameter f, using this method is defined as

$$\Delta f = \sqrt{\sum_{i=1}^{n}\left(\frac{\partial f}{\partial x_i}\Delta x_i\right)^2} \qquad 4.7$$

where x_i are the independent variables on which the parameter f depends, i.e.

$$f = f(x_1, x_2, \ldots\ldots, x_n) \qquad 4.8$$

The uncertainties of the various measurement devices are summarized in Table 4.3.

One example case of evaluating the uncertainty associated with the heat load to the flexible heater is presented here. The voltage across and the current through the heater for the case considered is 87 V and 0.66 A respectively. Heat load to the heater is obtained using Eqn. 4.2.

$$Q_{heater} = V_{heater}\, I_{heater}$$

$Q_{heater} = 57.42W$

$u(V_{heater}) = \pm 3$ % of the reading = 2.61 V

$u(I_{heater}) = \pm 2$ % of the reading = 0.0132 A

$u(Q_{heater}) = [\{V_{heater} * u(I_{heater})\}^2 + \{I_{heater} * u(V_{heater})\}^2]^{0.5}$

$u(Q_{heater}) = 2.07$ W = 3.61% < 5%

The uncertainties of the calculated quantities used in the analysis are summarized in Table 4.4.

Table 4.3: Uncertainty of the measured quantities

Measurement (Symbols)	Device(s)	Uncertainty
AC Current to Heater (I_{heater})	Extech True RMS Power Multimeter	± (2 %)
AC Voltage to Heater (V_{heater})	Extech True RMS Power Multimeter	± (3 %)
Water Temperature (T_o, T_i)	Platinum RTD & Omega DP251 Precision Thermometer	± 0.014 °C
	Platinum RTD & Paperless Recorder VG06 Reader	0.03 – 0.08 °C for an operating range of 0 – 100 °C
Water Flow Rate ($\dot{m}$)	Exact Flow Dual rotor Turbine Flow-meter & Omron K3NR Rate Meter	0.19 %
	Omega FTB601B Turbine Flow-meter & Omega DPF700 Rate Meter	1 %
Temperature	Omega T-type thermocouple	± 0.5 °C
DC Current to TEC (I_{TEC})	Aligent 6655A DC Power Supply	0.15% + 15mA
DC Voltage to TEC (V_{TEC})	Aligent 6655A DC Power Supply	0.07% + 30mV

Table 4.4: Uncertainty of the calculated quantities

Quantity	Equation	Uncertainty
Electrical Power to Heater	$Q_{heater} = V_{heater} I_{heater}$	± 20% for Q<8W ± 15% for 8<Q<35W ± 5% for 35<Q<75W
Water Temperature Rise	$T_o - T_i$	± 0.0198 °C for TEC path ± 0.063 °C for Conventional Passive Path
Heat Gain by Water	$Q_{water} = \dot{m}_C C_p (T_o - T_i)_C + \dot{m}_T C_p (T_o - T_i)_T$	± 20% for Q<15W ± 15% for 15<Q<30W ± 5% for 30<Q<75W
Heat Pipe Effective Thermal Resistance	$R_{HP} = \frac{T_{EVP} - T_{COND}}{Q_{heater}}$	± 0.014 °C/W
External Resistor's Thermal Resistance	$R_{acrylic} = \frac{T_{hot} - T_{cold}}{Q_{heater}}$	± 0.026 °C/W

Chapter 5 RESULTS & DISCUSSION

The objective of the experiments was to validate the model predictions within the experimental uncertainty. The results for the conventional passive system (r_C = 1) is presented first as a reference thermal management system, followed by the only TEC system (r_C = 0) and finally the hybrid systems with r_C = 0.5 and 0.33.

5.1. Conventional Passive Thermal Management System (r_C = 1)

The conventional passive system in this study is a heat pipe unit as shown in Figure 4.3 (a) which simulates the practical thermal management system shown in Figure 4.2 (a). At a design chip temperature of 85 °C, the experimental maximum heat dissipation capacity and the model prediction are shown in Figure 5.1 as a function of operating ambient temperature. The model prediction is in good agreement with the experimental results within the experimental uncertainty. The maximum heat dissipation capacity decreases with an increase in ambient temperature, as expected. The region marked as T_{chip} < 85 °C is the safe operating zone where the chip temperature will be below its design

temperature. The region marked as $T_{chip} > 85$ °C is the region where the chip temperature is greater than its design temperature.

5.2. ONLY TEC SYSTEM ($r_C = 0$)

When only the thermoelectric cooler (TEC) system is used, there can be two modes of operation: (i) TEC electrically off mode and (ii) TEC electrically on mode. The TEC electrically off mode refers to the system when the TEC modules were turned off and the TEC modules thus act as a passive thermal resistor in the system. The variation of the maximum heat dissipation capacity with the ambient temperature for the TEC modules electrically off condition is shown in Figure 5.2 for an operating chip temperature of 85 °C. In this operating mode the maximum heat dissipation capacity at any ambient temperature was lower than that of the conventional passive system ($r_C = 1$). This is because the total thermal resistance in this system is significantly higher compared to the conventional passive system due to the higher thermal resistance of the TEC modules. The experimental results for the TEC modules in both the open and short circuit conditions are shown along with the model prediction for the open circuit case. The short circuit of the TEC off mode refers to the case where the two ends of the modules were electrically shorted while the open circuit refers to the case where the two ends of the TEC modules are electrically open. The model can not predict the performance of the TEC off condition for short circuit case as the current flowing through the entire circuit due to the Seebeck effect was unknown. However this current flow provides a better cooling of the chip due to the Peltier effect compared to the open circuit case and thus results in a higher heat dissipation capacity.

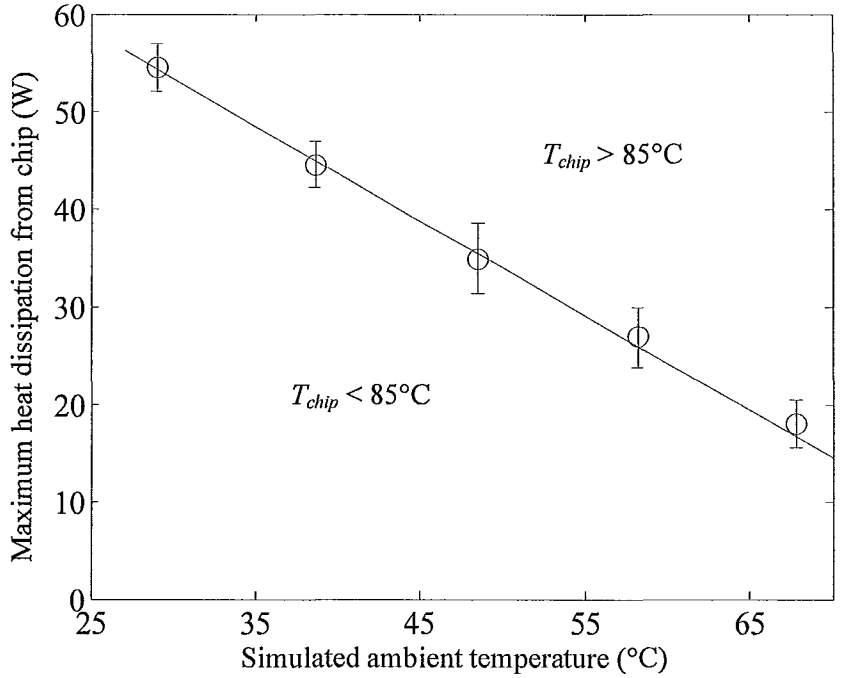


Figure 5.1: Variation in maximum heat dissipation capacity (○ Experiment, — Model) with ambient temperature for the conventional passive system (r_C = 1) at T_{chip} = of 85 °C.

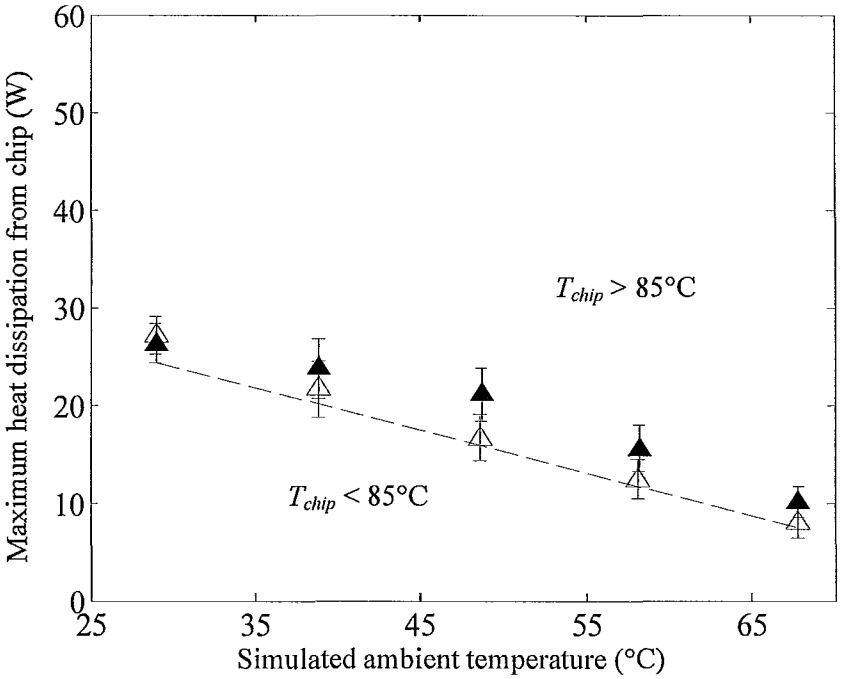


Figure 5.2: Variation in maximum heat dissipation capacity with ambient temperature for only TEC system (r_C = 0) off condition at T_{chip} = of 85 °C for Δ open circuit, ▲ short circuit and — — open circuit model prediction.

There is good agreement between the experimental results and the model predictions for the open circuit TEC off condition. As the safe operating envelope is much smaller than that for the conventional passive system, the TEC modules need to be electrically turned on to obtain a better performance. The maximum heat dissipation for the short circuited TEC modules show a slight improvement in the operational envelope, but is still significantly lower compared to the conventional passive system.

When the thermoelectric modules are powered on, the performance will depend on the applied DC current. For the TEC module the applied DC voltage across it or the input power depends on the applied current and the ambient temperature. Since the applied current is the independent variable, the performance characteristics are presented with respect to the applied DC current.

The variation in experimental and predicted chip temperatures for the only TEC system ($r_C = 0$) with applied electric current to the TEC modules is shown in Figure 5.3 for a fixed ambient temperature of 38.5 °C and a fixed heat load of 30 W. There is a range of electric current for which the chip temperature is below its safe design temperature. For the particular example presented in Figure 5.3, this range is approximately from 0.63 A to 2.45 A. The lower current is of interest here as it will result in a higher overall coefficient of performance for the system due to the lower input power to the TEC modules. The coefficient of performance of the system, COP_{sys} is defined as the ratio of the heat dissipation from the chip to the input electric power to the TEC modules and is shown in Figure 5.4 for different applied currents to the TEC modules for the case shown in Figure 5.3. The COP_{sys} decreases as the applied DC current increases. To achieve the highest

COP_{sys} while maintaining the chip temperature below its safe design temperature the applied current has to be the lowest within the operating current range. For the example presented the highest COP_{sys} is approximately 19 corresponding to an operating current of approximately 0.63 A. The model predictions are within ± 2% of the experimental results for chip temperature and for the system *COP* for the particular example presented here.

The corresponding family of curves for different heat dissipation from the chip at an ambient temperature of 40 °C obtained from the model are shown in Figure 5.5. As the heat dissipation from the chip increases the operating range of the DC current to the TEC modules to keep $T_{chip} < 85$ °C decreases (Figure 5.5). The maximum heat dissipation capacity, Q_{max} is defined as the maximum amount of heat the system can dissipate while keeping $T_{chip} = T_{design}$. The Q_{max} for a design temperature of 85 °C at the given ambient temperature of 40 °C is approximately 35 W with the corresponding COP_{sys} of 2.3 at an operating current of approximately 1.5 A (Figure 5.5).

The model predictions of the effect of the applied DC current on the heat dissipation from the chip at $T_{amb} = 30$ °C when $T_{chip} = 85$ °C for the only TEC system ($r_C = 0$) is shown in Figure 5.6. In thermoelectric cooling there are three important phenomena which determine the thermoelectric module performance. The Peltier effect at the cold side of the TEC modules cools the chip due to the applied DC current which is opposed by the Joule heating and the conduction of heat from the hot side to the cold side of the modules. Peltier cooling is linearly proportional to the applied current while the Joule heating is proportional to the current squared. The heat conduction from the hot side to the cold side of the TEC module depends on the temperature difference between the hot and the cold

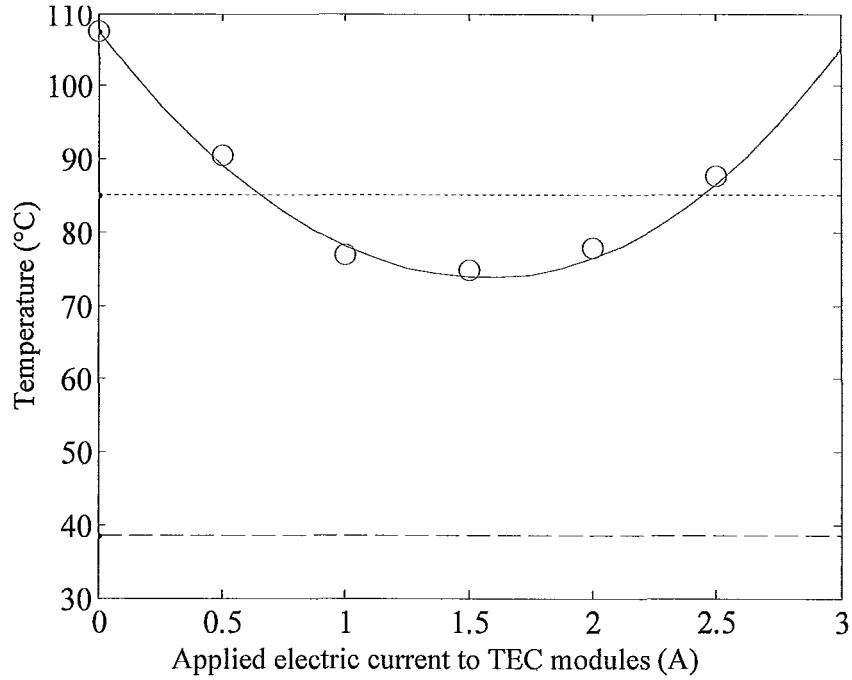


Figure 5.3: Effect of applied current on chip temperature (○ Experiment, — Model) for only TEC system ($r_C = 0$) at $Q_{chip} = 30$W and – – $T_{amb} = 38.5$ °C. (- - - $T_{design} = 85$ °C).

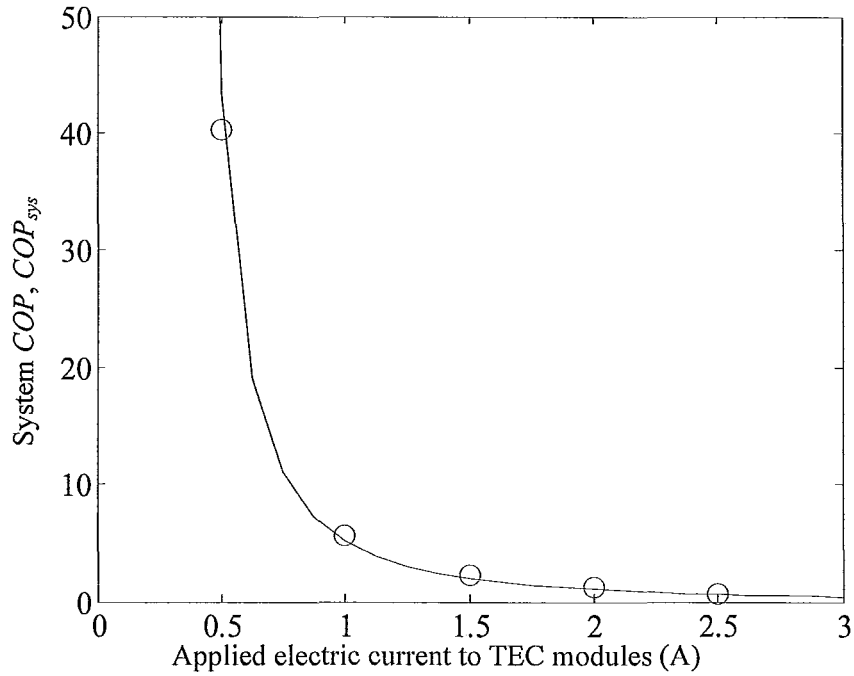


Figure 5.4: Effect of applied current on the system *COP* (○ Experiment, — Model) for only TEC system ($r_C = 0$) at $Q_{chip} = 30$ W and $T_{amb} = 38.5$ °C.

side temperature. The hot and cold side temperatures depend on the applied current, thus making the conduction heat nonlinear to the applied current. At the lower range of applied current to the TEC modules the net heat dissipation from the chip increases with an increase in applied current due to the pronounced Peltier effect over the Joule heating and the conduction. The heat dissipation reaches a maximum then decreases at higher currents due to the Joule heating and conduction becoming more prominent over the Peltier effect.

The effect of the applied DC current on the heat dissipation from the chip and the corresponding system *COP* at different ambient temperatures when T_{chip} = 85 °C are shown in Figure 5.7. Both the experimental data and model predictions for ambient temperatures of 29, 38.9, 48.6 and 58.2 °C are shown in these figures. The model predictions are in good agreement with the experimental results for both the heat dissipation from the chip and the system *COP* within the experimental uncertainty. The results show that when T_{chip} = 85 °C at a certain applied current to the TEC modules, the only TEC system (r_C = 0) can dissipate more heat at lower ambient temperature and less heat at higher ambient temperature (Figure 5.7 (a)). The area below the curve for a given ambient temperature marked as T_{chip} < 85 °C refers to the operating zone where the chip temperature is below its design temperature, while the area marked as T_{chip} > 85 °C refers to the zone where chip temperature will be higher than its safe design temperature. The operating zone to maintain T_{chip} < 85 °C is greater for lower ambient temperature and reduces when ambient temperature increases. At a given ambient temperature there is a

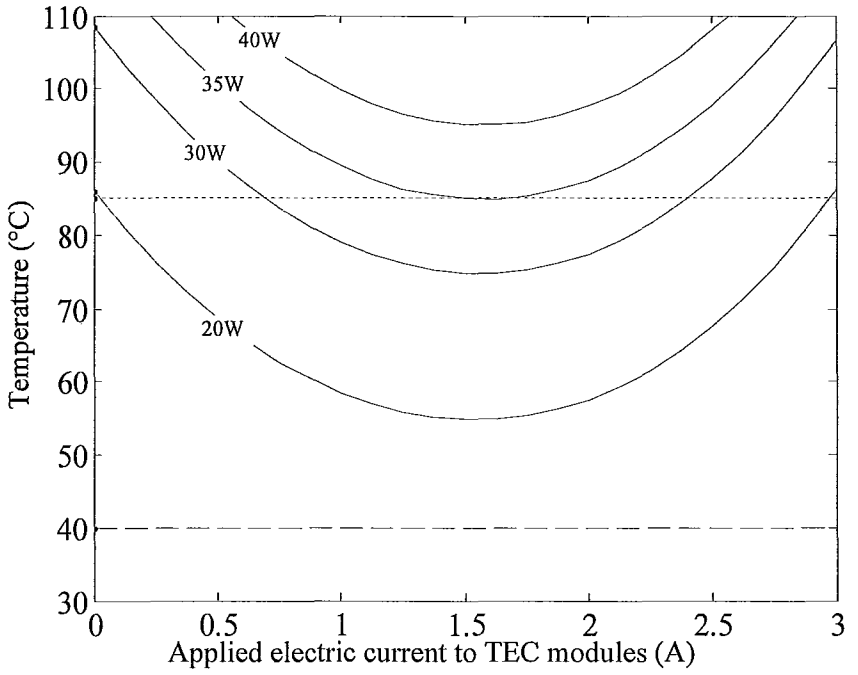


Figure 5.5: Model prediction of chip temperature at different heat loads from chip and different applied currents for only TEC system ($r_C = 0$). —— T_{chip}, - - - T_{design} (85 °C) and — — T_{amb} (40 °C).

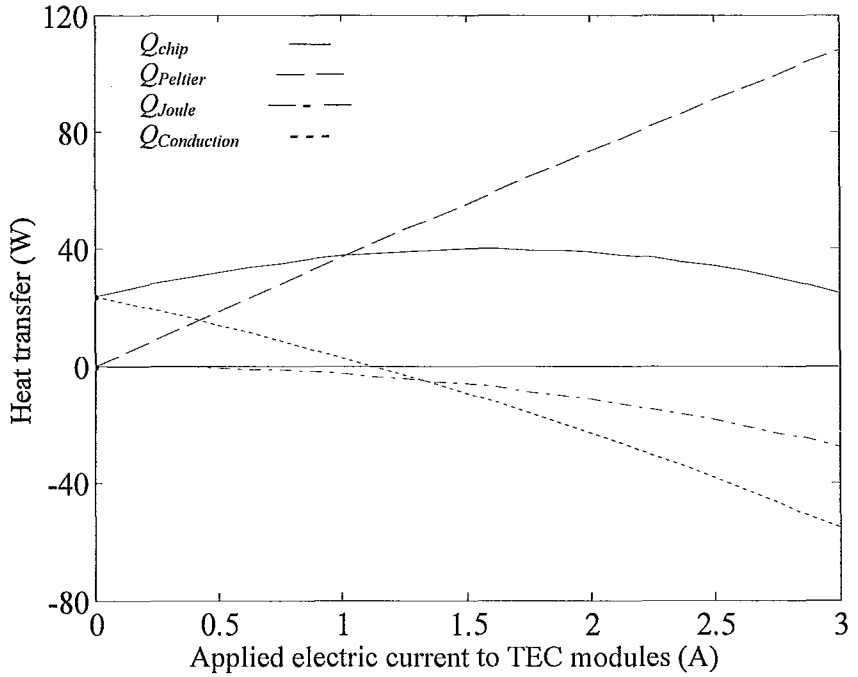


Figure 5.6: Peltier effect, Joule heating and conduction in a TEC module at T_{amb} = 30 °C and T_{chip} = 85 °C.

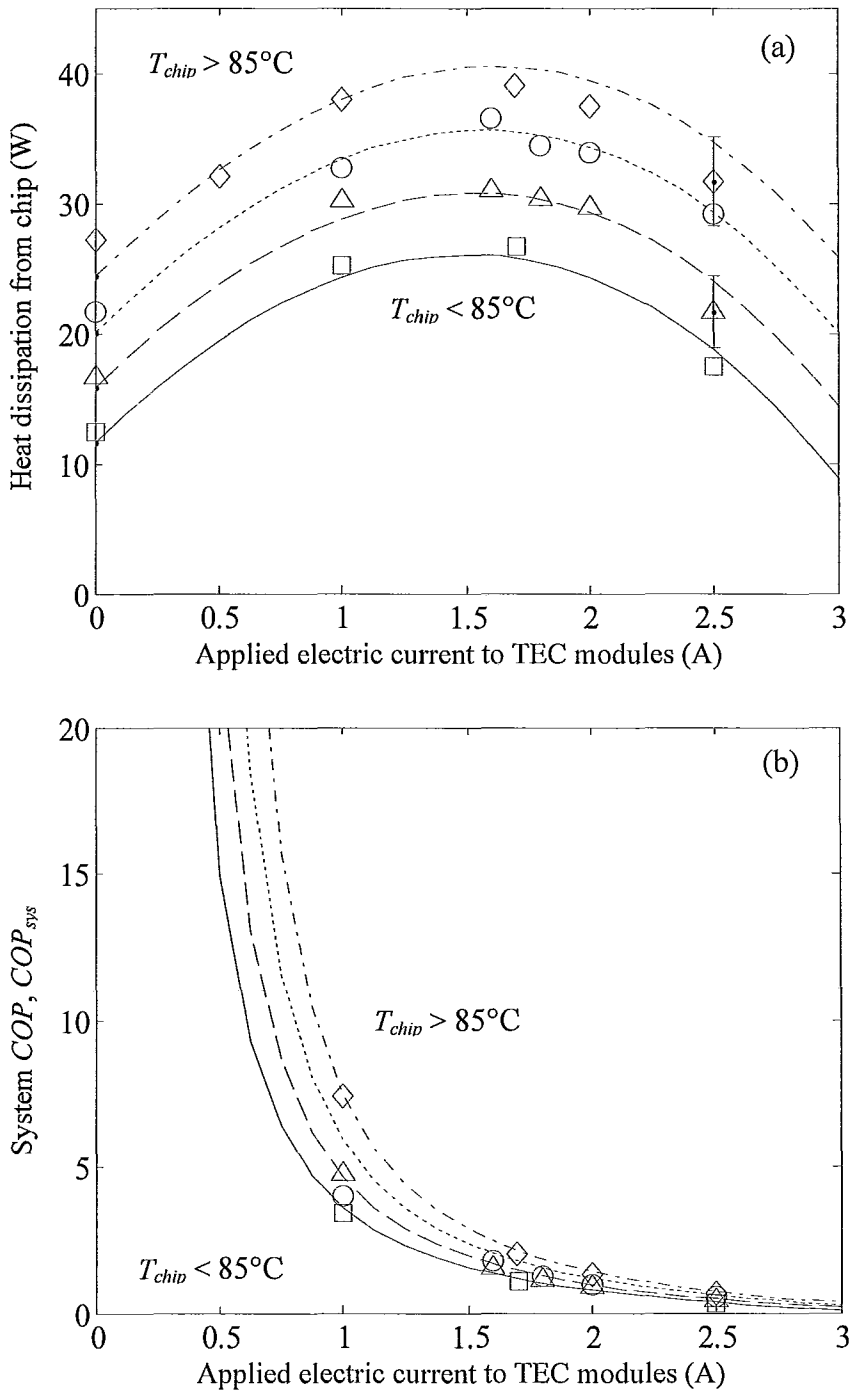


Figure 5.7: Variation of (a) heat dissipation from chip and (b) system COP with applied current at T_{amb} = 29 °C (◊ Experiment, — - — Model), 38.9 °C (○ Experiment, - - - Model), 48.6 °C (△ Experiment, — — Model) and 58.2 °C (□ Experiment, — Model) for only TEC system (r_C = 0) at T_{chip} = 85 °C.

range of current that can be applied to the TEC modules to dissipate a given amount of heat from the chip while maintaining the chip temperature below its design value. The lowest current in the range is of interest as it will result in a higher system *COP* (Figure 5.7 (b)).

The maximum heat dissipation capacity, Q_{max} at a given ambient temperature was obtained from a curve fit to the experimental data of Figure 5.7 (a). The Q_{max} at an ambient temperature can also be determined from the model. The associated DC current to achieve the Q_{max} at an ambient temperature is defined as the optimum current, I_{opt}. At any ambient temperature the I_{opt} was approximately the same from the curve fit to the experimental data and the model which for the only TEC system ($r_C = 0$) is approximately 1.6 A.

The experimental and model Q_{max} results at different ambient temperatures are shown in Figure 5.8 for only TEC system ($r_C = 0$) at on mode. As the ambient temperature increases the maximum heat dissipation capacity decreases to keep the chip temperature below its design temperature. The region denoted by $T_{chip} < 85$ °C would be the operational zone of the system.

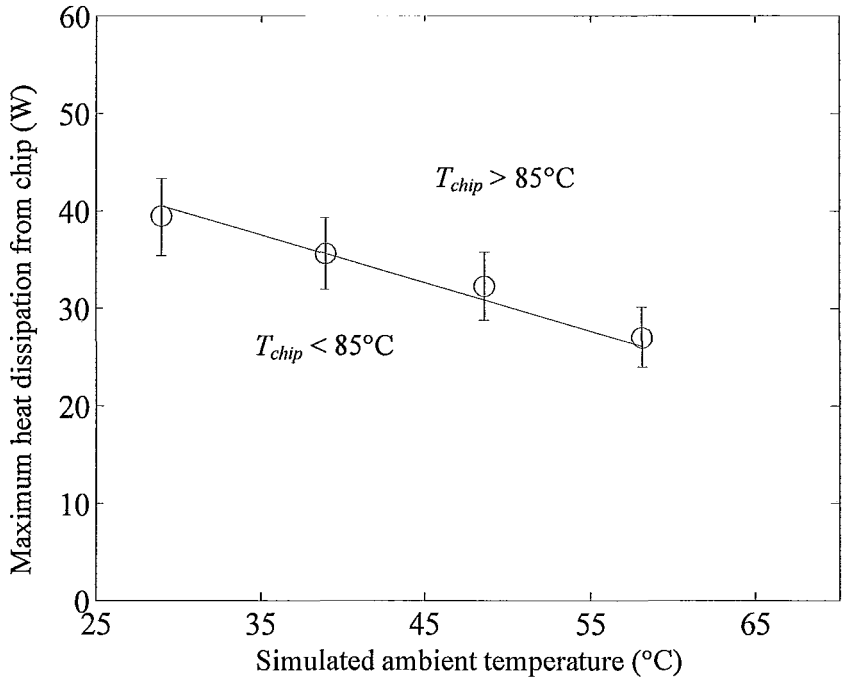


Figure 5.8: Variation in maximum heat dissipation capacity (○ Experiment, —— Model) with ambient temperature for only TEC system ($r_C = 0$) on condition at T_{chip} = 85 °C.

5.3. HYBRID SYSTEM

The performance of the hybrid system will depend on the fraction of the total heat sink area dedicated to each path. The thermal resistance of the heat sink dedicated to each path can be expressed from Eqn. 3.5 and 3.11as

$$R_{\infty,C} = \frac{1}{r_C} R_{\infty,tot} \qquad 3.5$$

$$R_{\infty,T} = \frac{1}{1-r_C} R_{\infty,tot} \qquad 3.11$$

where $R_{\infty,tot}$ is the thermal resistance of the entire heat sink area, $R_{\infty,C}$ and $R_{\infty,T}$ are the thermal resistances of the heat sink area corresponding to the passive and TEC paths respectively. For instance when r_C = 0.5, 50% of the total heat sink area is dedicated to each path and the heat sink thermal resistance will be twice the thermal resistance of the total heat sink. For r_C = 0.33, 33% of the total heat sink area is dedicated to the conventional passive path with the rest dedicated to the TEC path. In terms of thermal resistance, the heat sink thermal resistance for the conventional passive path would be three times the total heat sink resistance while it would be 1.5 times the total heat sink resistance for the TEC path. The hybrid system can be operated with the TEC system in the (i) Electrically off mode and (ii) Electrically on mode.

5.3.1. Hybrid System with $r_C = 0.5$

The thermal resistance of the TEC path is greater than the heat pipe based passive path when the TEC modules are not powered on. Thus the heat transfer through the passive path will be greater than through the TEC path in this case. The experimental data shows that about 60% of the heat dissipation from the chip was transported through the passive path and the rest through the TEC path at the off mode. The variation of the maximum heat dissipation capacity with the ambient temperature for T_{chip} = 85 °C is shown in Figure 5.9. The model prediction is within ± 2% of the experimental results for the open circuit TEC off condition.

The effect of applied DC current to the TEC modules on the chip temperature is presented in Figure 5.10 for two different heat loads for the hybrid system with r_C = 0.5. The model predictions are within ± 2.5 and ± 2% of the experimental results for the chip temperature at the heat dissipations of 37.2 and 43.5 W respectively at an ambient temperature of 38.6 °C. There is a range of electric current for which the chip temperature remains below its safe design temperature of 85 °C. For the heat dissipation of 43.5 W this range is approximately from 0.4 to 1.7A while for 37.2 W the current ranges approximately from -0.1 to 2.2 A. When the heat load from the chip increases, this operating range of the electric current decreases.

The corresponding experimental and model prediction of the coefficient of performance of the entire system, COP_{sys} for the different applied current to the TEC modules are shown in Figure 5.11. The model predictions are within ± 4% and ± 5% for

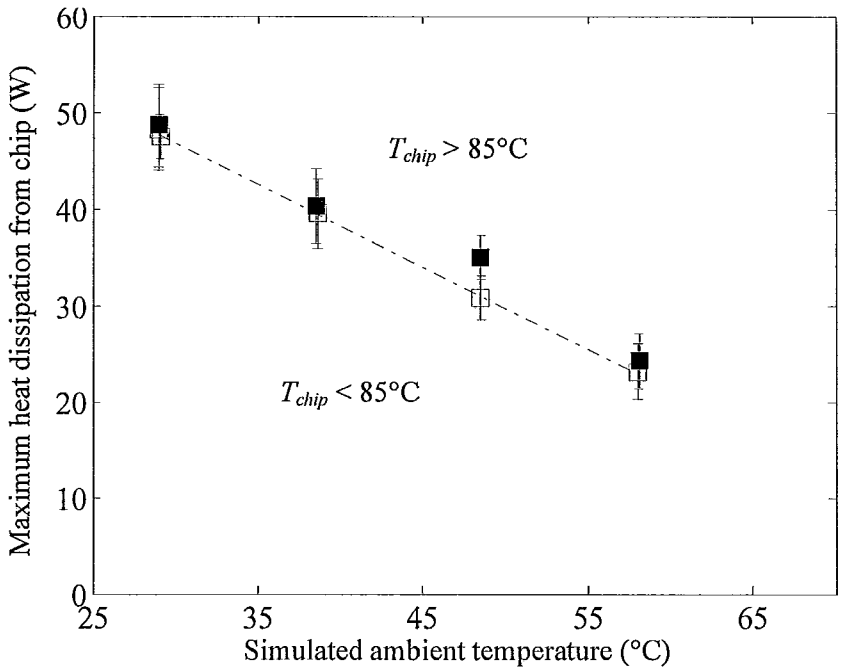


Figure 5.9: Variation in maximum heat dissipation capacity with ambient temperature for hybrid system with r_C = 0.5 off condition at T_{chip} = 85 °C for □ open circuit, ■ short circuit and — - — open circuit model prediction.

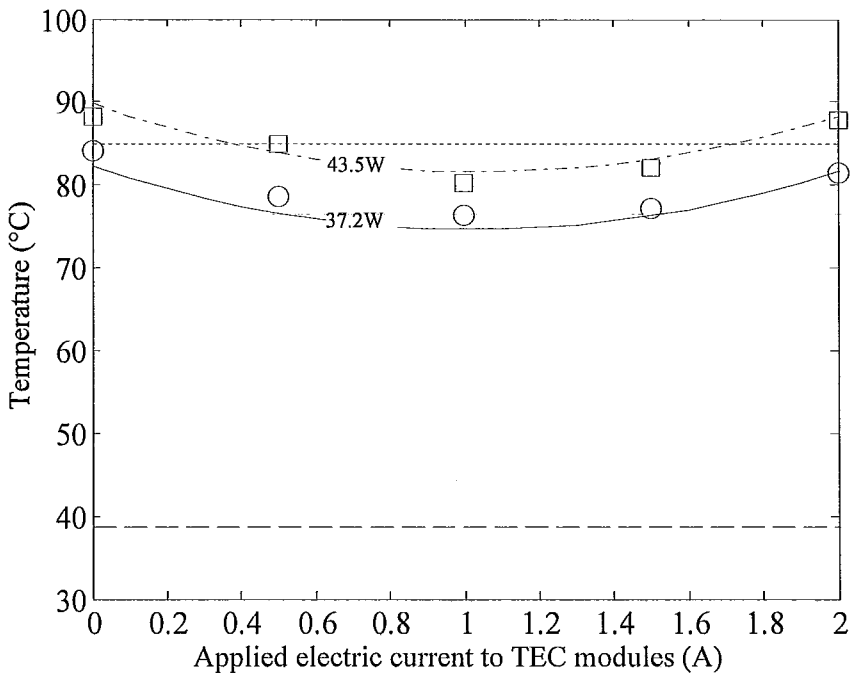


Figure 5.10: Effect of applied current on chip temperature for hybrid system with r_C = 0.5 at Q_{chip} = 37.2 W (○ Experiment, — Model) and 43.5 W (□ Experiment, — - — Model) at — — T_{amb} = 38.6 °C. (- - - T_{design} = 85 °C).

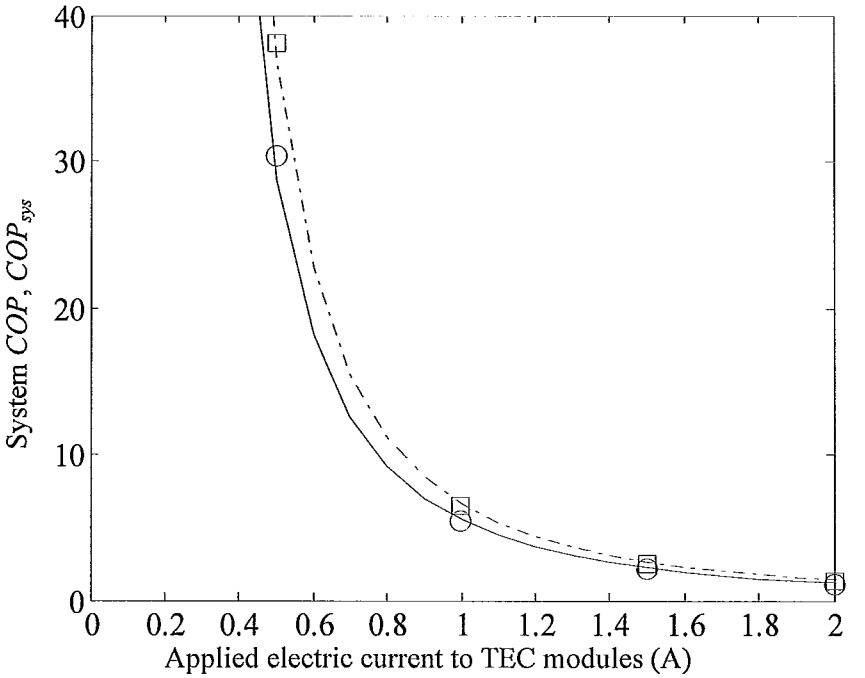


Figure 5.11: Effect of applied current on system *COP* for hybrid system with $r_C = 0.5$ at $Q_{chip} = 37.2$ W (○ Experiment, — Model) and 43.5 W (□ Experiment, — - — Model) at $T_{amb} = 38.6$ °C.

the system *COP* at heat dissipation of 37.2 and 43.5 W respectively. To achieve the highest COP_{sys} while maintaining the chip temperature below its safe design temperature the applied current has to be the lowest of the operating current range. For example, when the heat load from the chip is 43.5 W, the corresponding COP_{sys} while keeping $T_{chip} < 85$ °C are 55 and 2 at the two boundary currents of approximately 0.4 and 1.7 A respectively. Thus the COP_{sys} can be significantly improved by selecting the lowest current of the operating current range. This operating current for a given heat load from chip and a known ambient temperature can be obtained either by solving the governing equations or graphically from Figure 5.10.

The effect of ambient temperature on the heat dissipation from the chip at $T_{chip} =$ 85 °C for the hybrid system with $r_C = 0.5$ for a range of applied DC current to the TEC modules are presented in Figure 5.12. Both heat dissipation (Figure 5.12(a)) and system *COP* (Figure 5.12(b)) model predictions are in quite good agreement with the experimental data.

The maximum heat dissipation capacity, Q_{max} at an ambient temperature was obtained from a curve fit to the experimental data as it was done for the only TEC system ($r_C =$ 0). The Q_{max} was also obtained from the model and the model predictions are compared to the experimental data in Figure 5.13 for the hybrid system with $r_C = 0.5$ at on mode. The model predictions are in good agreement with the experimental results within the experimental uncertainty.

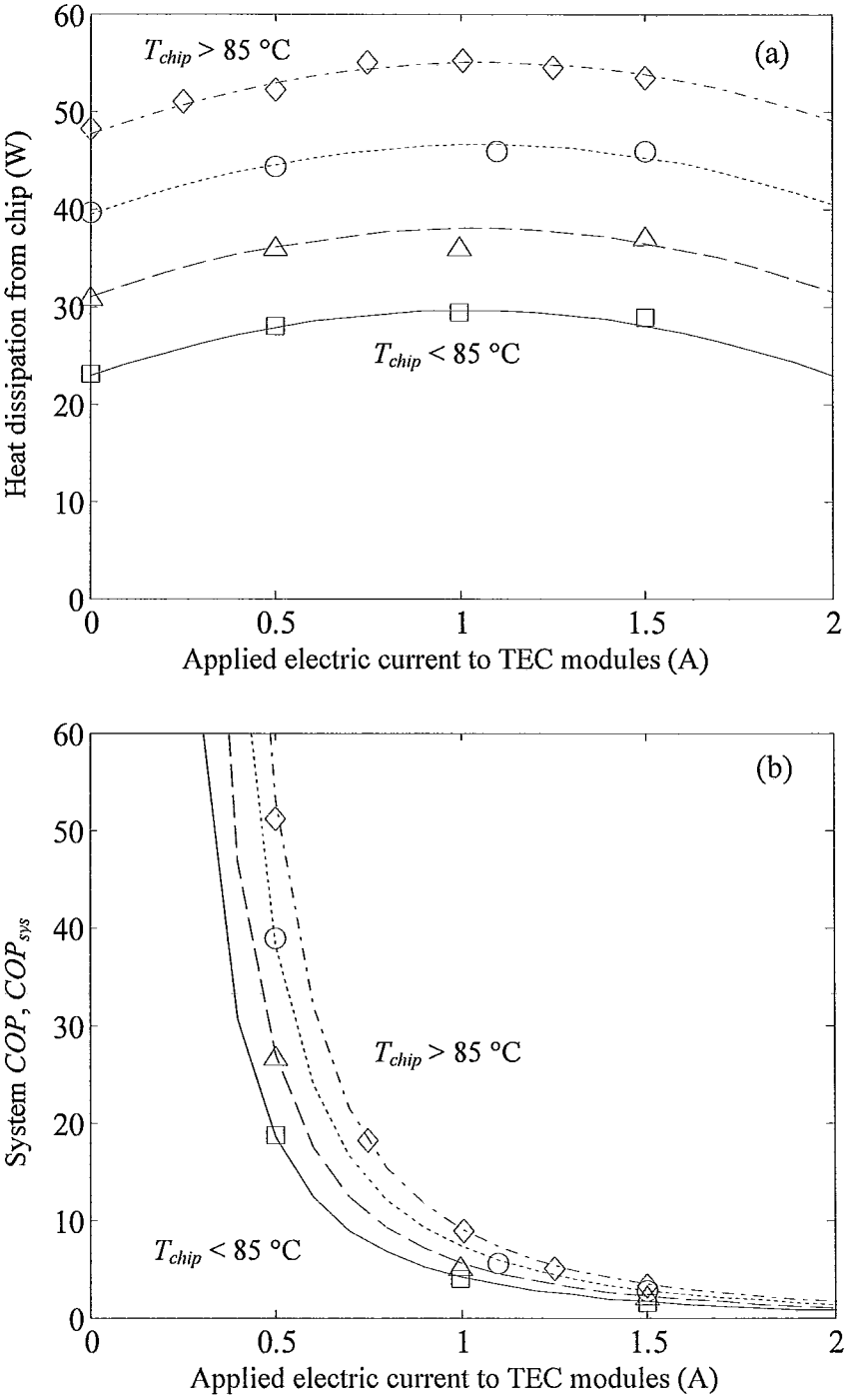


Figure 5.12: Variation of (a) heat dissipation from chip and (b) system COP with applied current at T_{amb} = 29 °C (◊ Experiment, — - — Model), 38.6 °C (○ Experiment, - - - Model), 48.5 °C (Δ Experiment, — — Model) and 58 °C (□ Experiment, —— Model) for hybrid system with r_C = 0.5 and at T_{chip} = 85 °C.

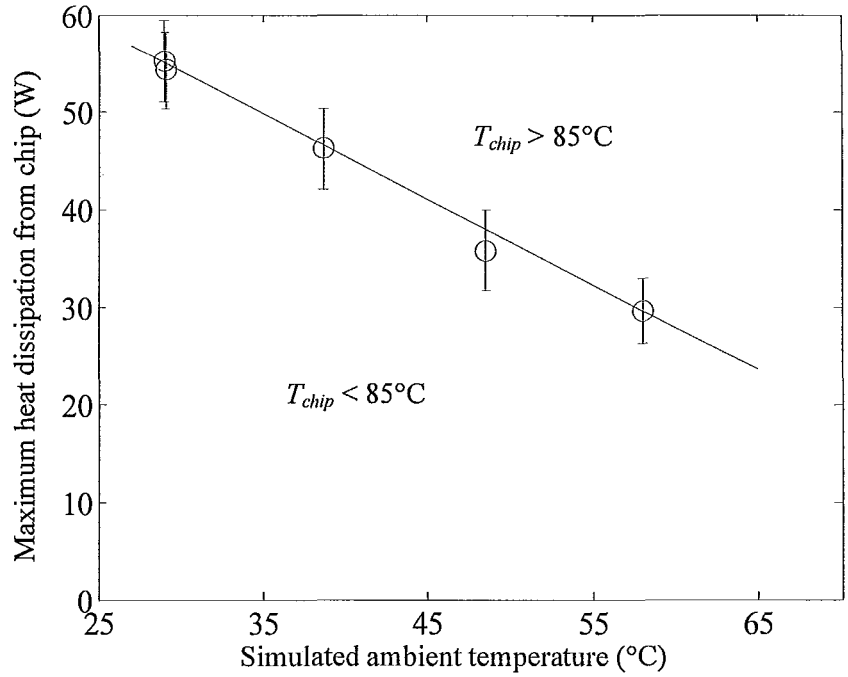


Figure 5.13: Variation in maximum heat dissipation capacity (○ Experiment, —— Model) with ambient temperature for hybrid system with r_C = 0.5 on condition at T_{chip} = 85 °C.

5.3.2. Hybrid System with $r_C = 0.33$

When the TEC modules are turned off, about 53% of the heat dissipation from the chip is transported through the TEC path and the rest through the conventional passive path for the hybrid system with $r_C = 0.33$ as in this case the thermal resistance of the TEC path is smaller than that of the conventional passive path. The variation of the maximum heat dissipation capacity with the ambient temperature is shown in Figure 5.14 for $T_{chip} = 85$ °C. The model prediction is in good agreement with the experimental result within the experimental uncertainty for the open circuited TEC off condition.

The variation of chip temperature and the corresponding system *COP* with the applied electric current to the TEC modules when the heat dissipation from the chip is 40 W at an ambient temperature of 39.1 °C is shown in Figure 5.15 and Figure 5.16 respectively for the hybrid system with $r_C = 0.33$. The model prediction for the chip temperature and the system *COP* are within ± 3% and ± 10% respectively of the experimental results. The operating current ranges from approximately 0.4 to 2.2 A to maintain the chip temperature below its design point of 85 °C. The corresponding system *COP* is in the range of 95 and 1.1 respectively.

Several experiments were performed for a range of ambient temperature and applied current keeping $T_{chip} =$ 85 °C for the hybrid system with $r_C = 0.33$ and the experimental results along with the model predictions are shown in Figure 5.17. The variation of maximum heat dissipation capacity with the operating T_{amb} is shown in Figure 5.18 for the curve fitted Q_{max} obtained from Figure 5.17 (a) and the model prediction.

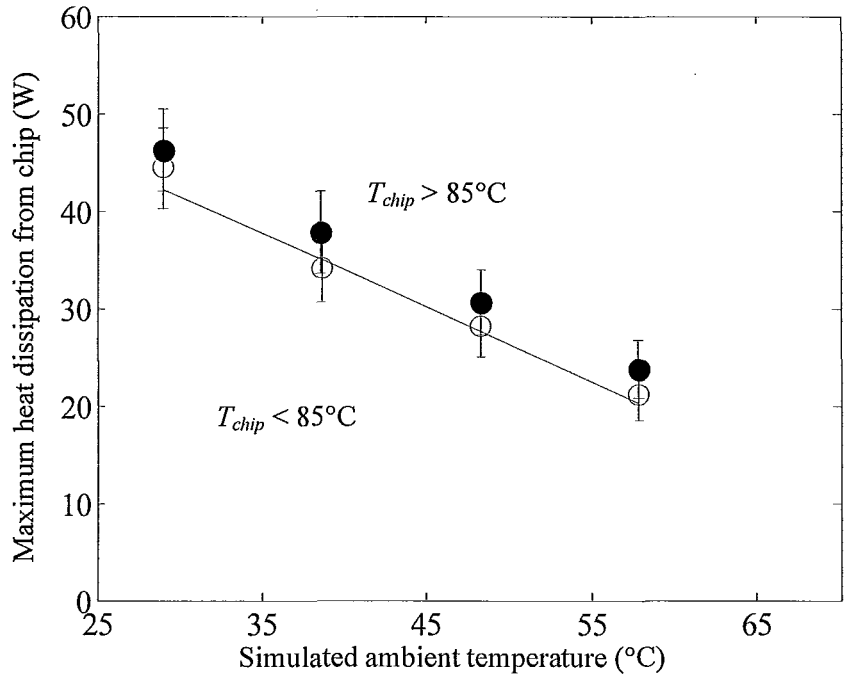


Figure 5.14: Variation in maximum heat dissipation capacity with ambient temperature for hybrid system with r_C = 0.33 off condition at T_{chip} = 85 °C for ○ open circuit, ● short circuit and —— open circuit model prediction.

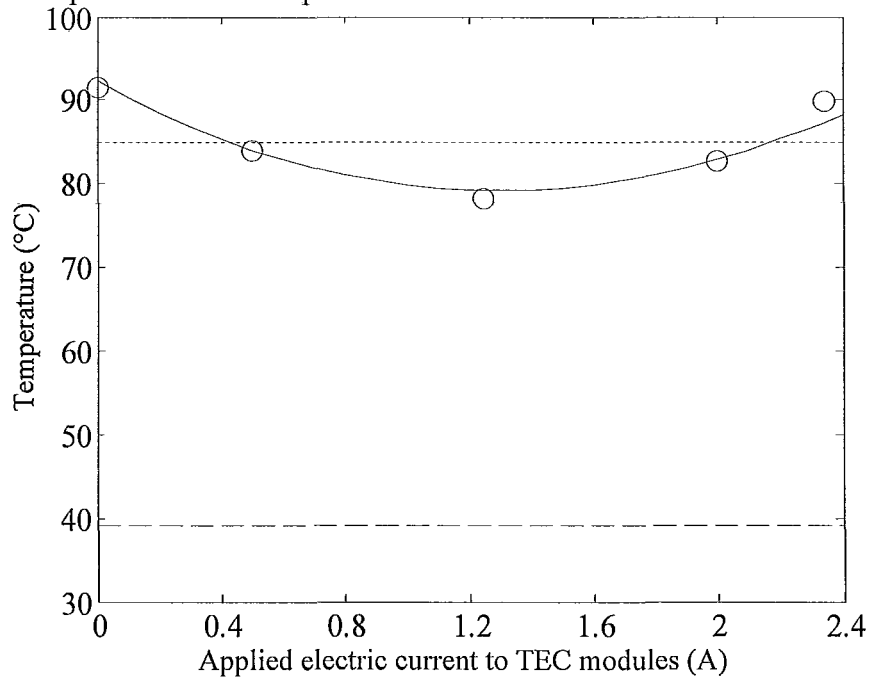


Figure 5.15: Effect of applied current on chip temperature (○ Experiment, — Model) for hybrid system with r_C = 0.33 at Q_{chip} = 40 W at —— T_{amb} = 39.1 °C. (- - - T_{design} = 85 °C).

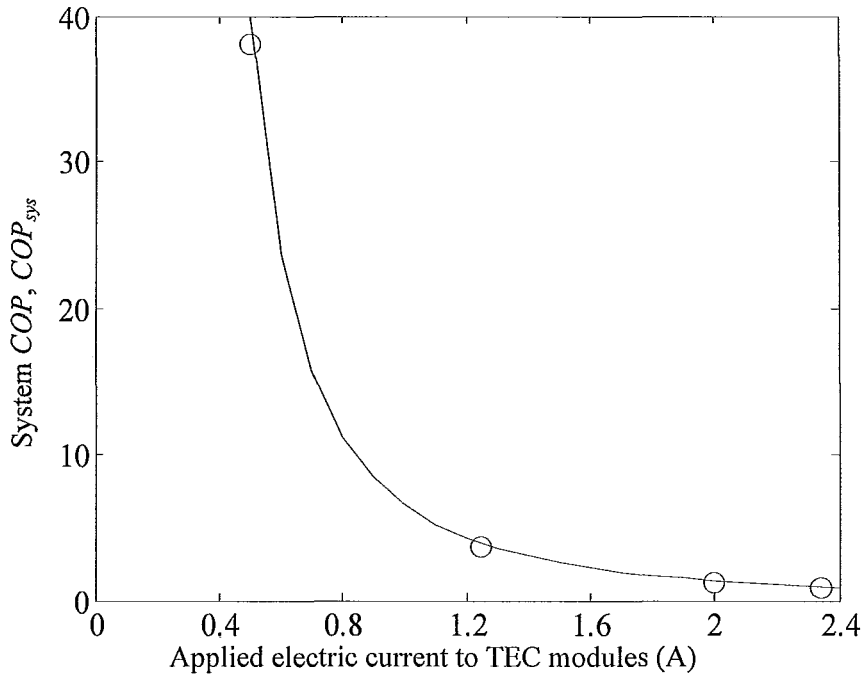


Figure 5.16: Effect of applied current on system *COP* (○ Experiment, — Model) for hybrid system with $r_C = 0.33$ at $Q_{chip} = 40$ W at $T_{amb} = 39.1$ °C.

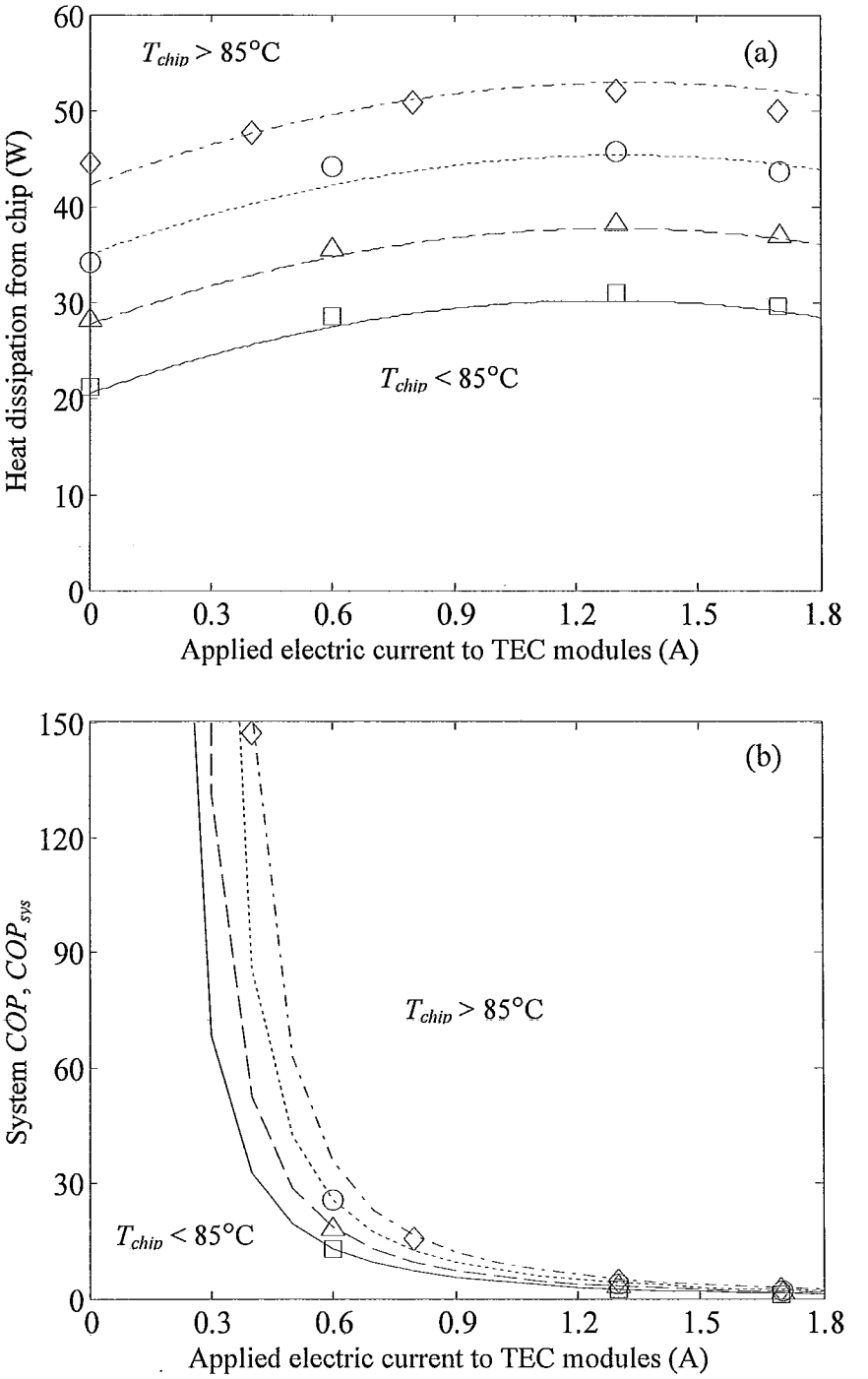


Figure 5.17: Variation of (a) heat dissipation from chip and (b) system *COP* with applied current at T_{amb} = 29 °C (◊ Experiment, — - — Model), 38.6 °C (○ Experiment, - - - Model), 48.3 °C (Δ Experiment, — — Model) and 57.9 °C (□ Experiment, —— Model) for hybrid system with r_C = 0.33 and at T_{chip} = 85 °C.

5.4. EFFECT OF r_C ON CHIP TEMPERATURE

To understand the effect of the heat sink area dedicated to the conventional passive path (r_C) on the chip temperature for the hybrid system ($0 < r_C < 1$) at different applied DC current, the model prediction at an ambient temperature of 40 °C and a heat load of 36 W from the chip is shown in Figure 5.19. The results show that when r_C increases at a certain ambient temperature the required DC current to the TEC modules to achieve the minimum chip temperature decreases. More importantly the minimum current of the safe operating current range also decreases to maintain $T_{chip} < 85$ °C. Thus to achieve better or increased system *COP* while dissipating the same amount of heat from chip at a certain ambient temperature the higher r_C has to be selected for the hybrid system ($0 < r_C < 1$). For the particular example shown in Figure 5.19, when $r_C = 0.6$ the hybrid system does not need its TEC modules to be electrically on to dissipate 36W of heat from chip at 40 °C ambient temperature.

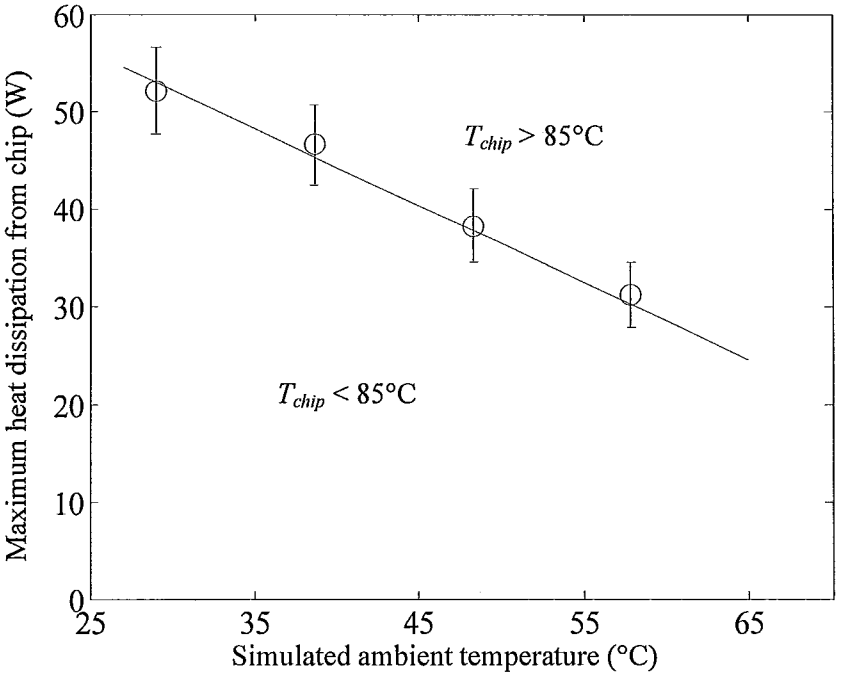


Figure 5.18: Variation in maximum heat dissipation capacity (○ Experiment, —— Model) with ambient temperature for hybrid system with r_C = 0.33 on condition at T_{chip} = 85 °C.

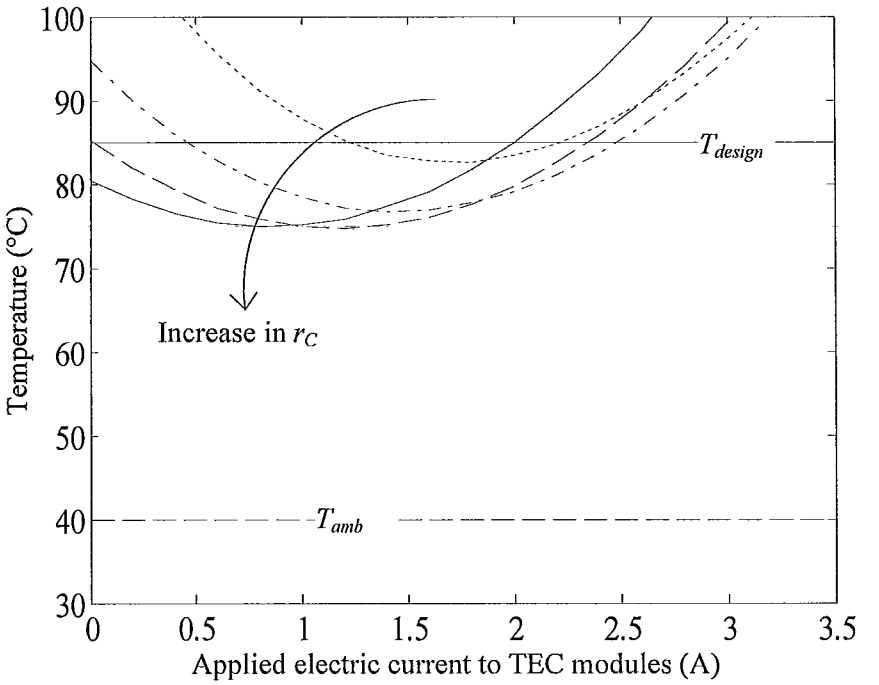


Figure 5.19: Effect of applied current on chip temperature for different system configurations of - - - r_C = 0, — - — r_C = 0.2, — — r_C = 0.4 and —— r_C = 0.6 at Q_{chip} = 36 W and ····· T_{amb} = 40 °C. (—— T_{design} = 85 °C).

5.5. Effect of Ambient Temperature on Maximum Heat Dissipation Capacity

The effect of maximum heat dissipation capacity (Q_{max}) at T_{chip} = 85°C is shown in Figure 5.20 as a function of ambient temperature for different r_C. Both the experimental data and the model predictions are plotted on the same figure. The maximum heat dissipation capacity at any r_C decreases with an increase in ambient temperature, as expected. The only TEC system (r_C = 0), when operational can improve the heat dissipation capacity at high ambient temperatures but at low ambient temperature the fully passive system (r_C = 1) can achieve higher Q_{max} compared to the only TEC system (r_C = 0). The cross over point in this operating envelope is approximately 54 °C and 30 W. When a hybrid system ($0 < r_C < 1$) is used the performance improves in terms of Q_{max} even at lower ambient temperature. For instance the cross over point for r_C = 0.33 is approximately 36 °C and 47 W. The selection of r_C for a thermal management system will depend on the operating ambient temperature of the electronics package, rated heat dissipation from the chip and the external thermal resistance. The hybrid system with r_C = 0.5 for the particular example shown in Figure 5.20 shows an improvement in maximum heat dissipation capacity at almost any ambient temperatures except at very low ambient temperature which in this case is less than 30°C.

The maximum heat dissipation capacity when the TEC is off is the lowest for r_C = 0 (only TEC system) and increases as more area is dedicated to the passive path (Figure 5.20). The maximum heat dissipation capacity when the TEC is off is approximately 49%

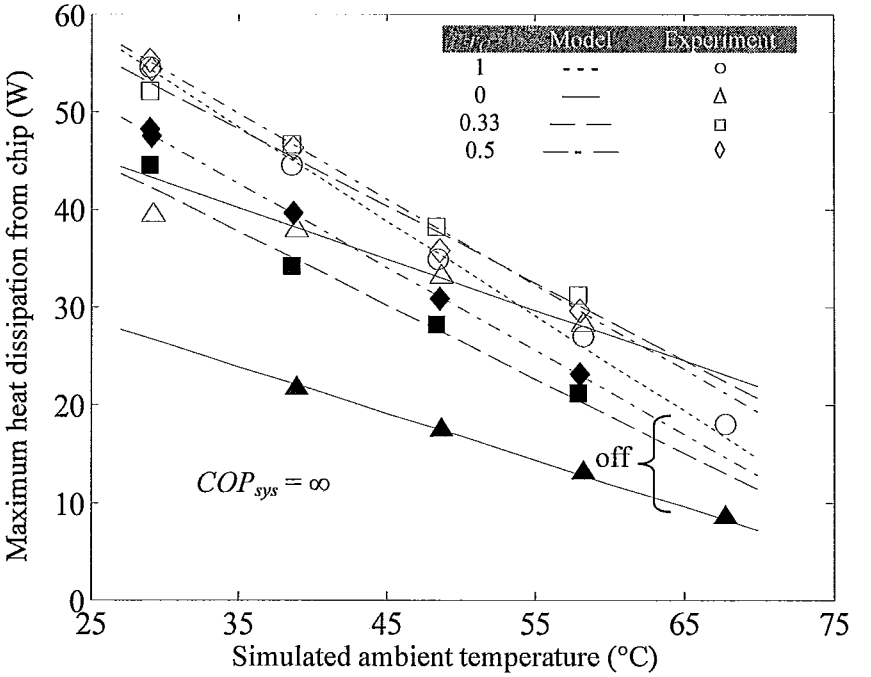


Figure 5.20: Variation in maximum heat dissipation capacity with ambient temperature at T_{chip} = 85 °C with TEC on (open symbols for Experiment and black lines for Model prediction) and off (filled symbols for Experiment and gray lines for Model prediction).

of the fully passive system for $r_C = 0$ and is approximately 78 and 88% of the passive system for $r_C = 0.33$ and 0.5 respectively. As r_C increases this percentage increases, but the heat dissipation capacity when the thermoelectric modules are on decreases at higher ambient temperatures. Thus r_C would need to be selected so that the system can handle the most adverse operating conditions. For example, for a rated heat dissipation from chip of 35W the only TEC system ($r_C = 0$) is operational up to an ambient temperature of 45°C, the conventional passive system ($r_C = 1$) is operational up to an ambient temperature of 49°C and the hybrid system with $r_C = 0.5$ is operational up to approximately 52°C to satisfy $T_{chip} \leq 85$°C. Similarly at an ambient temperature of 50°C, the only TEC system ($r_C = 0$) has a maximum heat dissipation capacity (Q_{max}) of 32 W, the conventional passive system ($r_C = 1$) is capable of a Q_{max} of 34 W and the hybrid system with $r_C = 0.5$ can dissipate maximum of 37 W while keeping $T_{chip} \leq 85$°C. For this particular heat sink thermal resistance, the hybrid system with $r_C = 0.5$ when operational can dissipate more heat than either the conventional passive ($r_C = 1$) or the only TEC ($r_C = 0$) system for up to an ambient temperature of approximately 63 °C.

There are situations where the electronics are running at partial load conditions. At these situations, the heat load from the chip is less than its rated heat dissipation. Thus, the performance of the thermal management system at partial load conditions needs to be considered in selecting a design. It would be useful if the r_C could be selected in such a way that most of the moderate conditions both in terms of ambient temperature and the heat dissipation from the chip can be satisfied keeping the TEC off while turning them on with the necessary amount of DC current when the situation is adverse to maximize the

System *COP*. The overall coefficient of performance will be better for the hybrid system ($0 < r_C < 1$) than the only TEC system ($r_C = 0$) at any ambient temperature, because it operates at a much lower current (Figure 5.7 (b), Figure 5.12 (b), Figure 5.17 (b)) and because it does not need to be turned on for moderate conditions until the heat dissipation from the chip reaches the graphs for TEC off condition in Figure 5.20.

5.6. Operating Current and COP_{sys} Contours

The required current to the TEC modules to maintain $T_{chip} < 85$ °C and the corresponding system *COP* at different ambient temperatures for $r_C = 0$, 0.33 and 0.5 are shown in Figure 5.21 to Figure 5.23. The upper curves in these figures are at the optimum current to produce maximum heat dissipation capacity and the lower curves are for TEC off condition. The comparison between different r_C for the system *COP* of 10 and 50 is shown in Figure 5.24. At any condition of ambient temperature and heat load from chip, the COP_{sys} for the hybrid system with $r_C = 0.5$ is improved compared to $r_C = 0$ or 0.33 as comparatively lower current is required for $r_C = 0.5$ than $r_C = 0$ or 0.33. For example, the hybrid system with $r_C = 0.5$ when operated at an ambient temperature of 45 °C and heat load from chip of 35W, requires a current of approximately 0.1 A (Figure 5.23 (a)); whereas the only TEC system ($r_C = 0$) and the hybrid system with 0.33 requires approximately 1.6 A (Figure 5.21 (a)) and 0.4 A (Figure 5.22 (a)) to satisfy the same condition. The corresponding COP_{sys} at that condition for the hybrid system with $r_C = 0.5$

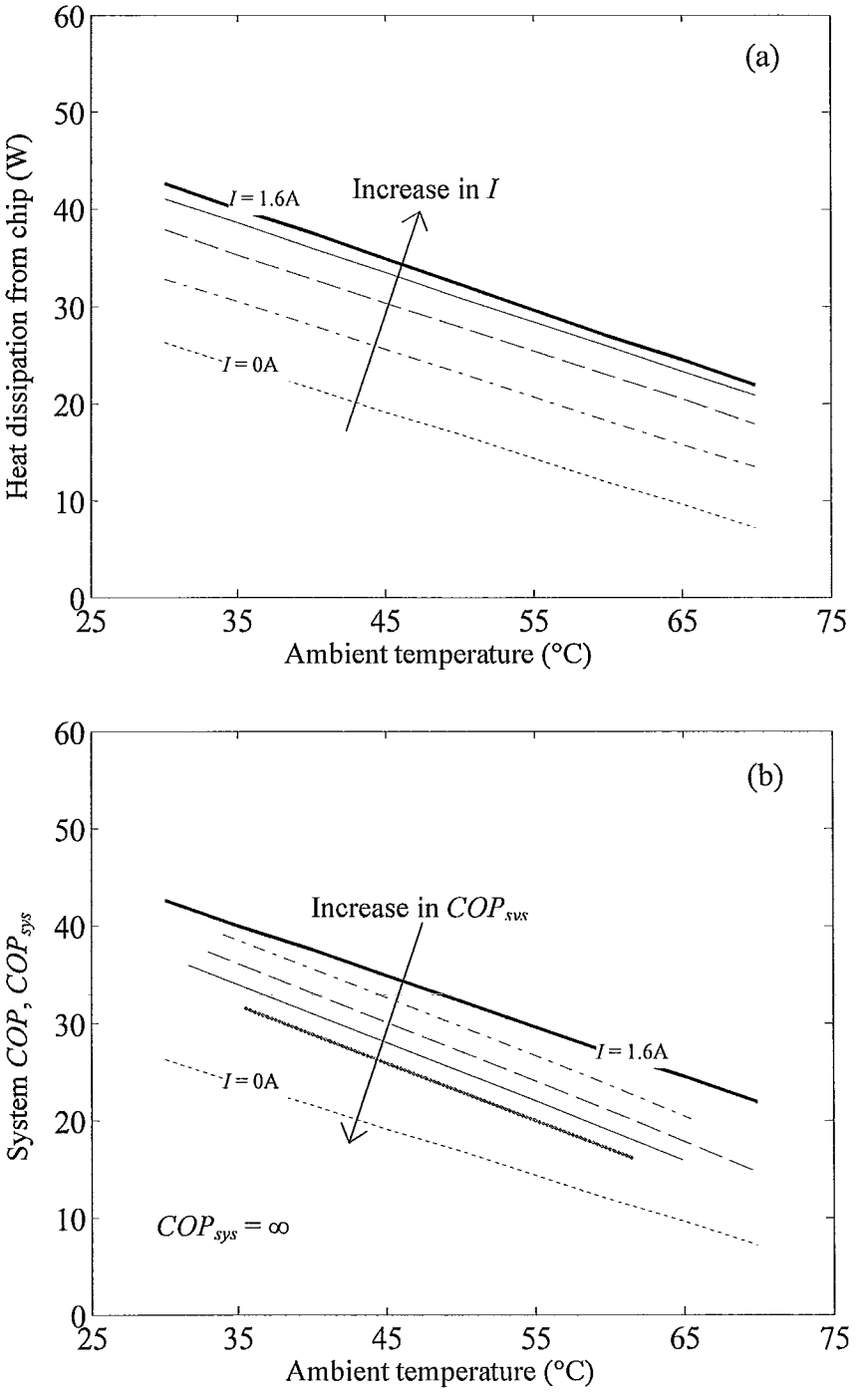


Figure 5.21:(a) Applied current contours of I = - - - 0 A, — - — 0.4 A, — — 0.8 A, —— 1.2 A and ▬▬ 1.6 A and (b) corresponding system COP contours of COP_{sys} = — - — 5, — — 10, —— 20 and ▬▬ 50 at different heat loads and ambient temperatures for only TEC system (r_C = 0) at T_{chip} = 85 °C.

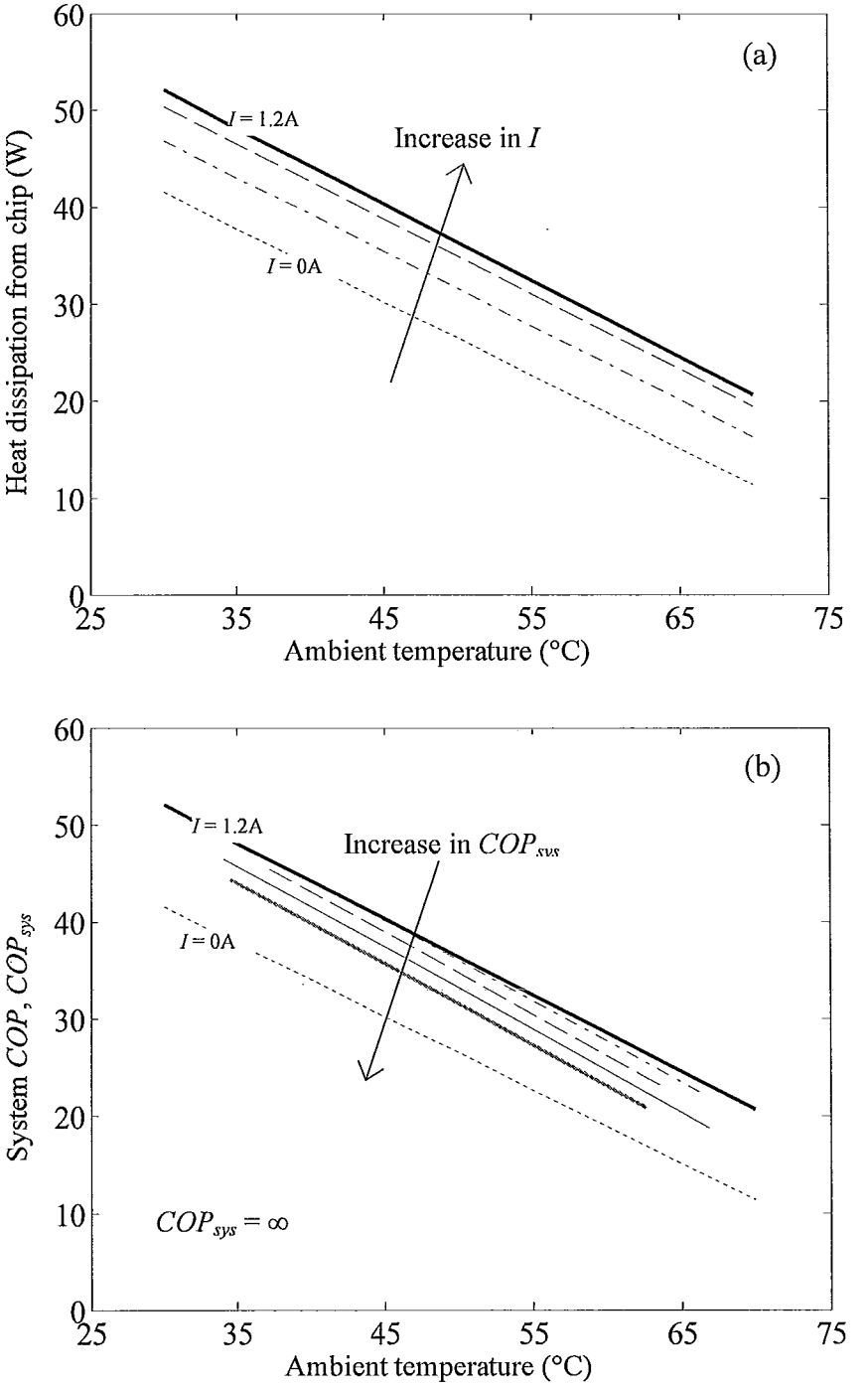


Figure 5.22: (a) Applied current contours of I = - - - 0 A, — - — 0.4 A, — — 0.8 A and ▬▬ 1.2 A and (b) corresponding system COP contours of COP_{sys} = — - — 5, — — 10, —— 20 and ▒▒▒ 50 at different heat loads and ambient temperatures for hybrid system with r_C = 0.33 at T_{chip} = 85 °C.

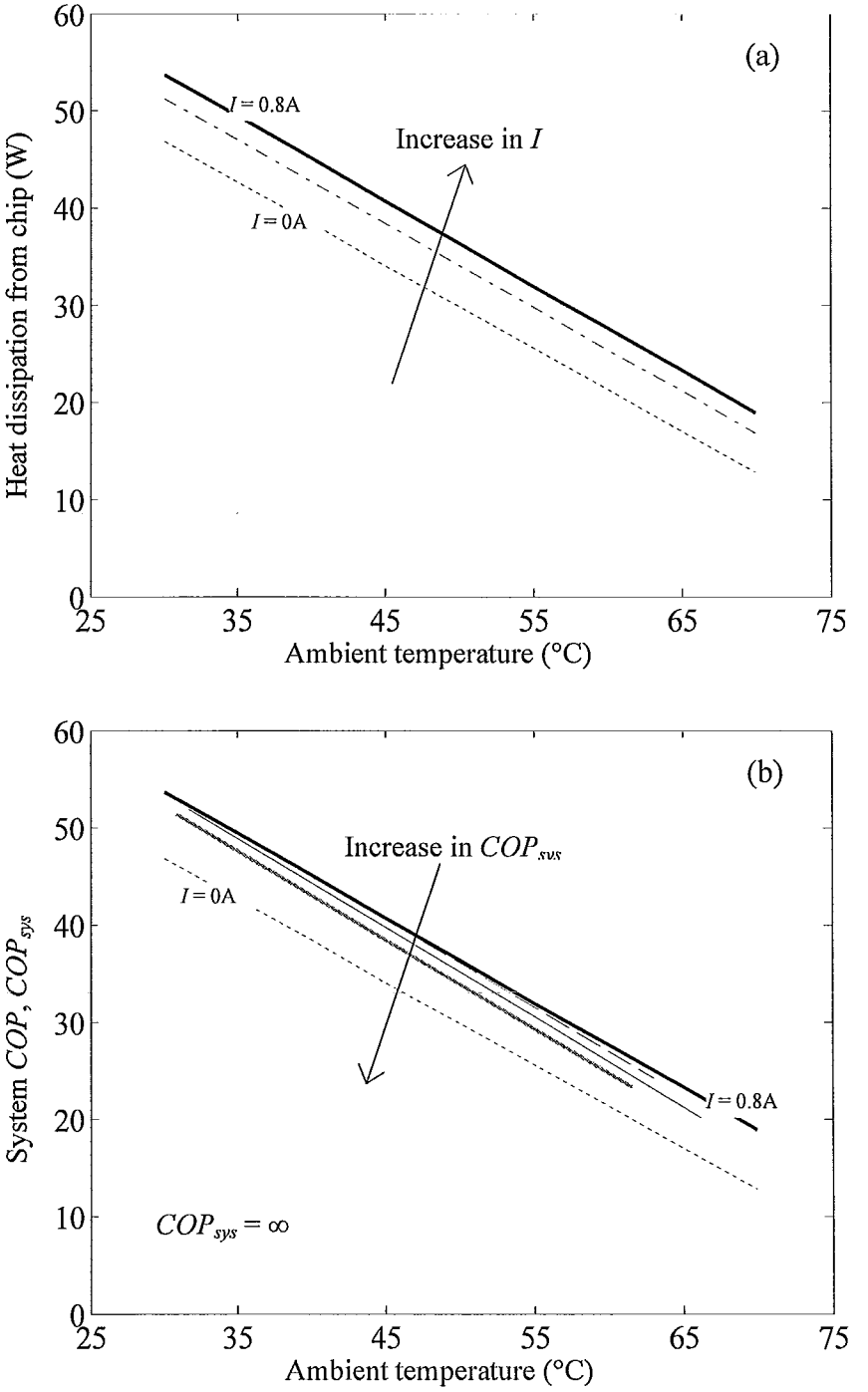


Figure 5.23: (a) Applied current contours of I = - - - 0 A, — - — 0.4 A and ▬▬ 0.8 A and (b) corresponding system COP contours of COP_{sys} = — — 10, —— 20 and ▒▒▒ 50 at different heat loads and ambient temperatures for hybrid system with $r_C = 0.5$ at T_{chip} = 85 °C.

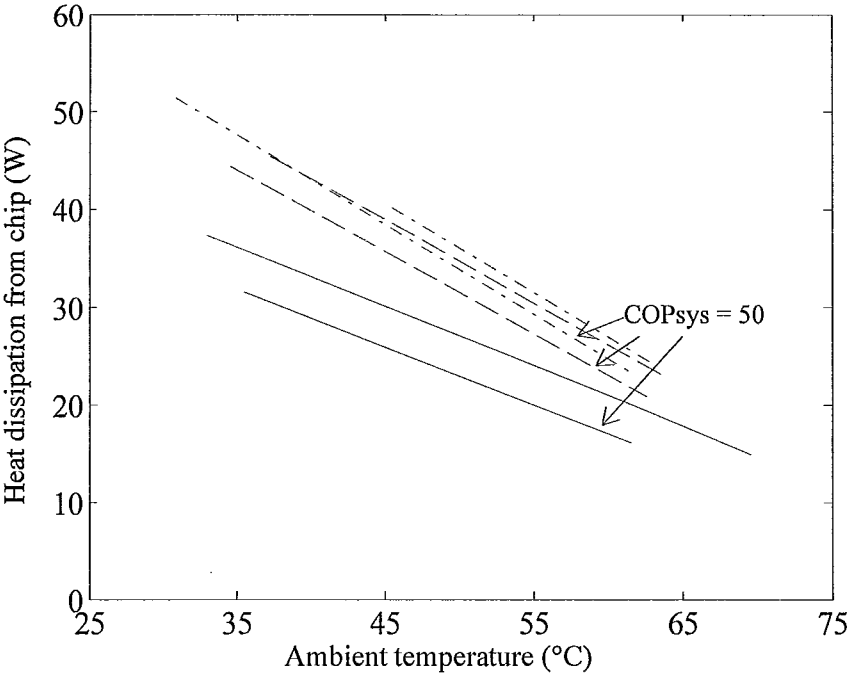


Figure 5.24: System *COP* contours at different heat loads and ambient temperatures for — $r_C = 0$, — — $r_C = 0.33$ and — · — $r_C = 0.5$ at $T_{chip} = 85$ °C (black lines for $COP_{sys} = 50$ and gray lines for $COP_{sys} = 10$).

is close to infinity (Figure 5.23 (b)), while for $r_C = 0.33$ it is approximately 50 (Figure 5.22 (b)) and for only TEC system ($r_C = 0$) is approximately 1 (Figure 5.21 (b)). As the required current decreases with an increase in r_C a higher COP_{sys} is achieved for any heat dissipation from chip and for any ambient temperature. In practice, the partial load cases could be satisfied by keeping the TEC modules off until T_{chip} exceeds 85 °C. The TEC could be turned on with a required variable current to it or by turning the modules on and off at a fixed current for adverse situations. When dissipating 25 W from the chip, the only TEC system ($r_C = 0$) is operational up to approximately 47 °C of ambient temperature with a 2 % power penalty (i.e., $COP_{sys} = 50$) and up to 54 °C with a 10 % power penalty (i.e., $COP_{sys} = 5$) as input power to the TEC modules (Figure 5.24). In case of the hybrid system with $r_C = 0.33$, to dissipate the same amount of heat from the chip, the system is operational up to approximately 58 °C of ambient temperature with a power penalty of 2 % (i.e., $COP_{sys} = 50$) while this ambient temperature could increase to approximately 62 °C with a power penalty of 10 % (i.e., $COP_{sys} = 10$) (Figure 5.24). Thus the hybrid system with $r_C = 0.33$ is capable of handling the same conditions in terms of ambient temperature and heat load from chip with lower power penalty compared to the only TEC system ($r_C = 0$). The hybrid system with $r_C = 0.5$ shows even better enhancement of system *COP* to satisfy the same condition (Figure 5.24).

The COP_{sys} for the hybrid system will be higher for a variable current supply than for a fixed current because the required current would be lower for the former case. The current to meet the most adverse condition could be determined from the model.

5.7. EFFECT OF r_C ON MAXIMUM HEAT DISSIPATION CAPACITY AND COP_{sys}

The selection of the heat sink area dedicated to the conventional passive path, r_C for an electronic packaging with known thermal resistance will depend on the ambient temperature and its rated heat dissipation from the chip. The effect of r_C on the maximum heat dissipation capacity from chip for TEC at on and off conditions are summarized in Figure 5.25 (a), while the effect on the corresponding *COP* of the system when the TEC modules are on are shown in and Figure 5.25 (b). At high ambient temperatures, an increase in r_C reduces the maximum heat dissipation capacity of the system when TEC is on, whereas it improves at low ambient temperature. For the TEC off condition, this capacity improves as r_C increases, i.e. as more heat sink area is dedicated to the conventional passive path. The corresponding COP_{sys} at that maximum heat dissipation capacity also improves as r_C increases for any ambient condition (Figure 5.25 (b)). Thus, r_C can be selected for a range of operational ambient temperature. The *COP* for the entire system also reduces as the ambient temperature increases. The optimum r_C can also be selected to dissipate the maximum heat from chip at a particular ambient temperature. For example, the optimum r_C at an ambient temperature of 40 °C is approximately 0.5 and the hybrid system with $r_C = 0.5$ at 40 °C ambient temperature can dissipate a maximum of about 45 W heat from chip when the TEC modules are on and about 38 W heat when the TEC modules are off while keeping the chip temperature below 85 °C (Figure 5.25 (a)). When this hybrid system ($r_C = 0.5$) is dissipating the maximum heat (about 45 W) from the chip, the system *COP* is approximately 6 and at partial heat load between 38 and 45 W the

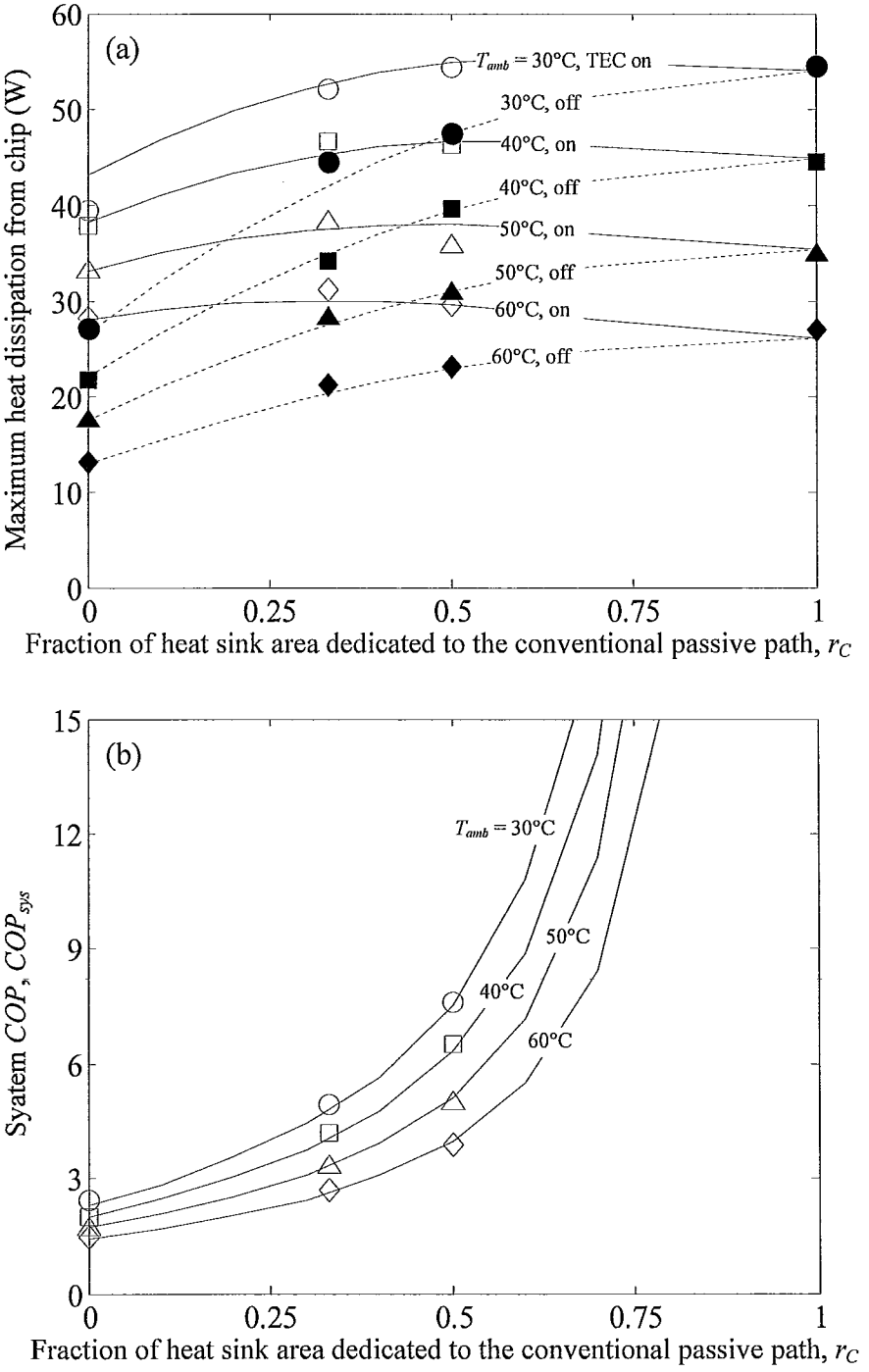


Figure 5.25: Variation of (a) maximum heat dissipation capacity and (b) corresponding system *COP* with r_C at T_{amb} = ○ 30, □ 40, Δ 50 and ◊ 60 °C. Symbols (open for TEC on and filled for TEC off) represent experimental results and lines (solid for TEC on and dashed for TEC off) represent model predictions.

system *COP* is greater than 5.6 (Figure 5.25 (b)).

5.8. Effect of Number of Thermoelectrics

The number of total thermocouples in the system has an impact on the performance. When number of modules, n (i.e., number of thermocouples, nN) increases in the system, the thermal resistance of the TEC path in the hybrid system or of the only TEC system decreases as the TEC modules are thermally in parallel in the system. Thus the maximum heat dissipation capacity increases at any ambient temperature for the TEC off mode. For the TEC on mode, there is an optimum number of modules to achieve the maximum heat dissipation capacity at an ambient temperature. The effect of number of TEC modules on the maximum heat dissipation capacity and the system *COP* for an operating ambient temperature of 30 and 60 °C is shown in Figure 5.26 at T_{chip} = 85°C from the model. Higher heat dissipation is achieved at lower ambient temperature, higher r_C and for TEC on conditions. The system *COP* improves at lower ambient temperature and higher r_C when the TEC modules are on. The required number of TEC modules can be selected from this analysis depending on the operating ambient temperature and the heat sink thermal resistance.

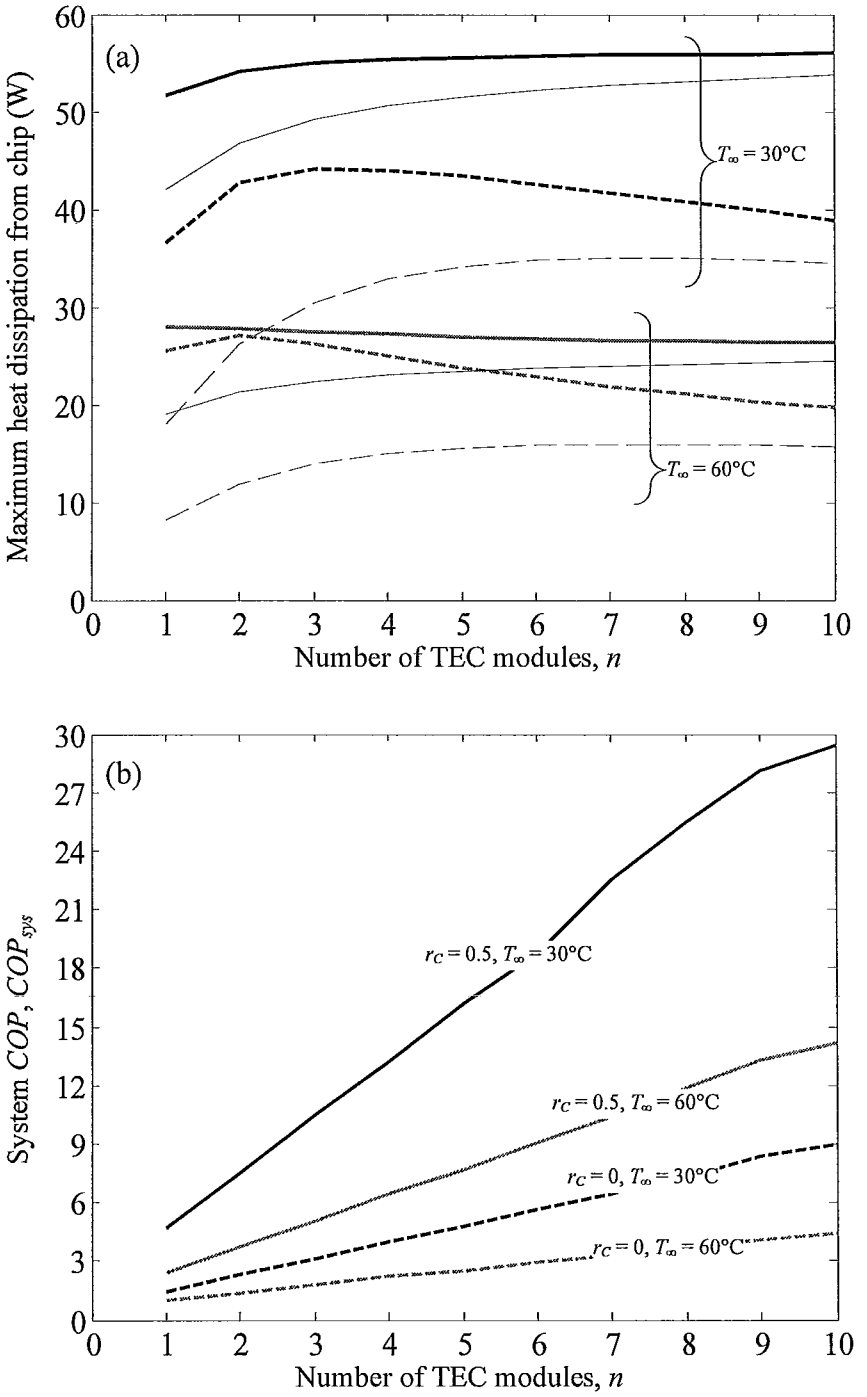


Figure 5.26: Effect of number of TEC modules on (a) maximum heat dissipation capacity and (b) corresponding system COP for $r_C = 0$ (dashed lines) and 0.5 (solid lines) at T_{amb} = 30 °C (black lines) and 60 °C (gray lines) from the model prediction at T_{chip} = 85 °C for TEC on (bold Lines) and off (regular lines) conditions.

5.9. Effect of Heat Sink Thermal Resistance

Different external cooling methods will result in different external thermal resistances. Typical ranges of external thermal resistances for natural convection, forced air convection and liquid cooling are 0.42 ~ 6.46, 0.26 ~ 2.84 and 0.17 ~ 0.36 °C/W respectively (Riffat and Ma, 2004) and depends on the fin geometry, density and air flow in case of air cooling and on channel geometry and liquid flow in case of liquid cooling. The model prediction for the effect of external thermal resistance on the maximum heat dissipation capacity from the chip (Q_{max}) and the corresponding system *COP* are shown in Figure 5.27 and Figure 5.28 for ambient temperature of 30 and 60 °C respectively both for the TEC modules on and off conditions. The ranges of external thermal resistances are also presented in Figure 5.27 (a). As the external resistance increases the maximum heat dissipation capacity decreases at any ambient temperature. Higher heat can be dissipated at lower ambient temperature compared to higher ambient temperature for a given external resistance and thus higher system *COP* is achieved.

At lower ambient temperature such as 30 °C the only heat pipe system (r_C = 1) can dissipate higher heat than the only TEC system (r_C = 0) and use of the hybrid system with r_C = 0.5 when the TEC modules are on improves the heat dissipation capacity by less than 2% for a range of heat sink thermal resistance of 0.6 to 1.6 °C/W (Figure 5.27 (a)). However, at higher ambient temperature such as 60 °C the only heat pipe system (r_C = 1) can dissipate up to 34% higher heat than only TEC system (r_C = 0) at on mode for a range

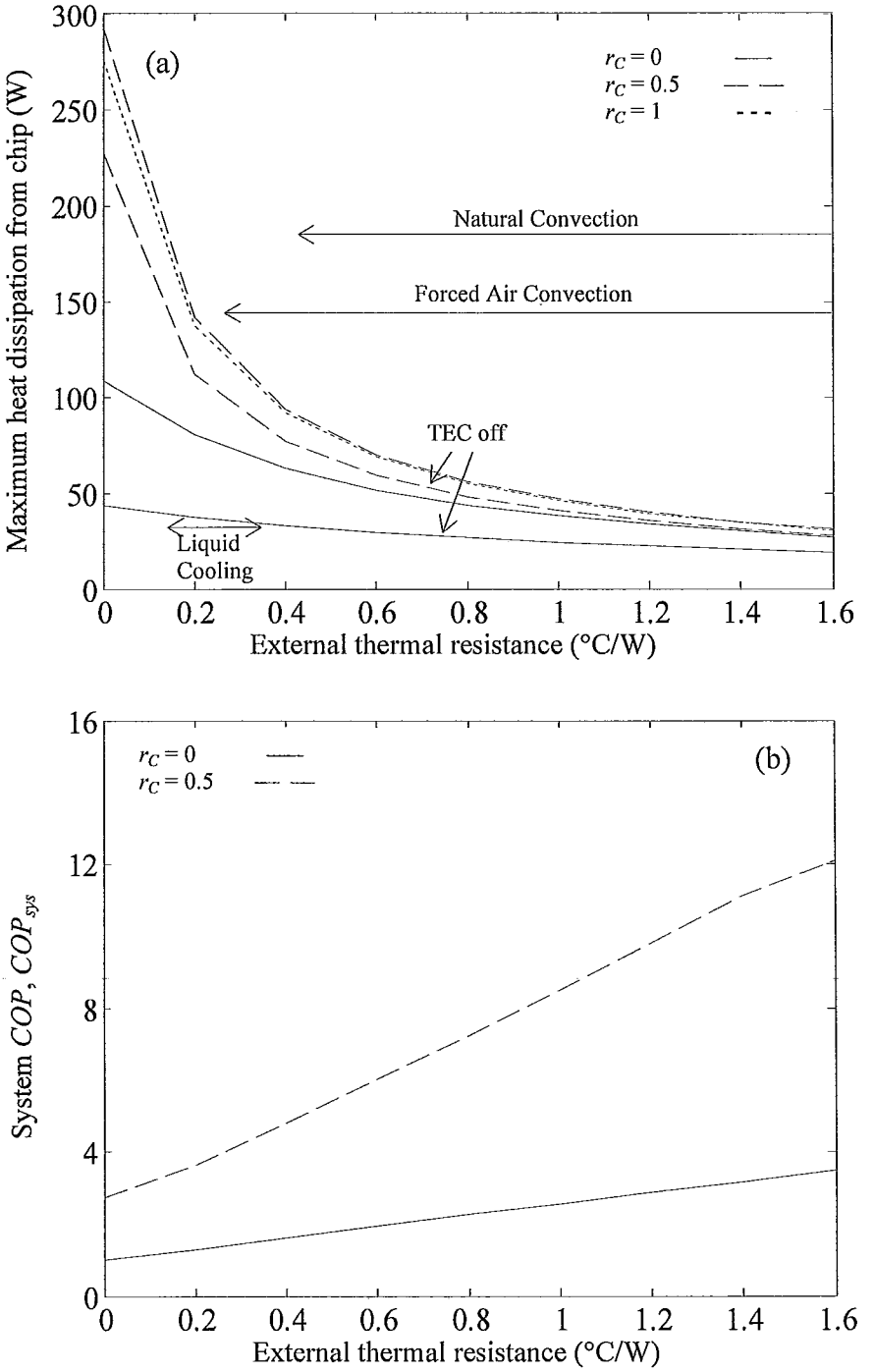


Figure 5.27: Effect of external thermal resistance on (a) maximum heat dissipation capacity and (b) corresponding system *COP* from the model for TEC on (black lines) and off (gray lines) conditions at T_{amb} = 30 °C and T_{chip} = 85 °C.

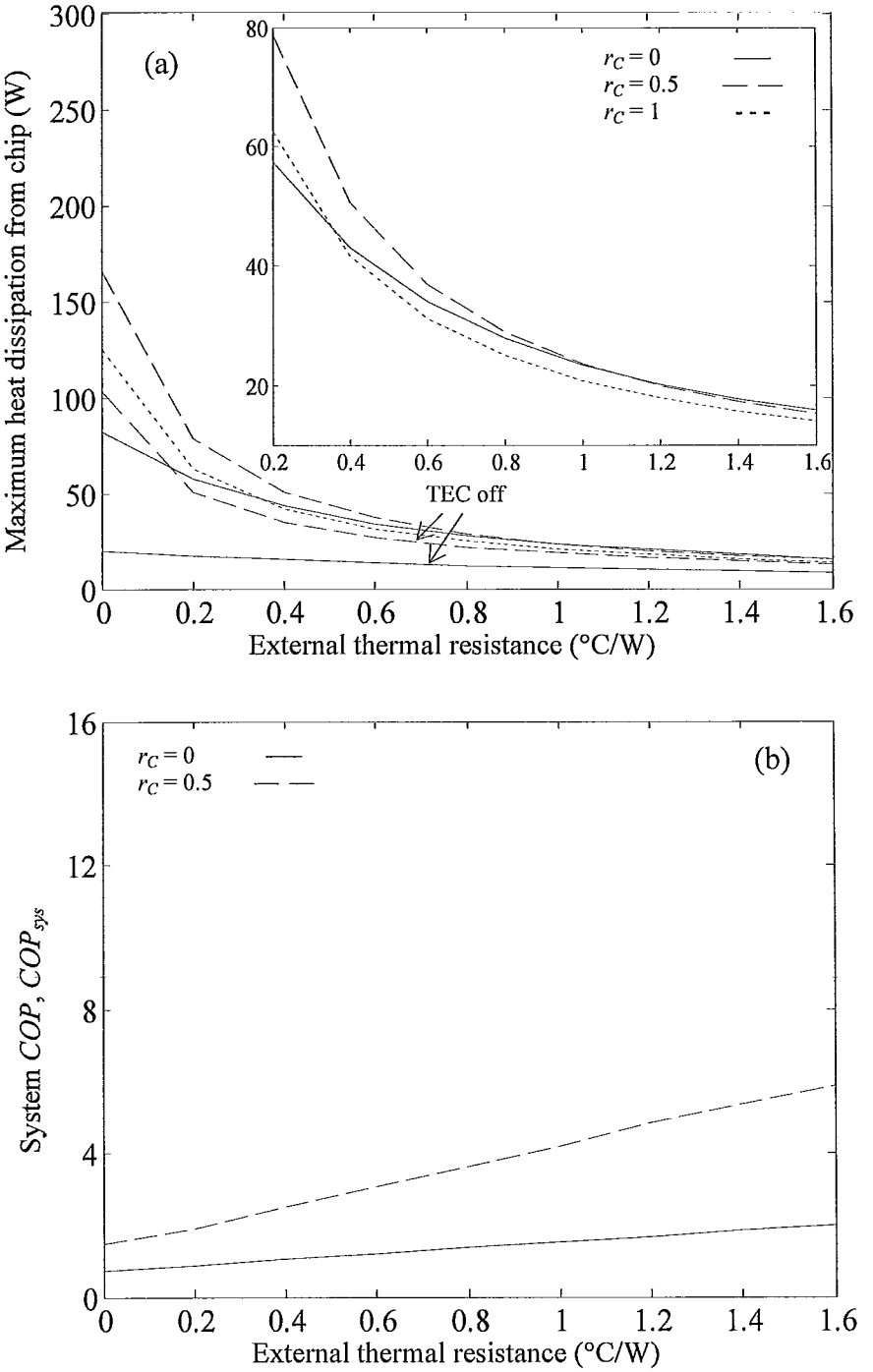


Figure 5.28: Effect of external thermal resistance on (a) maximum heat dissipation capacity and (b) corresponding system *COP* from the model for TEC on (black lines) and off (gray lines) conditions at T_{amb} = 60 °C and T_{chip} = 85 °C.

of heat sink thermal resistance of 0 to approximately 0.4 °C/W. For higher range of heat sink thermal resistance of 0.4 to 1.6 °C/W the only TEC system when the TEC modules are on can enhance the heat dissipation capacity by up to 13% compared to the only heat pipe system. When compared with the hybrid system with $r_C = 0.5$ with the TEC modules on the heat dissipation is enhanced by at least 10% over the range of heat sink thermal resistance of 0 to 1.6 °C/W than the only heat pipe system (Figure 5.28 (a) - inset).

For the only TEC system or hybrid system ($0 \leq r_C < 1$), TEC on condition can dissipate more heat than TEC off condition at any ambient temperature. The Hybrid system with $r_C = 0.5$ shows an improvement in system *COP* compared to the only TEC system ($r_C = 0$) at any ambient temperature. If the external resistance of the electronic package, the operating ambient temperature and the rated heat dissipation from the chip are known the required r_C can be selected using these set of graphs or the model.

Chapter 6 CONCLUSION & RECOMMENDATIONS

A model is developed for a hybrid thermal management system that incorporates a TEC based active path in parallel with a heat pipe based passive path for thermal management of electronic packaging systems. The advantage of such a hybrid system is that the heat pipe based passive path can primarily transport the heat load from the chip at moderate conditions keeping the TEC modules electrically off while the TEC modules can be turned on when the thermal conditions become adverse for the passive path alone. This results in a better overall system coefficient of performance. The model can be used as an engineering design tool to predict the performance of such a hybrid system if the temperature dependent thermo-element material properties along with the geometric properties are known. The hybrid technique proposed here can be extended to other thermal management systems in different applications.

Controlled experiments were performed to evaluate the model predictions for the hybrid system for thermal management of an electronic package. The heat dissipation from the chip was simulated by a flexible heater with the temperature of the heater representing the chip temperature. A cooling loop was used in the experiments as the heat sink. The

ambient temperature was controlled by changing the mean temperature of the water flowing through the cooling loop. The thermal resistance of the finned heat sink of the electronic package at natural convection was simulated by acrylic glass (PMMA, polymethyl methacrylic). The fraction of the heat sink area dedicated to each path of the hybrid model was controlled by using appropriate thicknesses of the acrylic glass in the passive and the active TEC paths in the experiments.

The different experiments performed were to observe (i) the effect of applied current and heat load from the chip on the chip temperature and system *COP* and (ii) the effect of applied electric current on the heat dissipation and the system *COP* for $T_{chip} = T_{design}$ at different ambient temperatures. An operating envelope was presented to compare between different hybrid configurations and the only TEC or only heat pipe based thermal management system. The maximum heat dissipation capacity and the corresponding system *COP* as a function of different hybrid configurations was also demonstrated. The model predictions were found to have reasonable agreement with the experimental results.

The performance of the hybrid system depends on the ratio of the heat sink area dedicated to the passive and the active paths. Selection of the required r_C, the heat sink area dedicated to the conventional passive path, will depend on design heat load from chip, the external thermal resistance and the operating ambient conditions. In general, when the operating ambient temperature increases the maximum heat dissipation capacity of the system, Q_{max} decreases. Dedicating more heat sink area to the passive path improves system *COP*, as less current is required. Increasing r_C also improves the maximum heat dissipation capacity at TEC off condition at any ambient temperatures. For TEC on

condition, the performance depends on the ambient temperature. At lower ambient temperatures there is an optimum r_C which results in maximum Q_{max} while at higher ambient temperatures an increase in r_C degrades the maximum heat dissipation capacity when the TEC modules are on. Though the performance at higher ambient temperature is slightly degraded for $0 < r_C < 1$ in terms of heat dissipation capacity compared to $r_C = 0$, the system *COP* is improved. The number of thermocouples or TEC module(s) has an effect on the performance of the system. There is an optimum number of TEC modules to achieve maximum Q_{max} when the modules are on while for the off condition an increase in the number of TEC modules increases Q_{max} capacity. However while selecting the number of modules the associated cost is also an important concern. The effect of total thermal resistance of the heat sink was also studied and the model prediction can be used to select the r_C for a given rated heat dissipation from the chip and the operating ambient temperature. The short circuited TEC off condition did not significantly improve the performance compared to the open circuited TEC off condition.

6.1. RECOMMENDATIONS FOR FUTURE WORK

The work presented in this research shows that the operating range of a thermal management system can be improved for a range of ambient temperature by using a hybrid system that consists of a conventional passive system and an active TEC system. The *COP* for the entire system is improved compared to an only TEC system as the TEC modules

can be kept electrically off for moderate operating conditions. Recommendations for the continuation of this work are :

- The model can be improved by incorporating the Thomson effect along with the effect of the interconnect material between the n and p-type semiconductors.
- Experimentally determine the effect of number of TEC modules on the performance of the system. For example, the maximum heat dissipation capacity (Q_{max}) and the corresponding system *COP* for T_{chip} = 85 °C can be obtained experimentally to validate the model predictions for those numbers of TEC modules. This experiment will require modifying the evaporator heat spreader to accommodate more TEC module(s).
- Experimentally evaluate the effect of heat sink thermal resistance on the performance of the system. A different thickness of the acrylic can be used for this experiment for the only TEC ($r_C = 0$) or the only passive ($r_C = 1$) system and corresponding thickness for the hybrid system ($0 < r_C < 1$) can be obtained for different r_C. These experiments will cover a range of cooling techniques such as forced air cooling or liquid cooling and provide an idea whether the use of the TEC modules can be useful in those systems.
- Geometric optimization can be performed numerically to maximize the heat dissipation capacity and the system *COP* for the hybrid system. This includes but not limited to the height (t_{TE}) and the cross-sectional area (A_{TE}) of the n or p-type materials (commonly referred to geometry factor, $G = A_{TE}/t_{TE}$), packing density ($= 2NA_{TE}/A_{sub}$).

APPENDIX A –TEMPERATURE DEPENDENT PROPERTIES OF THERMO-ELEMENTS

The properties of the thermo-element at different mean temperatures are presented in Table A.1 obtained from the manufacturer's specification sheet (Melcor). The properties presented by the manufacturer is for the mean temperature of the hot and cold side of the thermoelectric material and for either n or p-type semiconductor.

Table A.1: Thermo-element (n or p-type) material properties of TEC module CP 1.4-127-06L (Melcor)

Mean Temperature, K (°C)	Thermal Conductivity ($Wm^{-1}K^{-1}$)	Seebeck Coefficient (VK^{-1})	Electric resistivity (Ω.m)
273 (0)	1.61	0.000194	0.0000092
300 (27)	1.51	0.000202	0.0000101
325 (52)	1.53	0.000207	0.0000116
350 (77)	1.55	0.00021	0.0000128
375 (102)	1.58	0.0002	0.0000137
400 (127)	1.63	0.000196	0.0000148
425 (152)	1.73	0.00019	0.0000158
450 (177)	1.88	0.000186	0.0000168
475 (202)	2.09	0.000179	0.0000176

Thomson Effect

The heat transfer for one thermo-couple due to the Thomson effect after rearranging Eqn. 2.4 and Eqn. 2.5 is expressed as

$$Q_T = IT_{mean}(T_h - T_c)\frac{d\alpha}{dT} \qquad \text{A.1}$$

And the cooling effect due to the Peltier effect at the cold junction is expressed as (Goldsmid, 1961)

$$Q_P = I\alpha(T_c)T_c \qquad \text{A.2}$$

The temperature dependent Seebect coefficient for a mean temperature range of 273 K (0 °C) to 400 K (127 °C) is shown in Figure A.1. To determine the slope of Seebeck coefficient at a given mean temperature the second order curve fit equation is used. The ratio of the heat transfer due to the Thomson effect to that of the Peltier effect is plotted in Figure A.2 for the temperature difference ranging from 0 to 70 °C (specified ΔT_{max} = 67 °C) and for the mean temperature of 325 K (52 °C), 350 K (77 °C) and 375 K (102 °C) as these covers the range of are typical mean temperatures from the experiments performed. The Thomson effect was found to be <10% of the Peltier effect which causes the cooling at cold junction. As the Thomson effect is an order of magnitude smaller than Peltier effect it was neglected in the model.

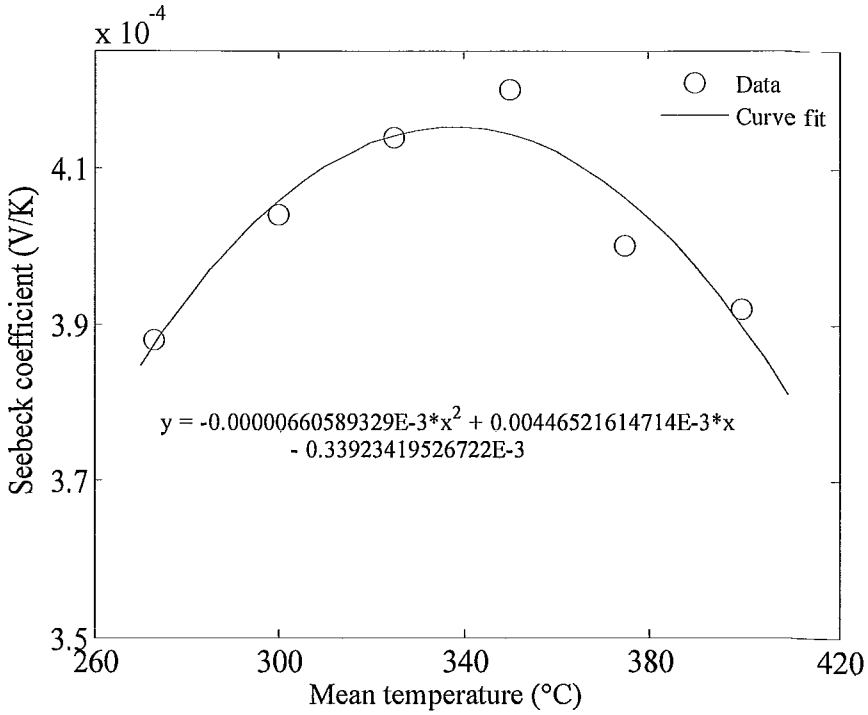


Figure A.1: Temperature dependent Seebeck coefficient (Melcor).

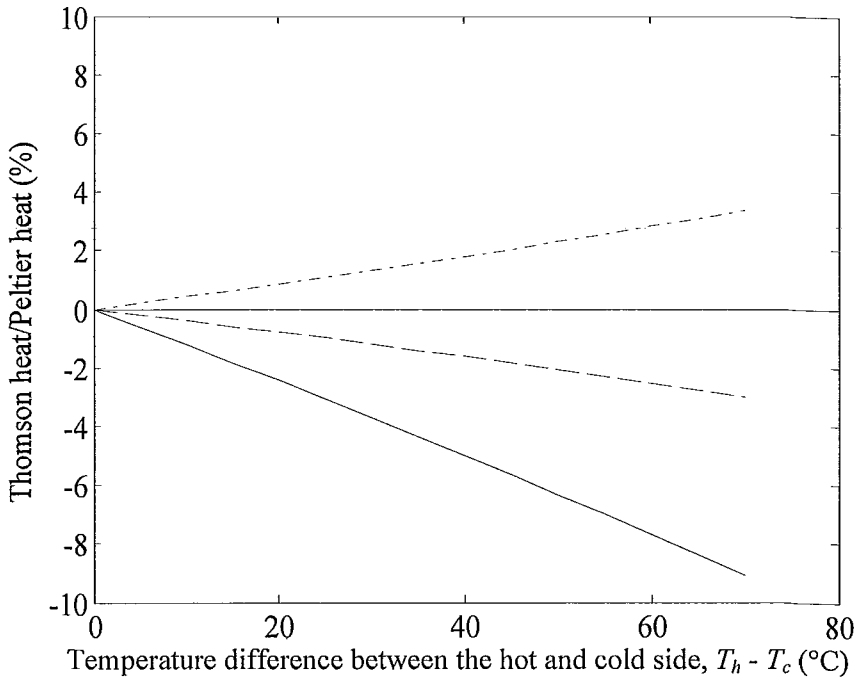


Figure A.2: Thomson to Peltier heat transfer ratio for a range of temperature difference between the hot and cold side of the TEC modules at mean temperature of — - — 325 K (52 °C), — — 350 K (77 °C) and —— 375 K (102 °C).

APPENDIX B –PARAMETRIC STUDIES

To minimize the contact thermal resistance thermal interface material (TIM) was applied in between different layers in the system, e.g., between the flexible heater and the evaporator heat spreader of the conventional passive path, between the ceramic substrates of the TEC modules and the associated evaporator heat spreaders, between the condenser heat spreaders and the acrylic layers, between the cold plates and the acrylic layers and in between the acrylic layers when more than one was used (Figure 4.8). The thermal resistance of the TIM was obtained as $3.68X10^{-5}$ $°Cm^2W^{-1}$ at a contact pressure of approximately 0.8 KPa. It would be air (with the thermal conductivity of approximately 0.0263 $Wm^{-1}K^{-1}$at 300K) in between those layers if no TIM was used and the thermal resistance of air would be approximately 0.0122 $°Cm^2W^{-1}$ at that contact pressure which is approximately 300 times greater than that of the TIM. The effect of this interface material thermal resistance is presented in Figure B.1 from the model. The heat dissipation from chip was less than 1.5% (with respect to air) smaller in case of air than the TIM used for the hybrid system with $r_C = 0.5$ at $T_{amb} = 50$ °C when $T_{chip} = 85$ °C.

Thermal conductivity of the ceramic substrate (k_{sub}) was obtained as 3.66 $Wm^{-1}K^{-1}$ from separate experiment and is described in section 4.4.1. The effect of the variation of k_{sub} on the heat dissipation from chip is presented in Figure B.2 for a hybrid system with r_C = 0.5 at T_{amb} = 40 °C when T_{chip} = 85 °C using the model. It was found that the heat dissipation from the chip varied less than 4% for a ± 50% change in the thermal conductivity of the ceramic substrate.

Thermal resistance of the heat pipe unit in the conventional passive (Figure 4.5 (a)) and that of the TEC based active path (Figure 4.5 (b)) was obtained as 0.3 and 0.2 $°CW^{-1}$ respectively from separate experiments and is described in section 4.4.2. The effect of the variation of these resistances on the heat dissipation from chip is presented in Figure B.3 and Figure B.4 respectively for a hybrid system with r_C = 0.5 at T_{amb} = 40 °C when T_{chip} = 85 °C using the model. The variation was found to have less than 8 and 5% effect on the heat dissipation from the chip for a ± 50% change in the thermal resistances of these heat pipe units respectively.

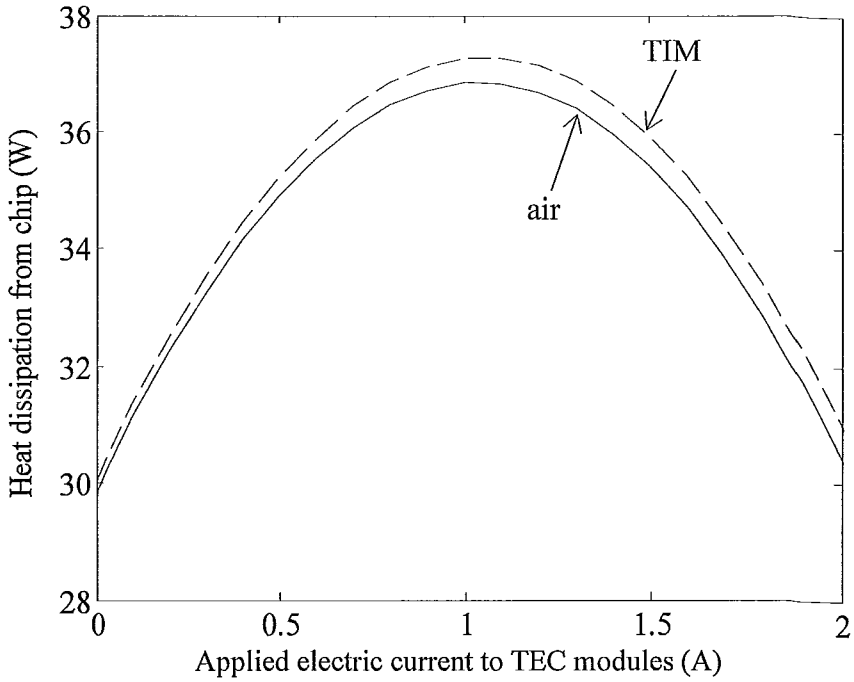


Figure B.1: Effect of thermal interface material (TIM) thermal resistance on the heat dissipation from the chip at different applied current at T_{amb} = 50 °C for the hybrid system with r_C = 0.5 and at T_{chip} = 85 °C.

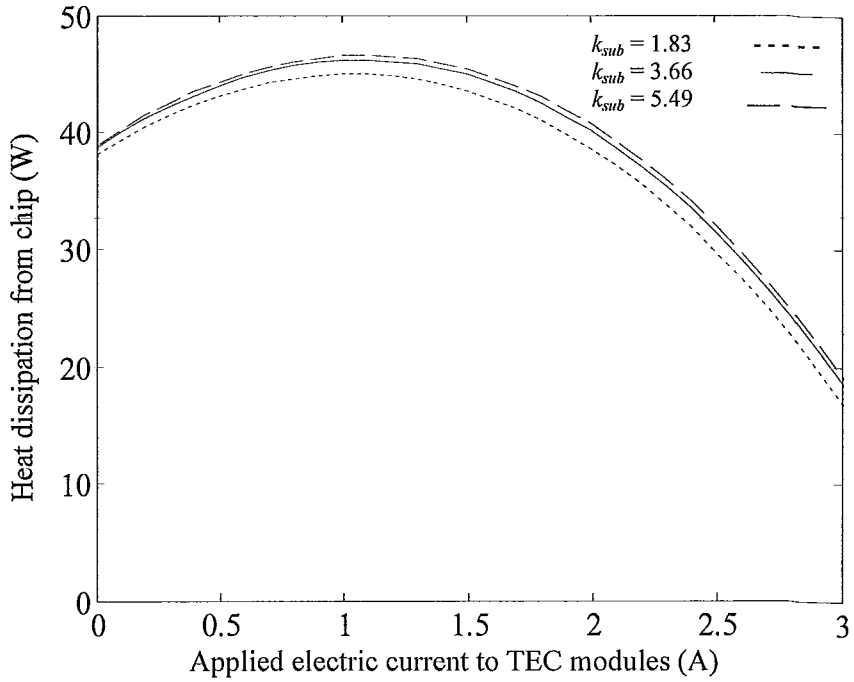


Figure B.2: Effect of the thermal conductivity of the ceramic substrate on heat dissipation from chip at different applied current at T_{amb} = 40 °C for hybrid system with r_C = 0.5 and at T_{chip} = 85 °C.

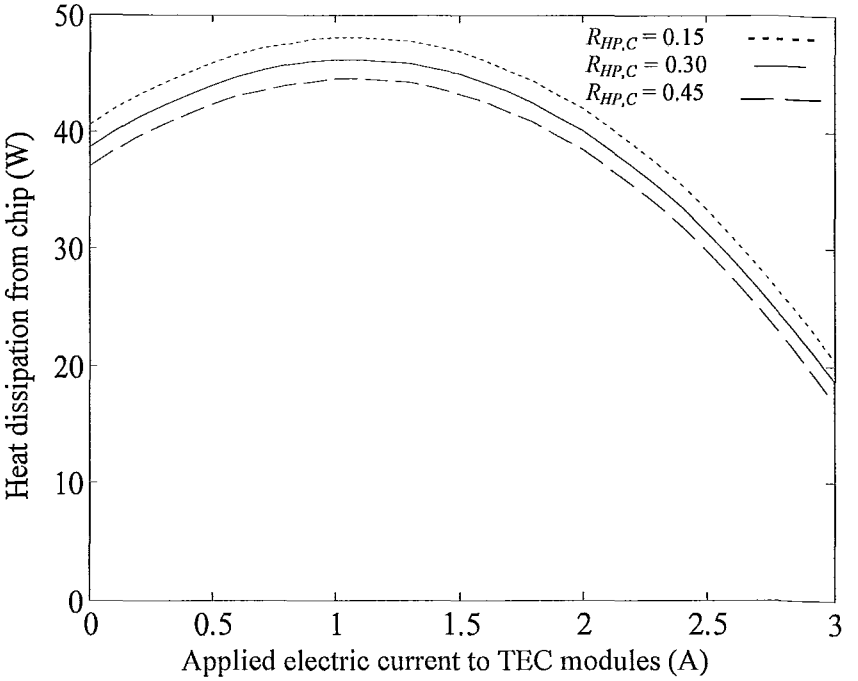


Figure B.3: Effect of the thermal resistance of the heat pipe unit in the conventional passive path on heat dissipation from chip at different applied current at T_{amb} = 40 °C for hybrid system with r_C = 0.5 and at T_{chip} = 85 °C.

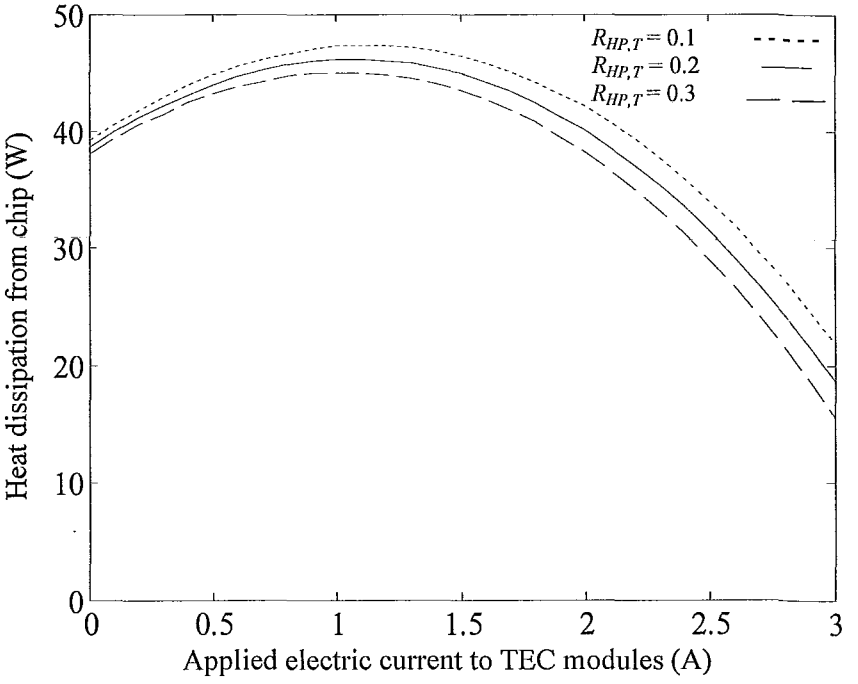


Figure B.4: Effect of the thermal resistance of the heat pipe unit in the TEC based active path on heat dissipation from chip at different applied current at T_{amb} = 40 °C for hybrid system with r_C = 0.5 and at T_{chip} = 85 °C.

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