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A Hysteresis Space Vector PWM for PV Tied Z-Source NPC-MLI With DC-Link Neutral Point Balancing

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ABSTRACT The Photo-voltaic (PV) tied Z-source Neutral-point clamped multilevel inverter (Z-NPC-MLI) is used in solar grid connected applications due to its single stage conversion and better performance. Though the Z source inverters adaptation is accepted in grid connected technology, the need for suitable controller and PWM scheme are necessary to meet out the performance such as shoot through switching, neutral point balancing, and harmonic reduction. The space vector pulse width modulation (SVPWM) strategy is a prominent modulation technique for Z-source NPC-MLIs due to the flexibility to select the appropriate voltage vector. Previous publications have shown the control of a Z-source MLI using the SVPWM with and without modification of shoot through switching. However, the current controller (CC) based SVPWM is not matured, which is the most essential consideration for the grid connected inverter to provide neutral point balancing, shoot through control for low harmonic distortion and a high quality current. With all these aims, this paper presents a PV tied Z-NPC-MLI grid connected system with a unique hysteresis current control SVPWM (HSVM) strategy with neutral point (NP) balancing control and direct current control in the inverter input side. Also, the proposed HSVM is assuring the grid connection with high quality voltage and current waveforms. This CC based SVPWM for Z-NPC MLI has been validated through simulation and FPGA based experimental investigations. The results are confirmed the feasibility and reliability of the proposed HSVM for the PV tie grid connected Z- Source NPC-MLI.

INDEX TERMS Z source MLI, neutral-point clamped inverter, space vector PWM (SVPWM), hysteresis current controller (HCC), neutral point balancing.

I. INTRODUCTION

Renewable resource (RER) is inevitable in the present power generation system (PGS) era which recently witnessed an exponential growth worldwide, and is expected to continue in the same direction. After hitting about 401GW of solar photo-voltaic (PV) power capacity by the end of 2017, global solar PV capacity is expected to hit 800GW soon [1]. The photo-voltaic (PV) power generation needs a two-stage power conversion (DC to DC by buck-boost converters and DC to AC by inverters). Nevertheless, due to this two-stage power conversion and converters usages, the overall system cost and efficiency is not desirable, since it involves more active and passive components [2]. After the arrival of Z source inverters [3], the two-stage power conversion (DC to DC and DC to AC) is made possible through single stage(DC to boosted AC), which reduced circuit size, losses and cost [4]. Hence Z-source inverter is considered an interesting topology for drives and PV applications [5]–[7] The combining Z source concept with multilevel inverters (MLIs) is most successful in terms of reduced conversion stage, enhanced system performance [8], [9]. Particularly, Neutral-point clamped (NPC) MLI is the good choice among other MLI topologies due to their circuit structure and operation is quite similar to conventional six switch voltage source inverter (VSI) [10].

In Z source inverter, the boost operation is decided by the shoot through (ST) switching state, in which the inverter input DC-link voltage is short circuited via Z source inductors and

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capacitors [11]. When the pulse width modulation (PWM) is used in the Z source inverter, it is fully capable to handle ST events for handling the inverter internal issues such as DC-link control and to improve quality of the output. The PWM approaches are investigated by adjusting the carrier positions and altering the shoot through (ST) for minimum, constant and maximum boosting methods. The SVPWM strategy provides opportunity to deal the switching sequence directly [12], [30], which facility is not possible in carrier based PWM. The P. C. Loh *et.al* has proposed SVPWM for controlling three-phase three-level Z-MLI with 24 ST options [13]. Followed by [14] F. B. Effah *et.al* developed a new set of ST options, where the authors used 12 ST states. These attempts have well concluded about controlling the inverter voltage. However, the current control is not attempted which the main factor of dc-link capacitor balancing.

In grid connected power systems, to overcome the transformer usage issue, researchers have proposed different PV powered transformerless (TL) inverters for both single and three-phase systems [15, 16]. There are many innovations in single phase TL inverter topologies, in which the idea is to only mitigate the leakage current by adding the extra power switches in the main inverter circuitry. In three-phase networks, the researchers are totally involved with PWM and current control design algorithms [17], [18]. The Z source MLIs are the better choice for PV applications compared to two-level VSIs, with respect to reduction of harmonic content output waveforms and common mode voltage (CMV) suppression filters and EMI filters. According to TL grid tied inverter, the control of the inductor current along with the grid voltage synchronization is essential. Therefore, the combined current controller (CC) and voltage control PWM is interesting for such TL grid connected system. There are a variety of CCs are available for controlling the electrical power [19]. Among them, the hysteresis current controller (HCC) is a potential one, as it has simple control competence associated with PWM methods [20], [21]. Very few attempts have been made on SVPWM based HCC [22], [23]. However, these methods are involving difficult mathematical operation to locate the active switching vector and also the capacitor balancing is very hard to attain. In practice, maintaining these capacitors is much challenging. This deceptive curtail reduces the NP capacitor's lifespan due to the NP fluctuation between the capacitors crops the high voltage and current harmonics, which leads to the inferior grid power quality. There are few attempts made for capacitors balancing through the separate balancing circuits as well as PWM algorithms [24]–[27], [31]–[33]. Here, rather a circuit based balancing; PWM algorithms gave an attractive result. Among the reported PWM methods and their ideologies, the SVPWM based consideration was superficies [29]. Based on the above organized discussion, the TL PV tied grid system requires a stable power converter, current controller and PWM technique for the straight forward operation, less cost, and high performance. In context with capacitor balancing in Z source NPC MLI, few examples found in [28], [31] using SVPWM and carrier level-shifted based control, which are not discussed about the current control.

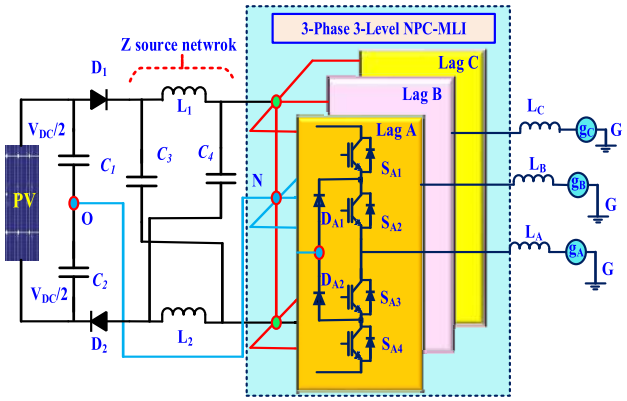

FIGURE 1. PV tied grid connected three-phase three-level Z source NPC-MLI.

With this motivation, this paper suggests the three-phase three-level PV connected Z source-MLI for the utility grid. The Hysteresis current control based SVPWM (HSVM) control system is designed for the grid synchronization. The proposed HSVM eliminates the low frequency oscillations using suitable ST (Upper and Lower ST), with regular switching events, which ensures the DC-link capacitors balancing along with current control. The proposed system is simulated and verified through MATLAB/Simulink software. The experimental prototype 2-kW solar panels attached grid connected three-phase three-level Z-NPC-MLI is established and the validation is done through Xilinx family SPARTAN-6 controller. The results obtained from the simulation and experiment is confirming the technical feasibility and advantages such as reduced harmonics and neutral point balancing of the proposed HSVM.

In addition the results have shown the uniqueness of the proposed current controller involvement with SVPWM for improving the inverter performance. The section II elaborates about the Z source NPC-MLI topology, concepts of shoot through, and design concepts of Z network. The HCC based SVPWM for Z-NPC-MLI is presented in section III. Section IV brings out the simulation and experimental verifications. Finally, conclusions are summarized in section V.

II. Z-SOURCE NPC-MLI TOPOLOGY

The Z-source concept applied to MLI gives more advantages like suppression the voltage ripples, flexible shoot through state and neutral point balancing. Therefore, this session describes the Z-NPC-MLI power circuit, its operation and the design of Z Network components along with analysis of topology.

A. Z-NPC-MLI

The Fig.1 shows the power circuit topology of Z-NPC-MLI in three-phase three-level structure, which consists of three legs, and each leg has four power switches ($S_{1A} - S_{4A}$) with

TABLE 1. ST and non ST operation of Z-NPC-MLI.

Mode	Switching State	Tuned on switches	Action	V_{out}
NST	+1	S_{X1} S_{X2}	-	$(V_{DC}/2)+L_1*(d_i/d_t)$
	0	S_{X2} S_{X3}	-	0
	-1	S_{X3} S_{X4}	-	$-(V_{DC}/2)-L_2*(d_i/d_t)$
ST	Full ST	S_{X1} S_{X2} S_{X3} S_{X4}	Charging L_1 & L_2	0
ST_T	Top ST	S_{X1} S_{X2} S_{X3}	L_1 Charging	0
ST_B	Bottom ST	S_{X2} S_{X3} S_{X4}	L_2 Charging	0

2 clamping diodes (D_{A1} and D_{A2}). The Z source impedance elements ($L_1 = L_2 = L, C_3 = C_4 = C$) are connected in the input side and obtaining power from DC-link. Two DC-link capacitors (C_1, C_2) are serially coupled with DC input source, which split the DC-link voltage as $V_{DC}/2$ for making the multilevel output as 0, $V_{DC}/2$, and V_{DC}. In the load side, each inverter leg is connected to grid by using inductor ($L_A = L_B = L_C = Lg$). The Z-NPC-MLI is operating with shoot through (ST) and non-shoot through (NST) modes. In ST mode, the input DC supply is short circuited through inverter switch and Z –network inductors, to store the energy in the inductors, L1 and L2. During NST mode, the DC power is converted to AC power (through normal inverter switching).

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By considering one leg in NPC-MLI, the operation is described by three switch options; 1(both upper switch ON), 0(middle switch ON),-1(both lower switch ON). Including Z source operation with NPC-MLI regular switching operations, the ST mode is created in order to short the input DC supply through inductors by switching ON all the four switches in the leg, which is called as full shoot through (FST). Alternatively, for reducing the switching losses, the top ST (top 3 switches is ON in a leg) and bottom ST (bottom 3 switches is ON in a leg). The table-I describes all the possible combinations of the switching options for Z-NPC-MLI.

B. ST AND NST OPERATION OF Z-NPC-MLI

The ST and NST mode of operation of the circuitry is shown in the Fig.2. During the ST mode, the inverter can be involved

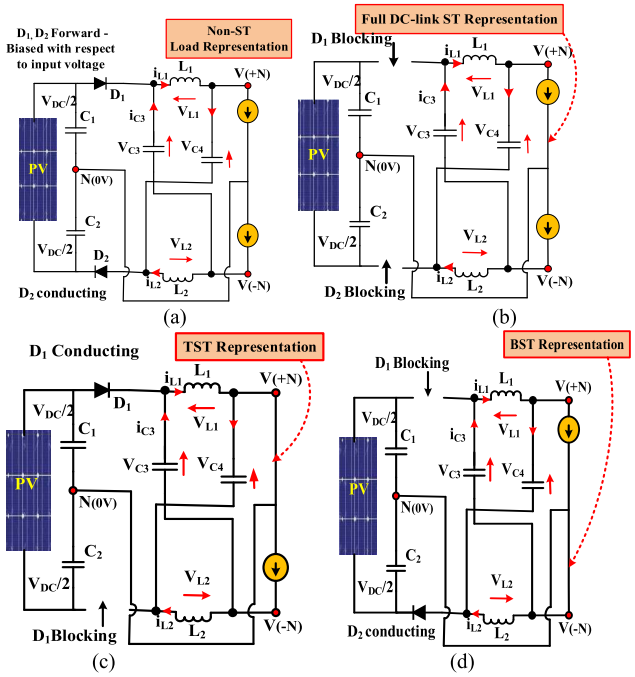

FIGURE 2. ST and NST mode operation of Z source NPC-MLI; (a) Non-ST (NST),(b) full-ST,(c)TST,(d)BST.

either full ST or partial ST [28]. Though, the both methods are shorting the input DC source via inductors L_1 and L_2, the full ST(FST) is not a best choice of balancing the inductor's charging profile (nonlinearity charging) and it roots the high magnitude of lower order harmonics in the output waveforms. Since the top-ST(TST) and bottom-ST(BST) has an individual control on the L_1 and L_2 charging characteristics, the combination of TST and BST maintains the inductors charging in parallel, which ensures the better quality output waveform [8], [13].

C. DESIGN OF Z SOURCE NETWORK

The In the Z network, calculation of the Z network elements (Inductor(L) and Capacitor(C)) and its charging, discharging and boosting functions are important. During ST period, while considering the symmetry charging and discharging nature on L ($L_1 = L_2 = L$) and C ($C_3 = C_4 = C$), the role of the inductor is to limit the current ripple during shoot-through state. The capacitor absorbs the current ripple and achieves a quite stable voltage. The inductor is charged by the capacitor during shoot-through time(T_{sh}). ΔI is current ripple of the inductor.Inductor and capacitor values are calculated as $L = \frac{VT_{sh}}{\Delta I}$ and $C = \frac{\bar{I}_L T_{sh}}{\Delta V_C}$ respectively. The average current of the inductor can be found from $\bar{I}_L = \frac{P}{V_{PV}}$. The ΔV_C is the assumed voltage ripple of the capacitor. V_{PV} is PV output voltage, P is the total power. The voltage across the inductors and capacitors are approaches to V_L and V_C respectively, where $V_{L1} = V_{L2} = V_L = L_1(di/dt) = L_2(di/dt)$ and $V_C = V_{C3} = V_{C4} = V_{DC}/2$. During the NST mode, $V_L = V_C = V_{DC}/2$. This condition is satisfied, since the

capacitors C_1 and C_2 are connected in parallel and voltage across the Z source network will be $2V_C$. In ideal conditions, $V_L = V_C$ and $2V_C = 2V_{dc}$. During this condition, the inverter output voltage, $V_o = 0$.

From the Fig 2, considering NST mode of operation (see Fig. 2.a); when diode D_1 and D_2 are in forward bias conduction,

The inductor voltage,

$$V_{L1} = V_{DC} - V_C \tag{1}$$

$$V(+) \Longrightarrow \frac{V_i}{2};\ V(-) \Longrightarrow -\frac{V_i}{2} \tag{2}$$

$$V_i = 2V_C - V_{DC} \tag{3}$$

During TST mode operation as shown in Fig.2.c, the diode D_1 is in conduction and D_2 is in blocking state. Hence, the inductor voltages are obtained as,

$$V_{L1} = \frac{V_{DC}}{2};\ V_{L2} = 0 \tag{4}$$

$$\text{and,}\ \ V(+) = 0V;\ V(-) = \frac{V_{DC}}{2} - V_{C3} \tag{5}$$

During BST mode operation as shown in Fig.2.d, the diode D_2 is in conduction and D_1 is in blocking state. Hence the inductor voltages are obtained as,

$$V_{L1} = 0; V_{L2} = \frac{V_{DC}}{2} \tag{6}$$

$$\text{and,}\ \ V(-) = 0V;\ V(+) = -\frac{V_{DC}}{2} + V_{C4} \tag{7}$$

At steady state condition, the Z- network inductors L_1 and L_2 average voltage in one T cycle is zero.

$$V_{L1} = \frac{(V_{DC} - V_C) * T_{NST} + \left(\frac{V_{DC}}{2}\right) * T_{TST} + \left(\frac{V_{DC}}{2}\right) * T_{BST}}{T} \tag{8}$$

$$T_{NST} + T_{TST} + T_{BST} = T \tag{9}$$

$$V_C = \frac{V_{DC} * \left(1 - \frac{T_{TST}+T_{BST}}{2T}\right)}{\left(1 - \frac{T_{TST}+T_{BST}}{T}\right)} \tag{10}$$

Using V_C in NST, TST and BST mode operations, the DC-link voltage of the inverter for NST, TST and BST is derived as,

$$V_{i\_NST} = \frac{V_{DC}}{\left(1 - \frac{T_{TST}+T_{BST}}{T}\right)} \tag{11}$$

$$V_{i\_TST} = V_{i\_BST} \frac{V_{DC}/2}{\left(1 - \frac{T_{TST}+T_{BST}}{T}\right)} \tag{12}$$

Form the Eqs. (11) and (12) during TST and BST, the voltage present in the DC-link is half that of NST. Hence, it is proven that by equally sharing TST and BST mode using input DC-link capacitors (C_1 and C_2), the inverter is boosting voltage with proper DC-link balancing, which helps to improve the THD performance on the output voltage and current waveform.

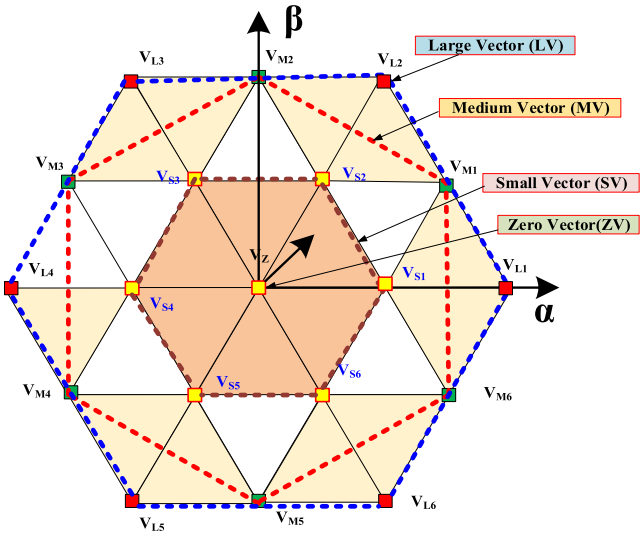

FIGURE 3. SVD of three-phase three-level Z-NPC-MLI.

The inverter peak ac voltage output, Vx_0(x={A,B,C}) is resulting as,

$$V_{x0} = \frac{M}{\sqrt{3}} V_{i\_NST} \tag{13}$$

$$V_{xo} = \{\frac{M}{\sqrt{3}} V_{DC} \frac{1}{\left(1 - \frac{T_{TST}+T_{BST}}{T}\right)} = \{\frac{M}{\sqrt{3}} V_{DC} B_F \tag{14}$$

where B_F is boosting factor ($B_F \geq 1$).

III. HCC BASED SVPWM FOR Z-NPC-MLI

SVPWM technique offers the flexibility in selection of switching states [14]. The hysteresis current control (HCC) method gives an opportunity of harmonics reduction. To widen the scope of SVPWM, the hysteresis current control strategy has been incorporated to achieve the better harmonic reduction and neutral point balancing in Z source NPC-MLI. The theory of SVPWM presented in view of conventional and proposed techniques. A closed loop PV-tied grid connected control strategy developed is described in this section.

A. OPERATION OF CONVENTIONAL SVPWM FOR NPC-MLI

The Fig. 3 shows the three-level space vector diagram (SVD) with the different switching state vectors. For normal inverter operation (during the NST mode), the inverter has four different switching vectors (zero vector {ZV}, small vector {SV}, medium vector {MV}, and large vector {LV}) to bring the multilevel output voltage [26]. These four switching vectors are forming a hexagon (called space vector diagram) using their 27 switching states, among which 3 for ZV, 12 for SV, 6 for MV and 6 for LV.

According to the SVD presented in Fig. 7, every switching action has an individual phase current, which affects the DC-link capacitors/NP balancing. For example, at SV switching state [1 0 0], the B and C phases are linked with neutral point 'O' and phase-A is associated to input DC link. Hence,

TABLE 2. ST and non ST operation of Z-NPC-MLI.

(+)ve SVs	i_{N_P}	(-) ve SVs	i_{NP}	MVs	i_{N_P}	LVs	i_{N_P}	ZVs	i_{N_P}
[0-1-1]	i_A	[1 0 0]	$-i_A$	[1 0-1]	i_A	[1-1-1]	0	[111]	0
[-10-1]	i_B	[0 1 0]	$-i_B$	[0 1-1]	i_B	[11-1]	0	[000]	0
[0 0-1]	i_C	[1 1 0]	$-i_C$	[-1 10]	i_C	[-11-1]	0	[-1-1-1]	0
[0 1 1]	i_A	[-10 0]	$-i_A$	[-1 01]	i_A	[-111]	0	-	-
[1 0 1]	i_B	[0-1 0]	$-i_B$	[0-1 1]	i_B	[-1-11]	0	-	-
[-1-10]	i_C	[0 0 1]	$-i_C$	[1-1 0]	i_C	[1-11]	0	-	-

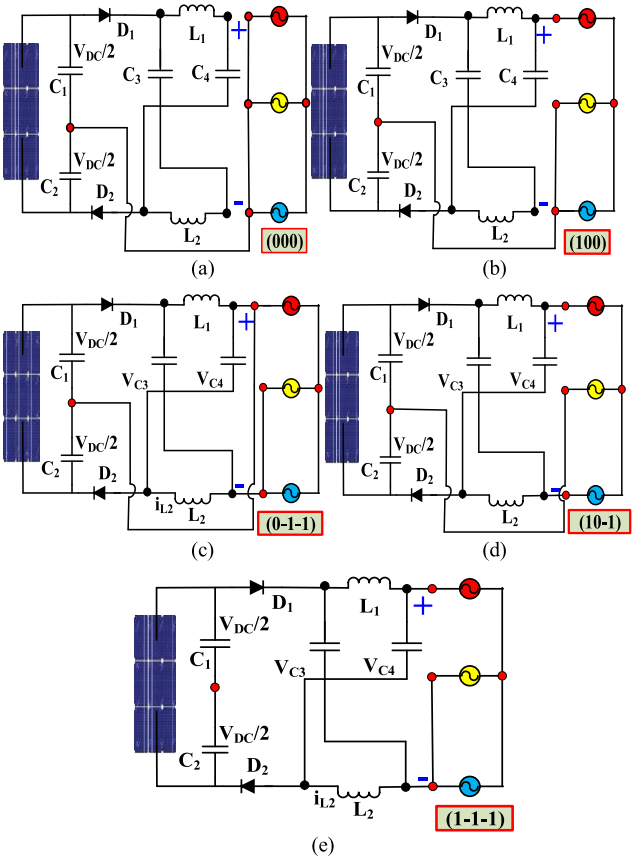

FIGURE 4. Switching state of Z source NPC-MLI; (a) ZV[000], (b) Negative current SV[100], (c) positive current SV[0 −1 −1],) (d) MV[10 −1], (e) LV[1 −1 −1].

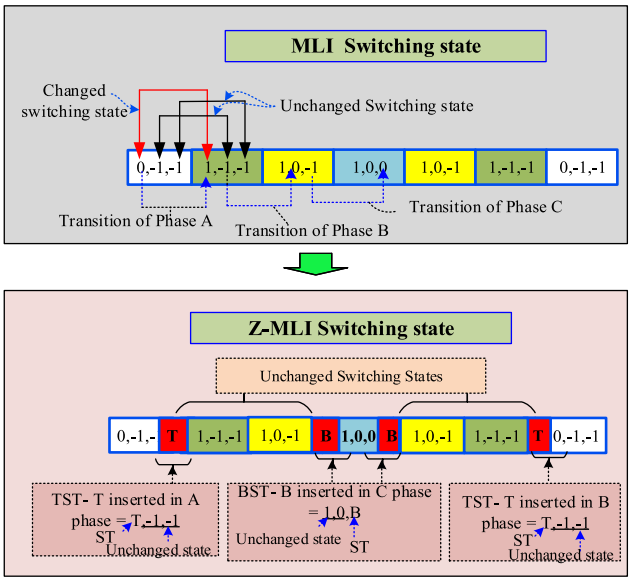

FIGURE 5. $\Delta_{1,2}$ ST switching state creation for Z-NPC-MLI.

neutral current ($I_N = i_A + i_B + i_C$) approaches to $-i_A$ ($i_B + i_C = -i_A$). For balanced DC-link condition, the I_N should be zero. Table-II shows the different switching of the three phase currents for the three-level NPC-MLI. Here, the ZV and SV have a redundant switching privilege, which helps balancing the DC-link. However, the MV and LV has only unique switching option for a sector. Hence, these vectors not helping for NP self-balancing. The Fig.4 shows the SVD with their different switching states of ZV, SV, MV and LV including phase currents.

Now, for creating TST and BST, the proposed SVPWM is considering SVs, since they have a redundant switching privilege which helps the inverter DC-link balancing. In the following section explains the operation of ZNPC-MLI SVPWM in detail.

The Fig. 5 shows the creating of ST switching for Z-NPC-MLI. The TST and BST chosen based on switching state transition. Considering sector-1, the sub-triangle $\Delta_{1,2}$ as shown in Fig.5, the regular MLI switching pattern is {[0 −1 −1], [1 −1 −1], [1 0 −1], [1 0 0], [1 0 −1], [1 −1 −1], [0 −1 −1]}. Here, considering proposed Z-MLI, ST is fixed through changes in the adjacent switching state. For example, the 1st switching state [0 −1 −1] and their next [1 −1 −1] the transition is only on A-phase switching (0→1). Therefore, the ST is fixed through TST in A-phase and fixed between [0 −1 −1] and [1 −1 −1].

Similarly, in the same $\Delta_1, 2$ switching states series [1 0 −1] and [1 0 0] differs from their C-phase. Hence the next ST is fixed through BST in C-phase and fixing in between [1 0 −1] and [1 0 0]. The TST and BST selections are chosen based on the current flow directions on the inverter from DC-link to load. When, bit change in 0→1, the TST is chosen and when the bit change in −1 →0, the BST has chosen. The ST interval for both TST and BST is depend on the boosting factor using Eq(12). In order to maintain the NP self-balancing and volt-sec balancing, the inverter switching selections are starting from A- phase to C- phase in a forward switching and following the reverse same sequence order. The TST and BST switching states timing is sharing from the regular switching, which ensure the symmetry output voltage.

For example in Fig.6, when the target vector lies in $\Delta_{1,2}$ the TST is time calculated from the boosting factor and it is fixed between [0 −1 -1] and [1 −1 −1] without changing switching frequency. Using this method, the number of power switching commutations in a switching cycle is same as traditional NPC-MLI, which ensures the switching losses in the

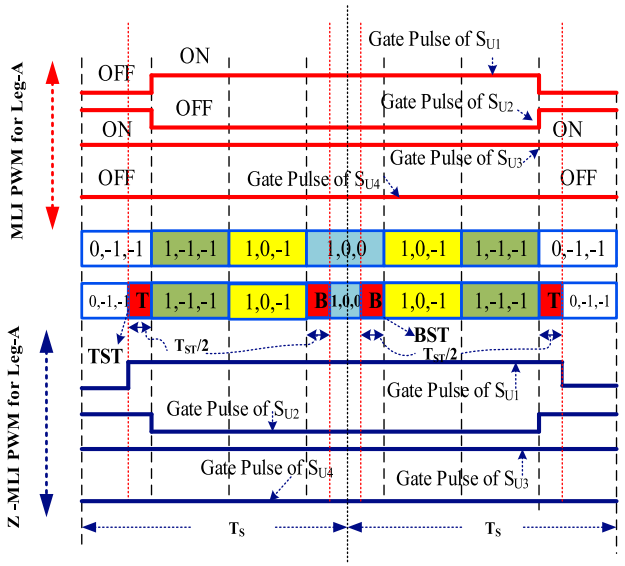

FIGURE 6. $\Delta_{1,2}$ ST and NST switching state and PWM pulse for Z-NPC-MLI.

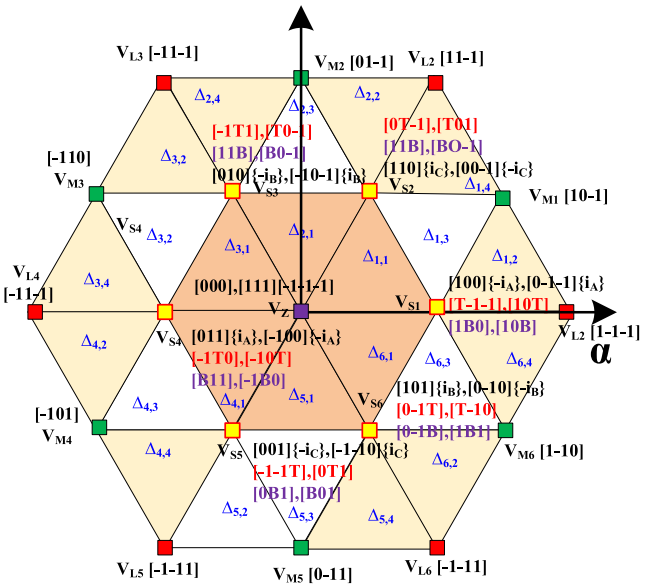

FIGURE 7. SVD for three phase three Level Z source NPC-MLI including TST, BST and individual phase currents for NST switching states.

Z-NPC-MLI. In this method, when the inverter is operating in lower modulation index (M_a)/ buck mode, there is no STs are inserted.

Therefore, this is ensuring the avoidance of collapse in inverter line to line voltage and NP balancing. In the next stage, the proposed HCC and the concepts used for neutral point balancing are discussed

B. HYSTERESIS CURRENT CONTROL BASED SVPWM

In proposed SVPWM current control method, the hysteresis bands are directly used to employ the four groups of (ZV, SV, MV and LV) vectors in SVD. Here the current control is made based on current error (error vector, $\vec{\Delta}_i$) and available switching options on SVD. The proposed structure is principally employed to retain the $\vec{i}_{Lact}$ close to the $\vec{i}_{Lref}$ inside the hysteresis band values. To compensate for the complication of achieving the CC along with capacitors balancing, the SVPWM is modified based on the hysteresis band 'H'.

Fixed frequency HCC can be obtained by calculating the hysteresis band H using the transient value of the V_g and output voltage of PV array.

Based on that, the hysteresis band 'H' is calculated as,

$$H = \frac{V_g(V_{PV} - 2.V_g)}{V_{PV}.L.f_s} \tag{15}$$

where, the variant parameters are V_{PV}, V_g, f_S and fixed one is filter inductor (L). When the reference current (i_{Lref}) and actual current (i_{Lact}) lie in SVD error vector, $\vec{\varepsilon_i}$ is calculated as,

$$\vec{\varepsilon_i} = \overrightarrow{i_{Lref}} - j\overrightarrow{i_{Lact}} \tag{16}$$

where, $\overrightarrow{i_{Lref}} = i_{Lref\alpha} + ji_{Lref\beta}$; $\overrightarrow{i_{Lact}} = i_{Lact\alpha} + ji_{Lact\beta}$ When the $\vec{\varepsilon_i}$ expressed in the SVD plane with $\alpha\beta$-vector

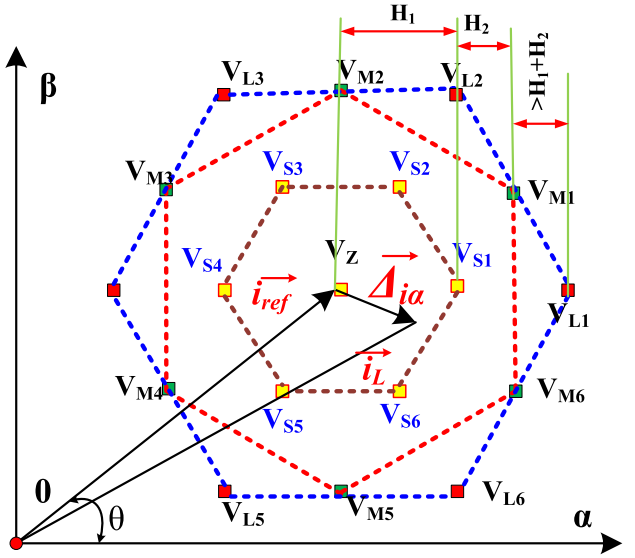

FIGURE 8. SVHCC for three-phase three-level Z source NPC-MLI.

components frame, the $\vec{\varepsilon_i}$ can be represented as,

$$\vec{\varepsilon_l} = \overrightarrow{\Delta_{l\alpha}} + j\overrightarrow{\Delta_{l\beta}} \tag{17}$$

From Eq (17), the position of the $\vec{\varepsilon_i}$ in SVD is calculated and then the switching vectors are selected to keep the $\vec{i}_{Lact}$ close to the $\vec{i}_{Lref}$. The Fig.8 shows the HSVM with $\vec{\varepsilon_i}$ and H. Here, the sector and sub-triangle, and its switching state selection is done based on the $\vec{\varepsilon_i}$ and H. The boundary area is determined by the hysteresis bands (H_1 and H_2).

The values of H_1 and H_2 depends on $\vec{i}_{Lref}$ and its control dynamics. The values of H will vary between zero and H (Eq.15). Here the maximum value of the H is related with maximum operation modulation (Modulation Index, M_a). To

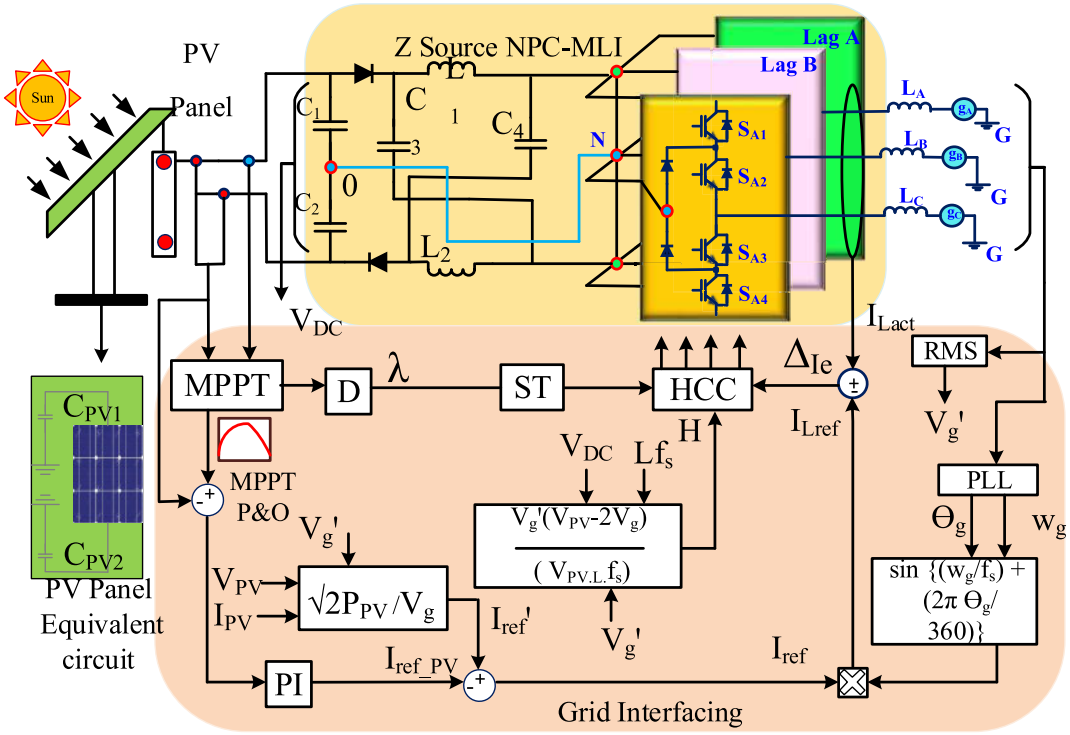

FIGURE 9. The Proposed Grid-connected PV connected Z-NPC-MLI control blocks representation.

find the value of $\overrightarrow{\varepsilon_i}$ and H, the proposed SVD operating in three environments which are H_1, H_2, and $> H_1 + H_2$.

During the H_1 interval the switching selection is directed to use for ZV and SV. Similarly, for H_2 the SV and MV, and when H is beyond $H_1 + H_2$, the SV, MV, LV switching states are selected.

C. NEUTRAL POINT/DC-LINK BALANCING

In the proposed HSVM is using nearest three vectors N3V switching selection vector selection [20], [22]. Based on the $\overrightarrow{\varepsilon_i}$ tip, the HSVM choose the sector and sub-triangle, and switch the vertices of the triangle in every switching period for the hysteresis region using all available vector to get zero phase current. For example, if $\overrightarrow{\varepsilon_i}$ tip is situated in H_1 region, the control lies in the triangle Δ_1, 1, switching vectors, V_{Z0}\{[000], [111], [−1 −1 −1]}, V_{S2}\{[110], [00-1]} and V_{S3}\{[010], [−10 −1]} are selected with their ST options. Similarly, when vector lies in $\Delta_{1,3}$, in order or to balance the NP the vector switching are chosen in redundant manner as shown in Fig.10. Here, the SV switching sequences [0 −1 −1], [110] has chosen as a starting switching state to synthesis the reference vector. Hence, at target reference vector lies in $\Delta_1, 3$ the vector synthesization is happen in two time to balance the capacitor. Other sub-triangles $\Delta_{1,2}$ and $\Delta_1, 4$ are have only one, since they involve MV and LV. As shown in Table-1, and in the LV phase current is zero. However, the MV showing the particular phase current which is causes the small disturbance in DC link balancing. As per the NP fluctuation standard this is considerably small.

Actual load current and reference current tracking performance with fixed H band (5Amps). The tracking performance is executed with 50Hz and 60 Hz reference current. From the waveform, it could see that the actual current is clearly tracking the reference current with decent steady state and transient response. To validate the DC-link capacitors (V_{C1} and V_{C2}) balancing for HSVM, the simulation is performed for both conventional and proposed HSVM, which are shown in Fig. 14 (a) and Fig. 14. (b), respectively. The NP fluctuation (NPF) is calculated from V_{C1} and V_{C2};

$$\text{NPF} = \frac{(\frac{V_{DC}}{2}) - V_{C1}}{V_{C1}} \tag{18}$$

From the Eq.(18), the proposed HSVM NPF is very less (calculated as ≈1%) the conventional Z-source SVPWM (calculated as ≈10%), which ensure the output voltage and current waveform quality. Based on the results, the proposed HSVM claims that it is not only controlling current and it is also maintaining the NP current.

D. CLOSED-LOOP PV TIED GRID-CONNECTED CONTROL STRATEGY OF PROPOSED Z-NPC-MLI

The grid-connected PV connected Z-NPC-MLI control blocks representation is shown in Fig. 9. The system is classified into four modules, namely; PV module, boosting X-network, Z-NPC-MLI, and grid interfacing control system. In the solar module, the PV voltage and current are measured and given to P&O technique based MPPT. Here the λ is arrived from MPP gain and given as ST to HCC. The ouput of

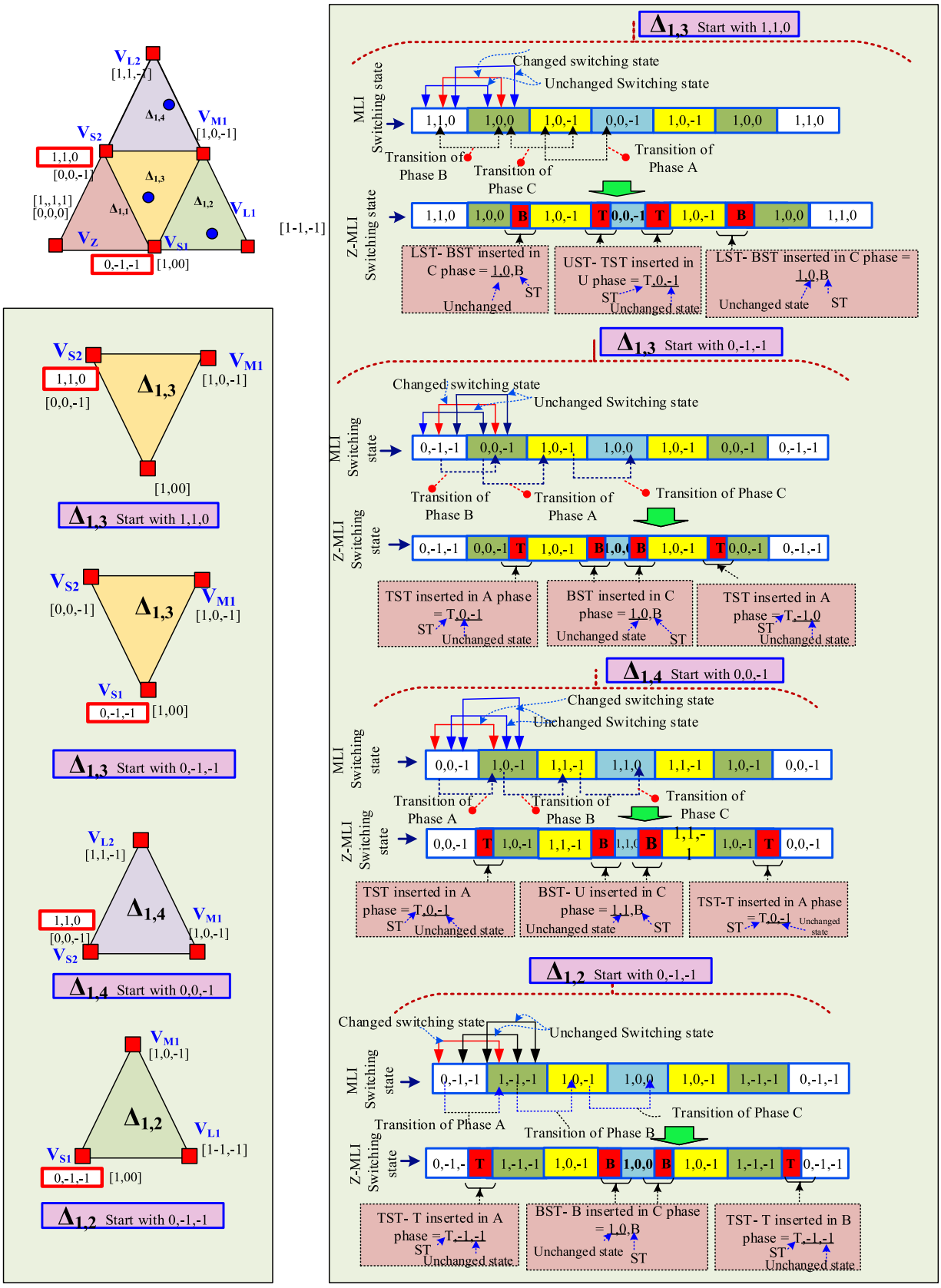

FIGURE 10. Sector-1 ST and NST switching state.

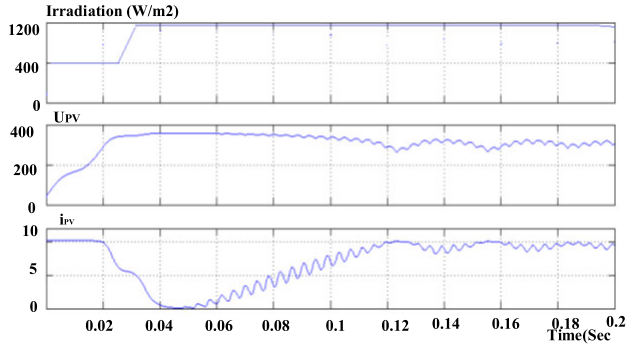

FIGURE 11. Simulation results of PV output.

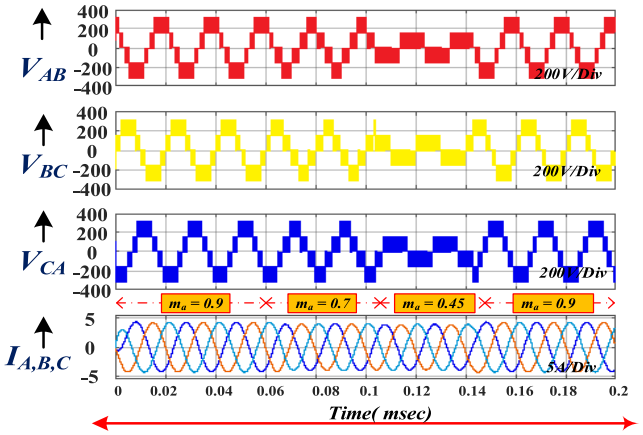

FIGURE 12. Simulation results of three phase voltage and current waveform of Z-NPC-MLI.

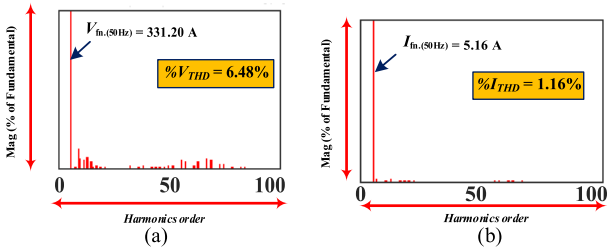

FIGURE 13. Simulation results of harmonics spectra for Z-NPC-MLI atm$_a$ = 0.9; (a) voltage harmonics spectra,(b)current harmonics spectra.

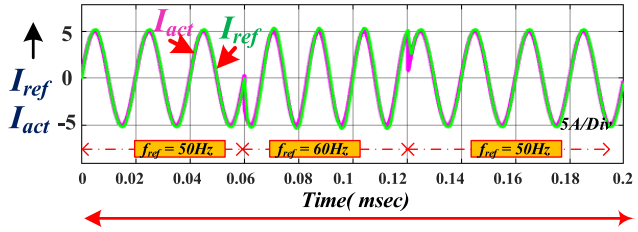

FIGURE 14. Simulation results of actual load current and reference current when H band is fixed at 5Amps.

the PV is connected directly to inverter DC-link and The C_1 and C_2 DC-link capacitors are splitting the DC-link voltage. This equaliency is maintained by the inverter proposed SVM switching.

In the outside, the PLL is implemented on the grid side to calculate grid angle θ_g and utility grid nominal frequency ($w_g = 2Vf_o$), f_o is grid voltage frequency) for the grid synchronization. The simplest Zero-Crossing Detection (ZCD) algorithm has been used. The RMS value of grid voltage (V_g') is measured and given to the I_{ref}' estimation block. The I_{ref}' sampling calculated from V_{PV}, I_{PV} and RMS values of grid voltage V_g' as below,

$$I_{ref}^{*} = \frac{\sqrt{2}V_{PV}I_{PV}}{V_g'} \tag{19}$$

This I_{ref}^{*} is compared with PV reference current (I_{PV-ref}) and estimating the final grid reference current dc- component (I_{ref}), which is multiplied with sin $((w_g + f_s) + (2\pi\theta_g/360))$ to calculate the final grid reference current (I_{ref}). It is also called a inductor reference current (I_{Lref}). The actual inductor I_{Lact} and I_{Lref} gives the error of inductor current Δ_{ie} based on the $\overrightarrow{\varepsilon_i} = (i_{Lref} - i_{Lact})$. Finally, the calculated real-time hysteresis band H using eq(15) and Δ_{ie} gives gate pulses. The error Δ_{ie} and λ obtain the inverter switching options and ST duty cycle for the boosting, current controller and capacitor balancing of the Z-NPC-MLI.

IV. SIMULATION AND EXPERIMENTATION

In order to validate the performance of proposed system. A closed loop PV grid tied Z_NPC MLI system has been modeled in MATLAB-SIMULINK environment and a prototype model with 2kW PV tied grid connected Z NPC MLI system has been developed to carried out the experimentation. Experimental setup is shown in Fig.16. of 2-kWp roof-top PV panels (12 serial-parallel panels, each 250W) feeding a 2-kW three-phase 3-level Z-NPC-MLI grid connected system is developed. Xilinx family SPARTAN-6 FPGA controller is used to implement the hysteresis current control based SVPWM control scheme.

A. SIMULATION STUDY

The 2kW PV array modules are configured (series model) to feed the power to inverter with each module rated at 152.5W. The NPC-MLI maintains the dc-link voltage close to 250V using two (C_1 and C_2) 470μF capacitors. The inverter is connected to 300V/50 Hz utility grid through 4 mH inductors. The simulation result of the PV is given in the Fig.11. The effects of variation of solar irradiation on PV observed here around 12hr 33min noon. The observed voltage and current in the range of 320V to 400V and 7A to 10.2 A respectively.

The inverter switching frequency (f_{sw}) is maintained throughout the operation of the inverter as 5 kHz. Initially, the Z-NPC-MLI is simulated and investigated with grid connected system with fixed hysteresis bands. The inverter boosting factor set a 1.6, the inverter output voltage approach to 337V. The Fig.12 shows the inverter line voltages and

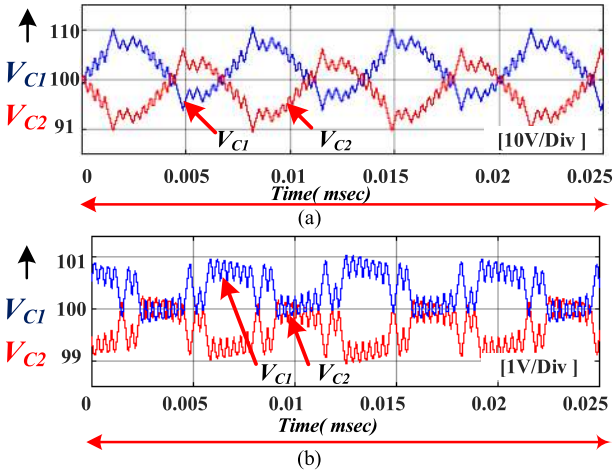

FIGURE 15. Simulation results of Z-NPC-MLI voltage across DC-link capacitors; (a) conventional SVM method, (b) HSVM.

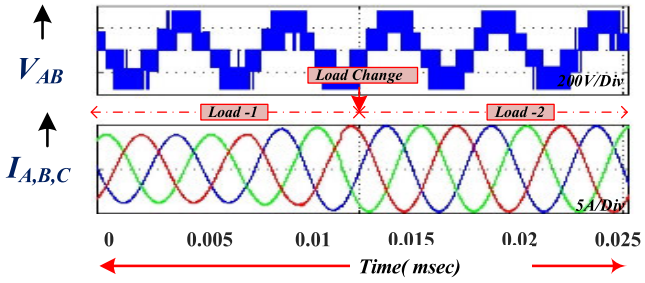

FIGURE 16. Simulation results -Transient response of inverter output currents.

phase value of load current for different operating conditions (different modulation index). During every operation instant, the inverter delivers the voltage and current with reduced harmonics in voltage and current. The Fig. 13 illustrates the voltage and current harmonics spectra for the maximum inverter operating point with $m_a = 0.9$. From the THD spectrum results in Fig.13, it is observed that, the inverter output having the nominal voltage THD (6.48%) and current THD (1.16%), due to the control of DC-link voltage, which are in the acceptable range.

The Fig. 14 shows load current responses while varying hysteresis band and change in reference current frequency. From the result, it can see that the load current tracks the reference current. The Fig. 15(a) and 14(b) shows the voltage across DC link capacitors with conventional SVPWM method and HSVM method respectively. It indicates that Neutral point fluctuation (NPF) of conventional SVPWM method is 10.6% where as 1.2% of NPF of proposed HSVM method [22]. Fig.16 shows the transient response of the proposed HSVM. During the change in load at 0.012msec, the HSVM topology has ensured the enhanced boosting factor and meeting out the load voltage and current requirements together with NP balancing.

The Fig. 17 common-mode voltage presented with different modulation indices. From that results it is understood

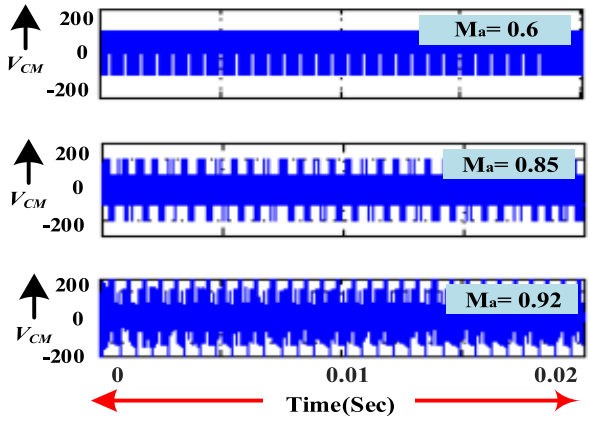

FIGURE 17. Simulation results – Common-mode voltage for the different modulation indies ($M_a = 0.6$, $M_a = 0.85$, and $M_a = 0.9$).

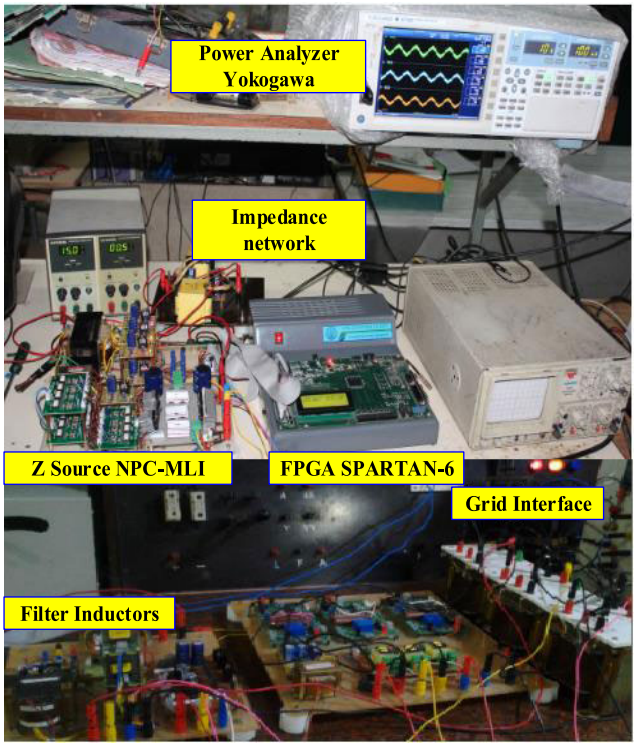

FIGURE 18. Experimental setup of proposed PV fed grid connected three phase three Level Z source NPC-MLI.

the common-mode voltage is maintaining as $V_{dc}/2$ for all modulation index operations.

B. EXPERIMENTAL STUDY

An experimental prototype model of 2-kWp roof-top PV panels (12 serial-parallel panels, each 250W) feeding a 2-kW three-phase 3-level Z-NPC-MLI grid connected system is developed. The complete experimental hardware set up is shown in Fig. 18. In the experiment, The Xilinx family SPARTAN-6 FPGA controller is used to implement the hysteresis current control based SVPWM control scheme. When

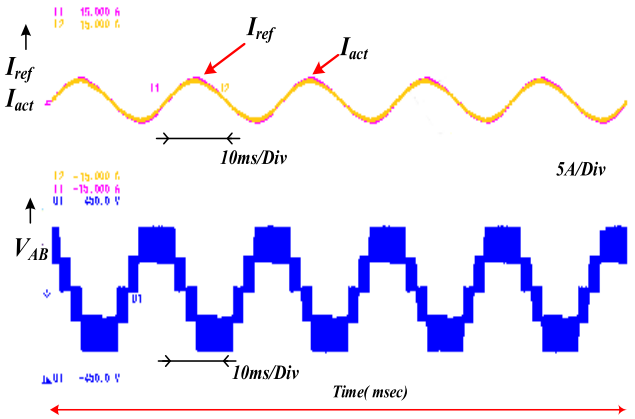

FIGURE 19. Experimental results for actual inverter current and reference current at $f_o = 50$ Hz and $V_{dc} = 200$ V, inverter Voltage (V_{AB}).

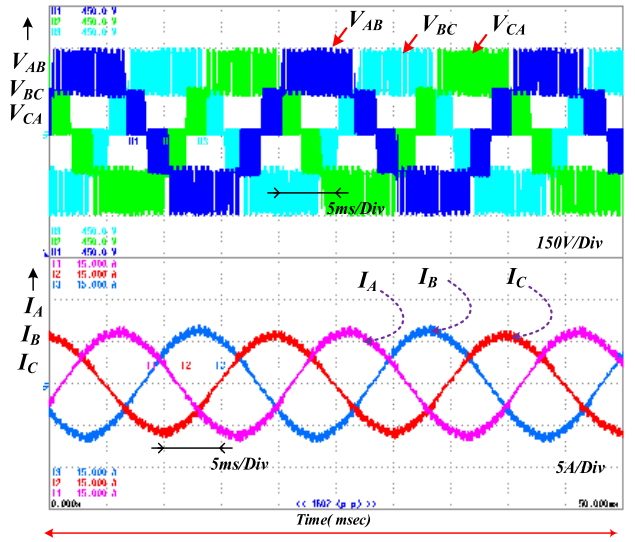

FIGURE 20. Experimental results for three phase inverter voltage and inverter current with $m_a = 0.8$ at $f_o = 50$Hz, $I_{load} = 5$A and $V_{dc} = 200$V.

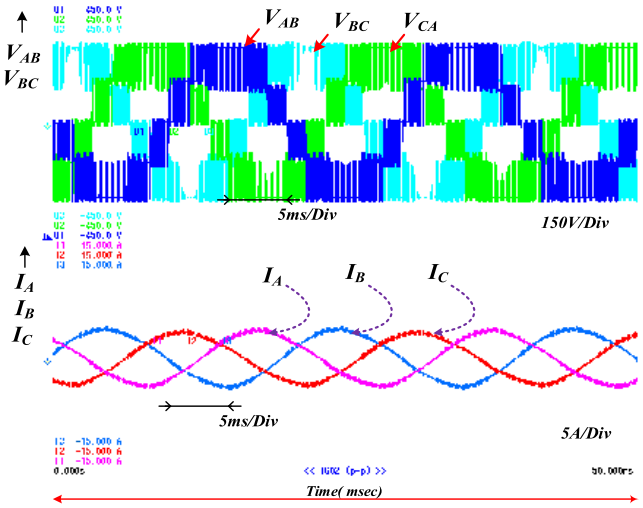

FIGURE 21. Experimental results for three phase inverter voltage and inverter current with $m_a = 0.9$ at $f_o = 50$Hz, $I_{load} = 3$A and $V_{dc} = 200$V.

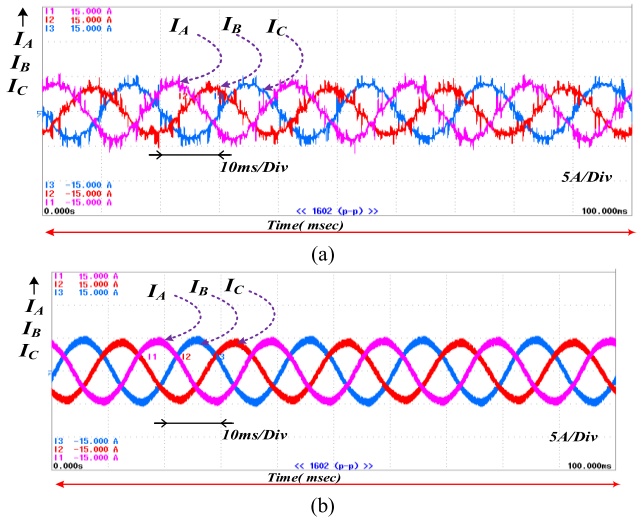

FIGURE 22. Experimental results for actual inverter current and reference current at $f_o = 50$Hz and $V_{dc} = 200$V; (a) Conventional SVM method (b) Proposed HSVM.

the inverter is operated under normal PV panel conditions (temperature: 27 °C and Irradiance: 1000 W/m2), the system deliver output of 300V, 50Hz. The MPPT controller maintains a DC-link voltage as 200V. The spectrum analyzer (YOKOGAWA) is used for capturing the waveforms and harmonics. The performance of proposed HSVM control method such as voltage, current magnitude harmonics and DC link capacitor Neutral point balancing carried out via simulation; at same conditions the experimentation has been carried out and they are validated. When modulation index (m_a) and boosting factor were set as 0.9 and 1.6(as similar specifications are taken in simulation), the inverter delivers output of ≈300V. At aforementioned operating specifications, the inverter is connected to grid and results are verified. The Fig.19 shows inverter current and reference load current waveform along with inverter output voltage. During this operating condition, the HSVM tracks grid reference and controlling the current with better NP balancing with 1.2%. The Fig.20 shows the three-phase output line voltage and phase current waveforms of the inverter for $m_a = 0.9$ at 5Amps Load. Similarly, Fig.20 and Fig.21 shows the inverter output voltage and current for $m_a = 0.8$ and $m_a = 0.9$. From the results, it is observed that the output current waveform of the inverter is maintained with boosting the voltage. With the current control method, the DC-link capacitor balancing is maintained, which helps to utilize the maximum inverter DC-link voltage with better harmonics profile on inverter voltage and current waveforms.

In order to validate the features such as low current THD and low NPF, the experimentation is carried out for conventional and proposed HCC based SVM. Fig. 22(a) and Fig.22 (b) shows the experimental results of inverter current for conventional and proposed HSVM respectively. Here,

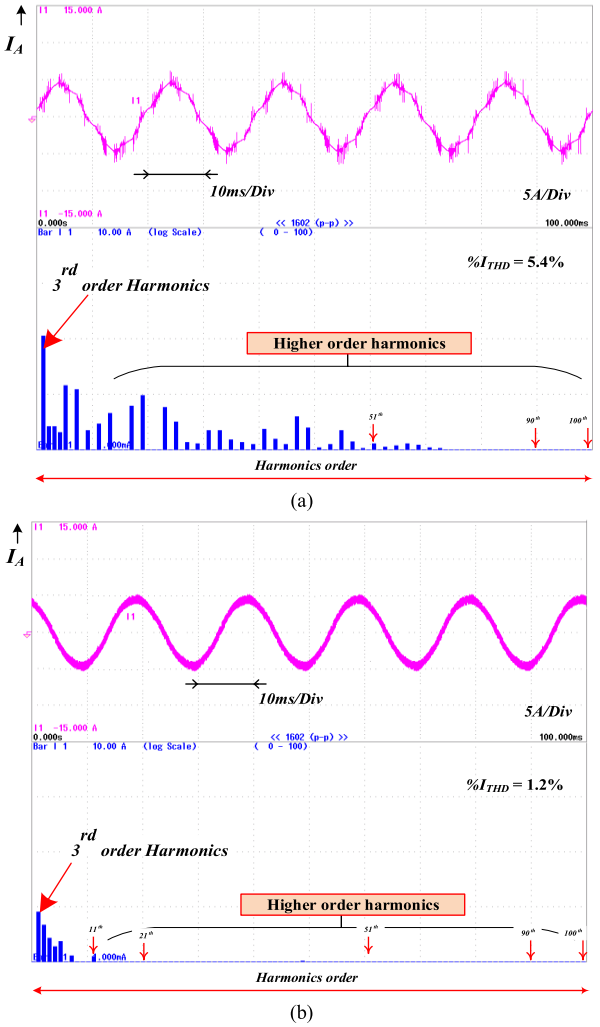

FIGURE 23. Experimental results for actual inverter current, reference current and THD spectra at $f_o = 50Hz$ and $V_{dc} = 200V$; (a) Conventional Z source SVPWM method, (b) HSVM.

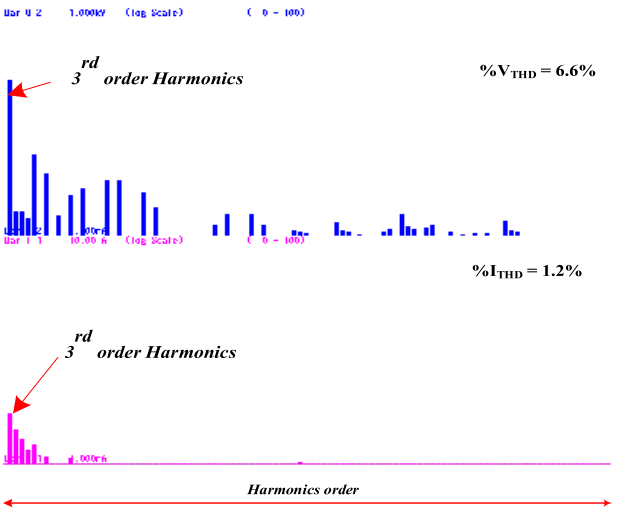

FIGURE 24. Experimental results; $V_{line}(V_{AB})$ THD spectra and I_{Aphase} THD spectra of HSVM method.

the HSVM maintains improved the current waveform in all the three-phases compared with the conventional SVPWM

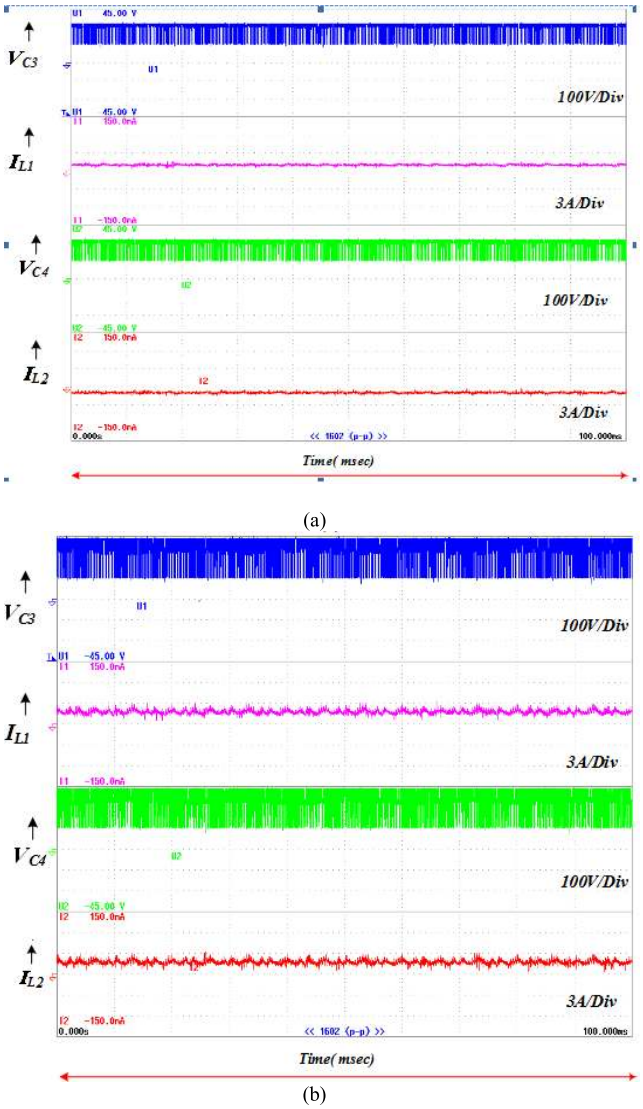

FIGURE 25. Experimental results; (a). $V_{C3}, V_{C4}, I_{L1}, I_{L2}$ during the lower STinterval and (b). $V_{C3}, V_{C4}, I_{L1}, I_{L2}$ during the higher ST interval.

topology. The Fig.23 (a) and Fig.23 (b) shows the experimental results of inverter current harmonics spectra for conventional and proposed HSVM. From the results, the proposed HSVM is having a minimal current THD spectrum as 1.2%, whereas a conventional method current THD spectrum is considerably high (5.4%) compare to HSVM. The Fig. 24 shows the experimental Voltage THD spectra and current THD spectra. By comparing the simulation results of current THD(1.16%), the experimental result of current THD(1.2%) is high due to the non- linear elements selection for Z network (L and C values) in real time.

The Fig. 25 (a) and (b) shows the impedance network capacitor voltages (C_3 and C_4) and inductor currents (L_1 and L_2) during lower and higher ST duty respectively. In the same operating condition, when $m_a = 0.9$, the inverter DC-link capacitor (C_1 and C_2) voltages, V_{C1} and V_{C2} are measured and compared for conventional and

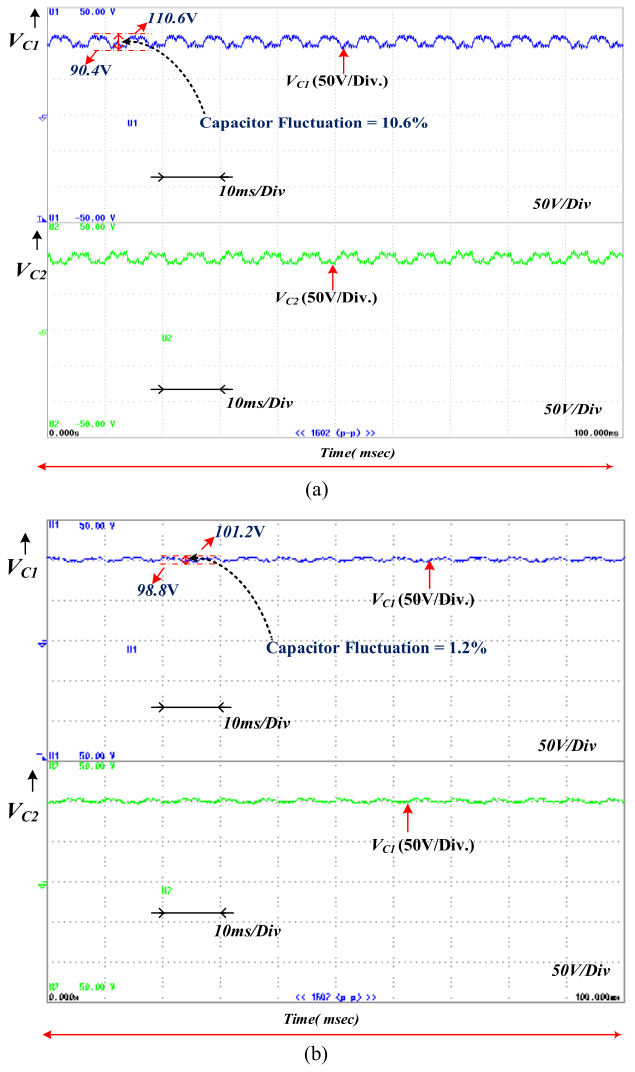

FIGURE 26. Experimental results of Z-NPC-MLI voltage across DC-link capacitors; (a) conventional Z source SVPWM method, (b) HSVM.

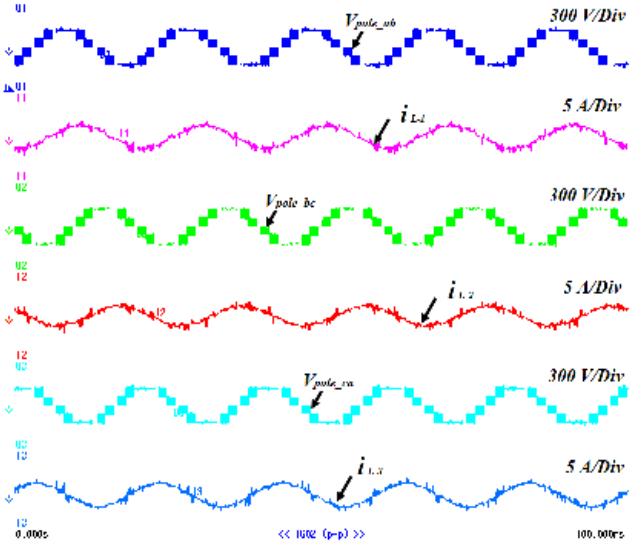

FIGURE 27. Experimental results for inverter voltage and current with 0.9 m_a at f_o = 50Hz.

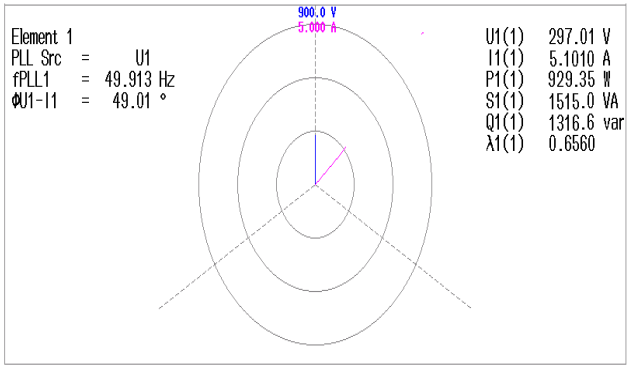

FIGURE 28. Experimental results; Phasor diagram of inverter.

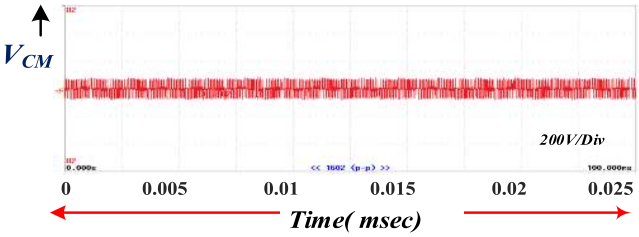

FIGURE 29. Experimental results - Common-mode voltage for m_a = 0.85.

proposed HSVM and, they are shown in Fig. 26 (a) and Fig.26 (b) respectively. In conventional method, the capacitors voltages (V_{C1} = 110.6V and V_{C2} = 90.4V) are fluctuating largely which causes the DC-link (neutral point) unbalancing (the NPF is calculated as 10.6%). This fluctuation causes the higher current THD. However, the proposed HSVM perform with capacitor balancing (V_{C1} = 101.2V and V_{C2} = 98.8V) with the NP fluctuation is 1.2%, which helps to utilize the maximum inverter DC-link voltage with better harmonics profile on inverter voltage and current waveforms. Fig. 27 shows the inverter voltage and current with $m_a = 0.9$ at f_o = 50Hz.

Based on the experimental results, during the steady state and transient conditions, the proposed HSVM control for Z-NPC MLI has a low value of NPF, and hence, the NP balancing is satisfied. The proposed HSVM can be used for other type of Z-source MLI. The proposed current controller and PWM functioned healthy with inverter and grid different operating condition. The observed inverter voltage and current to synchronize with grid is shown in Fig. 28. Here, the current and voltage is maintaining the grid frequency.

The Fig.29 common-mode voltage presented for $m_a = 0.85$. From that results it is understood the common-mode voltage is maintaining as $V_{dc}/2$. The CVM is maintained for all modulation indices as $V_{dc}/2$. The European efficiency of the inverter is calculated as 94.6%.

TABLE 3. Performance comparisons of conventional SVM and HSVM methods.

Method	Inverter Current THD	Neutral point Fluctuation
Conventional SVPWM	5.4%	10.6%
Proposed HSVM	1.2%	1.2%

C. COMPARISON OF CONVENTIONAL Z SOURCE SVPWM AND PROPOSED HSVM

The proposed HSVM uses minimal ST compare to conventional Z source SVPWM [8], [11], [13], [14]. In view of the inverter performance, the proposed HSVM is maintaining the I_{THD}(1.2%), and NPF (1.2%) which is very minimal. Comparison of conventional SVPWM and proposed HSVM is presented in Table 3.

V. CONCLUSION

In this paper the three-level Z source NPC-MLI has investigated for PV tied grid connected system. Further also developed the PV tied grid connected system with hysteresis current control combined Z source SVPWM is known as HSVM is developed. The proposed HSVM uses minimal ST compares to conventional Z source SVPWM. In addition the proposed HSVM eliminates the low frequency oscillations using suitable ST (Upper and Lower ST), with regular switching events, which ensures the neutral point DC-link capacitors balancing along with current control. The HSVM maintains the volt-second and inverter voltage boosting competence irrespective of the angular location of the reference vector throughout the inverter operation. A 2 kWp solar panels attached three-phase three-level IGBT based Z-NPC-MLI grid connected system is established with Xilinx family FPGA SPARTAN-6 controller. From the results, it shows that the performance of proposed method is superior than compare to conventional Z source SVPWM in terms of Neutral point fluctuation, current control capability and better harmonic performance. This proposed HSVM method well suited for wind tied inverters, industrial and Electrical vehicles motor applications.

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