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A Kind of Optoelectronic Memristor Model and Its Applications in Multi-Valued Logic

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Abstract: Memristors have been proved effective in intelligent computing systems owing to the advantages of non-volatility, nanometer size, low power consumption, compatibility with traditional CMOS technology, and rapid resistance transformation. In recent years, considerable work has been devoted to the question of how to design and optimize memristor models with different structures and physical mechanisms. Despite the fact that the optoelectronic effect inevitably makes the modelling process more complex and challenging, relatively few research works are dedicated to optoelectronic memristor modelling. Based on this, this paper develops an optoelectronic memristor model (containing mathematical model and circuit model). Moreover, the composite memristor circuit (series- and parallel-connected configuration) with a rotation mechanism is discussed. Further, a multi-valued logic circuit is designed, which is capable of performing multiple logic functions from 0–1, verifying the validity and effectiveness of the established memristor model, as well as opening up a new path for the circuit implementation of fuzzy logic.

Keywords: optoelectronic memristor; composite circuit; multi-valued logic; rotation mechanism

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1. Introduction

Memristors that are non-volatile and nano-sized, and that have low power consumption, compatibility with conventional CMOS technology, and variable resistance have been widely used in intelligent computing systems [1–5]. This novel circuit component, was first proposed by Chua L in 1971, represents the relationship between charge and flux [6]. The existence of a physical memristor was first verified by Hewlett-Packard Lab in 2008, and it was confirmed to be a nanoscale passive two-terminal circuit component [7]. The successful preparation of memristors has attracted a lot of attention among research scholars around the world, and numerous memristor devices with different structures and physical mechanisms have been prepared [8–10].

Owing to stringent manufacturing processes and high costs, actual memristors are difficult to prepare outside the laboratory [11–13]. Considerable work has been devoted to the study of mathematical and circuit models that can reproduce the complex dynamics of memristors, such as the HP model [14], the spintronic model [15], the threshold adaptive model (TEAM) [16], the voltage threshold adaptive model (VTEAM) [17], etc. However, the present modelling is mostly based on two factors: the voltage applied to the memristor and the current flowing through it, which cannot accommodate the physical memristor properties prepared with evolving materials [18–20]. Indeed, physical memristors are affected by multiple factors such as light, temperature, humidity, and magnetic field, increasing the complexity and difficulty of modelling [21–24], and relatively little and incomplete work has been done in this area. In order to approximate the electrical characteristics possessed

by physical amnesic resistors, this paper develops a model for optoelectronic memristors affected by both optical and electrical signals.

With the exploration of the binary characteristics of memristors, the application of memristors in logic circuits has received a lot of attention [25–28]. Existing research in the field of memristor-based logic implementation is mainly aimed at binary logic (e.g., material implication, memristor-aided logic, and memristor-ratioed logic), and ternary logic (e.g., balanced ternary logic and unbalanced ternary logic) [29–33]. However, relatively little research has been conducted on the implementation of multi-valued logic circuits based on memristors. Multi-valued logic with more logic states is an extension of traditional binary (or ternary) logic, which has only two (or three) logical states. Compared with binary (or ternary) logic, multi-valued logic carries more information in the process of processing a large amount of data, and has a faster operational speed, smaller area and size, and lower power consumption [34–36]. This paper presents the design of a multivalued logic circuit based on the established optoelectronic model. The research gaps and the main contributions of this paper are summarized in Table 1.

Table 1. The research gaps and the main contributions.

Research Gaps	Contributions
• Most of the existing memristor models are based on voltage and current factors, which fail to closely approximate the physical memristors that are affected by multiple factors.	• The illumination factor is introduced as a variable for modelling optoelectronic memristor, which provides a new idea for modelling memristors affected by multiple factors such as temperature, humidity, and magnetic field.
• The electrical characteristics of physical memristors are less unstable owing to vulnerability to the external environment.	• The electrical characteristics of the optoelectronic memristor and its composite circuit are analyzed from the perspective of the model.
• Existing research on memristor-based logic implementation mainly focuses on binary logic and ternary logic.	• A multi-valued logic circuit with 10 logic functions from 0–1 is proposed, which demonstrates the validity of the model and offers the possibility to explore fuzzy logic in the future.

The rest of the paper is organized as follows. Section 2 details the mathematical and PSIPCE models of a kind of optoelectronic memristor. Moreover, a series of tests and analysis on the electrical characteristics of the model is carried out in the same section. Section 3 discusses a composite circuit incorporating a rotation mechanism and proposes a multivalued logic circuit based on this circuit. The section concludes with a series of simulation experiments and analysis to verify the correctness of the proposed multi-valued logic and the validity of the model. Section 4 discusses the limitations of the designed multi-valued logic circuit and provides future research directions. Finally, Section 5 summarizes the whole work.

2. Optoelectronic Memristor Model and Electrical Characteristics Analysis

2.1. Background of Opoelectronic Memristor

Before modeling the optoelectronic memristor, the background of the optoelectronic memristor is studied in terms of both device structure and operating principles, which leads to a better understanding of the optoelectronic effects that affect the electrical characteristics of the memristor.

The modeled optoelectronic memristor device is prepared from ITO/MgO/HfO_2/ITO material, where two layers of transparent conductive oxide ITO are used as the top electrode (TE) and bottom electrode (BE) of the device [21]. The wide bandwidth oxide (MgO/HfO_2) introduces the optical functionality in the resistive switching device while maintaining the

optical transparency, and the MgO layer increases the durability, retention performance, and resistive ON/OFF ratio of the device. The specific device structure is shown in Figure 1a.

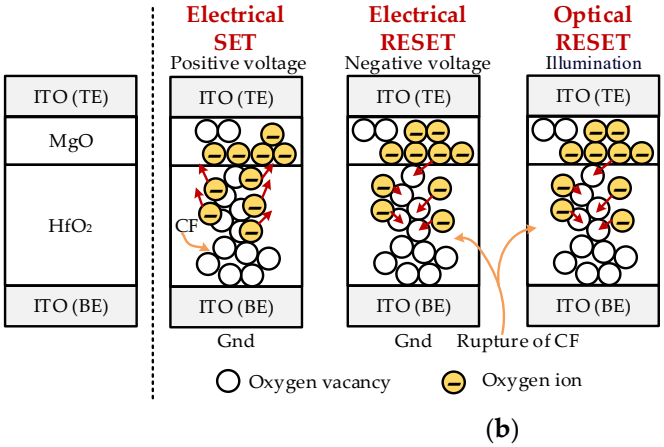

Figure 1. The schematic diagram of the optoelectronic memristor showing (**a**) device structure; and (**b**) working principle.

The working principle of the device is illustrated in Figure 1b, and it can be discussed in three cases depending on the voltage and light illumination. When a positive voltage is applied at the TE terminal and the BE terminal is grounded, the positive voltage induces the breakage of the Hf-O and Mg-O bonds, and a large number of oxygen vacancies (V_O) and oxygen ions (O^{2-}) are formed. Conductive filaments (CF) are formed inside the device, which causes the device to switch from a high resistance state (HRS) to a low resistance state (LRS). Owing to the larger amount of energy required to form V_O from MgO, most of the V_O during the setting process is produced by HfO_2. Notably, O^{2-} is not stacked near the TE interface, but at the intersection of MgO and HfO_2.

In the case that a negative voltage is applied at the TE terminal and the BE terminal is kept grounded, O^{2-} will recombine with V_O to form oxygen atoms under the negative voltage, leading to the rupture of CF. Further, the current is reset and the resistance state of the device is transformed to HRS.

In addition, the device is influenced by optical factors as well as electrical stimulation. The illumination is able to provide energy to O^{2-}, which in turn promotes O^{2-} and V_O to achieve recombination. The effects of illumination and negative voltage on the electrical characteristics of the device are similar, and both achieve the reset function.

2.2. Modelling of Opoelectronic Memristor

In order to facilitate subsequent studies on the application of the optoelectronic memristor, the device is modeled by improving the VTEAM modelling method and employing the optoelectronic effect. Its resistance can be represented by the following mathematical equation.

$$M(x) = R_{on} + \frac{R_{off} - R_{on}}{x_{off} - x_{on}}(x - x_{on}) \tag{1}$$

where M denotes the resistance of the optoelectronic memristor, which is limited to $[R_{on}, R_{off}]$. x is the state variable, with maximum and minimum values of x_{on} and x_{off}, and the dynamic function of x can be described by the following equation.

$$\frac{dx}{dt} = \begin{cases} \left[k_{on}\left(\frac{V(t)}{V_{th1}} - 1\right)^{\alpha_{on}} + \frac{I_p}{\varepsilon \cdot I_{pmax}}\right] \cdot f(x), & 0 < V_{th1} \le V(t) \\ \frac{I_p}{\varepsilon \cdot I_{pmax}} \cdot f(x), & V_{th2} < V(t) \le V_{th1} \\ \left[k_{off}\left(\frac{V(t)}{V_{th2}} - 1\right)^{\alpha_{off}} + \frac{I_p}{\varepsilon \cdot I_{pmax}}\right] \cdot f(x), & V(t) \le V_{th2} < 0 \end{cases} \tag{2}$$

$$f(x) = 1 - (\beta x - 1)^{2p} \tag{3}$$

where $k_{on}(V(t)/V_{th1} - 1)^{\alpha on}$ and $k_{off}(V(t)/V_{th2} - 1)^{\alpha off}$ are electrical effect simulation terms that achieve not only a decrease in resistance when a positive voltage is applied, but also an increase in resistance for negative voltages. k_{on}, k_{off}, α_{on}, and α_{off} are all fitting parameters of the model, V_{th1} and V_{th2} denote the positive and negative threshold voltage, respectively. $V(t)$ represents the voltage loaded onto the memristor. $I_p/(\varepsilon * I_{pmax})$ is the light effect simulation term to realize the function of increasing the memristance upon illumination. ε denotes the parameter capable of regulating the effect of light and I_{pmax} is the maximum illumination power intensity. I_p indicates the optical power intensity applied to the memristor. $f(x)$ acts as a window function for binding x to $[x_{on}, x_{off}]$. β and p are fitting parameters of the model.

Accordingly, a SPICE model of optoelectronic memristor is proposed to perform the subsequent circuit simulation. The specific sub-circuit description is shown in Table 2.

Table 2. PSPICE sub-circuit of optoelectronic memristor model.

* **Optoelectronic Memristor Model**
.SUBCKT optoelectronic memristor model Plus Minus PARAMS:
+ xon=0 xoff=3E−9 Alphaon=0.1 Alphaoff=0.1 Ron=100 Roff=3E3 kon=−1 koff=1 Ip=100
+ Epsilon=0.6 Ipmax=500 p=1 Beta=6.6666E8 Vth1=2 Vth2=−2 xinit=3E−9
******* Differential equation modelling*******
Gx 0 x value={f(V(x), V(Plus, Minus), kon, koff, Alphaon, Alphaoff, Vth1, Vth2, Epsilon,
+ Beta, p, Ip, Ipmax)}
Cx x 0 1 IC={xinit}
R x 0 1 T
**********Ohm's Law**********
Emem Plus Aux value={I(Emem)*(Roff-Ron)*(V(x)-xon)/(xoff-xon)}
Rs aux Minus {Ron}
Emx Mx 0 value={(Roff-Ron)*(V(x)-xon)/(xoff-xon)+Ron}
**********Functions**********
.func f(x, v, kon, koff, Alphaon, Alphaoff, Epsilon, Ip, Ipmax, Beta, p)=
+ {If(v>Vth1, f1(x, v, kon, Vth1, Alphaon, Epsilon, Ip, Beta, Ipmax, p),
+ If(v<Vth2, f2(x, v, koff, Vth2, Alphaoff, Epsilon, Ip, Beta, Ipmax, p),
+ f3(x, Epsilon, Ip, Beta, Ipmax, p))}
.func f1(x, v, kon, Vth1, Alphaon, Epsilon, Ip, Beta, Ipmax, p)=
+ {(kon*(v/Vth1−1)ˆAlphaon+Ip/(Epsilon*Ipmax))*(1-(Beta*x−1)ˆ(2*p))}
.func f2(x, v, koff, Vth2, Alphaoff, Epsilon, Ip, Beta, Ipmax, p)=
+ {(koff*(v/Vth2−1)ˆAlphaoff+Ip/(Epsilon*Ipmax))*(1-(Beta*x−1)ˆ(2*p))}
.func f3(x, Epsilon, Ip, Beta, Ipmax, p)={Ip/(Epsilon*Ipmax)*(1-(Beta*x−1)ˆ(2*p))}
.ENDS optoelectronic memristor

To evaluate the accuracy of the proposed model, we fit the model based on real experimental data, as shown in Figure 2. Figure 2a shows the $I-V$ curve of the memristor in the dark environment, where the black ball indicates the real experimental data and the red solid line indicates the fitting result of the model. Notably, the memristor is initialized to a high resistance state before conducting this experiment. Figure 2b shows the $I-V$ curves of the memristor before and after applying illumination to it, where the blue and black lines with triangles indicate the real experimental data pre- and post-illumination, respectively, and the gray and red lines show the fitting results pre- and post-illumination, respectively. Notably, the resistance of the initialized memristor is a lower resistance before carrying out this experiment and the illumination is white light (390–780 nm) with an optical power intensity of 100 W/m^2.

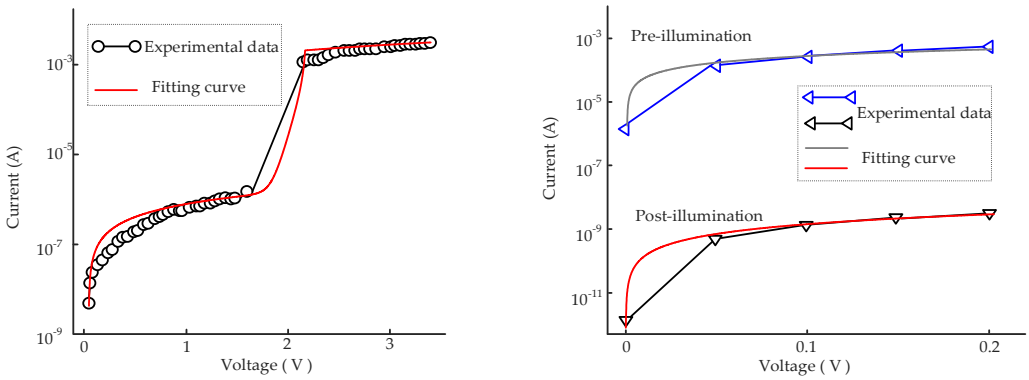

Figure 2. The fitting result of the model showing (**a**) $I-V$ curve of the memristor in the dark environment; and (**b**) $I-V$ curves of the memristor before and after applying illumination.

From Figure 2, the established memristor model has a good overlap with the actual memristor electrical characteristic curve. Root mean square error (RMSE) is introduced as an indicator for objective analysis, and its mathematical expression is shown below:

$$\mathrm{RMSE} = \sqrt{\frac{1}{n}\left(\frac{\sum_{i=1}^{n}\left(V_{\mathrm{real},i}-V_{\mathrm{fit},i}\right)^2}{V_{\mathrm{fit}}^2}+\frac{\sum_{i=1}^{n}\left(I_{\mathrm{real},i}-I_{\mathrm{fit},i}\right)^2}{I_{\mathrm{fit}}^2}\right)} \tag{4}$$

where n is the number of samples, $V_{\mathrm{real},i}$ and $I_{\mathrm{real},i}$ the voltage and current on the memristor during the testing process, and $V_{\mathrm{fit},i}$ and $I_{\mathrm{fit},i}$ represent the voltage and current on the model during the fitting process. V_{fit} and I_{fit} denote the Euclidean criterion for the voltage and current of the memristor model. Normally, a smaller RMSE represents a better fit.

From Figure 2a, the model can achieve the electrical setting function under positive voltage, where the model can be fitted to the measured data points with the RMSE value of 1.13%. As shown in Figure 2b, the simulated I-V curves are matched with the I-V curves in the pre- and post-illumination periods with RMSE values of 1.65% and 1.98%, respectively. When illumination is applied, the resistance of the memristor increases and the current flowing through the memristor decreases. In general, the fitting results show that the constructed optoelectronic memristor model is capable of characterizing the performance of the ITO/MgO/HfO_2/ITO memristor.

2.3. Electrical Characteristics Analysis

To demonstrate the electrical characteristics of the proposed optoelectronic memristor model, a series of tests and analysis circuit simulations are performed, and the experimental results are shown in Figures 3–5. The specific parameters of the memristor model are detailed in Tables 2 and 3. Notably, the experiments are conducted on a desktop workstation equipped with Core i7-10700 processor, 32 GB RAM and Windows 10 operating system using Matlab2018 and PSpice software.

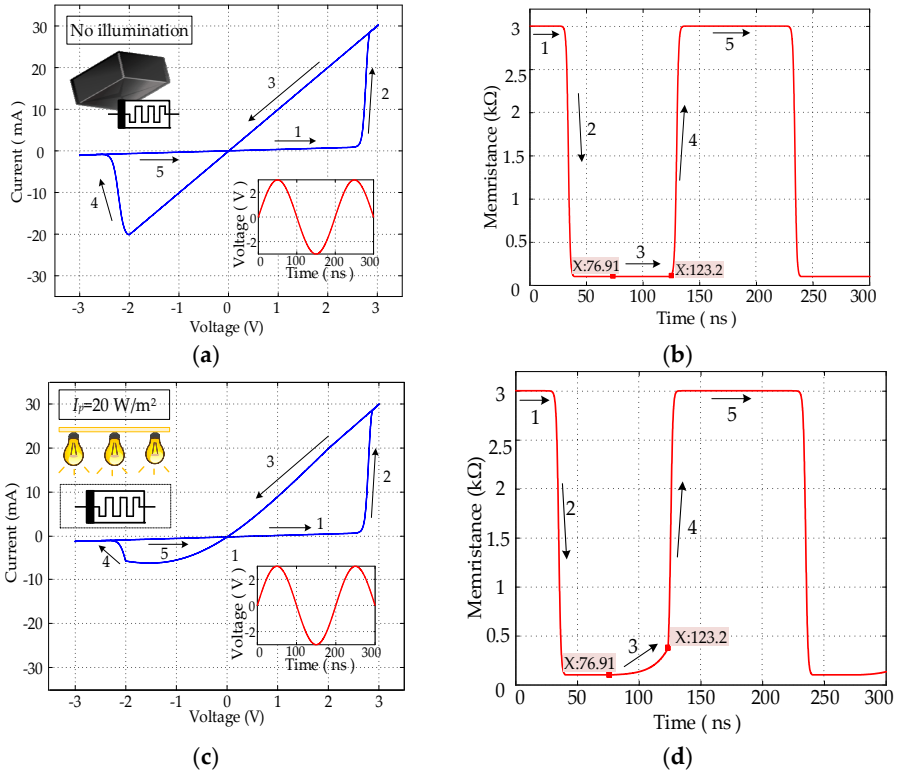

Figure 3. Simulation results under sine-wave voltage showing (**a**,**b**) $I-V$ and $M-t$ curves without illumination; and (**c**,**d**) $I-V$ and $M-t$ curves at optical radiation intensity of 20 W/m^2.

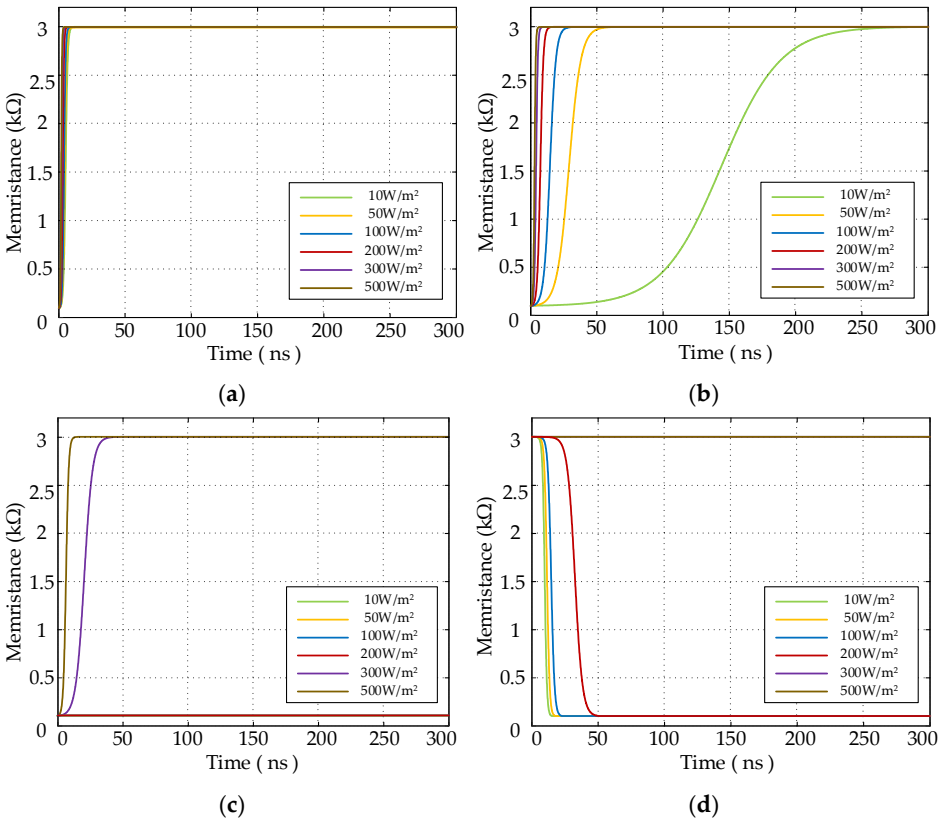

Figure 4. Simulation results at different optical power densities under constant voltages showing (**a**–**c**) $M-t$ curves of the memristor with initial resistance R_{on} at −3 V, 0 V, 3 V; and (**d**) $M-t$ curve of the memristor with initial resistance R_{off} at 3 V.

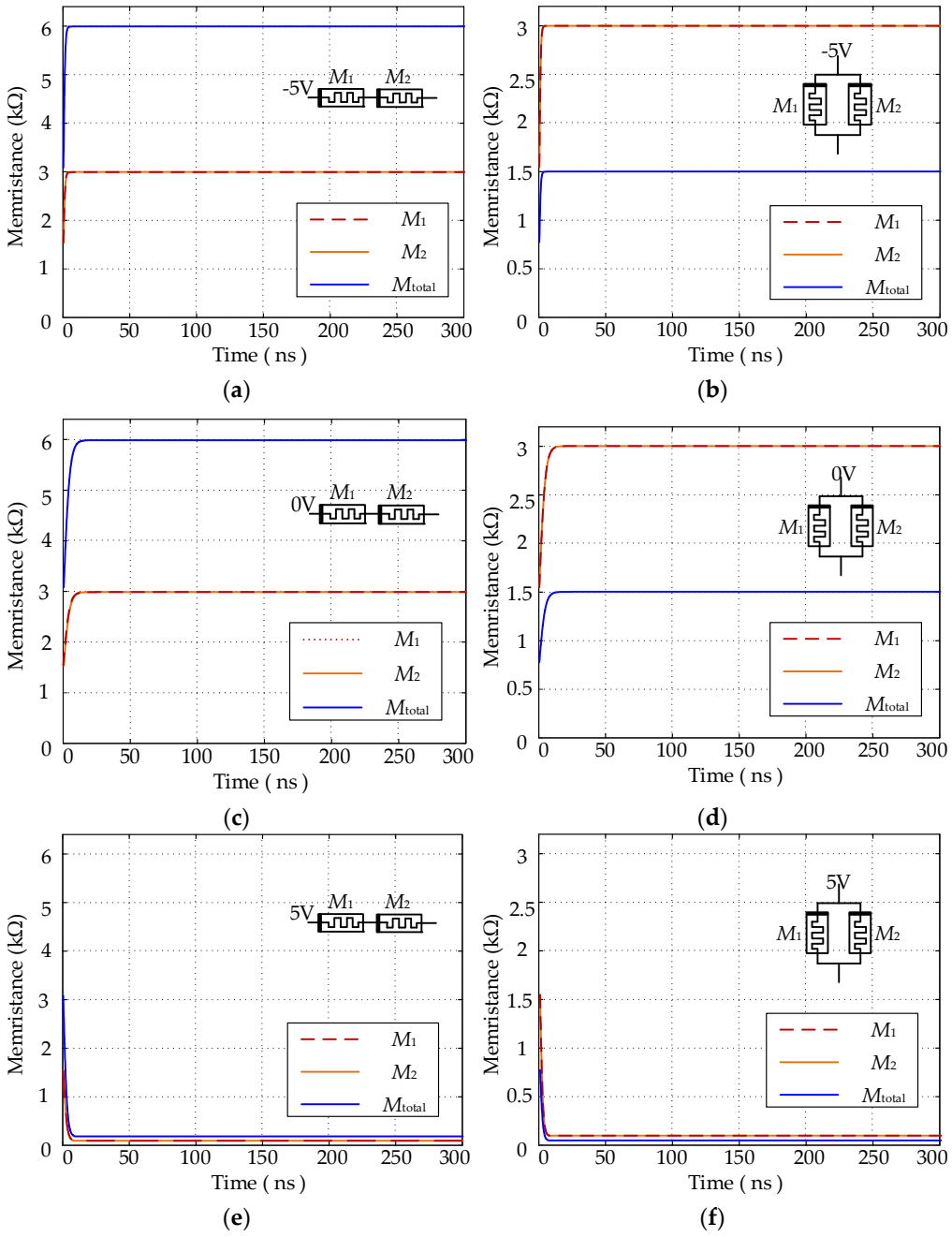

Figure 5. Electrical characteristic curves of the memristor composite circuit at the optical power density of 100 W/m^2 showing (**a**,**c**,**e**) $M-t$ curves of the series circuit at −5 V, 0 V, 5 V; and (**b**,**d**,**f**) $M-t$ curves of the parallel circuit at −5 V, 0 V, 5 V.

Figure 3 illustrates the electrical characteristics (volt-ampere characteristics and memristance variation rule) of the memristor under different illumination conditions. The relationship between the current flowing through the memristor model and the applied voltage is shown in Figure 3a,c, and the variation of memristance with time is shown in Figure 3b,d.

The $I-V$ characteristic curves in Figure 3a,c both show squeezed hysteresis curves at the origin, which demonstrates that the proposed memristor model conforms to the definition of a generalized memristor [37]. Notably, the model is relatively symmetrical in the positive and negative voltage regions under the condition of no illumination, whereas the area of the pinched hysteresis loop in the negative voltage region is greatly reduced upon optical stimulation, and the positive and negative regions are asymmetric. This

occurs because the light stimulus increases the memristance as well as the negative voltage, weakening the effect of the negative voltage on the electrical properties of the model.

Table 3. Parameters for the electrical characteristics analysis.

	Optical Power Density (W/m^2)	Electrical Stimulation (V)	Initial Value of Memristor (kΩ)
Figure 3a,b	$I_p = 0$	V = 3 sin($10^7 \pi t$)	3
Figure 3c,d	$I_p = 20$	V = 3 sin(t)	3
Figure 4a	I_p = 10, 50, 100, 200, 300, 500	V = −3	0.01
Figure 4b		V = 0	0.01
Figure 4c		V = 3	0.01
Figure 4d		V = 3	3
Figure 5a	$I_p = 100$	$V = -5$	1.5, 1.5
Figure 5b		V = −5	1.5, 1.5
Figure 5c		V = 0	1.5, 1.5
Figure 5d		V = 0	1.5, 1.5
Figure 5e		V = 5	1.5, 1.5
Figure 5f		V = 5	1.5, 1.5

From Figure 3b, it can be observed that the electrical characteristics of this memristor model are similar to those of the VTEAM model under conditions without illumination, and the variation of its resistance with time can be described in five stages. In stage 1, the resistance keeps R_{off} constant when the scanning voltage increases from 0 V to V_{th1}; in stage 2, the resistance decreases from R_{off} to R_{on} when applying the voltage to the memristor over V_{th1}; in stage 3, the resistance remains unchanged as the scanning voltage decreases from V_{th1} to V_{th2}; in stage 4, when the voltage is less than V_{th2}, the memristor transforms from the LRS to the HRS; and in stage 5, by the time the voltage increases from V_{th2} to 0 V, the resistance characteristics are the same as in stages 1 and 3, and the HRS is maintained. Comparing Figure 3b,d, it can be found that the optical stimulation causes an alteration of the resistance variation rule in stage 3, which is the time interval from 76.91 ns to 123.2 ns. The inclusion of the optical stimulus leads to the reversal of the soft breakdown, causing an increase in the resistance of the memristor. Notably, with the low power density of the applied optical signal here, the optical stimulus has less effect on the electrical characteristics of the memristor in comparison with the electrical stimulus and does not lead to a shift in the resistance variation pattern in the remaining phases.

Figure 4 shows the results of the effect of optical stimulation with different irradiation power densities and constant voltage of different amplitudes on the variation pattern of the memristance. Figure 4a–c shows the memristor response curves upon the application of electrical stimuli of 3 V, 0 V and −3 V to the memristor model with the initial resistance R_{on} within the time interval [0, 300]ns at different optical power densities (i.e., 10, 50, 100, 200, 300, and 500 W/m^2), respectively. Considering that the resistance state of the memristor with initial resistance R_{off} will not change with external electrical stimuli of −3 V and 0 V, thus only the effect of different optical power densities on the memristance under 3 V positive voltage is simulated. From Figure 4a,b, it is obvious that the higher the optical power density, the faster the rate of resistance enhancement. A summary analysis of Figure 4c,d shows that a sufficiently large optical stimulus can surpass the effect of positive voltage on the electrical characteristics of the memristor. Notably, the green, yellow, blue and red lines in Figure 4c are overlapped, and the purple and brown lines in Figure 4d are overlapped.

Figure 5 depicts the electrical characteristic curves of the memristor composite circuit (series- and parallel-connected configuration) at an optical power density of 100 W/m^2. Figure 5a,c,e illustrates the resistance variation curves of two optoelectronic memristors with the same initial resistance connected in series at −5 V, 0 V and 5 V electrical stimuli, respectively, while Figure 5b,d,f represents the resistance variation curves connected in parallel.

From Figure 5, since the model parameters (including the initial memristances) of the two memristors are the same, the corresponding resistance variation pattern (which can be referred to the resistance variation pattern in Figure 3d) is also the same, as shown in the overlapping of the red dashed line and the orange solid line. When two memristors are connected in series in the same direction, the resistance state of both memristors changes to the HRS under the combined effect of negative voltage and illumination, as shown in Figure 5a. In the case of illumination separately, as shown in Figure 5c, the resistances of both memristors also increase to R_{off}. Notably, compared to Figure 5a, the change (growth) curve of the resistance is relatively smooth owing to the lack of the effect of the negative voltage. Under the effect of positive voltage, as shown in Figure 5e, the resistance of both memristors decreases owing to the lower power density of illumination radiation, whose effect on the optoelectronic memristors is smaller than that of positive voltage. In addition, when two memristors are connected in parallel in the same direction, as shown in Figure 5b,d,f, the resistance variation trend of the two memristors is the same as that in series in the same direction. However, when the same voltage is applied to the input, the voltage divided by the parallel memristors is larger, so the rate of resistance variation is relatively faster. Moreover, the equivalent resistance M_{total} of the series circuit is calculated as the sum of the resistance M_1 and M_2, i.e., $M_{total} = M_1 + M_2$, and the equivalent resistance of the parallel circuit satisfies: $M_{total} = M_1 * M_2/(M_1 + M_2)$.

3. Rotation Mechanism Based Multi-Valued Logic

In this section, a composite memristor circuit (series- and parallel-connected configuration) incorporating a rotation mechanism is discussed. According to the composite circuit, a circuit capable of implementing 0–1 multiple logic functions is subsequently proposed. The specific operation procedure and simulation results are described as follows.

3.1. Rotation Mechanism Based Composite Circuit

The schematic diagram of the composite memristor circuit based on the rotation mechanism is depicted in Figure 6, where A, B, C are the ports of the connection line, and port B is the center of rotation. The rotation mechanism enables the conversion of series and parallel configuration circuits, and the circuit during the conversion contains an intermediate state in addition to the series and parallel states.

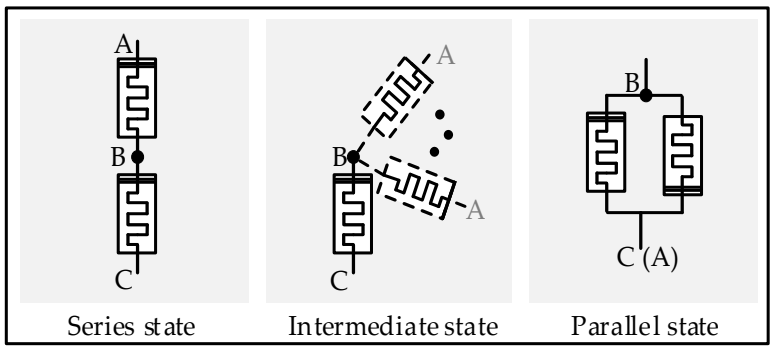

Figure 6. The circuit diagram of rotation mechanism.

3.2. Implementation of Multi-Valued Logic

Incorporating the composite circuit based on the rotation mechanism, a circuit for implementing multi-valued logic is designed (as illustrated in Figure 7). Note that the proposed circuit contains two valid states during rotation, i.e., state *I* and state *II*.

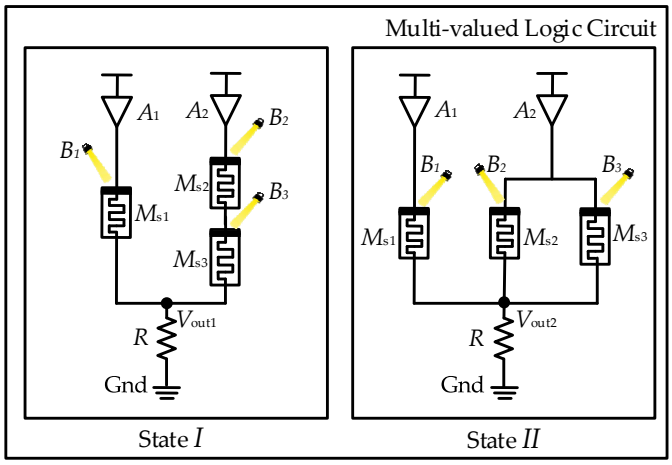

Figure 7. The diagram of multi-valued logic circuit based on rotation mechanism.

The memristors (M_{s1}, M_{s2}, and M_{s3}) employed in the circuit are the proposed optoelectronic memristors, whose resistances (R_{s1}, R_{s2}, and R_{s3}) are varied in [R_{on}, R_{off}] by the joint effect of electrical and optical stimulation. The input voltages (A_1 and A_2) and the optical power densities (B_1, B_2, and B_3) are the input state variables of the circuit. R is the regular resistor, and the voltage (V_{out1} and V_{out2}) across it indicates the output state variable of the logic circuit.

Before executing the multi-valued logic operation, the memristor M_{s1}, M_{s2}, and M_{s3} are required to be initialized to their lowest value R_{on}. The specific process of implementing multiple logic functions from 0 to 1 for the two states is described as follows.

3.2.1. State I for Multi-Valued Logic

For multi-valued logic operation, the electrical inputs (A_1 and A_2) always have two states V_{on} and V_{off}, representing the logic "1" and logic "0", respectively. Notably, the value of voltage V_{off} used in this section is 0 V. According to the principle of series voltage division and parallel current division, the node voltage V_{out1} can be calculated with the following equation.

$$V_{out1} = \begin{cases} 0 & A_1 = V_{off}, A_2 = V_{off} \\ \frac{R}{R+R_{s1}//(R_{s2}+R_{s3})} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{s1}}{R//R_{s1}+(R_{s2}+R_{s3})} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//(R_{s2}+R_{s3})}{R//(R_{s2}+R_{s3})+R_{s1}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (5)$$

When $A_1 = A_2 = V_{off}$, the node voltage V_{out1} is always 0 V, independent of whether the state of the memristor is changed or not, thus the case is not described when the optical stimulus is applied to the memristor. The optical inputs (B_1, B_2, and B_3), which always have two states I_{ph} and I_{pl}, representing the logic "1" and logic "0", respectively, can be discussed in the following six cases.

- Case A: When $B_1 = B_2 = B_3 = I_{pl}$, the node voltage V_{out1} can be computed as:

$$V_{out1} = \begin{cases} \frac{R}{R+R_{on}//2R_{on}} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{on}}{R//R_{on}+2R_{on}} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//2R_{on}}{R//2R_{on}+R_{on}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (6)$$

According to the resistance variation pattern of optoelectrical memristor, the low optical power density is not sufficient to trigger a change in the resistance of the optoelectrical memristor, thus the resistance of memristors (R_{s1}, R_{s2}, and R_{s3}) remains in the initial R_{on}.

- Case B: When $B_1 = I_{pl}$, $B_2 = I_{pl}$ and $B_3 = I_{ph}$ (or $B_1 = I_{pl}$, $B_2 = I_{ph}$ and $B_3 = I_{pl}$), the node voltage V_{out1} can be computed as:

$$V_{out1} = \begin{cases} \frac{R}{R+R_{on}//(R_{on}+R_{off})} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{on}}{R//R_{on}+R_{on}+R_{off}} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//(R_{on}+R_{off})}{R//(R_{on}+R_{off})+R_{on}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (7)$$

Here, the high optical power density has a greater effect on the resistance variation of the memristor than the positive voltage, with the memristance of R_{s3} or R_{s2} increasing from R_{on} to R_{off}. The memristors M_{s1} and M_{s2} (or M_{s1} and M_{s3}) remain in the low resistance state.

- Case C: When $B_1 = I_{pl}$ and $B_2 = B_3 = I_{ph}$, the node voltage V_{out1} can be computed as:

$$V_{out1} = \begin{cases} \frac{R}{R+R_{on}//2R_{off}} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{on}}{R//R_{on}+2R_{off}} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//2R_{off}}{R//2R_{off}+R_{on}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (8)$$

Here, the memristor M_{s1} remains in the initial low resistance state, and the resistances of M_{s2} and M_{s3} increase to the highest value R_{off}.

- Case D: When $B_1 = I_{ph}$ and $B_2 = B_3 = I_{pl}$, the node voltage V_{out1} can be computed as:

$$V_{out1} = \begin{cases} \frac{R}{R+R_{off}//2R_{on}} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{off}}{R//R_{off}+2R_{on}} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//2R_{on}}{R//2R_{on}+R_{off}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (9)$$

Here, the memristors M_{s2} and M_{s3} remain in the initial low resistance state, and the resistance of M_{s1} increases to the highest value R_{off}.

- Case E: When $B_1 = I_{ph}$, $B_2 = I_{pl}$ and $B_3 = I_{ph}$ (or $B_1 = I_{ph}$, $B_2 = I_{ph}$ and $B_3 = I_{pl}$), the node voltage V_{out1} can be computed as:

$$V_{out1} = \begin{cases} \frac{R}{R+R_{off}//(R_{on}+R_{off})} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{off}}{R//R_{off}+R_{on}+R_{off}} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//(R_{on}+R_{off})}{R//(R_{on}+R_{off})+R_{off}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (10)$$

Here, the memristors M_{s2} (or M_{s3}) remain in the initial low resistance state, and the resistance of M_{s1} and M_{s3} (or M_{s2}) increase to the highest value R_{off}.

- Case F: When $B_1 = B_2 = B_3 = I_{ph}$, the node voltage V_{out1} can be computed as:

$$V_{out1} = \begin{cases} \frac{R}{R+R_{off}//2R_{off}} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{off}}{R//R_{off}+2R_{off}} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//2R_{off}}{R//2R_{off}+R_{off}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (11)$$

Here, the memristors M_{s1}, M_{s2} and M_{s3} shift to the high resistance state, and correspondingly all the memrsistances (R_{s1}, R_{s2}, and R_{s3}) increase to the highest value R_{off}.

The node voltage V_{out1} in Case A is defined as logic "1" when the electrical inputs $A_1 = A_2 = V_{on}$, and the output logic value for the rest of the cases is the ratio between the output V_{out1} and the voltage corresponding to logic "1". Assuming $R_{off} \geq 10\,R$, $R \cong 3\,R_{on}$, the truth table of state I for multi-valued logic is shown in Table 4.

Table 4. Truth table of multi-valued logic circuit.

Electronical Inputs		**Optical Inputs**				**Output of state *I***	**Output of state *II***
A_1	A_2	Cases	B_1	B_2	B_3	V_{out1}	V_{out2}
0	0	-	×	×	×	0	0
1	1	Case A	0	0	0	1	1
		Case B	0	0/1	1/0	0.9	1
		Case C	0	1	1	0.9	0.9
		Case D	1	0	0	0.8	1
		Case E	1	0/1	1/0	0.2	0.9
		Case F	1	1	1	0.2	0.3
0	1	Case A	0	0	0	0.7	0.7
		Case B	0	0/1	1/0	0.9	0.5
		Case C	0	1	1	0.9	0.1
		Case D	1	0	0	0	1
		Case E	1	0/1	1/0	0.1	0.9
		Case F	1	1	1	0.1	0.2
1	0	Case A	0	0	0	0.3	0.4
		Case B	0	0/1	1/0	0	0.5
		Case C	0	1	1	0	0.8
		Case D	1	0	0	0.7	0
		Case E	1	0/1	1/0	0.1	0
		Case F	1	1	1	0	0.1

3.2.2. State II for Multi-Valued Logic

The memristors M_{s1} and M_{s2} are rotated from series to parallel in state *I*, and the computational equation for the node voltage V_{out2} is replaced as follows:

$$V_{out1} = \begin{cases} 0 & A_1 = V_{off}, A_2 = V_{off} \\ \frac{R}{R+R_{s1}//(R_{s2}//R_{s3})} V_{on} & A_1 = V_{on}, A_2 = V_{on} \\ \frac{R//R_{s1}}{R//R_{s1}+(R_{s2}//R_{s3})} V_{on} & A_1 = V_{off}, A_2 = V_{on} \\ \frac{R//(R_{s2}//R_{s3})}{R//(R_{s2}//R_{s3})+R_{s1}} V_{on} & A_1 = V_{on}, A_2 = V_{off} \end{cases} \quad (12)$$

In the same way as state *I*, which implements multi-valued logic, the node voltage V_{out2} can be further specified into the following six cases according to the optical inputs.

- Case A: When $B_1 = B_2 = B_3 = I_{pl}$, the variation of resistance R_{s1}, R_{s2}, and R_{s3} is the same as that of Case A in state *I*, thus the node voltage V_{out2} can be computed as:

$$V_{out2} = \begin{cases} \frac{R}{R+R_{on}//(R_{on}//R_{on})} V_{on} & V_1 = V_{on}, V_2 = V_{on} \\ \frac{R//(R_{on}//R_{on})}{R//(R_{on}//R_{on})+R_{on}} V_{on} & V_1 = V_{off}, V_2 = V_{on} \\ \frac{R//R_{on}}{R//R_{on}+R_{on}//R_{on}} V_{on} & V_1 = V_{on}, V_2 = V_{off} \end{cases} \quad (13)$$

- Case B: When $B_1 = I_{pl}$, $B_2 = I_{pl}$ and $B_3 = I_{ph}$ (or $B_1 = I_{pl}$, $B_2 = I_{ph}$ and $B_3 = I_{pl}$), the variation of resistance R_{s1}, R_{s2}, and R_{s3} is the same as that of Case B in state *I*, thus the node voltage V_{out2} can be computed as:

$$V_{out2} = \begin{cases} \frac{R}{R+R_{on}//(R_{on}//R_{off})} V_{on} & V_1 = V_{on}, V_2 = V_{on} \\ \frac{R//(R_{on}//R_{off})}{R//(R_{on}//R_{off})+R_{on}} V_{on} & V_1 = V_{off}, V_2 = V_{on} \\ \frac{R//R_{on}}{R//R_{on}+R_{off}//R_{on}} V_{on} & V_1 = V_{on}, V_2 = V_{off} \end{cases} \quad (14)$$

- Case C: When $B_1 = I_{pl}$ and $B_2 = B_3 = I_{ph}$, the variation of resistance R_{s1}, R_{s2}, and R_{s3} is the same as that of Case C in state *I*, thus the node voltage V_{out2} can be computed as:

$$V_{out2} = \begin{cases} \frac{R}{R+R_{on}//(R_{off}//R_{off})}V_{on} & V_1 = V_{on}, V_2 = V_{on} \\ \frac{R//(R_{off}//R_{off})}{R//(R_{off}//R_{off})+R_{on}}V_{on} & V_1 = V_{off}, V_2 = V_{on} \\ \frac{R//R_{on}}{R//R_{on}+R_{off}//R_{off}}V_{on} & V_1 = V_{on}, V_2 = V_{off} \end{cases} \quad (15)$$

- Case D: When $B_1 = I_{ph}$ and $B_2 = B_3 = I_{pl}$, the variation of resistance R_{s1}, R_{s2}, and R_{s3} is the same as that of Case D in state *I*, thus the node voltage V_{out2} can be computed as:

$$V_{out2} = \begin{cases} \frac{R}{R+R_{off}//(R_{on}//R_{on})}V_{on} & V_1 = V_{on}, V_2 = V_{on} \\ \frac{R//(R_{on}//R_{on})}{R//(R_{on}//R_{on})+R_{off}}V_{on} & V_1 = V_{off}, V_2 = V_{on} \\ \frac{R//R_{off}}{R//R_{off}+R_{on}//R_{on}}V_{on} & V_1 = V_{on}, V_2 = V_{off} \end{cases} \quad (16)$$

- Case E: When $B_1 = I_{ph}$, $B_2 = I_{pl}$ and $B_3 = I_{ph}$ (or $B_1 = I_{ph}$, $B_2 = I_{ph}$ and $B_3 = I_{pl}$), the variation of resistance R_{s1}, R_{s2}, and R_{s3} is the same as that of Case E in state *I*, thus the node voltage V_{out2} can be computed as:

$$V_{out2} = \begin{cases} \frac{R}{R+R_{off}//(R_{on}//R_{off})}V_{on} & V_1 = V_{on}, V_2 = V_{on} \\ \frac{R//(R_{on}//R_{off})}{R//(R_{on}//R_{off})+R_{off}}V_{on} & V_1 = V_{off}, V_2 = V_{on} \\ \frac{R//R_{off}}{R//R_{off}+R_{off}//R_{on}}V_{on} & V_1 = V_{on}, V_2 = V_{off} \end{cases} \quad (17)$$

- Case F: When $B_1 = B_2 = B_3 = I_{ph}$, the variation of resistance R_{s1}, R_{s2}, and R_{s3} is the same as that of Case F in state *I*, thus the node voltage V_{out2} can be computed as:

$$V_{out2} = \begin{cases} \frac{R}{R+R_{off}//(R_{off}//R_{off})}V_{on} & V_1 = V_{on}, V_2 = V_{on} \\ \frac{R//(R_{off}//R_{off})}{R//(R_{off}//R_{off})+R_{off}}V_{on} & V_1 = V_{off}, V_2 = V_{on} \\ \frac{R//R_{off}}{R//R_{off}+R_{off}//R_{off}}V_{on} & V_1 = V_{on}, V_2 = V_{off} \end{cases} \quad (18)$$

As in the previous section, the ratio between the node voltage V_{out2} and the voltage value V_{out1} is defined as the corresponding output logic state variable. Assuming $R_{off} \geq 10\,R$, $R \cong 3\,R_{on}$, the correlation between the inputs (electrical inputs and optical inputs) and the output of state *II* is also shown in Table 4.

From Table 4, it can be shown that the proposed multi-valued logic circuit (including state *I* and state *II*) can implement 10 logic functions in 0–1. In addition, since the output state variables are voltages, the circuit is easy to cascade for implementing circuits with more complex functions.

3.3. Circuit Smulations and Analysis

To verify the effectiveness of the designed multi-valued logic circuit, a series of simulation experiments was performed on the same workstation as in the previous section. At the device level, the circuit uses three identical memristors, and the specific parameter configurations of the devices are detailed in Table 2. Notably, in addition to the memristors, the circuit needs to be configured with a resistor with a resistance of 0.3 kΩ, satisfying $R = 3\,R_{on}$. At the circuit level, different input variables (the electrical input variables and the optical signal variables) are necessary for implementing the multi-valued logic, configuring $V_{on} = 3$ V, $V_{off} = 0$ V, $I_{ph} = 300$ W/m^2, and $I_{pl} = 0$ W/m^2.

Figure 8 shows the simulation results of the multi-valued logic circuit (including states *I* and *II*). A_1 (the orange solid line) and A_2 (the red dashed line) indicate the input electrical signals, which are represented in the figure as the first column E(0, 0), the second column

E(1, 1), the third column E(0, 1), and the last column E(1, 0) for four electrical writing cases. B_1 (the purple dotted line), B_2 (the green dashed line), and B_3 (the pink dashed line) indicate whether or not an optical signal is applied to the memristor, written by O(i, j, z), and correspond to the optical case in the previous section. V_{out1} and V_{out2} of state *I* and *II* are indicated by the yellow solid and the blue dashed lines, respectively. The logical state variables are represented by the yellow dashed and blue solid lines, respectively, denoted as L(m, n).

As in the theoretical analysis, the simulation results are classified into Case A–Case F depending on whether or not illumination is applied to the memristors. Under Case A, Case C, Case D, and Case F, the simulation results are further divided into four cases according to whether the voltage is applied at the input ports, corresponding to the first row, the fourth row, the fifth row, and the last row in Figure 8. In addition, Case B (Case E) contains two cases, $B_2 = I_{pl}$, $B_3 = I_{ph}$ and $B_2 = I_{ph}$, $B_3 = I_{pl}$, for which the simulation results in Figure 8 contain eight small diagrams. From the first column of Figure 8, the voltage is not available at the output regardless of whether there is a light input or not, which corresponds to logic "0", since there is no voltage at the input. From Figure 8, the relationship between the input logic state variables and the output logic state variables obtained from the simulation corresponds to the truth table (Table 4), demonstrating that the circuit is capable of implementing multiple logic functions from 0–1, as well as verifying the validity of the constructed optoelectronic memristor model.

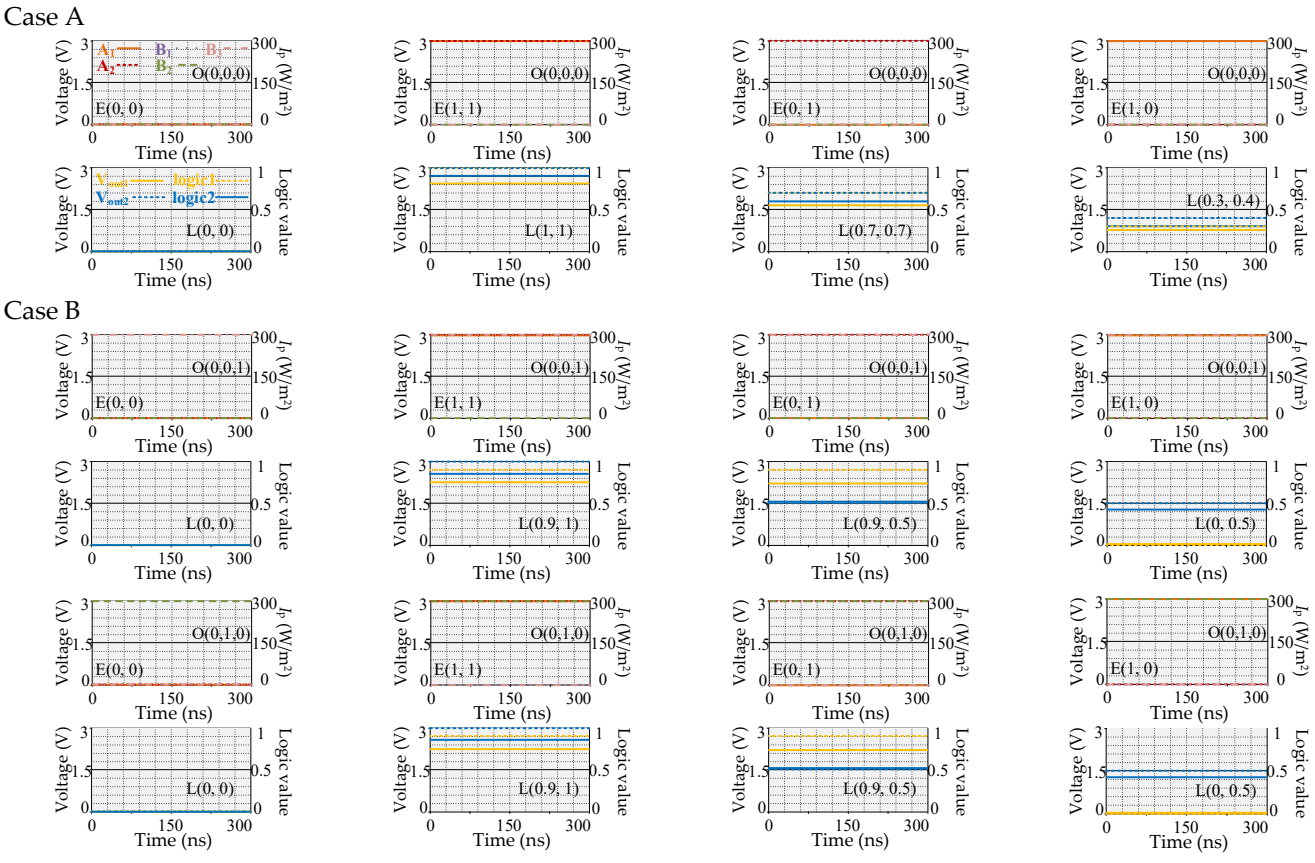

Figure 8. *Cont.*

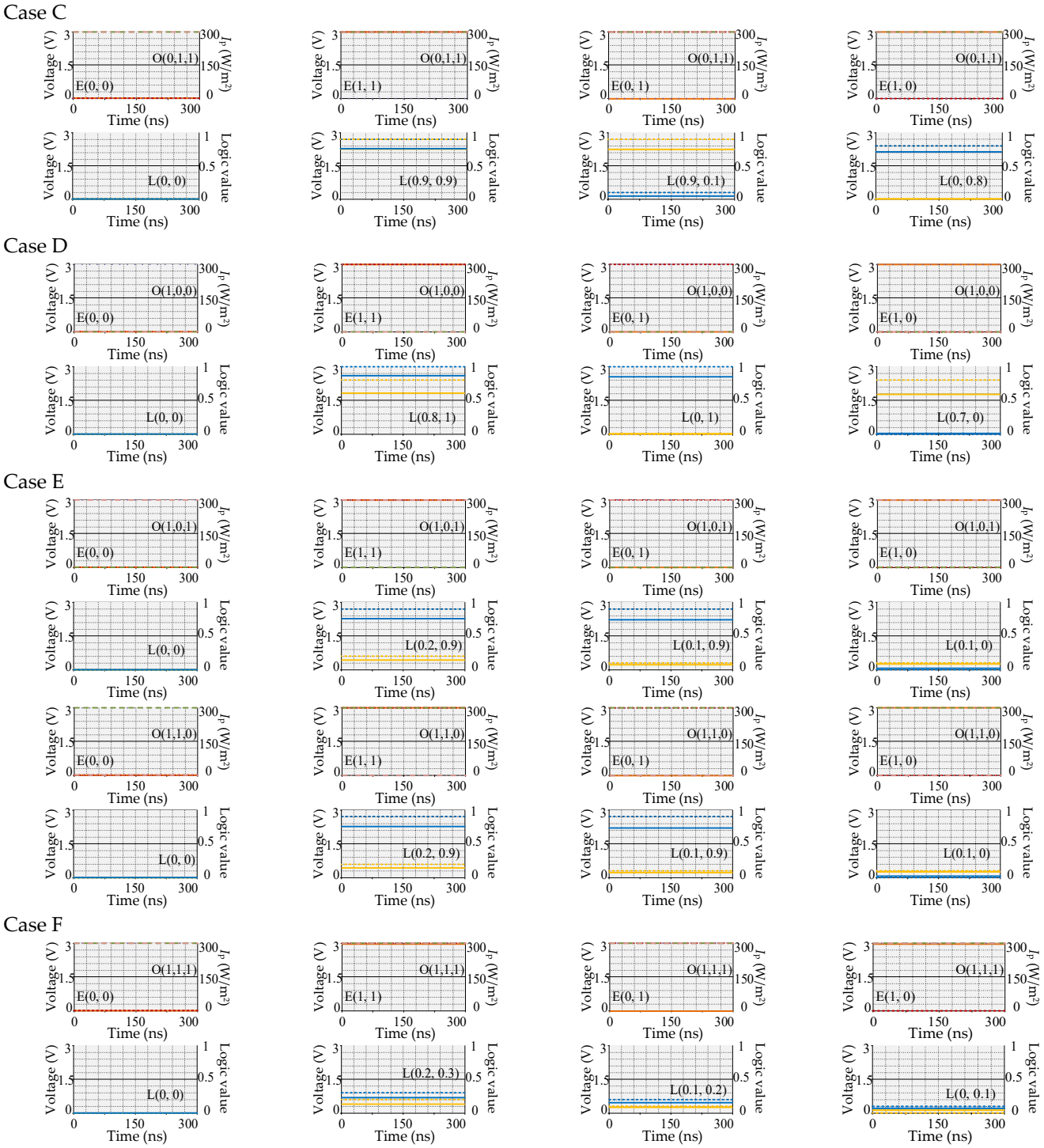

Figure 8. The simulation results of multi-valued logic circuit (including states *I* and *II*).

Then, the proposed multi-valued logic method is compared with five existing logic methods (i.e., material implication logic [29], memristor-aided logic [30], memristor ratioed logic [31], balanced ternary logic [32], and unbalanced ternary logic [33]). The comparison results including input variable, output variable, memristor type, computation form, need of resistors or transistors, initialization, cascading capacity and logic values are shown in Table 5.

Table 5. Comparison results of the proposed multi-valued logic circuits with other logic circuits.

	Proposed Logic	**Material Implication Logic**	**Memristor-Aided Logic**	**Memristor Ratioed Logic**	**Balanced Ternary Logic**	**Unbalanced Ternary Logic**
Input Variable	Voltage, illumination	M [1]	M [1]	Voltage	Voltage	Voltage
Output variable	Voltage	M [1]	M [1]	Voltage	Voltage	Voltage
Memristor type	Optoelectronic	HP	TEAM	VTEAM	VTEAM	Spintronic
Computation form	Parallel	Serial	Serial	Parallel	Parallel	Parallel
Need of resistors or transistors	√	√	×	√	√	√
Initialization	√	√	√	×	√	√
Cascading capacity	possible	difficult	difficult	possible	possible	possible
Logic values	Multi-valued	Binary	Binary	Binary	Ternary	Ternary

[1] M represents the memristance.

In Table 5, the proposed logic method differs from the other five logic methods in terms of input logic state variables by adding illumination variables that can affect the electrical characteristics of the device. The proposed logic circuit is easy to cascade because light is accessible and the output logic state variable is voltage. The memristor-aided logic has the simplest circuit structure and requires no additional circuit components other than the memristors. However, this method is calculated in series as in material implication logic, and the calculation process is more complicated. The proposed method requires initialization compared to the memristor ratioed logic, which increases the operation cost. In addition, the proposed method is able to implement multi-valued logic, while the other methods are restricted to binary and ternary logic.

4. Discussion

Currently, most of the research in the field of memristor logic implementation is aimed at binary logic and ternary logic. Nevertheless, relatively little research has been done to implement multi-valued logic circuits based on memristors, and there are abundant opportunities and challenges. The proposed multi-valued logic circuit cannot implement "0.5" in logic 0–1, and the circuit structure will be further improved to achieve complete logic functions in the future. Since the discrete logic output of the designed circuit cannot realize the affiliation function, continuous logic output will be explored in the future to build fuzzy systems.

5. Conclusions

This paper focuses on the modelling method of optoelectronic memristors. Specifically, the mathematical and circuit models of the optoelectronic memristor are developed using the optoelectronic effect that affects the electrical characteristics of such devices. Notably, the modelling approach is based on an improvement of the popular VTEAM modelling method. Moreover, the electrical characteristics (referring to the volt-ampere characteristics and memristance variation rule) of a single memristor and its series-parallel circuit under different illumination conditions and different voltages are tested. Furthermore, a rotation mechanism is introduced to realize the conversion between series and parallel circuits, and a multi-valued logic circuit containing two states (state *I* and state *II*) is designed. Simulation results demonstrate that the designed circuit is capable of implementing 10 logic functions from 0–1, which verifies the effectiveness of the established optoelectronic memristor model as well as providing a new approach to the circuit implementation of fuzzy logic.

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