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A LDO Regulator with Weighted Current Feedback Technique for 0.47nF-10nF Capacitive Load

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Abstract

A Weighted Current Feedback (WCF) technique for output capacitorless low-dropout (OCL-LDO) regulator is presented in this paper. Through feedback of a weighted current, the WCF permits smart management of the output impedance as well as the gain from the inter-gain stage. Based on the Routh–Hurwitz stability criterion, the WCF can avoid the right-half plane (RHP) pole and push the left-half plane (LHP) non-dominant complex pole pair to a higher frequency. Besides, it provides good regulator loop gain and fast transient response. Validated by UMC 65-nm CMOS process, the simulation and measurement results have shown that the WCF LDO regulator can operate at a C_L range from 470 pF to 10 nF with only 3.8 pF compensation capacitor. At a supply of 0.75 V and a quiescent current of 15.9 μA, the proposed circuit can support a maximum load current (I_L) of 50 mA. When I_L switches from 0 to 50 mA in 100 ns, the output can settle within 400 ns for the whole C_L range. For a case of single capacitor (C_L = 470 pF), the settling time is only 250 ns. The comparison results have shown that the WCF LDO regulator offers a comparable or better transient figure-of-merit (FOM) and additional merit to drive wide load capacitance range.

Keywords

Cascode Compensation, LDO regulator, Miller Compensation, Weighted Current Feedback (WCF), Wide Load Capacitance Range.

I. INTRODUCTION

Voltage regulators have been widely used to supply various function blocks in battery powered portable devices. A LDO regulator is very popular in power management IC design on the basis of its simple structure, fast response and low noise characteristic [1]. However, the LDO regulators using a μF level off-chip capacitor to achieve stable operation limit the ability for fully on-chip applications [2-6]. This turns out that the output capacitorless LDO (OCL-LDO) regulators [7-24] have received much attention recently. In System-on-Chip (SoC) environment pertaining to large scale digital circuits like DSP core(s) and memory banks, the effective supply line parasitic capacitance is large. To drive the circuits, the LDO regulator should support a wide load capacitance (C_L) range (few hundred pF to few nF) [25] with fast response. Furthermore, to ensure the accuracy of the LDO regulator, a multi-gain stage amplifier topology has to be adopted. Besides, under low power constraint, the output impedances of the gain stages can be high, resulting in several low frequency poles. This increases the design difficulty of the OCL-LDO regulator, especially for applications with wide range of C_L. In most of the reported OCL-LDO regulator designs, they usually drive a maximum C_L up to tens of pF or 100 pF [11, 12, 14, 17, 18, 20]. Few designs aim at driving relatively large C_L [8, 13, 16, 19, 24, 26]. Nevertheless, they have their limitations which are described in the following.

In [8], a Flipped Voltage Follower (FVF) topology is used as an output driver. It gives a very fast response with a recovering time of 0.54 ns. Since the quiescent current in this LDO regulator is 6 mA, it leads to unavoidable large quiescent power consumption. In addition, only a maximum C_L of 600 pF is reported. A direct voltage spike detection technique is reported in [13] that supports a 100 pF and a 1 nF capacitive load. Since the LDO regulator utilizes a simple folded FVF topology, the loop gain is fairly limited, thus trading off some of transient performances. In [16], an active compensation scheme is realized in order to enable the LDO regulator to drive a C_L up to 1 nF. However, several poles and zeros exist within the unity gain frequency (ω_{UGF}), leading to complicated pole-zero tracking. Any mismatch between poles and zeros will contribute slower transient response. In [19], a current amplifier is adopted to multiply the Miller capacitor which can extend the C_L driving capability to 1 nF. However, the design needs a large compensation

capacitor (tens of pF) to ensure stable operation. This may lead to relatively larger silicon area and slower transient speed. In [24, 26], a dual-summed Miller compensation is implemented. This is targeted to support a C_L range up to 10 nF but at the expense of increased settling time through the in-band zero for stability.

In view of the need to support a wide C_L range and good transient performance metrics under low quiescent power design objectives, a new circuit technique is demanded in the design of LDO regulators. In this paper, a weighted current feedback (WCF) technique, which aims at a wide C_L range (470 pF to 10 nF) for the LDO regulator design, is proposed.

In Section II, it presents the WCF circuit technique working principle. Section III describes the inter-gain stage's dynamic output impedance reduction as well as the small-signal model. Section IV presents the detailed stability analysis and the design strategy of WCF. This is then followed by the WCF LDO regulator circuit implementation in Section V. The experimental results, discussions and performance comparison are given in Section VI. Finally, the conclusion is drawn in Section VII.

II. PROPOSED WCF CIRCUIT TECHNIQUE

A. Conventional Multi-gain Stages in a LDO Regulator

Fig. 1 depicts the multi-gain stages in a LDO regulator. The regulator is usually a 3-stage amplifier plus a power transistor (M_P). It is noted that g_{mi} denotes the transconductance while R_i and C_i are the equivalent output resistance and lumped output parasitic capacitance of the i-th gain stage, respectively. R_O is the effective output resistance which includes the output resistance of power transistor as well as the loading resistance R_L. As can be seen from Fig. 1, the feedback system displays a four-pole (p_{-3dB}, p_2, p_3 and p_O) characteristic. In general design, p_O locates at a lower frequency than that of p_2 and p_3. Hence, p_2 and p_3 must be allocated to a higher frequency to ensure the stability. The typical implementation of 2^{nd} and 3^{rd} gain stages is to make node N_2 as a low impedance node ($R_2 \approx 1/g_m$) whereas node N_P as a high impedance node [10, 14, 15, 17, 20]. Since C_P is large due to a large power transistor M_P, p_3 is low especially under low power constraint. As reported in [14], two parasitic poles are generated with frequency inversely proportional to

$C_L R_O$. To stabilize the LDO regulator, C_L must be small. Moreover, since R_O is inversely proportional to I_L, a minimum workable I_L (e.g. 3 mA) is required to ensure a small R_O [14]. This restricts the LDO regulator's applications for a wide range of C_L and I_L. As such, a new circuit technique is needed to address this issue.

B. Proposed Negative Current Feedback Circuit Technique

In the proposed topology shown in Fig. 2, R_2 is designed to be high whereas R_P is designed to be dominantly small ($\approx 1/g_m$). With this arrangement, the 3rd gain stage can be dynamically biased. This will increase the charging/discharging rate of V_P. As a result, the speed of the regulator is greatly improved with respect to the conventional topology (Fig. 1). It is important to note that C_P and R_2 may be large. They lead to large $C_P R_P$ and $C_2 R_2$, respectively. Based on Routh–Hurwitz stability criterion, the large time constant $C_2 R_2$ and $C_P R_P$ may introduce a right-half-plane (RHP) pole. Therefore, a negative current feedback (NCF) technique is employed to avoid the RHP pole formation.

In the NCF block depicted in Fig. 2, the current sensor senses the voltage V_P and generates a transconductance current $g_{mf} V_P$ (g_{mf} is the transconductance of the current sensor). It is then fed back to the node N_2. Not only does the feedback current increase the bias current of 2nd stage as the first effect, it also forms a local negative current feedback loop (NCF loop in Fig. 2) as the second effect. Combining these two effects, the output impedance at node N_2 is reduced from R_2 to R_{2f} (R_{2f} is the negative current feedback loaded impedance at node N_2). As such, both $C_2 R_{2f}$ and the regulator loop gain are reduced. This permits the feedback system to fulfill the Routh–Hurwitz stability criterion. In addition, the NCF technique adds another advantage by shifting the non-dominant poles to a higher frequency. Hence the stability of the LDO regulator can be attained in the context of wide range of capacitive load and load current.

However, there are two tradeoff issues in the NCF LDO regulator. They are given as follows: (i) The gain of 2nd stage is reduced because of a smaller R_{2f}. This in turn reduces the total loop gain of the LDO regulator, thus sacrificing some regulation accuracy. (ii) The negative feedback current reduces the charging/discharging rate of the node N_2, which can reduce the transient speed. In view of the two drawbacks,

a weighted current feedback circuit technique is further proposed to tackle the limitations arising from the foundation NCF technique.

C. Proposed Weighted Current Feedback Circuit Technique

Fig. 3 shows a LDO regulator architecture using the WCF circuit technique. It comprises a fixed first gain stage, two variable gain stages (2^{nd} and 3^{rd} gain stages), a WCF block, a power transistor M_P, an overshoot reduction block and a frequency compensation network.

The shadowed area embodies the 2^{nd}, 3^{rd} gain stages as well as the WCF circuit (dash enclosed box). In the WCF topology, two sense transistors (M_{a1} and M_{a2}, size of M_{a2} > size of M_{a1}) sense the same voltage V_P and each generates respective feedback current (I_{a1}, I_{a2}) at the output of 2^{nd} gain stage. Moreover, the diode transistor M_{a3} is added in series with M_{a4} to control the operating region of M_{a2} during the change of load current. The working principle of the WCF technique can be explained from Fig. 4. (i) At low I_L (Fig. 4 (a)), both M_{a1} and M_{a2} are weakly biased for small negative current feedback. Each 2^{nd} and 3^{rd} gain stage works as a normal inverting amplifier. (ii) At moderated I_L (Fig. 4 (b)), both M_{a1} and M_{a2} are designed to work in saturation region. Two feedback currents (I_{a1}, I_{a2} and $I_{a2} > I_{a1}$) are generated and fed back to the node N_2. This results in a strong negative current feedback to the 2^{nd} stage. (iii) At high I_L (Fig. 4 (c)), only M_{a1} works in saturation region to give a small negative current feedback. M_{a2} is forced to work in linear region by the two diode transistors, M_{a3} and M_{a4}. As such, the negative current feedback is reduced. Owing to this weighted control mechanism in the WCF technique, the impedance at the node N_2 as well as the gain of 2^{nd} stage can be dynamically managed. Therefore, with reference to the proposed NCF technique, the advantages are as follows: (i) The gain of the WCF LDO regulator can be maintained reasonably well across the whole I_L range such that better regulation accuracy can be obtained. (ii) The charging/discharging rate of node N_2 is increased at high I_L, which results in faster transient speed.

The 3^{rd} gain stage is loaded by a resistor R_X and a diode transistor M_{d1}. The output impedance of this gain stage ($R_P \approx (1/g_{md1})//R_X$, g_{md1} represents the transconductance of M_{d1}) reduces when I_L increases. In this way, the load provides an adaptive bias when I_L changes. This subsequently increases the speed of 3^{rd} gain

stage.

Turning to the frequency compensation design, a combined frequency compensation scheme using both cascode and Miller compensation techniques is adopted. The dominant pole is mainly formed by the cascode compensation capacitor whilst a small Miller compensation capacitor is utilized to reduce the Q factor of the complex poles.

To complete the LDO architecture, an overshoot reduction block [20] is employed to reduce the overshoot magnitude and the settling time through a momentary discharging current.

III. DYNAMIC IMPEDANCE REDUCTION AND SMALL-SIGNAL MODEL

To investigate the negative current feedback loaded impedance R_{2f} at the node N_2, the small-signal model of the WCF LDO regulator is depicted in Fig. 5. It is obtained by breaking the loop at the output node as shown in Fig. 3. In the small-signal model, g_{mi}, R_i, and C_i have their usual meanings as defined in Section II-A. Particularly, C_c is the cascode compensation capacitor whereas C_m is the Miller compensation capacitor. C_L is the load capacitance which has a value ranging from 470 pF to 10 nF. Refer to Fig. 5, the total gain of the WCF feedback loop (A_{WCF}) in Fig. 3 is examined. It is given as

$$A_{WCF} = g_{m3} g_{mf} R_2 R_P \tag{1}$$

while R_{2f} can be obtained as

$$R_{2f} = \frac{R_2}{A_{WCF} + 1} = \frac{R_2}{\beta} = \frac{1}{g_{m3} g_{mf} R_P + 1/R_2} \tag{2}$$

By comparing the output impedance R_2 (without loaded feedback current source) in (2), R_{2f} is reduced by β (= $A_{WCF} + 1$) times. Moreover, R_{2f} can be reduced via either increasing A_{WCF} or decreasing R_2. Using this relationship, for the WCF LDO regulator, at low I_L, R_{2f} is large since β is small and R_2 is large. At moderate I_L, R_{2f} is significantly reduced with respect to R_2 due to a large β. At high I_L, since R_2 is already small due to a large current flowing in the 2nd gain stage, R_{2f} is small even with a small β.

Turning to the transfer function of the whole LDO regulator, it is derived using the following assumptions: (i) C_1, C_2 << C_m << C_c << C_L; (ii) $g_{m1}R_1$, $g_{m2}R_2$ >> 1, (iii) the input resistance at the cascode compensation node, is approximately equal to $1/g_{mc}$ and (iv) R_P is inversely proportional to I_L. Finally, the open-loop transfer function is obtained as follows:

$$A_{op}(s) = \frac{v_{fbout}}{v_{fbin}} = -\frac{A_{DC}\left(1 + s\,C_c/g_{mc}\right)}{1 + as + bs^2 + cs^3 + ds^4 + es^5} \tag{3}$$

where

$$a = C_L R_O + C_c g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \beta \tag{4}$$

$$b = C_m C_L R_1 R_O + C_c C_m g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \left(\beta g_{mc}\right) \tag{5}$$

$$c = C_m C_L R_1 R_O \left(C_c / g_{mc} + C_P R_P / \beta\right) \tag{6}$$

$$d = C_c C_m C_P C_L R_1 R_P R_O / \left(\beta g_{mc}\right) \tag{7}$$

$$e = C_c C_m C_2 C_P C_L R_1 R_2 R_P R_O / \left(\beta g_{mc}\right) \tag{8}$$

The DC loop gain of the LDO regulator is given by

$$A_{DC} = g_{m1} g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \beta \tag{9}$$

which indicates that the loop gain is reduced by a factor of β. This correlates well with the impedance reduction at the node N_2, namely, $R_{2f} = R_2/\beta$. Besides, the cascode compensation generates a zero which is expressed as

$$z = -g_{mc}/C_c \tag{10}$$

Using (3) − (10), the stability of LDO regulator can be analyzed in the following Section.

IV. STABILITY ANALYSIS AND WCF DESIGN STRATEGY

The design strategy of the WCF technique is on the basis of the stability of the LDO regulator at different C_L and I_L conditions. Firstly, using the Routh–Hurwitz stability criterion, the required β (denoted as β_{RH}) can be obtained. Secondly, under a PM of 45° constraint, the required β (denoted as β_{PM}) is also investigated. The respective analysis is explained in the following.

As can be seen from (4) to (8), all the parameters in the transfer function are dependent on the value of C_LR_O. Besides, R_O is inversely proportional to I_L. For this reason, the design strategy for β and the stability of the regulator are analyzed in three cases: (I) C_LR_O is large (low I_L). The first term in (4) and (5) are dominant. (II) C_LR_O is moderate (low I_L). The first term is comparable with second term in (4) and the first term in (5) is dominant. (III) C_LR_O is small (moderate I_L and high I_L). The second term in (4) and (5) are dominant. Besides, the term C_PR_P/β in (6) is small due to a small R_P. Finally, the respective simplified expression for variables from a to e is summarized in Table I.

A. Design Strategy of β using Routh−Hurwitz Stability Criterion

Routh−Hurwitz stability criterion has been widely used in the multi-stage amplifier designs [27-29]. It is simply evaluated by constructing the Routh Table A-I in Appendix using the closed-loop transfer function. To achieve stability for the feedback system, the coefficients for a_0–a_5 and b_1, c_1, d_1 in the second column of Table A-I must be positive. Since a_0–a_5 is always larger than zero, the design condition for β_{RH} can be obtained by setting b_1, c_1 and d_1 larger than zero respectively. Refer to the WCF LDO regulator, the closed-loop transfer function can be expressed as

$$A_{cl}(s) = \frac{A_{op}(s)}{1 - A_{op}(s)} \approx \frac{-A_{DC}\left(1 + s\,C_c/g_{mc}\right)}{A_{DC} + \left(A_{DC}C_c/g_{mc} + a\right)s + bs^2 + cs^3 + ds^4 + es^5} \tag{11}$$

where $A_{op}(s)$ is the open-loop transfer function defined in (3). By substituting the approximated expression for variables a to e from Table I as well as (9)–(10) into (11), the Routh table parameter expansion for Large,

Moderate and Small C_LR_O cases is listed in Appendix Table A-II. Based on these parameters, β_{RH} for each case is analyzed as follows:

Case I): Large C_LR_O (Low I_L) condition, the Routh Table parameters are shown in Case I of Table A-II. To meet the stability criterion, the following conditions must be satisfied. They are obtained as

$$C_m C_L R_1 R_O \left(C_c / g_{mc} + C_P R_P / \beta_{RH} \right) > 0 \tag{12}$$

$$C_m C_L R_1 R_O > 0 \tag{13}$$

$$\beta_{RH} > C_c g_{m1} g_{m2} g_{m3} g_{mp} R_1 R_2 R_P / \left(C_L g_{mc} \right) \tag{14}$$

For (12) and (13), it is obviously valid for any β_{RH}. As for (14), the right hand side term is inversely proportional to C_L. Due to C_L ranges from 470 pF to 10 nF, β_{RH} is small in this case.

Case II): Moderate C_LR_O (Low I_L) condition, when C_LR_O is equal to the cascode compensation term, namely,

$$C_c g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \beta = C_L R_O \tag{15}$$

the Routh Table parameters are shown in Case II of Table A-II. As indicated, b_1 and c_1 for Case I and Case II are the same. The design conditions for $b_1 > 0$ and $c_1 > 0$ can still be expressed by (12) and (13), respectively. Since (12) and (13) are always valid for any $\beta_{RH,}$ the condition for β_{RH} to meet the criterion is obtained as

$$\beta_{RH} > C_P g_{m1} R_P / \left(2C_c \right) \tag{16}$$

From (16), the right hand side term is proportional to $g_{m1}R_P$. Since the maximum value for R_P is R_X as explained in Section II-C, β_{RH} can be made small by proper sizing of R_P and g_{m1}.

Case III): Small C_LR_O (Moderate and High I_L) condition, the Routh Table parameters are shown in Case III of Table A-II. To meet the criterion, the following three design requirements for β_{RH} must be fulfilled. They are expressed as

$$\beta_{RH} > C_2 g_{m2} g_{m3} g_{mp} R_2^2 R_P / C_L \tag{17}$$

$$\beta_{RH} > \left(1 + g_{m1}/g_{mc}\right) C_P g_{mc} R_P / C_m \tag{18}$$

$$\beta_{RH} > \frac{C_2 g_{m2} g_{m3} g_{mp} R_2^2 R_P}{C_L} + \left(1 + \frac{g_{m1}}{g_{mc}}\right) \frac{C_P g_{mc} R_P}{C_m} \tag{19}$$

If the condition in (19) is met, (17) and (18) will be valid as well, but not vice versa. This suggests that (19) determines the only choice out of three β_{RH} inequalities. As such, at moderate I_L, R_2 and R_P are fairly large. β_{RH} is the largest. On the other hand, at high I_L, R_P is small owing to the large biasing current flowing in the diode transistor M_{d1} of 3rd gain stage. R_2 is also small due to the dynamic bias introduced by the WCF block. Thus β_{RH} at high I_L condition is reduced with respect to that of moderate I_L case. Based on the above analysis, Table II summarizes the β_{RH} at different I_L conditions. From this table, it confirms that the WCF should be made strong at moderate I_L condition whilst weak at both low and high I_L conditions.

Consider the WCF technique employed in the LDO regulator as discussed in Section II-C, the feedback factor β (β_{sim}) and R_{2f} are simulated with respect to I_L. As observed in Fig. 6, the WCF technique can significantly reduce R_2, especially for moderate and high I_L. Moreover, when I_L increases, β_{sim} increases to around 25 dB at I_L = 200 μA first. Then it drops below 5 dB when I_L is larger than 10 mA.

To verify that the WCF design can fulfill the stability criterion using numerical examples, the theoretical β_{RH} at different I_L conditions are calculated using the right hand side term of inequalities (14), (16) and (19). The design parameters and stability verification using theoretical β_{RH} and simulated β_{sim} at I_L = 0 mA, 1 mA and 50 mA are shown in Table III. It can be seen that the WCF can meet the β_{RH} requirement for all three I_L conditions for both C_L = 470 pF and 10 nF.

From the above analysis together with the numerical examples, the WCF technique can provide an appropriate feedback to meet the Routh−Hurwitz stability criterion for low, moderate and high I_L conditions using the design equations (14), (16) and (19). As a result, these equations provide the design guidelines for the amount of feedback in the WCF at different I_L conditions.

B. Pole and Zero Locations

The feedback factor β, R_{2f}, poles, zero and related parameters for Large, Moderate and Small C_LR_O cases are presented in Table IV. Owing to the cascode compensation, a LHP zero, expressed in (10), is generated. It locates outside the ω_{UGF}. Hence, it will not jeopardize the settling time of LDO regulator. The pole location analysis for each case is discussed as follows:

Case I – Large C_LR_O (Low I_L): At this condition, C_LR_O forms the low frequency dominant pole (p_{-3dB} = $1/(C_LR_O)$). Since p_{-3dB} locates at a very low frequency, the ω_{UGF} is small. At this juncture, all the parasitic poles locate at relative high frequencies. The LDO regulator can maintain a stable operation. This is the reason why a weak negative current feedback is designed. It also correlates well with the Routh−Hurwitz stability criterion analysis in Section IV-A that at large C_LR_O condition, β_{RH} is small using (14). In view of the weak feedback, the regulator's gain and speed do not significantly change with respect to the regulator without WCF technique.

Case II – Moderate C_LR_O (Low I_L): In this case, p_{-3dB} is constituted by both the C_LR_O and the cascode compensation. The ω_{UGF} is increased with respect to that in Case I. However, ω_{UGF} remains small and only half of its maximum value. Besides, $|p_{2,3}|_f$ is also increased slightly when compared to that in Case I. The regulator can achieve a stable operation with a small feedback as suggested in (16).

Case III – Small C_LR_O (Moderate and High I_L): In this case, p_{-3dB} is mainly constituted by the cascode compensation. Moreover, though the loop gain of regulator is reduced by a factor of β according to (9), the dominant pole p_{-3dB} frequency is increased by the same factor, which yields a constant ω_{UGF}.

For $|p_{2,3}|_f$, they are reduced by a factor of $\sqrt{\beta}$. However, $|p_{2,3}|_f$ can still be designed to be higher than that of ω_{UGF} through choosing a proper value of g_{mc} and C_c. This can be derived as

$$\sqrt{\frac{g_{m2}g_{m3}g_{mp}g_{mc}R_2R_P}{\beta C_m C_L}} \geq \frac{g_{m1}}{C_c} \tag{20}$$

which can be rewritten in a form of

$$C_c\sqrt{g_{mc}} \geq g_{m1}\sqrt{\frac{\beta C_m C_L}{g_{m2}g_{m3}g_{mp}R_2R_P}} \tag{21}$$

From (21), both C_c and g_{mc} can be increased to ensure that $|p_{2,3}|_f$ locates at a higher frequency than ω_{UGF}. By substituting the design parameters from Table III with I_L = 1 mA to (21) as a numerical example, the calculated minimum C_c is 1.5 pF. Since the designed C_c is 3.5 pF in the WCF LDO regulator, it is more than the required theoretical minimum value.

Of another important design consideration, besides the WCF LDO regulator can fulfill the Routh–Hurwitz stability criterion as discussed in Case III of Section IV-A, the open-loop transfer function (3) generates a high frequency LHP complex pole pair $|p_{4,5}|_f$. Its frequency is multiplied by a factor of $\sqrt{\beta}$ with respect to that without the feedback. In this way, at moderate I_L, due to a large β, the complex pole pair $|p_{4,5}|_f$ is located far away from the ω_{UGF}. At high I_L, though β is reduced with reference to that at moderate I_L, due to very small R_P and R_2, the complex pole pair $|p_{4,5}|_f$ still locates at a much higher frequency than ω_{UGF}. This confirms the stability of LDO regulator at both moderate and high I_L conditions.

Fig. 7 depicts the simulated open-loop gain and phase of the WCF LDO regulator for C_L = 470 pF and C_L = 10 nF under different I_L conditions. It can be seen that the LDO regulator can provides a stable operation for both C_L corners. Fig. 8 shows the phase margin (PM) and gain margin (GM) for C_L = 470 pF, 1 nF, 3.3 nF and 10 nF when sweeping I_L. The regulator achieves a minimum PM of 45° and a minimum GM of 11 dB. This has illustrated that the WCF LDO regulator is stable under different C_L and I_L combinations. The detailed explanation is discussed in next Section.

C. Phase Margin under C_L and I_L Variations

Refer to the PM plot in Fig. 8, for C_L = 3.3 nF and 10 nF, when the I_L increases from 1 μA to 50 mA, the PM of LDO regulator initially decreases to around 45° and then it increases until to 100°. This observation stems from different dominant factors between C_LR_O and cascode compensation term in the formation of p_{-3dB}. The analysis can also be partitioned into three regions: (i) Under large C_LR_O condition (low I_L), due to a small ω_{UGF}, $|p_{2,3}|_f$ is located at a much higher frequency than ω_{UGF}, resulting in a large PM. (ii) when I_L

increases, R_O reduces. The continual reduction of C_LR_O increases the ω_{UGF}. Since the load current I_L is still low, the $|p_{2,3}|_f$ is almost constant based on Table IV. As such, the PM of regulator will keep reducing as the ω_{UGF} becomes closer to the $|p_{2,3}|_f$. When C_LR_O becomes moderate and comparable with cascode compensation term, the PM is approaching to the vicinity of the minimum point. (iii) When I_L further increases, C_LR_O becomes small. On the contrary, the cascode compensation becomes the dominant term, leading to the fixed ω_{UGF} ($=g_{m1}/C_c$). Besides, $|p_{2,3}|_f$ will increase since g_{mp} becomes larger. This will cause the PM to rise when I_L increases.

Based on the analysis in Section IV-A, if the feedback factor β can meet the design conditions stated in (14), (16) and (19) according to the Routh–Hurwitz stability criterion, $|p_{4,5}|_f$ will be pushed to a much higher frequency than ω_{UGF}. This indicates that $|p_{4,5}|_f$ will not influence the PM of regulator. With this assumption, the PM of feedback system can be approximated as

$$PM \approx 90^o - \tan^{-1}\left\{\frac{\omega_{UGF}}{Q_{|p_{2,3}|_f}\left|p_{2,3}\right|_f\left[1-\left(\omega_{UGF}/\left|p_{2,3}\right|_f\right)^2\right]}\right\}+\tan^{-1}\left(\frac{\omega_{UGF}}{z_1}\right) \tag{22}$$

based on [15]. Through substituting the respective expression of ω_{UGF}, $|p_{2,3}|_f$ and $Q_{|p_{2,3}|_f}$ for Large, Moderate and Small C_LR_O case in Table IV into (22), the design requirement of β_{PM} for a minimum PM of 45^o is analyzed as follows:

Case (I) – Large C_LR_O (Low I_L): To achieve a PM $\geq 45^o$, the necessary condition for β_{PM} to be satisfied is

$$\beta_{PM} \geq \frac{C_m g_{m1} g_{m2} g_{m3} g_{mp} R_1^2 R_2 R_P}{C_L} \tag{23}$$

From (23), the minimum β_{PM} (β_{PM_min}) is inversely proportional to C_L. A large C_L gives a smaller ω_{UGF} which subsequently reduces the feedback requirement for a PM $\geq 45^o$.

Case (II) – Moderate C_LR_O (Low I_L): In the situation when the cascode compensation effect equals to

that of C_LR_O as defined in (15), for a larger C_L, a larger g_{mp} (implying a large I_L) in the left hand side is needed to balance the right hand side term. This implies that the minimum PM region will shift slightly to the right when C_L increases in context of whole current range (0−50mA). This is consistent with the observation of PM plot in Fig. 8. For a PM ≥ 45 °, it suggests that β_{PM} should fulfill the condition of

$$\beta_{PM} \geq \frac{C_m C_P g_{m1}^2 R_1 R_P}{8C_c^2 - \left(2 + g_{m1}/g_{mc}\right) C_m C_c g_{m1} R_1} \tag{24}$$

It is noted that I_L is still small even the balance point for (15) shifts to a higher I_L when C_L increases. Moreover, since R_P is inversely proportional to $\sqrt{I_L S_{d1} / S_p}$, where S_p and S_{d1} is the respective aspect ratio of the power transistor M_P and the driving transistor M_{d1} in Fig. 3, R_P is approximated independent of C_L. As a result, β_{PM_min} is almost constant for the whole C_L range from (24).

Case (III) – Small C_LR_O (Moderate and High I_L): As indicated in small C_LR_O case of Table IV, $|p_{2,3}|_f$ is inversely proportional to $\sqrt{\beta}$. β should not be made too large to achieve a minimum 45° PM. The condition for the β_{PM} becomes

$$\beta_{PM} \leq \frac{C_c^2 g_{mc} g_{m2} g_{m3} g_{mp} R_2 R_P}{C_m C_L g_{m1}^2} \tag{25}$$

From (25), the maximum allowable β_{PM} (β_{PM_max}) is proportional to g_{mp}. At small C_LR_O case, due to large I_L, g_{mp} becomes large, contributing a large β_{PM_max}. On the other hand, due to the WCF technique to reduce the feedback at large I_L, the design β is not easily exceeding the β_{PM_max} defined in (25).

To verify the WCF regulator can fulfill the design requirement for a minimum 45° PM using numerical examples, β_{PM_min} or β_{PM_max} at different C_LR_O conditions are calculated using (23)−(25). Using the design parameters in Table III, the theoretical β_{PM} and simulated β_{sim} for Large, Moderate and Small C_LR_O are shown in Table V. It is noted that (i) for Large C_LR_O case, β_{PM} at C_L = 3.3 nF and I_L = 0 mA is chosen. This is because, for C_L = 470 pF and 1 nF, the C_LR_O is already comparable with the cascode compensation term at 0 mA. For 10 nF, β_{PM_min} is smaller than that of 3.3 nF. (ii) For Moderate C_LR_O case, the worst β_{PM} at C_L = 470

pF, I_L = 0 mA is chosen. (iii) For Small C_LR_O cases, the β_{PM} at C_L = 10 nF, I_L = 50 mA is chosen. The results in Table V indicate that the WCF can meet the β requirement for all three C_LR_O conditions. A minimum PM of 45^o can be achieved as depicted in Fig. 8.

In brief, for regulator's stability, both the Routh–Hurwitz stability criterion and 45^o minimum PM should be fulfilled. By combining the design equations of β_{RH} in Section IV-A [(14), (16) and (19)] and β_{PM} in Section IV-C [(23)-(25)], the required β is summarized in Table VI. For large C_LR_O case (Case I), since $C_mR_1 >> C_c/g_{mc}$, if the condition in (23) is met, (14) is valid as well. This suggests that (23) is the only choice for design inequalities. For Moderate C_LR_O case (Case II), the design equations are decided by (16) and (24) together. For small C_LR_O case (Case III), (19) and (25) gives the lower and upper bound for β_{req} respectively. Using this table, the design guidelines for β is investigated in details.

D. Combined Frequency Compensation and Q-Factor

The WCF LDO regulator employs a combined cascode and Miller compensation. The dominant pole is determined by the cascode compensation since it can push the non-dominant pole to a higher frequency under a large capacitive load in comparison to the Miller compensation counterpart [30]. Unfortunately, the cascode compensation easily gives gain peaking due to a large parasitic Q factor [31]. To overcome the drawback, a small Miller compensation capacitor is added in this LDO regulator so as to reduce the Q factor. This is mainly because the Q factor value is inversely proportional to the capacitance at the Miller node [31]. This can also be validated from the Q factor expressions shown in Table IV. At moderate and high I_L conditions (cascode compensation dominating), $Q_{|p_{2,3}|_f}$ is inversely proportional to $\sqrt{C_m}$. A large C_m contributes to a small Q factor which can reduce the peaking effect arising from the complex pole pair $|p_{2,3}|_f$. However, a large C_m will reduce the frequency of $|p_{2,3}|_f$ as well. This will jeopardize the cascode effect. For this reason, C_m is designed to be small (0.3 pF) in the WCF topology to achieve a reasonable Q factor whilst keeping the complex pole pair $|p_{2,3}|_f$ locating outside the ω_{UGF}.

E. Minimum C_L for a Stable Operation

As discussed in Section IV−C, when C_L is 470 pF, the dominant pole is in moderate C_LR_O region at I_L = 0 mA. If the minimum C_L (470 pF) is further reduced to a smaller value, the dominant pole will directly move into small C_LR_O region. To meet the Routh−Hurwitz stability criterion, β_{RH} must fulfill (19) across the whole I_L range. However, at small I_L, R_P becomes large and it causes a large β_{RH}. This suggests that a very strong feedback is needed at low I_L to ensure stable operation. The gain as well as the speed of regulator will be limited. Based on the tradeoff design considerations, the output C_L of regulator is preferably to start from the mid-range capacitive load (470 pF) onwards.

V. CIRCUIT IMPLEMENTATION

The complete schematic implementation of the WCF LDO regulator is shown in Fig. 9. It utilizes a folded cascode error amplifier constituted by (M_0 – M_8) as the first gain stage. The 2nd, 3rd inverting gain stages and the WCF block employ the same structure as that in Fig. 3. The overshoot reduction block (C_B, R_B, M_{13}) senses the voltage swing at the node N_P and generates a momentary sinking current to reduce the overshoot magnitude as well as settling time of the LDO regulator.

To compare the regulation accuracy and the speed of LDO regulator with the two proposed NCF and WCF technique, a NCF LDO regulator is also built and simulated. In the NCF LDO regulator, M_{a3} in the WCF block (Fig. 9) is removed. In such an arrangement, both M_{a1} and M_{a2} are working in saturation region. This turns out that the negative current feedback is kept strong for both moderate and high I_L conditions. Fig. 10 shows the exemplary transient responses of the LDO regulator with NCF and WCF technique. Under the same load current switching condition, it can be observed that the WCF LDO regulator displays a 1.5 times smaller undershoot and overshoot, and an approximate 2 times better load regulation with respect to the NCF LDO regulator. This has demonstrated that the WCF technique addresses the limitations of the NCF and achieves a better optimization of stability, accuracy and speed.

VI. EXPERIMENTAL RESULTS AND DISCUSSIONS

The WCF LDO regulator is implemented using UMC 65-nm CMOS process. The microphotograph of the WCF regulator is shown in Fig. 11. Excluding the supply and output PADs as connectors, the active area is 0.0133 mm^2. At a 0.75 V supply voltage, the WCF LDO regulator can support a maximum I_L of 50 mA. The dropout voltage is less than 0.2 V at full I_L. The measured quiescent current at zero I_L is 15.9 μA. With a total 3.8 pF (3.5 pF cascode + 0.3 pF Miller) compensation capacitance, the WCF LDO regulator offers stable operation for C_L ranging from 470 pF to 10 nF across the whole I_L range.

It is noted that external reference voltages are used and off-chip capacitors are added to model the C_L of the LDO regulator during the measurement. To test the stability and the performance of the WCF LDO regulator for the whole C_L range, four standard load capacitors (470 pF, 1 nF, 3.3 nF and 10 nF) have been chosen. In addition, two I_L switching cases (0 to maximum I_L and 1 mA to maximum I_L) are used to measure the transient performance.

Fig. 12 shows the measured load transient responses of the WCF LDO regulator when I_L is switching from 0 to 50 mA with an edge time of 100 ns for all four load capacitors. The supply voltage is 0.75 V and the output voltage is 0.55 V. As can be observed from the graphs, the undershoots are 113 mV, 109 mV, 98 mV, 72 mV whereas the overshoots are 29 mV, 29 mV, 27 mV, 32 mV for C_L = 470 pF, 1 nF, 3.3 nF and 10 nF, respectively. The undershoot becomes smaller when the load capacitor increases. This is because a larger capacitor is able to absorb a larger transient current during I_L switching. In addition, due to the intelligent control of WCF and the high speed property of the 3rd gain stage, the settling time of the WCF LDO regulator is quite small. The measured settling time are 248 ns, 244 ns, 252 ns and 368 ns for C_L = 470 pF, 1 nF, 3.3 nF and 10 nF, respectively.

Fig. 13 shows the transient responses of the WCF LDO regulator at V_{DD} = 0.75 V when I_L switches from 1 mA to 50 mA (vice versa) for C_L = 470 pF and C_L = 10 nF. Using an identical edge time of 100 ns, the undershoots are substantially reduced when compared with that of I_L switching from 0 to 50 mA. The undershoots are 24 mV, 35 mV whereas the overshoots are 24 mV, 29 mV for C_L = 470 pF and 10 nF,

respectively.

Fig. 14 depicts the transient responses of the WCF LDO regulator at V_{DD} = 1.2 V when I_L switches from 1 mA to 50 mA (vice versa) for C_L = 470 pF and C_L = 10 nF. The LDO regulator works well for a 1.2 V supply. Comparing the results with V_{DD} = 0.75 V in Fig. 13, the undershoot and overshoot increase by around 15 mV. This is because, at V_{DD} = 1.2 V, the large feedback transistor M_{a2} turns off at a higher I_L than that of V_{DD} = 0.75 V. Therefore, the regulator's speed at high I_L is slightly reduced. This leads to a small amount increment for transient undershoot and overshoot.

The line transient response at I_L = 1 mA, C_L = 470 pF is depicted in Fig. 15. When V_{DD} switches from 0.75 V to 1.2 V with a 10 μs edge time, the maximum output voltage spike is 4.3 mV and the introduced increment of error voltage is only 1.8 mV. Fig. 16 shows the measured power supply rejection (PSR) of the WCF LDO regulator for C_L = 470 pF at different I_L conditions. At 1 kHz, it can be seen that the minimum PSR is around -44 dB when I_L = 1 mA. This is due to some loop gain reduction from the large feedback (β) as revealed in (9). At full I_L, the regulator achieves a PSR of -51 dB. Fig. 17 depicts the measured output noise response of the LDO regulator at C_L = 470 pF and I_L = 0 mA. It can be seen that the noise is -98.7 dBm/Hz (2.6 $\mu V/\sqrt{Hz}$) at 100 Hz and -105 dBm/Hz (1.25 $\mu V/\sqrt{Hz}$) at 100 kHz, respectively.

Performance comparison between the WCF LDO regulator and the other reported state-of-the-art OCL-LDO regulators is presented in Table VII. With the WCF circuit technique, the LDO regulator achieves good performance metrics with an additional merit to drive a wide C_L range. To compare the load transient performance, the OCL-LDO regulator figure-of-merit (FOM) [14] is adopted. This is given by

$$FOM = K\left(\frac{\Delta V_{OUT} \times I_Q}{\Delta I_{OUT}}\right) \tag{26}$$

where K is the edge time ratio and defined as

$$K = \frac{\Delta\text{t used in the measurement}}{\text{the smallest } \Delta\text{t among the designs for comparison}} \tag{27}$$

To provide a comparison, all the results in Table VII for the WCF LDO regulator is based on C_L = 470 pF which is regarded as the closer load capacitance value with respect to the reported works. Since some of the designs [13, 14, 16] were tested using some amount of minimum loading currents, two FOMs of the WCF LDO regulator are used for comparison. The first FOM (left column) represents the performance metric for I_L switching from 0 to 50 mA while the second FOM (right column) represents the performance metric for I_L switching from 1 mA to 50 mA.

As can be seen from Table VII, the WCF LDO regulator design achieves a comparable or better FOM with respect to the reported OCL-LDO regulators. In addition, it can drive a wide C_L range with fast settling time and good performance metrics such as load regulation, line regulation and PSR.

VII. CONCLUSION

A weighted current feedback (WCF) technique is proposed in this paper. It establishes a weighted negative current feedback loop and provides an adaptive bias to the inter-gain stage. This permits smart management of the output impedance and gain of the inter-gain stage. As a result, using the WCF circuit technique and Routh–Hurwitz stability criterion to devise the design strategy to access the stability, the regulator can achieve stable operation, high accuracy and fast response simultaneously with small quiescent power consumption.

Validated by UMC 65-nm CMOS process, the simulation and measurement results have demonstrated that the WCF technique can stabilize the LDO regulator for load capacitance ranging from 470 pF to 10 nF whilst maintaining a very good transient performance metrics. The WCF regulator design reaches a comparable or better FOM with respect to the reported OCL-LDO regulators. Therefore, the WCF LDO regulator topology is useful for fully on-chip applications with wide load capacitance range.

VIII. ACKNOWLEDGMENT

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APPENDIX

For the denominator of the closed-loop transfer function in (11), it can be represented as

$$\begin{aligned} D(s) &= A_{DC} + \left(\frac{A_{DC} C_c}{g_{mc}} + a \right) s + bs^2 + cs^3 + ds^4 + es^5 \\ &= a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5 \end{aligned} \tag{I-1}$$

The Routh Table is constructed and shown Table A-I. For stable system, it should not have RHP poles. This requires the coefficients for a_0– a_5, b_1, c_1, d_1 to be positive. By substituting the approximated expression for variables a to e in Table I and (9)–(10) into (I-1), the Routh table parameters for large $C_L R_O$ (Case I), Moderate $C_L R_O$ (Case II) and Small $C_L R_O$ (Case III) are listed in Table A-II.

Figure Captions:

Fig. 1. Conventional multi-gain stages in a LDO regulator.

Fig. 2. Proposed Negative Current Feedback (NCF) topology embedded in multi-gain stages in a LDO regulator.

Fig. 3. A LDO regulator architecture using the WCF technique.

Fig. 4. Simplified schematic structure of 2^{nd}, 3^{rd} gain stages and WCF for (a) low I_L, (b) moderate I_L, and (c) high I_L.

Fig. 5. Small-signal model of the WCF LDO regulator architecture.

Fig. 6. Simulated β (β_{sim}) and R_{2f} at different I_L conditions.

Fig. 7. Simulated open-loop gain and phase at different I_L for (a) C_L = 470 pF and (b) C_L = 10 nF at V_{DD} = 0.75 V.

Fig. 8. Simulated phase margin (PM) and gain margin (GM) for C_L = 470 pF, 1 nF, 3.3 nF and 10 nF when sweeping I_L at V_{DD} = 0. 75V.

Fig. 9. Schematic of the WCF LDO regulator.

Fig. 10. Exemplary transient response of the LDO regulator with proposed NCF and WCF technique.

Fig. 11. Microphotograph of the WCF LDO regulator.

Fig. 12. Measured load transient responses with V_{DD} = 0.75 V, V_{OUT} = 0.55 V for (a) C_L = 470 pF, (b) C_L = 1 nF, (c) C_L = 3.3 nF and (d) C_L = 10 nF.

Fig. 13. Measured load transient responses at V_{DD} = 0.75 V with I_L switching from 1 mA to 50 mA (vice versa) for (a) C_L = 470 pF and (b) C_L = 10 nF.

Fig. 14. Measured load transient responses at V_{DD} = 1.2 V with I_L switching from 1 mA to 50 mA (vice versa) for (a) C_L = 470 pF and (b) C_L = 10 nF.

Fig. 15. Measured line transient response at I_L = 1mA and C_L = 470 pF.

Fig. 16. Measured PSR at C_L = 470 pF for different I_L.

Fig. 17. Measured output noise at C_L = 470 pF with 0 mA I_L.

Table Captions:

TABLE I: APPROXIMATED VARIABLES FROM a TO e FOR LARGE, MODERATE AND SMALL C_LR_O CASES

TABLE II: SUMMARY OF THE REQUIRED β_{RH} AT DIFFERENT I_L CONDITIONS TO MEET ROUTH−HURWITZ CRITERION

TABLE III: DESIGN PARAMETERS, STABILITY VERIFICATION USING THEORETICAL β_{RH} AND SIMULATED β_{sim}

TABLE IV: FEEDBACK FACTOR β, POLES, ZERO, Q-FACTOR, ω_{UGF} FOR LARGE, MODERATE AND SMALL C_LR_O CASES

TABLE V: NUMERICAL EXAMPLE FOR PM VERIFICATION USING THEORETICAL β_{PM} AND SIMULATED β_{sim}

TABLE VI: COMBINED β DESIGN INEQUALITIES USING β_{RH} AND β_{PM}

TABLE VII: PERFORMANCE COMPARISON WITH THE REPORTED OCL-LDO REGULATORS

TABLE A-I: ROUTH TABLE FOR A 5^{TH} ORDER POLYNOMIAL

TABLE A-II: ROUTH TABLE PARAMETER EXPANSION FOR THE WCF LDO REGULATOR CLOSED-LOOP TRANSFER FUNCTION IN (11)

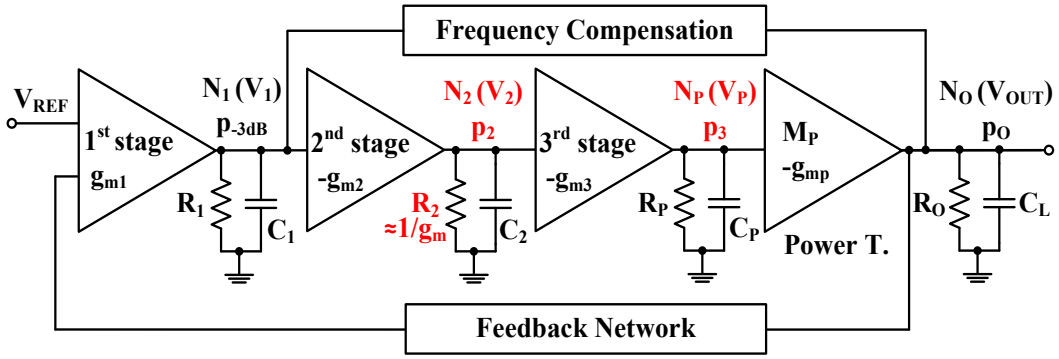

Fig. 1. Conventional multi-gain stages in a LDO regulator.

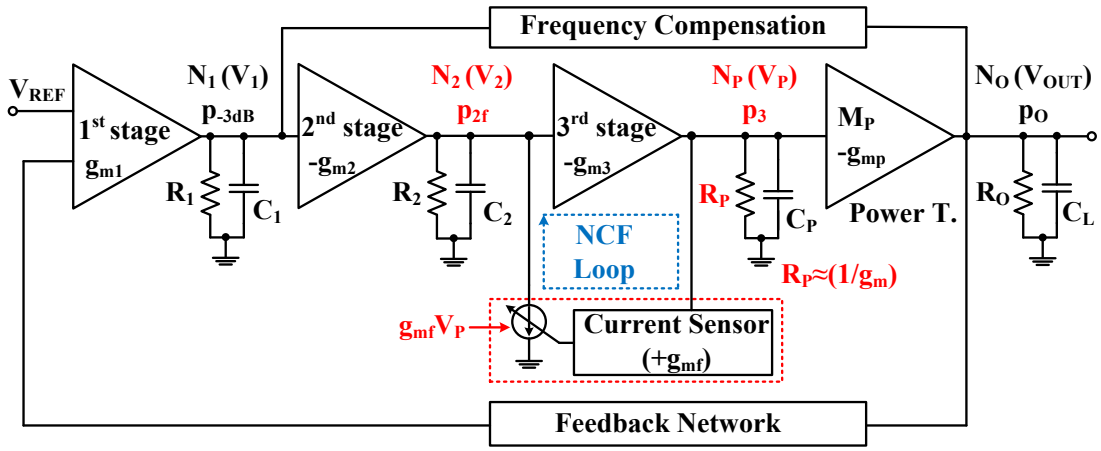

Fig. 2. Proposed Negative Current Feedback (NCF) topology embedded in multi-gain stages in a LDO regulator.

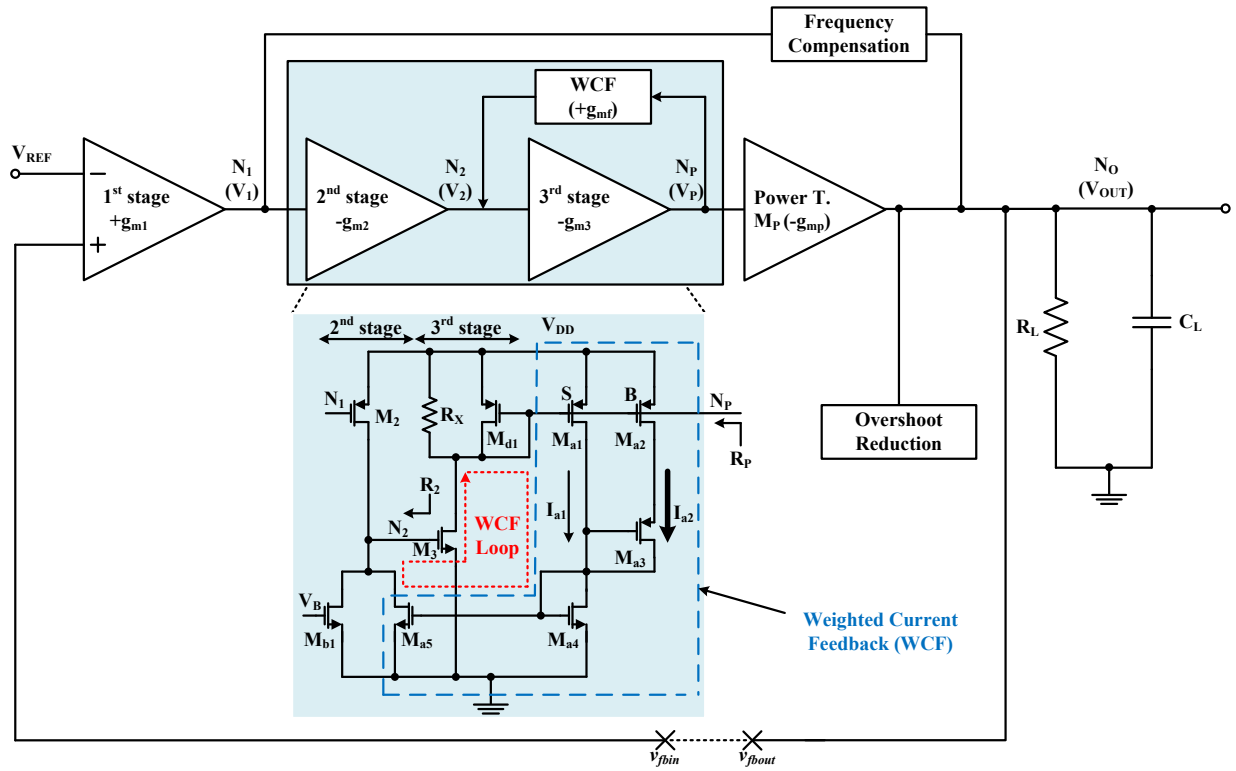

Fig. 3. A LDO regulator architecture using the WCF technique.

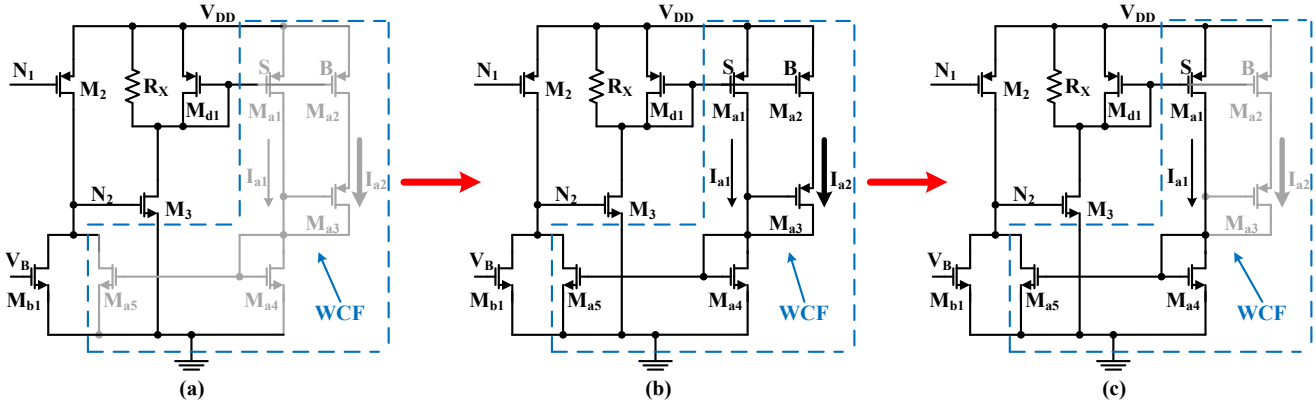

Fig. 4. Simplified schematic structure of 2nd, 3rd gain stages and WCF for (a) low I_L, (b) moderate I_L, and (c) high I_L.

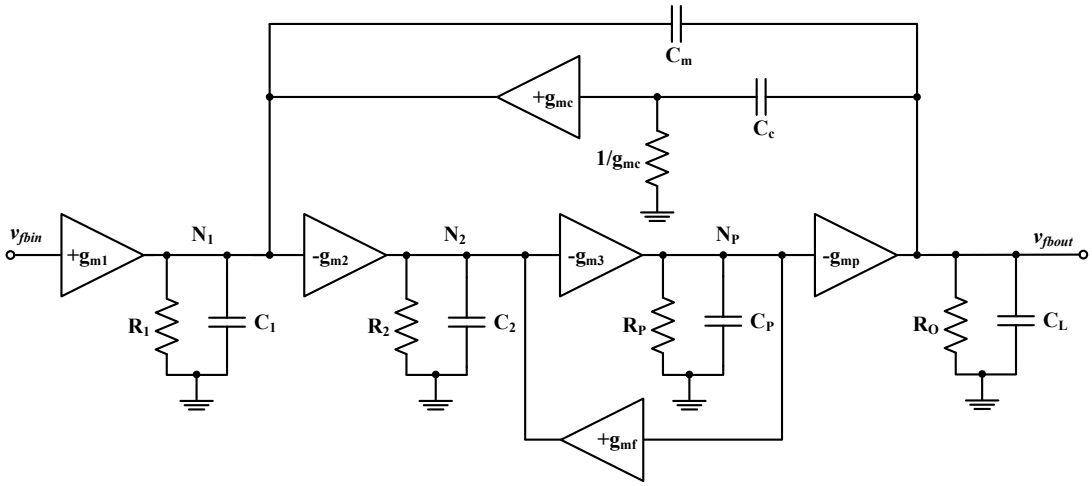

Fig. 5. Small-signal model of the WCF LDO regulator architecture.

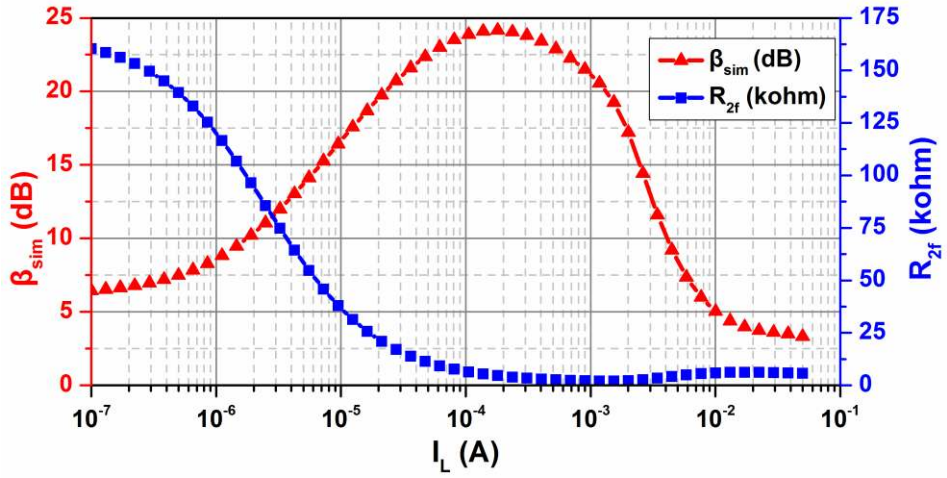

Fig. 6. Simulated β (β_{sim}) and R_{2f} at different I_L conditions.

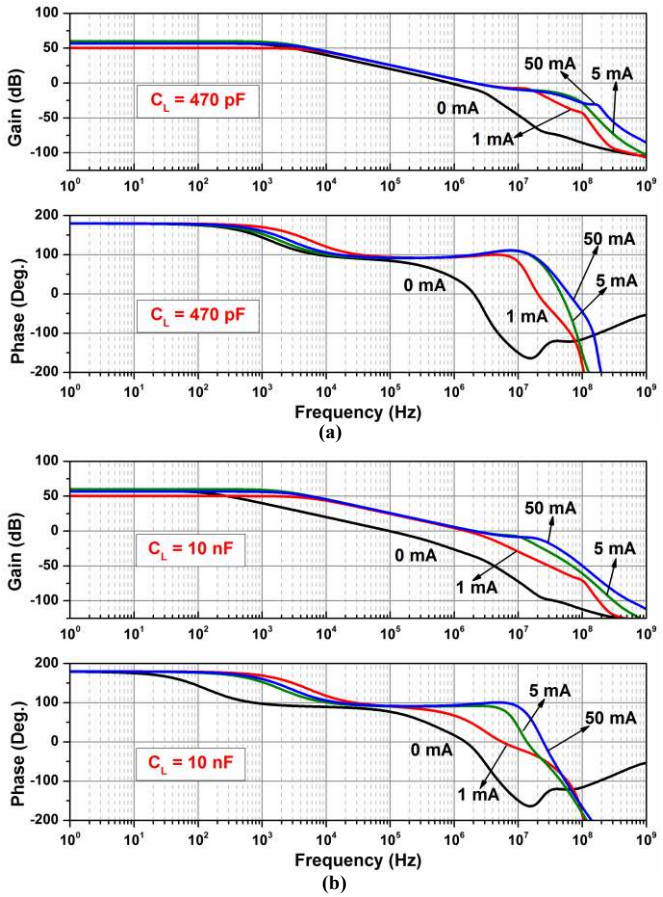

Fig. 7. Simulated open-loop gain and phase at different I_L for (a) C_L = 470 pF and (b) C_L = 10 nF with V_{DD} = 0.75 V.

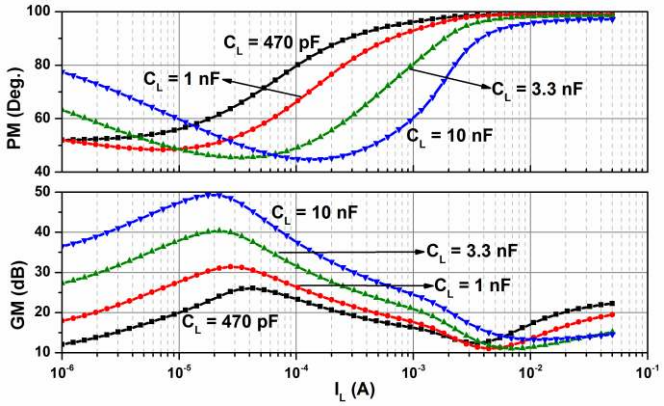

Fig. 8. Simulated phase margin (PM) and gain margin (GM) for C_L = 470 pF, 1 nF, 3.3 nF and 10 nF when sweeping I_L at V_{DD} = 0.75 V.

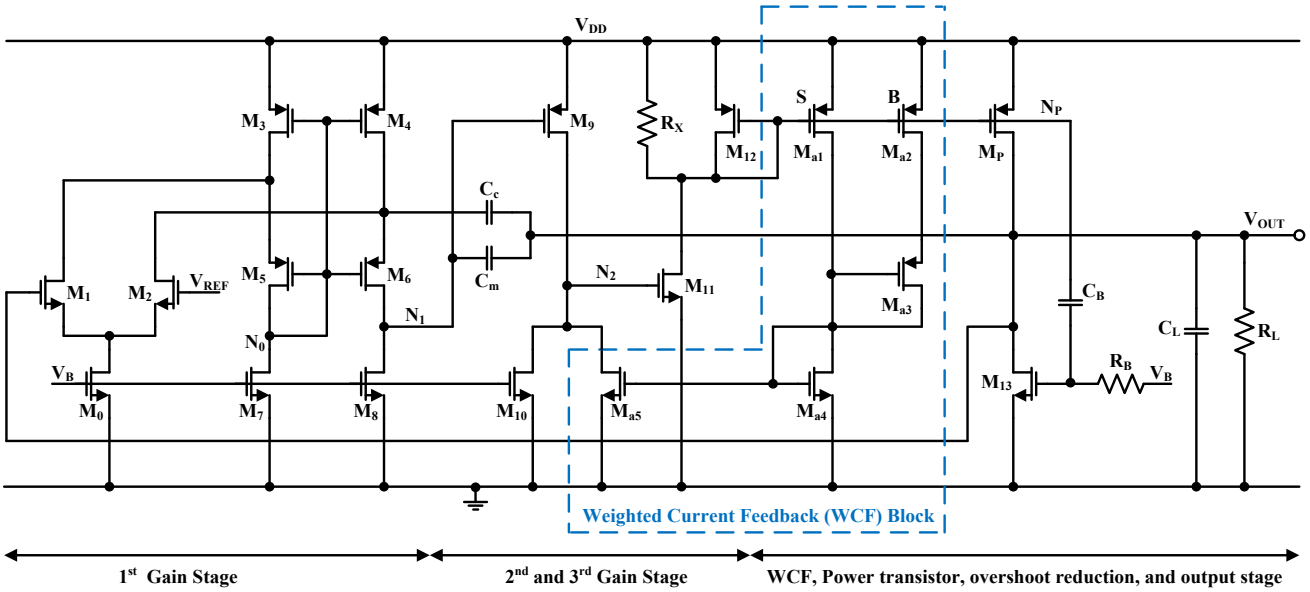

Fig. 9. Schematic of the WCF LDO regulator.

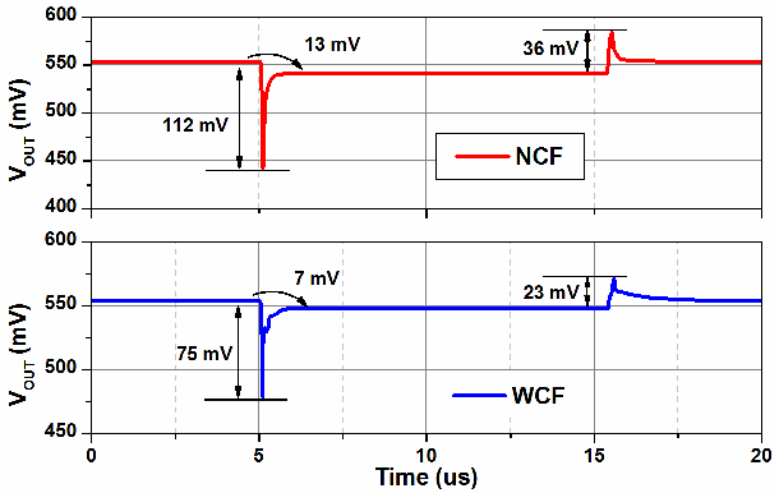

Fig. 10. Exemplary transient response of the LDO regulator with proposed NCF and WCF technique.

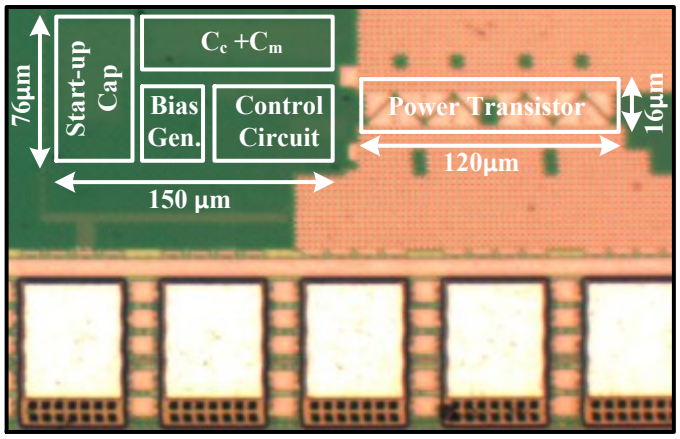

Fig. 11. Microphotograph of the WCF LDO regulator.

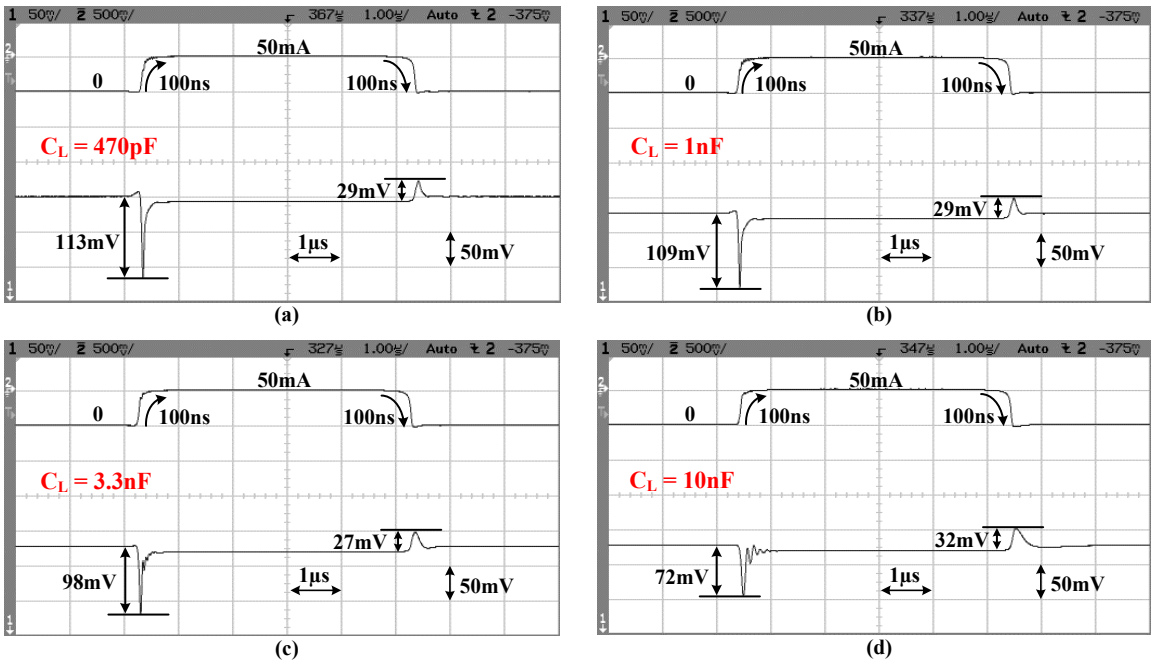

Fig. 12. Measured load transient responses with V_{DD} = 0.75 V, V_{OUT} = 0.55 V for (a) C_L = 470 pF, (b) C_L = 1 nF, (c) C_L = 3.3 nF and (d) C_L = 10 nF.

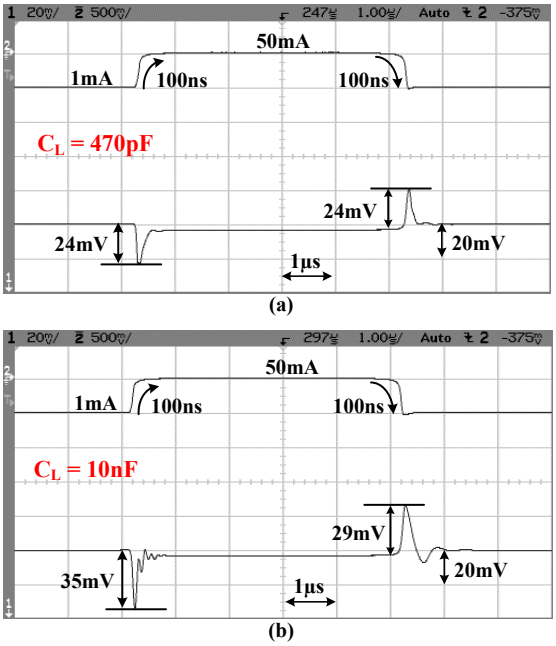

Fig. 13. Measured load transient responses at V_{DD} = 0.75 V with I_L switching from 1 mA to 50 mA (vice versa) for (a) C_L = 470 pF and (b) C_L = 10 nF.

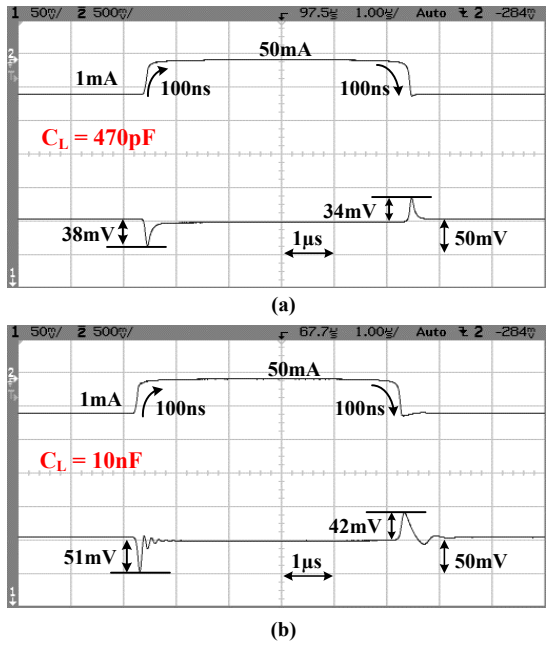

Fig. 14. Measured load transient responses at V_{DD} = 1.2 V with I_L switching from 1 mA to 50 mA (vice versa) for (a) C_L = 470 pF and (b) C_L = 10 nF.

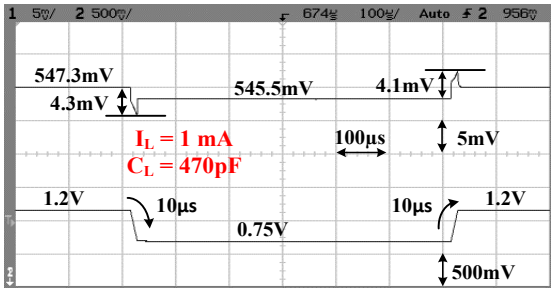

Fig. 15. Measured line transient response at I_L = 1mA and C_L = 470 pF.

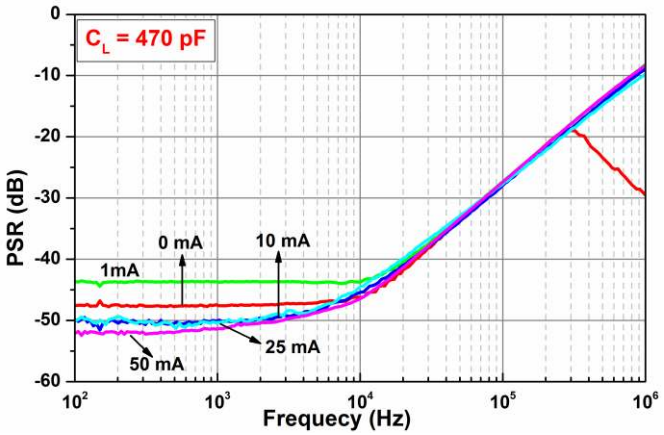

Fig. 16. Measured PSR at C_L = 470 pF for different I_L.

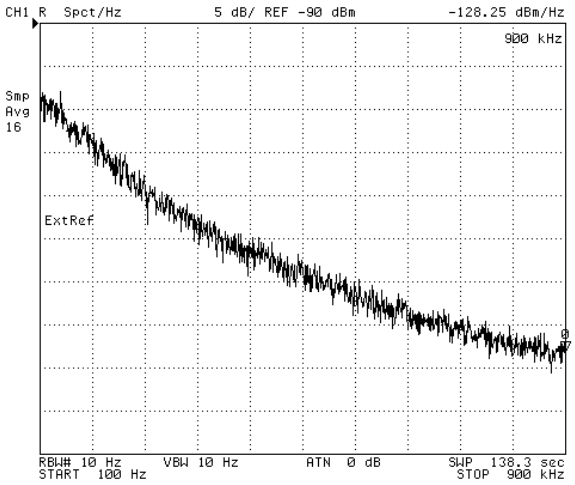

Fig. 17. Measured Output Noise at C_L = 470 pF with 0 mA I_L.

TABLE I
APPROXIMATED VARIABLES FROM a TO e FOR LARGE, MODERATE AND SMALL C_LR_O CASES

Parameter		Large C_LR_O	Moderate C_LR_O	Small C_LR_O
Var.	Eqn.			
a	(4)	C_LR_O	$2C_LR_O$	$C_cg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/\beta$
b	(5)	$C_mC_LR_1R_O$		$C_cC_mg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/(\beta g_{mc})$
c	(6)	$C_mC_LR_1R_O(C_c/g_{mc}+C_PR_P/\beta)$		$C_cC_mC_LR_1R_O/g_{mc}$
d	(7)	$C_cC_mC_PC_LR_1R_PR_O/(\beta g_{mc})$		
e	(8)	$C_cC_mC_2C_PC_LR_1R_2R_PR_O/(\beta g_{mc})$		

TABLE II
SUMMARY OF THE REQUIRED β_{RH} AT DIFFERENT I_L CONDITIONS TO MEET ROUTH–HURWITZ CRITERION

Parameter	Low I_L	Moderate I_L	High I_L
R_P, R_2	Large	Moderate	Small
g_{m2}, g_{m3}, g_{mp}	Small	Moderate	Large
β_{RH} design eqn.	(14) and (16)	(19)	(19)
β_{RH} value	Small	Large	Small

TABLE III
DESIGN PARAMETERS, STABILITY VERIFICATION USING THEORETICAL β_{RH} AND SIMULATED β_{sim}

Parameter	I_L = 0 mA		I_L = 1 mA		I_L = 50 mA	
g_{m1} (µS)	51		51		51	
g_{m2} (µS)	24		357		755	
g_{m3} (µS)	71		452		5290	
g_{mp} (µS)	31		2.03e4		3.1e5	
g_{mc} (µS)	131		131		131	
R_1 (kΩ)	617		617		617	
R_2 (kΩ)	342		22.2		6.46	
R_P (kΩ)	22.4		4.56		0.207	
C_c (pF)	3.5		3.5		3.5	
C_m (pF)	0.3		0.3		0.3	
C_2 (fF)	26		31		30	
C_p (pF)	2.58		3.22		3.09	
Theoretical β_{RH} and Simulated β_{sim}						
C_L	470 pF	10 nF	470 pF	10 nF	470 pF	10 nF
β_{RH} design eqn.	(16)	(14)	(19)	(19)	(19)	(19)
β_{RH} (dB)	−7.5	-29.4	19.5	19.1	0.6	-7.5
β_{sim} (dB)	6		22		3.3	
$\beta_{sim} > \beta_{RH}$ for stability	Yes		Yes		Yes	

TABLE IV
FEEDBACK FACTOR β, POLES, ZERO, Q-FACTOR, ω_{UGF} FOR LARGE, MODERATE AND SMALL C_LR_O CASES

Parameter	Case I: Large C_LR_O	Case II: Moderate C_LR_O	Case III: Small C_LR_O	
	Low I_L		Moderate I_L	High I_L
Feedback	Weak		Strong	Weak
β	$g_{m3}g_{mf}R_2R_P+1$			
A_{DC}	$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/\beta$			
z_1	$-g_{mc}/C_c$			
p_{-3dB}	$-1/(C_LR_O)$	$-1/(2C_LR_O)$	$-\beta/\left(C_cg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O\right)$	
$\lvert p_{2,3}\rvert_f$	$\sqrt{\beta g_{mc}/\left[(\beta C_c+C_Pg_{mc}R_P)C_mR_1\right]}$	$\sqrt{2\beta g_{mc}/\left[(\beta C_c+C_Pg_{mc}R_P)C_mR_1\right]}$	$\sqrt{g_{m2}g_{m3}g_{mp}g_{mc}R_2R_P/(\beta C_mC_L)}$	
$\lvert p_{4,5}\rvert_f$	$\sqrt{(\beta C_c+C_Pg_{mc}R_P)/(C_cC_2C_PR_2R_P)}$		$\sqrt{\beta/(C_2C_PR_2R_P)}$	
$Q_{\lvert p_{2,3}\rvert_f}$	$\sqrt{(\beta C_c+C_Pg_{mc}R_P)/(\beta C_mg_{mc}R_1)}$	$\sqrt{2(\beta C_c+C_Pg_{mc}R_P)/(\beta C_mg_{mc}R_1)}$	$\sqrt{\beta C_Lg_{mc}/\left(C_mg_{m2}g_{m3}g_{mp}R_2R_P\right)}$	
$Q_{\lvert p_{4,5}\rvert_f}$	$\sqrt{\left[(\beta C_c+C_Pg_{mc}R_P)C_2R_2\right]/(C_cC_PR_P)}$		$\sqrt{\beta C_2R_2/(C_PR_P)}$	
ω_{UGF}	$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_P/(\beta C_L)$	$g_{m1}/(2C_c)$	g_{m1}/C_c	

TABLE V
NUMERICAL EXAMPLE FOR PM VERIFICATION USING THEORETICAL β_{PM} AND SIMULATED β_{sim}

Parameter	Large C_LR_O	Moderate C_LR_O	Small C_LR_O
C_L	3.3 nF	470 pF	10 nF
I_L	0 mA	0 mA	50 mA
β_{PM} Design Eqn.	(23)	(24)	(25)
β_{PM} (dB)	-2.9	3.3	50.6
β_{sim} (dB)	6	6	3.3
Criterion For 45° PM	$\beta_{sim}\geq\beta_{PM}$	$\beta_{sim}\geq\beta_{PM}$	$\beta_{sim}\leq\beta_{PM}$
Meet Criterion	Yes	Yes	Yes
Simulated PM	63°	52°	97°

TABLE VI
COMBINED β DESIGN INEQUALITIES USING β_{RH} AND β_{PM}

Case	β
I	$\beta\geq C_mg_{m1}g_{m2}g_{m3}g_{mp}R_1^2R_2R_P/C_L$
II	$\left[\beta>C_Pg_{m1}R_P/(2C_c)\right]\&\left[\beta\geq\dfrac{C_mC_Pg_{m1}^2R_1R_P}{8C_c^2-(2+g_{m1}/g_{mc})C_mC_cg_{m1}R_1}\right]$
III	$\dfrac{C_2g_{m2}g_{m3}g_{mp}R_2^2R_P}{C_L}+\left(1+\dfrac{g_{m1}}{g_{mc}}\right)\dfrac{C_Pg_{mc}R_P}{C_m}<\beta\leq\dfrac{C_c^2g_{mc}g_{m2}g_{m3}g_{mp}R_2R_P}{C_mC_Lg_{m1}^2}$

Case I: Large C_LR_O using (23). Case II: Moderate C_LR_O using (16) and (24).
Case III: Small C_LR_O using (19) and (25).

TABLE VII
PERFORMANCE COMPARISON WITH THE REPORTED OCL-LDO REGULATORS

Parameter	[8]	[11]	[13]	[14]	[16]	[17]	[18]	[19]	[20]	[21]	This Work	
Year	2005	2007	2010	2010	2012	2012	2012	2012	2013	2013	**2014**	
Technology (μm)	0.09	0.35	0.35	0.09	0.09	0.35	0.35	0.35	0.065	0.11	**0.065**	
Chip Area (mm^2)	0.098	0.12	0.155	0.019	0.005#	0.0987	0.064	0.4	0.017	0.21	**0.0133**	
V_{IN} (V)	1.2	3	0.95-1.4	0.75-1.2	1.2	1.2	2.5-4	1.2-1.5	1.2	1.8-3.8	**0.75-1.2**	
V_{OUT} (V)	0.9	2.8	0.7-1.2	0.5-1	1	1	2.35	1	1	1.6-3.6	**0.55**	
Dropout Voltage (mV)	300	200	200	200	200	200	150	200	200	200	**200**	
I_Q (μA)	6000	65	43	8	408	28-380.1	7	45	0.9-82.4	41.5	**15.9* - 487**	
I_{OUT} (max) (mA)	100	50	100	100	100	100	100	50	100	200	**50**	
Total On-Chip Cap. (pF)	600	21	6	7	1.8	10	7.5	41	4.5	43.2	**4.1**	
Load Cap. Range (F)	600p	0-100p	0, 100p, 1n	0-50p	0-1n	0-100p	0-100p	0-1n	0-100p	40p	**470p-10n**	
Line Reg. (mV/V)	N/A	23	N/A	3.78	4.3	0.39	1	N/A	4.7	8.9	**4**	
Load Reg. (mV/mA)	1.8	0.56	0.4	0.1	0.003	0.0782	0.08	N/A	0.3	0.108	**0.18**	
PSR @1kHz (dB)	N/A	-57	N/A	-44	-56	-49.8	N/A	N/A	-58(@10kHz)	N/A	**-51**	
Settling Time (μs)	N/A	15	3	5	N/A	N/A	~0.15	~4	6	0.65	**0.25**	
$I_{L(min)}$ (mA)†	0	0	1	3	1	0	0.05	1	0	0.5	**0**	**1**
ΔI_{OUT} (mA)	100	50	99	97	100	100	99.95	49	100	199.5	**50**	**49**
ΔV_{OUT} (mV)	90	90	70	114	35	105	243	70	68.8	385	**113**	**24**
Edge Time (μs)	0.0001	1	1	0.1	0.01	1	0.5	1	300	0.5	**0.1**	**0.1**
Edge Time Ratio K	1	10000	10000	1000	100	10000	5000	10000	3000	5000	**1000**	**1000**
FOM	0.0054	1.17	0.304	0.0094	0.014	0.294	0.085	0.643	0.0019	0.4	**0.036**	**0.0079**

* Quiescent current includes the current consumption of bias circuit. † The minimum I_L used to test the transient performance. # Estimated area.

TABLE A-I
ROUTH TABLE FOR A 5TH ORDER POLYNOMIAL

s^5	a_5	a_3	a_1
s^4	a_4	a_2	a_0
s^3	$b_1 = (a_3a_4 - a_2a_5)/a_4$	$b_2 = (a_1a_4 - a_0a_5)/a_4$	0
s^2	$c_1 = (a_2b_1 - a_4b_2)/b_1$	$c_2 = a_0$	0
s^1	$d_1 = (b_2c_1 - a_0b_1)/c_1$	0	0
s^0	$e_1 = a_0$	0	0

TABLE A-II

ROUTH TABLE PARAMETER EXPANSION FOR THE WCF LDO REGULATOR CLOSED-LOOP TRANSFER FUNCTION IN (11)

Par.	Case I (Large $C_L R_O$)	Case II (Moderate $C_L R_O$)	Case III (Small $C_L R_O$)
a_0	$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/\beta$		$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/\beta$
a_1	C_LR_O	$(2+g_{m1}/g_{mc})C_LR_O$	$(1+g_{m1}/g_{mc})C_cg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/\beta$
a_2	$C_mC_LR_1R_O$		$C_cC_mg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/(\beta g_{mc})$
a_3	$C_mC_LR_1R_O(C_c/g_{mc}+C_PR_P/\beta)$		$C_cC_mC_LR_1R_O/g_{mc}$
a_4	$C_cC_mC_PC_LR_1R_PR_O/(\beta g_{mc})$		$C_cC_mC_PC_LR_1R_PR_O/(\beta g_{mc})$
a_5	$C_cC_mC_2C_PC_LR_1R_2R_PR_O/(\beta g_{mc})$		$C_cC_mC_2C_PC_LR_1R_2R_PR_O/(\beta g_{mc})$
b_1	$C_mC_LR_1R_O(C_c/g_{mc}+C_PR_P/\beta)$		$\left(C_L-C_2\,g_{m2}g_{m3}g_{mp}R_2^2R_P/\beta\right)C_cC_mR_1R_O/g_{mc}$
b_2	C_LR_O	$(2+g_{m1}/g_{mc})C_LR_O$	$(1+g_{m1}/g_{mc})C_cg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/\beta$
c_1	$C_mC_LR_1R_O$		$\left[\chi C_m/g_{mc}-(1+g_{m1}/g_{mc})C_PC_LR_P/\beta\right]C_cg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O/(\beta\chi)$ *
c_2	a_0		a_0
d_1	$C_LR_O-\dfrac{C_cg_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_PR_O}{\beta g_{mc}}$	$C_LR_O\left[2-\dfrac{C_PR_Pg_{m1}}{\beta C_c}\right]$	$\dfrac{\left\{\left(1+\dfrac{g_{m1}}{g_{mc}}\right)\left[\chi\dfrac{C_m}{g_{mc}}-\left(1+\dfrac{g_{m1}}{g_{mc}}\right)\dfrac{C_PC_LR_P}{\beta}\right]C_cg_{m2}g_{m3}g_{mp}R_1R_2R_PR_O\right\}\Big/\beta-\dfrac{\chi^2C_mg_{m1}R_1R_O}{g_{mc}}}{\chi C_m/g_{mc}-(1+g_{m1}/g_{mc})C_PC_LR_P/\beta}$ *

* $\chi = C_L - C_2 g_{m2}g_{m3}g_{mp}R_2^2R_P/\beta$