A Local Oscillator for Chip-Scale Atomic Clocks at NIST

A. Brannon, M. Janković, J. Breitbarth, Z. Popović
Electrical Engineering
University of Colorado at Boulder
Boulder, CO, USA
alan.brannon@colorado.edu

V. Gerginov, V. Shah, S. Knappe, L. Hollberg, J. Kitching
Time and Frequency Division
National Institute of Standards and Technology
Boulder, CO, USA

***Abstract*—We describe the first local oscillator (LO) that demonstrates viability in terms of performance, size, and power, for chip-scale atomic clocks (CSAC) and has been integrated with the physics package at the National Institute of Standards and Technology (NIST) in Boulder, CO. This voltage-controlled oscillator (VCO) achieves the lowest combined size, DC power consumption, phase noise, and thermal frequency drift among those previously reported, while achieving a tuning range large enough to compensate for part tolerances but small enough to permit precision locking to an atomic resonance. We discuss the design of the LO and the integration with the NIST physics package.**

I. Introduction

In recent years, chip-scale atomic clocks have progressed from concept [1] to working subsystems [2-6] and prototypes [7]. The goal, specified by the Defense Advanced Research Projects Agency (DARPA) has been to create a frequency reference that is less than 1 cm^3 in size, that achieves a frequency instability below 10^{-11} at one hour of integration, and that operates on less than 30 mW of power. This would approach the stability of commercially-available compact atomic clocks while providing improvement by two orders of magnitude in both size and power consumption. The first demonstrations of the viability of chip-scale atomic clock technology [4,5] achieved the size and stability goals but required more than 100 mW of power to operate since they were not designed for low power dissipation. Since then, physics packages requiring less than 10 mW have been demonstrated [6] as have local oscillators (LO) requiring only 3 mW of power [2]. Combined, these results show that meeting the power specification for the CSAC project is realizable while maintaining the size and stability limits. We discuss the design of this VCO at the component level and then at the circuit level using a combination of the virtual-ground technique [8] and harmonic balance analysis. Measured data show phase noise better than -100 dBc/Hz at a 10 kHz offset, power consumption less than 5 mW, thermal drift near ±2 ppm/K at room temperature, and vibration sensitivity near 0.2 ppm/g ($g \approx 9.81$ m/s^2). We discuss integrating the LO with the NIST physics package, including the unique challenges presented by the combination of driving a vertical cavity surface-emitting laser (VCSEL) load, providing a coupled and stabilized output, and maintaining small size.

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II. Design

A. Specifications

The goals we have identified for the VCO of a chip-scale atomic clock can be summarized as follows:

- Expected phase noise better than –25 dBc/Hz at 100 Hz offset (calculated from the total package fractional frequency instability requirement $6x10^{-10}$ for a 1 second integration time);
- Output power at –6 dBm when assuming the VCSEL presents a 50-Ω load (as this is not the case, simply matching for the load will allow even lower power output);
- Small footprint of <1 cm^2, fabricated on one side of a thin substrate;
- Low DC power consumption of at most 10 mW;
- Low thermal frequency drift on the order of ±10 ppm/K;
- A frequency tuning range that is as small as possible but large enough to compensate for thermal drift over large temperature ranges and for manufacturing tolerances;
- Low-cost manufacturability for high yield.

B. Component-Level Design

The frequency-determining element is a ceramic-filled quarterwave coaxial resonator that is surface-mountable and

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readily manufactured for precision frequency tolerances. The high dielectric permittivity of 37.4 permits reduced size with an acceptable tradeoff in quality factor. The measured unloaded Q is 210 at 3.4 GHz [2].

Because a transistor's unity gain frequency f_T decreases as collector current decreases, our device possesses a generally high f_T. However, the value is roughly twice the operating frequency at the operating point of 1 mA collector current. This is done to achieve high enough loop gain to permit oscillation but to prevent the transistor from strong compression and to reduce oscillations at higher harmonics. Additionally, the transistor has a large collector area, permitting a high maximum collector current, which reduces shot noise due to current crowding. Finally, a silicon-based bipolar junction transistor (BJT) is chosen in a small package to present a low flicker noise corner and a small physical size.

A narrow tuning range near 3 MHz permits corrections for part tolerances and temperature changes. It is accomplished with an abrupt-junction varactor with low equivalent series resistance (ESR), though theory and simulations show only a weak dependence of phase noise on varactor ESR. This is because the varactor is weakly coupled to the circuit by a small series capacitor, reducing the equivalent series capacitance in the varactor Q formula,

$$Q = 1/\omega CR, \qquad (1)$$

where ω is the operating frequency in radians per second, C is the series capacitance and R is the ESR. Since both C and R can depend on operating frequency, and typical varactors are specified at 50 MHz, we modified Stauffer's approach [9] and developed an equivalent circuit model for the varactor at 3.4 GHz [10]. Since the load of the oscillator is the vertical-cavity surface-emitting laser (VCSEL) on the physics package, we measured the laser's impedance at 3.4 GHz under normal operating conditions, described in [10]. Finally, the other passive devices (capacitors and inductors) are chosen for low ESR, and packages are small-sized 0201 components to reduce the overall size.

C. Circuit-Level Design

First, to gain an intuition for the overall circuit operation, we employ the "transmission analysis with virtual ground" technique developed by Alechno [8]. With this technique, the circuit at the top of Fig. 1 is redrawn as an idealized gain block in series with an idealized feedback block. The feedback loop is then broken at a point shown at the bottom of Fig. 1. The actual transmission through the break point is modeled as follows: To allow maximum power insertion into the loop at port 1, the impedance of this port is set equal to the complex conjugate of the device input impedance for our operating conditions. The reflection between the resonator and the BJT is modeled at port 2 by setting this port's impedance equal to the input impedance of the transistor. Our use of this technique does not take into consideration the feedback due to package parasitics and bilateral device feedback, nor does it model the reflections at or transmission through the ground plane since it is treated as a single node rather than a structure with physical properties. However, this technique is a useful alternative to harmonic balance analysis because the general behavior of the amplitude and phase in the feedback loop is observable. Since some post-production tuning is expected whenever there is a very narrow specification on the design frequency, there is benefit in modeling the effect of individual circuit components on the feedback loop. Finally, a standard harmonic balance analysis is performed on the circuit at the top of Fig. 1 to simulate the phase noise, output power levels and harmonics. As shown in [2], for a simulated DC bias of 1.3 V, a simulated output power of -5 dBm is obtained. Measured results in Table I show good agreement since 1.3 V bias yields -5 dBm with a DC power consumption of 2.8 mW.

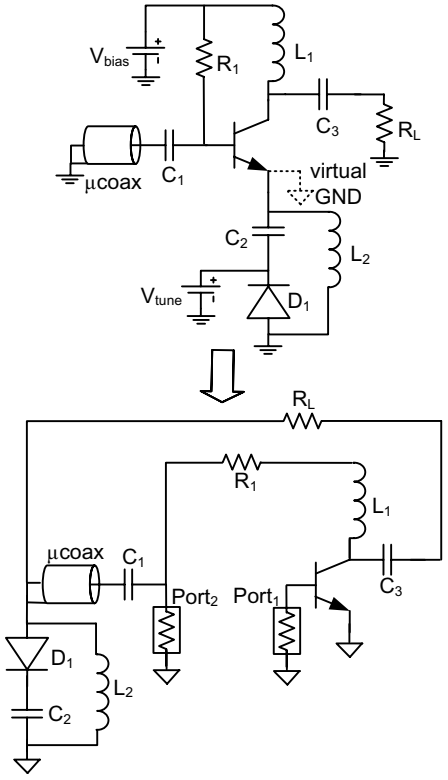

Figure 1. Transformation of the VCO for transmission analysis. A virtual ground is inserted and the circuit is redrawn showing an idealized gain block with an idealized passive feedback network. The simulated magnitude and phase change is observed from port 1 to port 2.

TABLE I. MEASURED DC BIAS POWER AND RF OUTPUT POWER

Bias (V)	DC Input (mW)	RF Output (dBm)
1.5	4.5	-2
1.3	2.8	-5
1.2	2.1	-6
1.0	0.7	-16

III. MEASURED RESULTS

A. Phase Noise

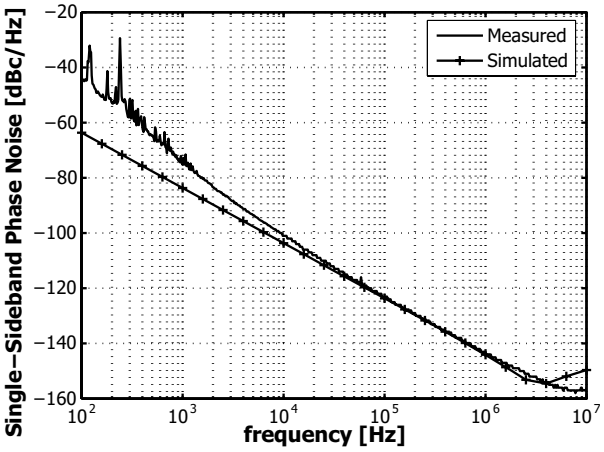

Figure 2. Measured and simulated phase noise for the 3.4 GHz LO. The data were only measured to a maximum offset frequency of 100kHz. The device model did not include the flicker corner, resulting in the disagreement at small offset frequencies.

The phase noise was measured using the discriminator method [11] with a 125 ns low-loss coaxial delay line. The noise floor of the measurement was 15 dB below the measured results presented. The measured and simulated single-sideband phase noises are shown in Fig. 2 as a function of offset frequency from the carrier. Good agreement between simulation and measurement is shown except for small offset frequencies because the transistor model did not include flicker noise. For large offset frequencies, an unexplained rise in simulated phase noise at the noise floor is shown. The measured phase noise is -102 dBc/Hz at 10 kHz offset and -45 dBc/Hz at 100 Hz, well below the goal of -25 dBc/Hz at 100 Hz.

B. Thermal Drift

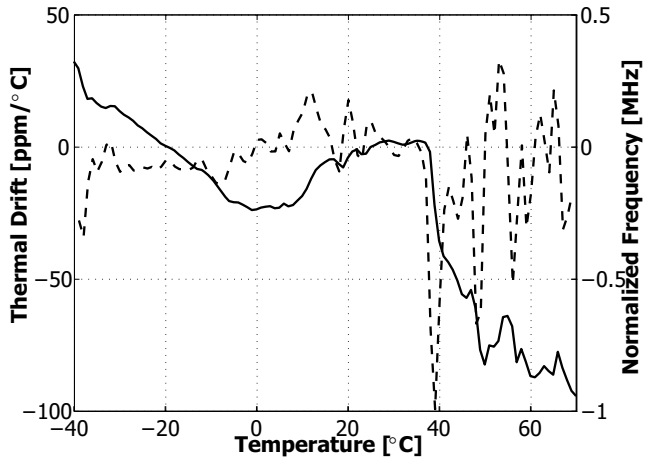

Figure 3. Measured frequency drift with temperature.

An attempt was made to compensate for temperature-related drift due to resonator expansion and the temperature-variable phase shift of the transistor [10]. The ceramic filling inside the resonator is chosen to have a negative phase shift of the same magnitude as the contribution from the transistor. The oscillator was placed in a temperature-controlled oven and ramped over temperature from -40 °C to +70 °C and the measured frequency drift versus temperature is shown in Fig. 3. The best stability is achieved near and below room temperature, with generally better than ±20 ppm/K below 30 °C.

C. Vibration Sensitivity

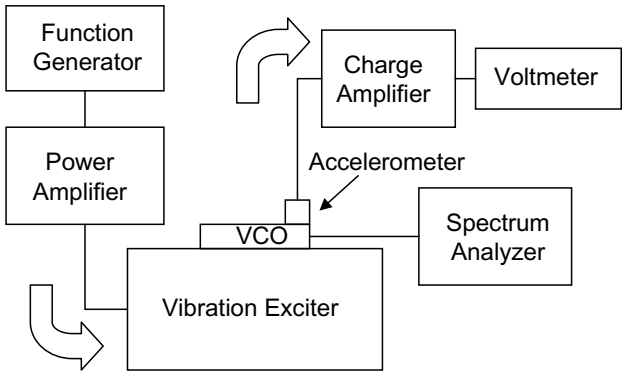

Figure 4. Diagram showing the setup for measuring vibration sensitivity.

Two VCOs of the same design were affixed to a vibration exciter and an accelerometer was bolted to the circuit substrates as shown in Fig. 4. The mechanically-generated sidebands were observed with a spectrum analyzer and this frequency shift was compared to the measured acceleration. The measured vibration sensitivities at a vibration frequency of 10 kHz were 201 ppb/g and 347 ppb/g for the respective VCOs. At lower vibration frequencies, the oscillators appeared less sensitive but the frequency change was more difficult to measure, likely due to insufficient electrical shielding of the oscillator against radiated fields and the movement of DC bias and tune cables.

IV. BOARD-LEVEL INTEGRATION

The VCO has been integrated on a board with a NIST physics package [5] as shown in Fig. 5. The physics package is based on ^{87}Rb contained in a micromachined cell and excited by a vertical cavity surface-emitting laser stabilized at 795 nm. The physics package has an intrinsic stability of $1\text{x}10^{-10}$ at one second, as measured by locking a large synthesizer to the physics package resonance. The inputs to the integrated VCO and physics package are DC bias and tune for the oscillator, laser current bias, and currents to indium-tin-oxide (ITO) heaters on the physics package. The outputs are a stabilized 3.4173 GHz signal, photodetector current, and temperature sense voltages for the rubidium vapor cell and the VCSEL. Control electronics for temperature stabilization and locking the VCO and the

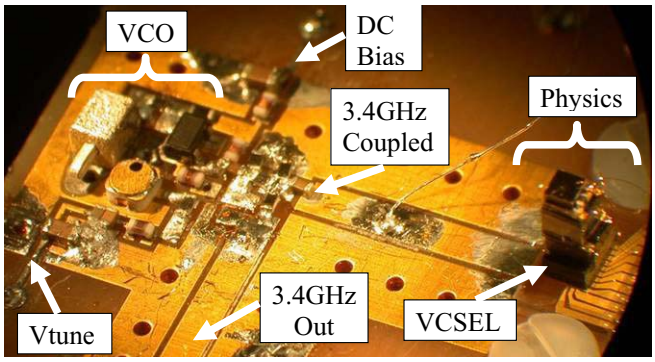

Figure 7. Photograph of the VCO integrated with the NIST physics package. Inputs are DC bias and tune voltage for the VCO and laser bias, photodetector bias, and heater current for the physics package. Outputs are stabilized 3.4 GHz, photodetector signal, and thermal sensor voltage.

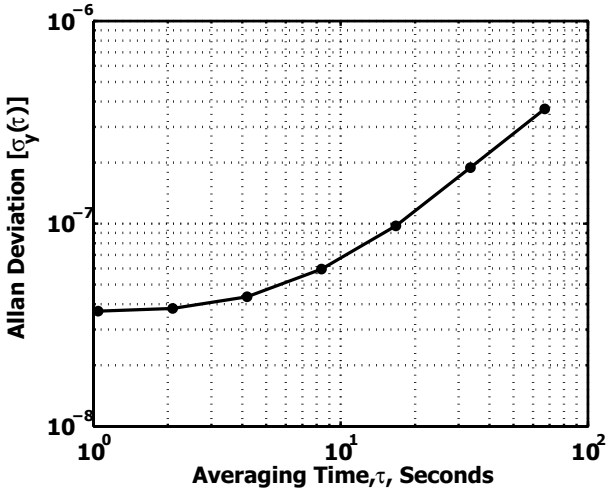

Figure 5. Measured instability of the free-running VCO.

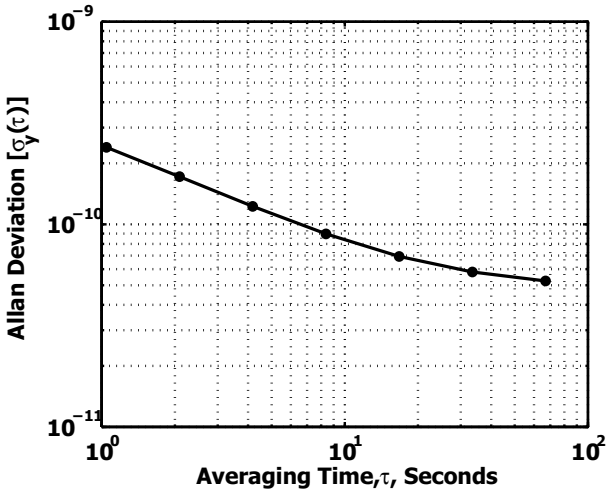

Figure 6. Measured instability of the VCO locked to the physics package.

VCSEL to the atomic resonances are presently external and attempts are being made to integrate these also. The VCO modulates the VCSEL sufficiently with DC power consumption between 2 mW and 3 mW. It is sufficiently stable to meet the required frequency stability of $6\times10^{-10} / \tau^{1/2}$ when locked to the atomic coherent population trapping (CPT) resonance. This lock is achieved with a 3 kHz modulation on the VCO that is fed through a lock-in amplifier and servo. As shown in Fig. 5, the output matching of the oscillator is achieved with a simple lumped-element 6 dB attenuator. This, combined with the losses from long bondwires to the VCSEL and losses through the laser bias wire, results in an inefficient but manageable design. An impedance-matched output with shorter bondwires and a bias tee of higher-impedance for the laser current should lead to a more efficient design. Fig. 6 shows the frequency instability of the oscillator while free-running and Fig. 7 shows the frequency instability of the oscillator while locked to the atomic CPT resonance of the integrated physics package. The short-term goals are met and exceeded with the Allan Deviation of 2.4×10^{-10} at one second of integration time. For longer measurements (not shown), there is a drift mostly due to temperature changes of the laser and the atoms. Methods are being investigated to improve this for greater long-term stability [13,14].

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