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A Low Complexity Algorithm for Efficiency Optimization of Dual Active Bridge Converters

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ABSTRACT This paper proposes a triple phase shift modulation (TPS) with an optimization technique that aims at maximizing the efficiency of the dual active bridge converter. Such a converter is often used to interface renewable or energy storage systems in smart dc power systems, where loss minimization via TPS is crucial, especially at light-load conditions. In this paper, favorable modulation parameters are found first, aiming at minimum rms currents and zero voltage switching, by considering only some fundamental converter parameters, namely, the input and output voltages, the transformer ratio, and the leakage inductance. Then, on the basis of the closed-form analytical description of the converter behavior over the determined modulation patterns, trajectories in the modulation planes that are capable of improving the total efficiency are identified. It is shown that such trajectories lead to close-to-optimal efficiency operation, which can be exploited to implement fast perturb-and-observe methods requiring just minimal converter parameters knowledge. The results are verified experimentally on a 1.5-kW prototype. It is shown that the proposed approach achieves close-to-optimal efficiency operation under different input voltages, being the error with respect to the measured optimal points obtained by a brute-force approach lower than about 0.2%.

INDEX TERMS Dual active bridge (DAB), light-load operation, maximum efficiency point identification, TPS optimization, zero voltage switching (ZVS).

I. INTRODUCTION

DC-DC electronic power converter (EPC) are widely used in modern energy processing applications. As represented in Fig. 1, EPC are required to connect energy storage systems and renewable sources to distribution busses operating at different voltage levels in stationary microgrids [1] as well as in electrified vehicles [2], [3]. As a crucial technology in such applications, there is steady motivation in strengthening their valuable merits. Among these, efficiency is one of the most prominent, attracting notable research efforts on optimized design and control [4]–[8]. Efficiency is particularly important in battery-powered applications to minimize unnecessary losses and maximize autonomy. In applications operating at low power levels for significant time, which may be common, for example, in residential dc-microgrids, maximum light-load efficiency is essential indeed. Fig. 1 reports an example of this latter application where a common dc-bus voltage is present and regulated to a relatively high voltage level (e.g., 400 V) by a grid-interface converter while EPCs interface resources, like batteries, operating at lower voltages (e.g., 40-60 V) [9].

The literature reports various topologies with different characteristics in terms of power level, cost, reliability, efficiency, power density, weight, integration, and complexity [10]. Among these, the isolated dual active bridge (DAB) is often considered for its several merits [11], [12]. This topology is specifically considered in this work with the goal of efficiency maximization.

Efficiency is influenced by a number of design and operation parameters. When considering modulation schemes, a couple of important issues are the high conduction loss, especially when operating at input-output voltage ratios

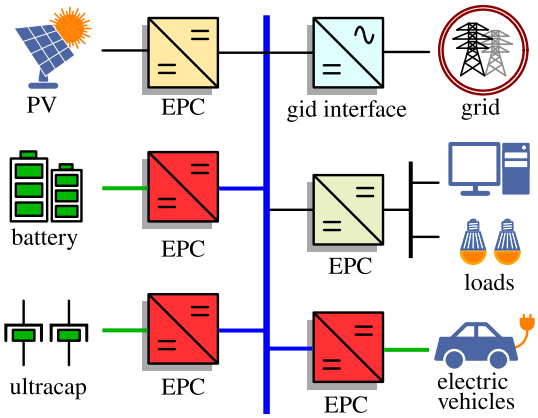


FIGURE 1. Typical scenario with bidirectional EPCs highlighted in red. High-voltage (e.g., 400 V) dc-bus displayed in blue, low-voltage lines (e.g., 40–60 V) in green.

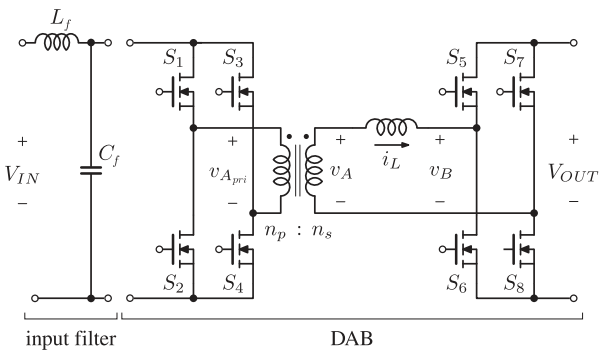


FIGURE 2. Dual active bridge (DAB) converter topology.

different from the transformer turns ratio [13], [14], and the high switching loss in absence of zero voltage switching (ZVS) turn-on, as typically happens at light-load [15], [16]. Several modulation strategies have been presented in the literature to cope with these issues [17]–[19]. The phase shift modulation (PSM) [12] is a simple modulation technique to control the power transfer in the DAB topology. In addition, PSM can achieve optimal operation in some specific operating conditions, but it gives low efficiency in generic operating conditions, especially at light-load [13]. Efficiency gains can be achieved by exploiting the degrees of freedom available in the modulation. An example is the trapezoidal modulation, which allows low rms currents and lower switching losses as compared to PSM. In [15], trapezoidal modulation is combined with appropriate transformer magnetizing current design, which commonly gives negligible contribution at the transformer ports, in order to extend ZVS to all the switches of the topology. Other advanced modulation techniques exploiting the available degrees of freedom of the topology are, for example, the extended phase shift modulation (EPS) [20], the dual phase shift modulation (DPS) [21], and the triple phase shift (TPS) [22]. The TPS is a general modulation scheme and it is considered herein. TPS strategies for conduction loss and efficiency optimization have been proposed, for example, in [4], [5], [23], [24]. These modulations make use of accurate models of the converter operation and loss contributions [25], which may be not always easily retrievable and deployable. Complexity can be reduced by considering rms current minimization only and neglecting ZVS operation, facilitating the real-time computation of TPS modulation maps, as shown in [26], [27], which, on the other hand, unfavorably affect light-load efficiency.

The mentioned efficiency improvements are obtained herein by a TPS approach and an efficiency maximization procedure, called maximum efficiency point identification (MEPI) algorithm, that aim at optimal operating conditions especially at light-load. This is achieved by topology analysis and by using simple models and basic information on the converter parameters. The efficiency maximization procedure can be performed directly on the converter and allows to slide on the modulation plane toward operating regions of maximum efficiency. Unlike approaches based only on off-line information on the converter [4], [5], [23], [24], [26]–[29], a perturb and observe approach for efficiency maximization is proposed herein. Remarkably, it differs from other on-line approaches based on generic optimization methods like [30], [31] that do not exploit any knowledge on the converter operation. Indeed, the MEPI algorithm optimization is performed via an on-line procedure that adjusts the converter modulation parameters along optimization trajectories identified by the presented converter analysis using just elemental converter information (i.e., transformer turns ratio) and measurements on the converter input and output ports. Optimization by the proposed MEPI algorithm is achieved regardless of the knowledge of other converter parameters, which is a feature linked to closed-loop approaches, and exploiting simple trajectories in the modulation plane, which are identified on the basis of the presented topological analyses.

In the reminder of the paper, Section II introduces the converter topology and sets preliminary losses considerations. Section III reports the procedure used for converter analysis in the different operating modes, which is then exploited in the TPS scheme presented in Section IV for light-load loss mitigation. The switching patterns identified by the TPS scheme are analyzed in Section V. On the basis of the analyses, Section VI presents the proposed MEPI algorithm. Finally, Section VII reports experimental results considering a 1.5-kW DAB converter prototype. Section VIII concludes the paper.

II. PRELIMINARY CONSIDERATIONS

A. DUAL ACTIVE BRIDGE TOPOLOGY

The basic DAB topology is schematically displayed in Fig. 2. It consists of a high-frequency transformer and two full bridges connected at the primary, low-voltage side and at the secondary, high-voltage side. The transformer allows galvanic isolation and step-up/down ratios between the two sides; its leakage inductance, possibly combined with an additional external inductor, is exploited as energy transfer element.

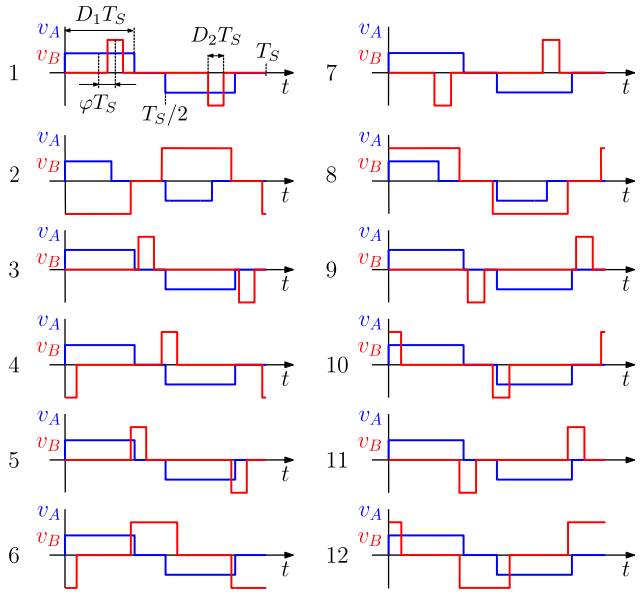


FIGURE 3. Possible switching patterns for v_A and v_B using TPS.

The two bridges can be driven to impose three-level voltage waveforms v_A and v_B to achieve desired power transfer. Fig. 3 displays the possible switching patterns, categorized by the order of the switching edges of voltages v_A and v_B (see Fig. 2) [22], [32]. Such patterns are referred to as *cases* herein. The sequences can be distinguished by the three parameters highlighted for the first pattern visible in Fig. 3, namely, the pulse duration D_1 and D_2 and the phase shift φ. By referring to the PSM, D_1, D_2 are equal to a half while φ is used to regulate the power transfer.

B. LOSS CONTRIBUTIONS

Various kinds of losses affect total efficiency. The two main sources of loss considered herein to devise an efficient TPS technique are the conduction losses [13], [25] and the switching losses [33].

The conduction loss can be modeled as:

$$P_{cond} = 2R_{on,LV}\left(n I_L^{\mathrm{RMS}}\right)^2 + 2R_{on,HV} I_L^{\mathrm{RMS}\,2} + R_{pri}\left(n I_L^{\mathrm{RMS}}\right)^2 + R_{sec} I_L^{\mathrm{RMS}\,2} \quad (1)$$

where $R_{on,LV}$ is the on-state resistance of the low-voltage switches, $R_{on,HV}$ is the on-state resistance of the high-voltage switches, R_{pri} is the low-voltage side winding resistance, R_{sec} is the high-voltage side winding resistance, $n = n_s/n_p$ is the turns ratio and I_L^{RMS} the rms current through the equivalent energy transfer inductance L. The terms R_{pri} and R_{sec} are the ac resistances of the windings of the transformer determined at the switching frequency f_S. Then, total conduction loss minimization is performed by referring to the term $I_L^{\mathrm{RMS}\,2}$, considering such a loss contribution proportional to the total rms current. Similar considerations can be found in literature too (see, e.g., [4]).

For what concerns the switching loss, accurate models are presented in [25] and [34]. An effective means to minimize such a loss contribution is to guarantee ZVS [16], [34], [35] at the turn-on. Then, considering a constant deadtime separating a switch turn-off from the turn-on of the complementary one, ZVS can be achieved by ensuring a sufficiently intense current of appropriate sign at the beginning of the deadtime. Additional increases of the switched currents while in ZVS is detrimental, because it would increase body diodes conduction and turn-off losses [25]. Then, a limit on minimum switched currents allows minimum switching losses, which can be determined exactly as discussed in [33], [36]. Assuming, as a first approximation, a constant inductor current during the deadtime, a ZVS condition consisting in a minimum current constraint I_{S_x}, specific to the switch S_x turning on, is:

$$I_{S_x} \geq I_{ZVS}^{\min} = \frac{C_{eq,Q} V_{DC}}{t_{dead}} \quad (2)$$

where $C_{eq,Q}$ indicates the equivalent charge capacitance [33] at the node, V_{DC} its voltage at the switching instant (i.e., V_{IN} or V_{OUT}), and t_{dead} the deadtime. Notably, the switching loss typically amounts to a predominant portion of the total converter loss in the application referred to herein [4], especially in absence of soft switching.

Core losses are not considered in the optimization approach described herein because *i*) they typically account to a small portion of the total loss [25], and *ii*) their variations with the modulation parameters are low as compared to the other loss contributions variations. This can be verified considering a specific design by means of the modified Steinmetz equation [37]. On this basis, core loss does not impact the effectiveness of the proposed approach in achieving optimal operation, as confirmed in the experimental results discussed in Section VII.

The principle of the modulation approach presented in the following is to choose the modulation parameters D_1, D_2 and φ such that (2) is satisfied while I_L^{RMS} is the lowest possible, to minimize (1). In fact, from the twelve cases in Fig. 3, it is possible to compute the behavior of the inductor current i_L, which gives information on the rms current values linked to conduction losses and on the current values at the switching instants to recognize ZVS conditions [7], [33], [38].

III. SWITCHING PATTERNS ANALYSIS

For the implementation of the TPS and the efficiency maximization approach, each pattern shown in Fig. 3 can be analyzed separately. Let us consider, for example, the first pattern, represented in detail in Fig. 4. To each switching edge of v_A or v_B, it is possible to associate a corresponding current. Call I_0 the current at the first switching edge of v_A, $D_3 = \varphi + (D_1 - D_2)/2$ the normalized distance between the rising edges of v_A and v_B, and V_A and V_B the amplitude of v_A and v_B, respectively, as displayed in Fig. 4. It yields:

$$I_1 = I_0 + \int_0^{D_3 T_S} \frac{V_A}{L}\,\mathrm{d}t = I_0 + \frac{V_A}{L} D_3 T_S \quad (3)$$

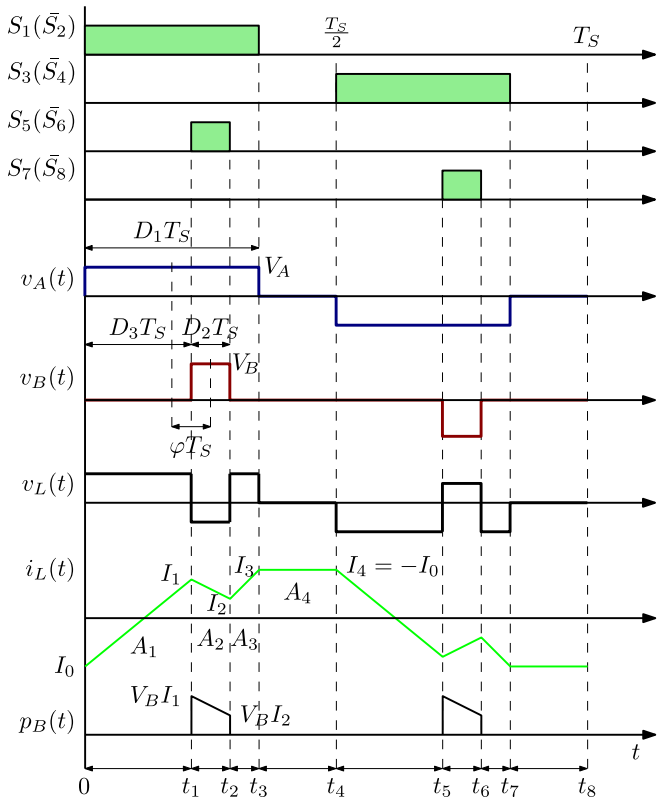


FIGURE 4. Waveforms resulting from Case 1 in Fig. 3 ($V_A < V_B$).

$$I_2 = I_1 + \int_{D_3T_S}^{[D_2+D_3]T_S} \frac{V_A - V_B}{L}\,\mathrm{d}t = I_1 + \frac{V_A - V_B}{L} D_2 T_S \tag{4}$$

$$I_3 = I_2 + \int_{[D_2+D_3]T_S}^{D_1T_S} \frac{V_A}{L}\,\mathrm{d}t = I_2 + \frac{V_A}{L}[D_1 - D_2 - D_3]T_S \tag{5}$$

$$I_4 = I_3 + \int_{D_1T_S}^{\frac{T_S}{2}} \frac{0}{L}\,\mathrm{d}t = I_3 \tag{6}$$

$$I_4 = -I_0 \tag{7}$$

By substituting (3) in (4), (4) in (5), (5) in (6), and (6) in (7), the currents at the switching instants can be rewritten as:

$$I_0 = \frac{-D_1V_A + D_2V_B}{2f_SL} \tag{8}$$

$$I_1 = \frac{-D_2V_A + 2\varphi V_A + D_2V_B}{2f_SL} \tag{9}$$

$$I_2 = \frac{D_2V_A + 2\varphi V_A - D_2V_B}{2f_SL} \tag{10}$$

$$I_3 = \frac{-D_2V_B + D_1V_A}{2f_SL} \tag{11}$$

$$I_4 = -I_0 = \frac{-D_2V_B + D_1V_A}{2f_SL} \tag{12}$$

It is worth highlighting that, in principle, (2) should be satisfied for all the instantaneous current values indicated above to ensure ZVS for both the input and output bridges.

The rms current values can be calculated in closed form too. Recalling the odd symmetry of the DAB inductor current:

$$I_L^{\mathrm{RMS}} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_L^2(t)} = \sqrt{\frac{2}{T_S}\int_0^{\frac{T_S}{2}} i_L^2(t)\,\mathrm{d}t} \tag{13}$$

and dividing the first half of T_S in the four terms A_1, A_2, A_3, A_4, (13) becomes:

$$I_L^{\mathrm{RMS}} = \sqrt{\frac{2}{T_S}(A_1 + A_2 + A_3 + A_4)} \tag{14}$$

with A_1, A_2, A_3, A_4 defined as:

$$A_1 = \int_0^{D_3T_s} \left(I_0 + \frac{V_A}{L}\right)^2 \mathrm{d}t \tag{15}$$

$$A_2 = \int_{D_3T_S}^{(D_2+D_3)T_S} \left(I_1 + \frac{V_A - V_B}{L}\right)^2 \mathrm{d}t \tag{16}$$

$$A_3 = \int_{(D_2+D_3)T_S}^{D_1T_S} \left(I_2 + \frac{V_A}{L}\right)^2 \mathrm{d}t \tag{17}$$

$$A_4 = \int_{D_1T_S}^{\frac{T_S}{2}} \left(I_3 + \frac{0}{L}\right)^2 \mathrm{d}t \tag{18}$$

Substituting (15)-(18) in (14), it yields:

$$I_L^{\mathrm{RMS}} = \frac{1}{2\sqrt{3}f_SL}\big(2D_2V_AV_B\big(D_2^2 + 3\big(D_1 - 1\big)D_1 + 12\varphi^2\big) + \big(3 - 4D_1\big)D_1^2V_A^2 + \big(3 - 4D_2\big)D_2^2V_B^2\big)^{\frac{1}{2}} \tag{19}$$

Finally, by referring to the instantaneous power calculated at the output, visible in Fig. 4, it is possible to compute the total average power:

$$\begin{aligned} P &= \frac{1}{T_S}\int_0^{T_S} v_B(t)i_L(t)\,\mathrm{d}t = \frac{2}{T_S}\int_0^{\frac{T_S}{2}} v_B(t)i_L(t)\,\mathrm{d}t \\ &= \frac{2}{T_S}\int_{D_3T_S}^{(D_2+D_3)T_S} V_B\left(I_1 + \frac{V_A - V_B}{L}(t - D_3T_S)\right)\mathrm{d}t \\ &= \frac{2D_2\varphi V_AV_B}{f_SL} \end{aligned} \tag{20}$$

The same analysis can be iterated for all the cases displayed in Fig. 3. The resulting power delivery equations are listed in Table 1, for completeness.

Although many of the numerical values given by the above relations can be obtained by circuit simulation too, the derived closed-form relations give useful information to define converter modulation parameters, as shown in the following sections.

IV. TRIPLE PHASE SHIFT MODULATION

On the basis of Section II and the analytical models described in Section III for the patterns in Fig. 3, a TPS modulation can be defined where the triplets D_1, D_2, φ are computed to minimize the power loss at given operating conditions. The

TABLE 1. Power Delivery Equations of the Patterns in Fig. 3

Case	Output Power P_{OUT}	
1	$\frac{2D_2\varphi V_A V_B}{f_S L}$	
2^+	$\frac{D_1(1-2\varphi)V_A V_B}{f_S L}$	for positive power flow, $\varphi > 0$
2^-	$\frac{-D_1(2\varphi+1)V_A V_B}{f_S L}$	for negative power flow, $\varphi < 0$
3	$\frac{D_1 D_2 V_A V_B}{f_S L}$	
4	$\frac{-V_A V_B\left((D_1+2\varphi-1)^2-2D_2(D_1-2\varphi+1)+D_2^2\right)}{4f_S L}$	
5	$\frac{-V_A V_B\left(-2D_1(D_2+2\varphi)+(D_2-2\varphi)^2+D_1^2\right)}{4f_S L}$	
6	$\frac{V_A V_B\left(-2(D_1-1)D_1-2(D_2-1)D_2-8\varphi^2+4\varphi-1\right)}{4f_S L}$	
7^+	$\frac{D_2(1-2\varphi)V_A V_B}{f_S L}$	for positive power flow, $\varphi > 0$
7^-	$\frac{-D_2(2\varphi+1)V_A V_B}{f_S L}$	for negative power flow, $\varphi < 0$
8	$\frac{2D_1\varphi V_A V_B}{f_S L}$	
9	$\frac{-D_1 D_2 V_A V_B}{f_S L}$	
10	$\frac{V_A V_B\left(D_1(4\varphi-2D_2)+(D_2+2\varphi)^2+D_1^2\right)}{4f_S L}$	
11	$\frac{V_A V_B\left(-2D_1(D_2+2\varphi+1)+(D_2-2\varphi-1)^2+D_1^2\right)}{4f_S L}$	
12	$\frac{V_A V_B\left(2(D_1-1)D_1+2(D_2-1)D_2+8\varphi^2+4\varphi+1\right)}{4f_S L}$	

principle of the TPS modulation strategy formulated in the following is to select those triplets that give switching sequences that favor ZVS conditions and, for equivalent ZVS conditions, sequences presenting minimum rms current through the energy transfer path. The corresponding algorithm, which is depicted in Fig. 5, can be stated for a particular input voltage level V_{IN} as follows:

i) The nominal power range is partitioned into disjoint intervals of desired discretization width $\{P_i\}_{i=1\ldots N}$.

ii) The series $\{I_i^{\mathrm{RMS}}\}_{i=1\ldots N}$ and $\{ZVS_i\}_{i=1\ldots N}$ of the corresponding i_L rms values and of the ZVS conditions, respectively, are created and initialized to the worst case values. Accordingly, rms currents are initialized to a high value and ZVS conditions are initialized to zero, meaning no switches in ZVS, $ZVS_i = 1$ means all the switches experience ZVS.

iii) All the possible combinations of the modulation parameters, with the desired discretization width, within the desired span D_1, $D_2 \in (0,\ 0.5]$ and $\varphi \in (0,\ 0.25]$, are considered at the particular input voltage level V_{IN}.

iv) For each combination $\mathbf{x} = (D_1,\ D_2,\ \varphi,\ V_{IN})$, rms inductor currents $I_L^{\mathrm{RMS}}(\mathbf{x})$ and power levels $P_{OUT}(\mathbf{x})$ are computed and the index i^* such that $P_{OUT}(\mathbf{x}) \in P_{i^*}$ is determined. Also, ZVS constraints (2) at $\mathbf{x}$ are evaluated considering the relevant switching pattern. Then, $\mathbf{x}$ becomes the new combination to be associated with P_{i^*} at V_{IN} if either of the following conditions are met:

a) $\mathbf{x}$ satisfies ZVS conditions for all the switches while *i*) the previously evaluated combinations giving output power within P_{i^*} do not (i.e., ZVS_{i^*} is 0) or *ii*) $\mathbf{x}$ shows lower rms current (i.e., $I_L^{\mathrm{RMS}}(\mathbf{x}) < I_{i^*}^{\mathrm{RMS}}$).

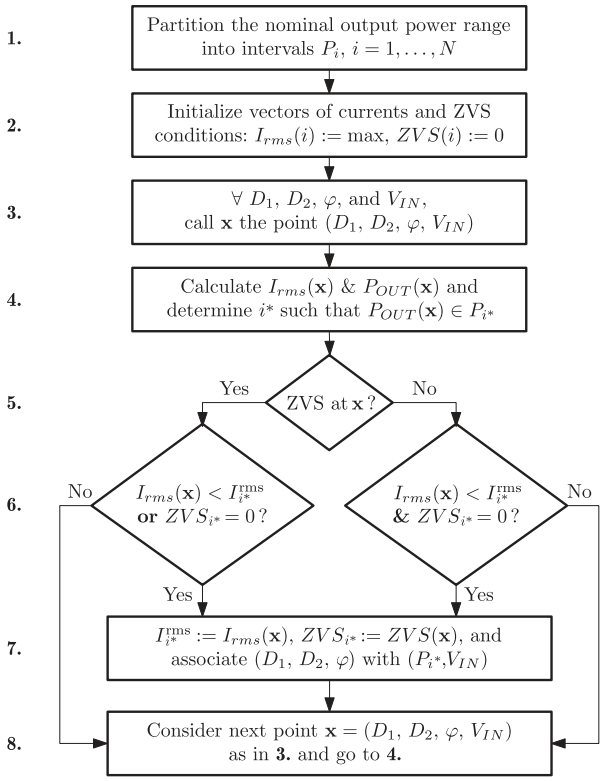


FIGURE 5. Proposed TPS modulation scheme for loss reduction. Duty-cycle and phase-shift values are considered discretized.

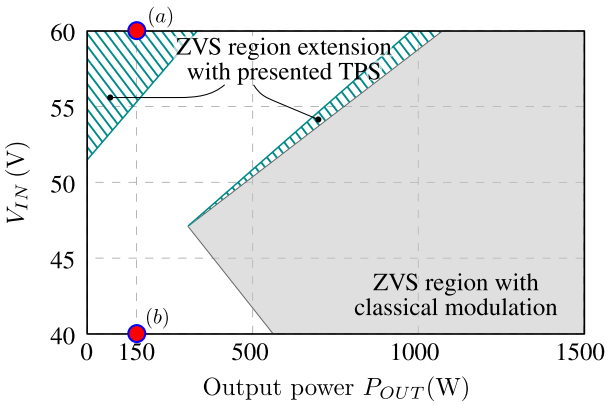


FIGURE 6. ZVS regions as defined in (2) that result by PSM (grey regions) and the ZVS extensions attained by the considered TPS (tiling-pattern regions) in Fig. 5. Highlighted the operating points considered in Section V, $V_{OUT} = 400$ V.

b) ZVS_{i^*} is 0 and $\mathbf{x}$ shows lower rms current than the previously evaluated combinations giving output power within P_{i^*} (i.e., $I_L^{\mathrm{RMS}}(\mathbf{x}) < I_{i^*}^{\mathrm{RMS}}$).

This approach gives the ZVS regions in Fig. 6, for both the input and the output bridges, and the favorable cases in Fig. 7. Fig. 6 also displays the classical PSM to show how ZVS operation is extended by the considered TPS approach, which contributes, as shown in Section VII-B, to improve operation efficiency. The shown results refer to a converter

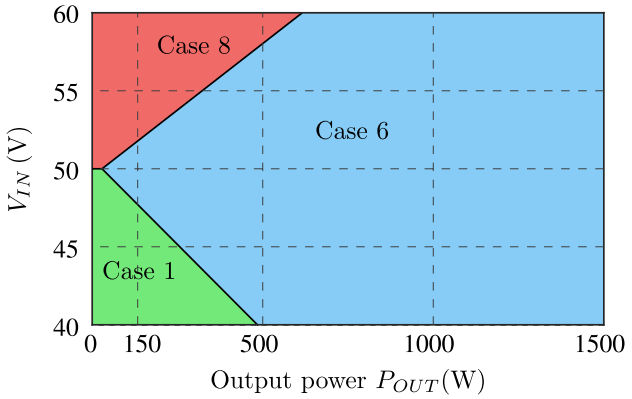


FIGURE 7. Cases resulting from the TPS algorithm described in Section IV, allowing the ZVS region extensions in Fig. 6. $V_{OUT} = 400$ V.

with parameters as indicated in the experimental section (i.e., Section VII).

V. ANALYSIS OF OPTIMAL SWITCHING PATTERNS

The approach presented in the previous section aims at modulation parameters allowing ZVS for input and output bridges and rms current minimization. It results in the identification of regions in the V_{IN}-P_{OUT} plane where specific switching patterns appear as the most favorable with respect to the considered performance figures. These regions are displayed in Fig. 7, showing Case 1, Case 6, and Case 8 as a set of cases covering the whole voltage *versus* power plane. For medium-high power levels and near the condition $V_{OUT}/V_{IN} = 1$, Case 6 appears as the most favorable [4], [18], [28], [29], [39]. For light-load operation, Case 8 and Case 1 are relevant when far from condition $V_{OUT}/V_{IN} = 1$ [4], [28], [29]. Case 8 applies for voltage ratios V_{OUT}/V_{IN} lower than the transformer turns ratio n , referred to as buck mode in the following, while Case 1 applies in the complementary condition, referred to as boost mode [39]. On this basis, these two cases are analyzed in the following for light-load efficiency maximization.

A. BUCK MODE ($V_{OUT}/V_{IN} < n$)

Consider voltage ratios lower than the transformer turns ratio, namely, Case 8 (see Fig. 7), represented in more details in Fig. 8. By the analysis outlined in Section III the current values at the switching instants can be derived as reported in Table 2. ZVS condition (2) determines the constraints reported in Table 3. Using the information in Table 2 and in Table 3, the following explicit constraints result.

- Input switches S_1, S_3:

$$I_0 = \frac{-D_1V_A + D_1V_B + 2\varphi V_B}{2f_SL} \leq -\frac{I^{\min}_{ZVS,in}}{n} \qquad (21)$$

- Input switches S_2, S_4:

$$I_1 = \frac{D_1V_A - D_1V_B + 2\varphi V_B}{2f_SL} \geq \frac{I^{\min}_{ZVS,in}}{n} \qquad (22)$$

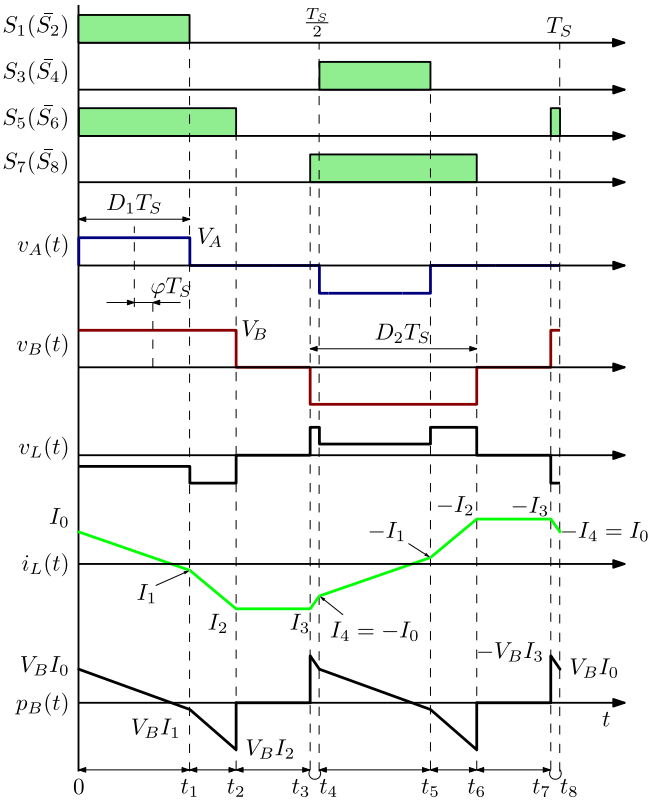


FIGURE 8. Waveforms resulting from Case 8 in Fig. 3 ($V_A < V_B$).

TABLE 2. Case 8

Conditions:	$D_2 \geq D_1 \quad \& \quad \frac{-D_2+D_1}{2} \leq \varphi \leq \frac{D_2-D_1}{2}$
Analysis Results:	
$I_0 = \frac{-D_1V_A+D_1V_B+2\varphi V_B}{2f_SL}$	$I_1 = \frac{D_1V_A-D_1V_B+2\varphi V_B}{2f_SL}$
$I_2 = I_3 = \frac{-D_2V_B+D_1V_A}{2f_SL}$	$I_4 = -I_0 = \frac{D_1V_A-D_1V_B-2\varphi V_B}{2f_SL}$
$I_L^{\text{rms}} = \frac{1}{2\sqrt{3}f_SL}\Big(2D_1V_AV_B\left(D_1^2+3\left(D_2-1\right)D_2+12\varphi^2\right)+$	
$+\left(3-4D_1\right)D_1^2V_A^2+\left(3-4D_2\right)D_2^2V_B^2\Big)^{\frac{1}{2}}$	
$P_{OUT} = \frac{2D_1\varphi V_AV_B}{f_SL}$	

TABLE 3. ZVS Conditions for Case 8 Based on Section II-B

Switch	I @ turn-on	ZVS condition
S_1	nI_0	$nI_0 \leq -I^{\min}_{ZVS,in}$
S_2	nI_1	$nI_1 \geq I^{\min}_{ZVS,in}$
S_3	$-nI_0$	$nI_0 \leq -I^{\min}_{ZVS,in}$
S_4	$-nI_1$	$nI_1 \geq I^{\min}_{ZVS,in}$
S_5	$-I_3$	$I_3 \leq -I^{\min}_{ZVS,out}$
S_6	I_2	$I_2 \leq -I^{\min}_{ZVS,out}$
S_7	I_3	$I_3 \leq -I^{\min}_{ZVS,out}$
S_8	$-I_2$	$I_2 \leq -I^{\min}_{ZVS,out}$

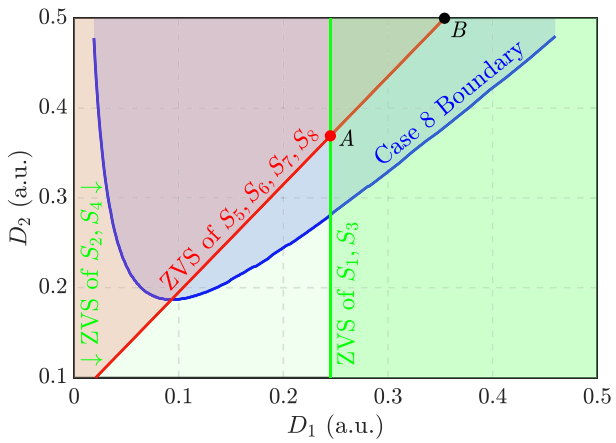


FIGURE 9. D_1-D_2 map at $V_{IN} = 60$ V, $V_{OUT} = 400$ V, $P_{OUT} = 150$ W for Case 8 (blue area). Over the intersection of the three areas (red, light-green, and dark-green), ZVS is ensured for all switches. The black dot *B* denotes the point with minimum rms currents while in ZVS, as per the TPS in Section IV. The red dot *A* denotes the point with minimum switching currents while in ZVS, achieved by the approach in Section VI.

- Output switches S_5, S_6, S_7, S_8:

$$I_2 = I_3 = \frac{-D_2 V_B + D_1 V_A}{2 f_S L} \leq -I^{\min}_{ZVS,out} \qquad (23)$$

Inequalities (21)-(23) can be rewritten for a fixed output power (i.e., P_{OUT}, in Table 2) as:

$$(V_A - V_B) V_A D_1^2 - f_S L \left[P_{OUT} + \frac{2 V_A I^{\min}_{ZVS,in}}{n} D_1 \right] \geq 0 \qquad (24)$$

$$(V_A - V_B) V_A D_1^2 + f_S L \left[P_{OUT} - \frac{2 V_A I^{\min}_{ZVS,in}}{n} D_1 \right] \geq 0 \qquad (25)$$

$$D_2 \geq \frac{V_A}{V_B} D_1 + \frac{I^{\min}_{ZVS,out} 2 f_S L}{V_B} = m_8 D_1 + q_8 \qquad (26)$$

respectively, which can be exploited for optimization.

The obtained results are reported in graphical form in Fig. 9. The figure shows the modulation parameters map at $V_{IN} = 60$ V, $P_{OUT} = 150$ W that satisfies (24)–(26), while the remaining modulation parameter φ is set to guarantee fixed output power. The figure displays *i*) in blue color, the region pertaining to Case 8, *ii*) in red color, the region where ZVS for the output switches S_5, S_6, S_7, S_8 is achieved, and *iii*) in dark-green color, the region where ZVS for the input switches S_1, S_3 is achieved—in this operating condition (22) is always satisfied for S_2, S_4 (light-green area). The lines marking ZVS boundaries correspond to theoretical minimum values of switched currents to ensure ZVS within Case 8. For example, the dot *A* in Fig. 9, lying on the intersection between the ZVS boundaries, gives minimum instantaneous currents at the switching instants for both the bridges while preserving ZVS. Instead, the dot *B* can be found by the approach described in Section IV and it represents the point with minimum rms current while achieving ZVS for both the bridges. Notably, by moving along the red line from *B* to *A*, lower switching currents can be achieved for the input bridge switches [5], [25] with relatively higher rms currents, increasing in this way the conduction loss in favor of lower switching loss. This can be beneficial in terms of total converter efficiency in light-load, in which situation switching losses prevail.

TABLE 4. Case 1

Conditions: $D_1 \geq D_2$ & $\frac{D_2 - D_1}{2} \leq \varphi \leq \frac{D_1 - D_2}{2}$
Analysis Results:
$I_0 = \frac{-D_1 V_A + D_2 V_B}{2 f_S L}$ $\quad I_1 = \frac{-D_2 V_A + 2\varphi V_A + D_2 V_B}{2 f_S L}$
$I_2 = \frac{D_2 V_A + 2\varphi V_A - D_2 V_B}{2 f_S L}$ $\quad I_3 = I_4 = -I_0 = \frac{D_1 V_A - D_1 V_B - 2\varphi V_B}{2 f_S L}$
$I_L^{\text{rms}} = \frac{1}{2\sqrt{3} f_S L} \Big(2 D_2 V_A V_B \left(D_2^2 + 3 (D_1 - 1) D_1 + 12\varphi^2 \right) + + (3 - 4D_1) D_1^2 V_A^2 + (3 - 4D_2) D_2^2 V_B^2 \Big)^{\frac{1}{2}}$
$P_{OUT} = \frac{2 D_2 \varphi V_A V_B}{f_S L}$

TABLE 5. ZVS Conditions for Case 1 Based on Section II-B

Switch	I @ turn-on	ZVS condition
S_1	nI_0	$nI_0 \leq -I^{\min}_{ZVS,in}$
S_2	nI_3	$nI_3 \geq I^{\min}_{ZVS,in}$
S_3	$-nI_0$	$nI_0 \leq -I^{\min}_{ZVS,in}$
S_4	$-nI_3$	$nI_3 \geq I^{\min}_{ZVS,in}$
S_5	I_1	$I_1 \geq I^{\min}_{ZVS,out}$
S_6	I_2	$I_2 \leq -I^{\min}_{ZVS,out}$
S_7	$-I_1$	$I_1 \geq I^{\min}_{ZVS,out}$
S_8	$-I_2$	$I_2 \leq -I^{\min}_{ZVS,out}$

B. BOOST MODE ($V_{OUT}/V_{IN} > n$)

Similar considerations can be done for this complementary condition too, which is related to Case 1 (see Fig. 7), represented in more details in Fig. 4. Table 4 and Table 5 report the results from the analysis of the converter waveforms as outlined in Section III and the ZVS constraints, respectively. It results:

- Input switches S_1, S_2, S_3, S_4:

$$I_0 = -I_3 = \frac{-D_1 V_A + D_2 V_B}{2 f_S L} \leq -\frac{I^{\min}_{ZVS,in}}{n} \qquad (27)$$

- Output switches S_5, S_7:

$$I_1 = \frac{-D_2 V_A + 2\varphi V_A + D_2 V_B}{2 f_S L} \geq I^{\min}_{ZVS,out} \qquad (28)$$

- Output switches S_6, S_8:

$$I_2 = \frac{D_2 V_A + 2\varphi V_A - D_2 V_B}{2 f_S L} \leq -I^{\min}_{ZVS,out} \qquad (29)$$

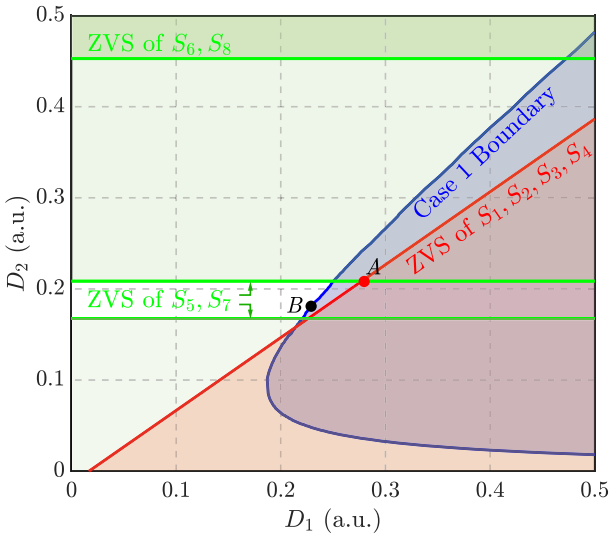


FIGURE 10. D_1-D_2 map at $V_{IN} = 40$ V, $V_{OUT} = 400$ V, $P_{OUT} = 150$ W for Case 1 (blue area). Over the intersection of the three areas (light-green, red, and dark-green), ZVS is ensured for all switches. The black dot *B* denotes minimum rms currents, as per TPS in Section IV. The red dot *A* denotes highest number of switches experiencing ZVS with minimum switching currents.

Inequalities (27)-(29) can be rewritten for a fixed output power (i.e., P_{OUT}, in Table 4) as:

$$D_2 \leq \frac{V_A}{V_B} D_1 - \frac{I^{\min}_{ZVS,in} 2 f_S L}{n V_B} = m_1 D_1 + q_1 \quad (30)$$

$$[V_B - V_A] V_B D_2^2 + L f_S \left[P_{OUT} - 2 V_B I^{\min}_{ZVS,out} D_2\right] \geq 0 \quad (31)$$

$$[V_B - V_A] V_B D_2^2 - L f_S \left[P_{OUT} + 2 V_B I^{\min}_{ZVS,out} D_2\right] \geq 0 \quad (32)$$

Remarkably, the obtained equations represent the dual of those obtained in Section V-A. Analogously, the graphical representation of the obtained results is given in Fig. 10 considering the operating point $V_{IN} = 40$ V, $P_{OUT} = 150$ W. The figure displays *i*) in blue color, the region pertaining to Case 1, *ii*) in red color, the region where ZVS for the input switches S_1, S_2, S_3, S_4 is achieved, and *iii*) in light-green color, the region where ZVS for the output switches S_5, S_7 is achieved, *iv*) in (dark)-green color, the region where ZVS for output switches S_6, S_8 is achieved. The same considerations done in Section V-A apply here too. In Fig. 10, the dot *B* denotes the point found by the algorithm in Section IV, featuring minimum rms. In such a point ZVS is not achieved. Instead, dot *A* brings to minimum instantaneous currents at the switching instants whilst preserving ZVS for the highest number of switches, namely, $S_{1\div4}$ and S_5, S_7. At light-load the choice of dot *A* in the maps of Fig. 9 and Fig. 10 reduces the main loss contribution given by the switching loss. Notably, the low instantaneous currents at dot *A* minimize the conduction angle of the body diodes (refer to, e.g., [33], [36]) making the related conduction loss contribution negligible.

Finally, it is worth remarking that an accurate balance among conduction and switching losses, crucial for efficiency maximization, is hard to obtain with approaches based on off-line modeling and converter analysis.

On the light of the above considerations, the next section proposes a simple closed-loop procedure that aims to find the optimal modulation parameters in terms of operation efficiency.

VI. MAXIMUM EFFICIENCY POINT IDENTIFICATION

The TPS in Section IV is based on simplified converter models and allows to sensibly improve converter efficiency as compared to PSM. Still, as it is typically the case with TPS modulation values computed off-line, converter parameters uncertainties and other secondary effects (e.g., temperature dependences of MOSFETs on-resistances) are not included in the methodology [23], which potentially gives room for additional efficiency improvements. These are explored by the following maximum efficiency point identification (MEPI) algorithm.

The proposed principle consists in adjusting the modulation parameters D_1 and D_2 in such a way to selectively modify the switching currents of the input and output bridges along trajectories of low rms currents. The aim is to balance switching losses, related to the kind of switching (i.e., soft or hard) given by the switched currents, and conduction losses, related to the primary and secondary rms currents. This is done by exploiting the equations presented in Section V while the output power is kept constant, as often done, by a, faster, $P_{OUT} - \varphi$ control loop.

A. LIGHT-LOAD OPERATION

To illustrate the technique, let us refer to the buck operation mode first, for which the equations in Section V-A apply. The basic steps reported in the following and schematically represented in Fig. 11(a) are performed.

- Consider an initial point 1 in the D_1-D_2 space belonging to Case 8 (see Fig. 11(b)). Call $(D_1^{sub,opt}, D_2^{sub,opt})$ this initial point, which can be, for example, the point given by the TPS in Section IV, potentially sub-optimal.
- $D_1^{sub,opt}$ is initially kept constant, thus switching currents of the low-voltage bridge (nI_0 and nI_1 in Table 3) remain constant [see (21) and (22)], while $D_2^{sub,opt}$ is adjusted until maximum efficiency is reached. This intermediate point $(D_1^{sub,opt}, D_2^*)$ at light-load theoretically coincides with the ZVS boundary line of the output switches (i.e., point 2 in Fig. 11(b)), where the related switching loss contribution is minimum.
- From (26) and D_2^*, derive $q = D_2^* - m D_1^{sub,opt}$, which is linked to the actual value of $I^{\min}_{ZVS,out}$ giving the minimum switching currents I_2 and I_3 for ZVS of the high-voltage bridge.
- By exploiting (26), vary D_1, D_2 along the line $q = D_2 - mD_1$ to adjust the input bridge switching currents while keeping fixed the output bridge switching currents until reaching maximum efficiency, at point 3 (D_1^{opt}, D_2^{opt}) in Fig. 11(b).

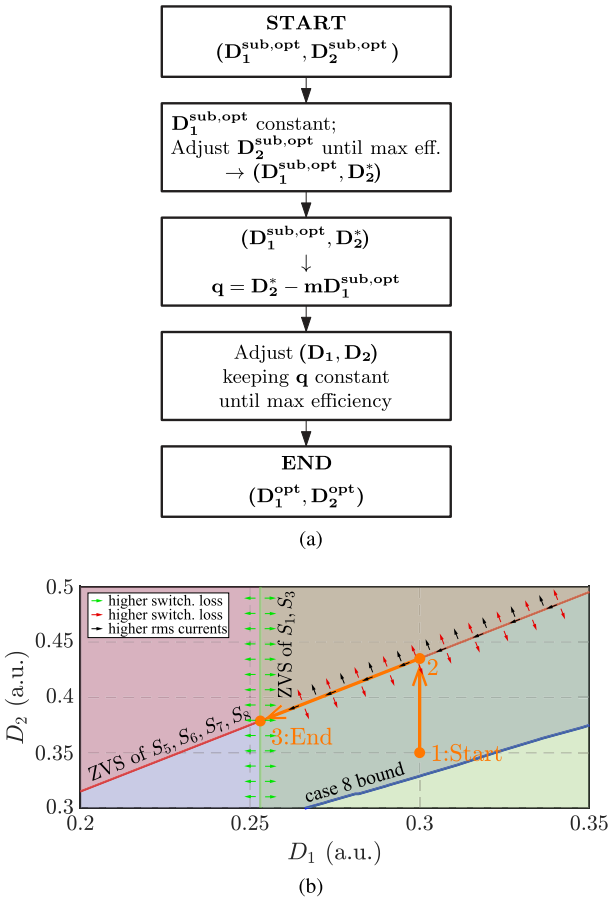


FIGURE 11. Maximum efficiency point identification approach over the D_1-D_2 map of Case 8 (Fig. 9) for the buck mode range. (a) MEPI algorithm of Section VI-A; (b) example of resulting trajectories by the MEPI starting from D_1, D_2 such that ZVS is achieved only for the input bridge but not with the minimum switched currents.

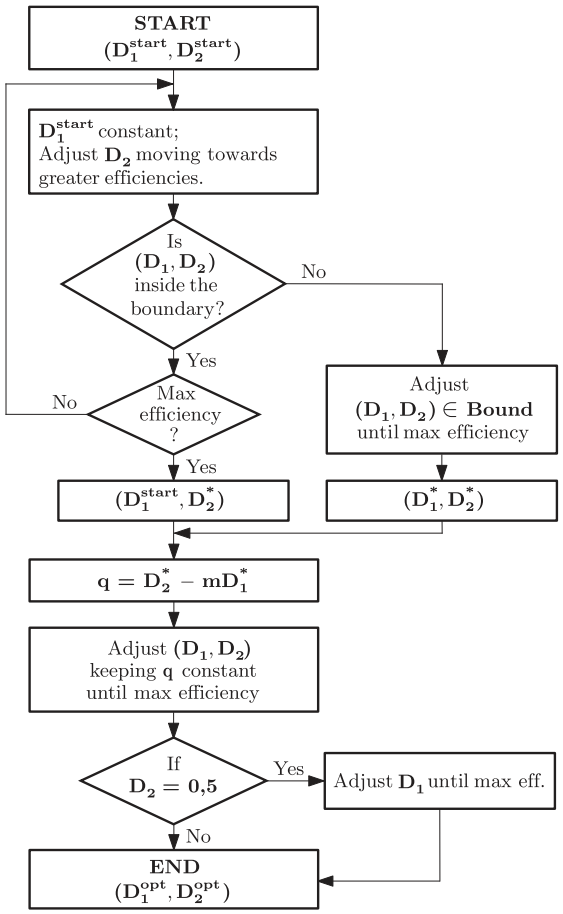


FIGURE 12. Maximum efficiency point identification algorithm of Section VI-B.

The maximum efficiency point identification as stated above is applicable at light-load within Case 8 throughout the buck-mode voltage range. Similarly, performing the analysis by exploiting the results in Section V-B, the same procedure of Fig. 11(a) can be attained, with the only difference that D_1 and D_2 are swapped; this analogy stems from the duality highlighted in the remark related to (30)–(32) of same section.

It is worth noticing that the presented algorithm allows to estimate on-line the parameter q of inequalities (26) and (30). The parameter q lumps together the most critical parameters for ZVS operation, allowing to perform optimization without their knowledge.

B. FULL POWER-RANGE

The point of operation found by the procedure above is the one that aims at minimum overall loss at light-load by considering regions in the modulation parameter space that are close to TPS boundaries for the input and output bridges and that are characterized by low rms currents. Such regions are close to the dot *A* in Fig. 9 and Fig. 10.

Differently, at higher transferred powers the switched currents increase. On the one hand this facilitates condition (2), but on the other it increases the relative weight of the conduction loss. The modulation parameters computed by the TPS technique belong to Case 6 and present D_1, while in boost mode, or D_2, while in buck mode, saturated to a half. This complies with the results in [4], [18], [28], [29], [35]. On the light of that, a single degree of freedom constituted by the modulation parameter that is not saturated remains available, namely, D_1 in buck mode or D_2 in boost mode. These final considerations can be integrated in the algorithm described in Section VI-A, extending the efficiency maximization procedure to the whole output power range. The resulting maximum efficiency point identification algorithm relevant to the complete output power range is reported in Fig. 12.

The proposed algorithm can be extended for negative power flows too, as Case 1 and Case 8 remain the optimal switching patterns for the light-load operation and Case 6 is substituted by the symmetrical Case 12 for the medium-high power range.

Being the technique aimed at efficiency optimization, it can be executed at a much lower peace than converter control (e.g., 1–10 Hz).

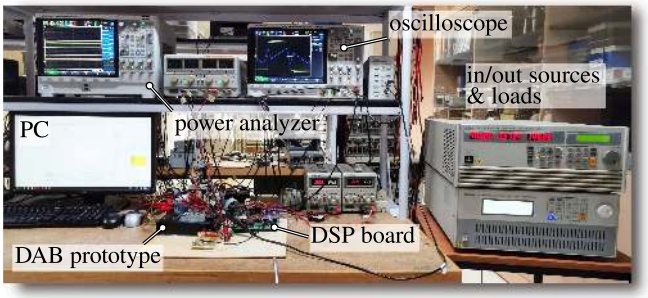


FIGURE 13. Experimental setup for MEPI validation.

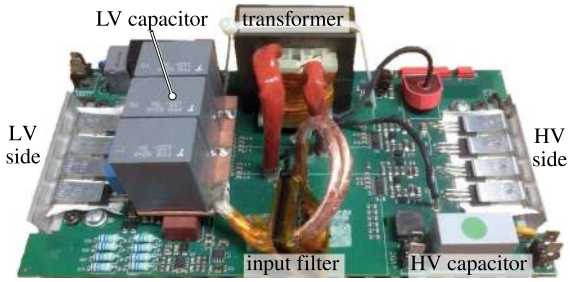


FIGURE 14. DAB converter prototype.

TABLE 6. Parameters of the DAB Prototype in Fig. 14

Parameters		Value
Input voltage V_{IN}	(V)	40 - 60
Output voltage V_{OUT}	(V)	400
Nominal power P_N	(kW)	1.5
Switching frequency $f_S = 1/T_S$	(kHz)	60
Energy transfer inductance	(μH)	186
Turns ratio $n = n_s/n_p$		8
Low-voltage side devices		IPP023N10N5
High-voltage side devices		FCP110N65F

VII. EXPERIMENTAL VALIDATION

A. MEASUREMENT SETUP

In order to verify the analyses presented in Section IV and the optimization technique of Section VI, the automatic measurement setup in Fig. 13 was built around the experimental DAB prototype in Fig. 14, whose parameters are listed in Table 6. The block diagram in Fig. 15 shows the main elements of the setup. The input of the DAB converter is fed by a Chroma 62050P-100-100 dc power supply, the output is connected to a Chroma 63 202 electronic load set in constant voltage mode. The input and the output ports are connected to a Keysight PA2203 A power analyzer. The power analyzer is set to use a so called continuous whole-cycle analysis, with a time window of 1-s length within which measurements are performed on an integer number of contiguous cycles. A LAUNCHXL-F28377S development board hosting a Texas Instruments DSP TMS320F28377S is used to implement the modulators and

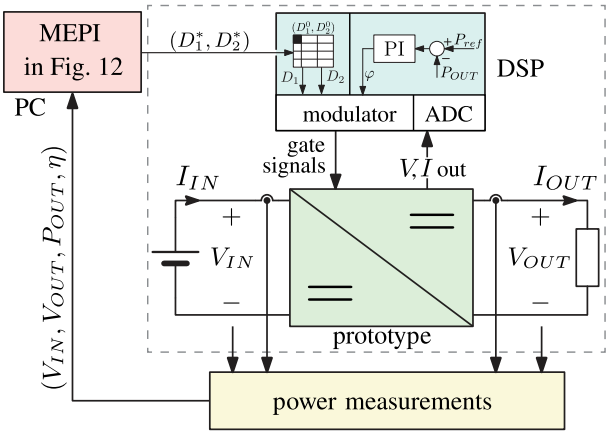


FIGURE 15. Block diagram of the experimental setup in Fig. 13.

generate the PWM signals. Modulation parameters resolution is 0.12% for D_1, D_2, and 0.06% for φ.

The following kind of results have been collected:

- *Verification of the TPS modulation:* the converter operates with D_1, D_2 as defined by the proposed TPS in Section IV and stored in the DSP memory. The output power is regulated by an inner proportional-integrative (PI) controller by acting on φ. The MEPI technique is disabled.
- *Verification of the MEPI technique*: the converter operates with D_1, D_2 identified by the MEPI technique in Section VI, initialized using the TPS values found by the analysis in Section IV. As before, the output power is regulated by the PI controller acting on φ. The MEPI in Fig. 12 is performed on-line on a desktop computer calculating the perspective optimal values D_1^*, D_2^* that are written in the DSP memory. The diagram in Fig. 15 shows the relevant relations.

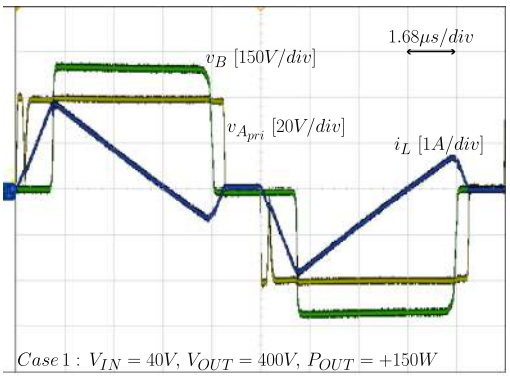
To benchmark the effectiveness of the approach, the converter efficiency limit was estimated by a brute-force exploration of the modulation space, as done, for example, in [40].

B. EXPERIMENTAL RESULTS

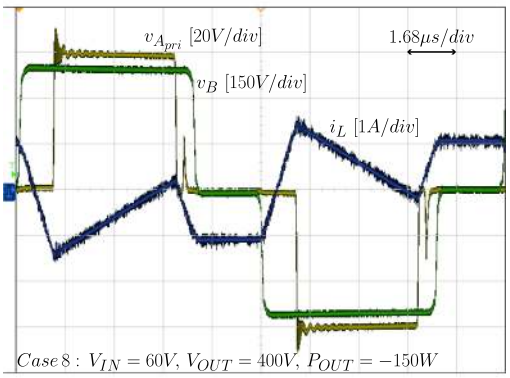
The operation of the converter operation with the proposed TPS and MEPI is shown in the following considering different transferred power and input and output voltage levels. The results are reported below.

a) Steady-state operation: first of all, the steady state operation is displayed in Fig. 16, considering Case 1, Case 8, and Case 6 identified in Section IV.

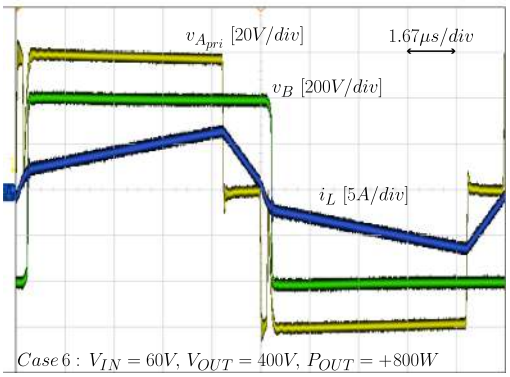
b) Efficiency curves: Fig. 17(a), with $V_{IN} = 60\,\text{V}$, and Fig. 17(b), with $V_{IN} = 40\,\text{V}$, display the measured efficiency curves considering the classical PSM, the TPS in Section IV, and the MEPI of Section VI. In addition, the estimated limit efficiency curve is included. Notably, the proposed TPS shows significant improvements as compared with the PSM, especially in light-load operation: efficiency increases by 24% at



(a)

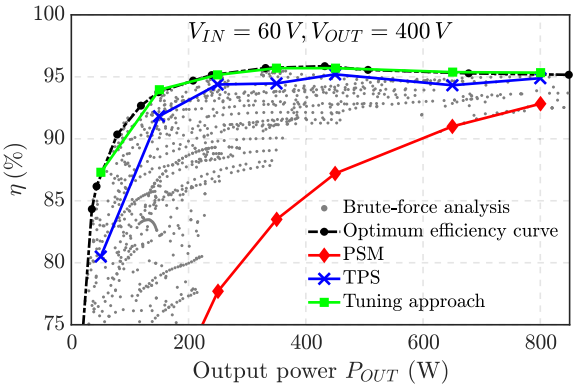


(b)

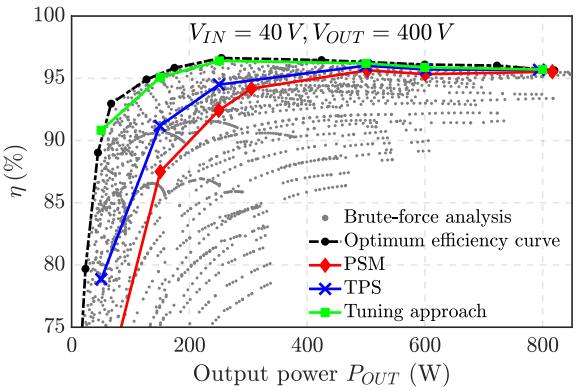


(c)

FIGURE 16. **DAB experimental waveforms with TPS, $V_{OUT} = 400$ V and (a) Case 1: $V_{IN} = 40$ V, $P_{OUT} = +150$ W; (b) Case 8: $V_{IN} = 60$ V, $P_{OUT} = -150$ W; (c) Case 6: $V_{IN} = 60$ V, $P_{OUT} = +800$ W.**



(a)



(b)

FIGURE 17. **Measured efficiencies by applying the classical PSM, the TPS in Section IV, and the approach in Section VI. (a) $V_{IN} = 60$ V; (b) $V_{IN} = 40$ V and $V_{OUT} = 400$ V. The black line is the estimated maximum efficiency curve. Numerical values are reported in Table 8 and in Table 9.**

$P_{OUT} = 150$ W for $V_{IN} = 60$ V and about 4% of increment for $V_{IN} = 40$ V at the same power level.

c) Switches ZVS transitions: the improvements above are linked to the ZVS and rms current minimization allowed by the computed modulation parameters D_1 and D_2 of the proposed TPS. In fact, as can be seen from Fig. 6, using PSM full ZVS of both the bridges is obtained in the grey region, whilst outside this region only the input bridge operates in ZVS if $nV_{IN} > V_{OUT}$, and the output bridge operates in ZVS if $nV_{IN} < V_{OUT}$ [13]. On the other side, using the proposed TPS an additional full ZVS region for $nV_{IN} > V_{OUT}$ is obtained, which implies a full ZVS operation of the output bridge too. At the considered operating point $V_{IN} = 60$ V, $V_{OUT} = 400$ V, $P_{OUT} = 150$ W with PSM only the input bridge is operating with ZVS, while the output bridge experiences hard commutations, bringing to significant switching loss. Instead, by applying TPS both the bridges achieve ZVS, significantly reducing output bridge losses. The effect is visible on the thermography in Fig. 18. Apart from some hot-spots related to sensing and auxiliary circuits that are non relevant and not included in the current analysis, the temperatures significantly reduce from (a) to (b) in the region of the prototype where the high-voltage side switches are installed (see Fig. 14), thanks to the ZVS achieved by TPS. Fig. 19 also shows the achieved ZVS transition of the output bridge by the TPS parameters.

d) Maximum efficiency point identification: Fig. 20 shows the result of applying the MEPI algorithm described in Section VI at $P_{OUT} = 150$ W, with different values of output voltage, while reverse power flow is considered in Fig. 21. Fig. 20(a) refers to the case of input voltage equal to 40 V, Fig. 20(b) with input voltage equal to 40 V. Both the figures report the obtained efficiencies at each step. Fig. 22 reports the corresponding trajectories in the D_1-D_2 plane: subfigure (a) for $V_{IN} = 60$ V, subfigure (b) for $V_{IN} = 40$ V. Significant

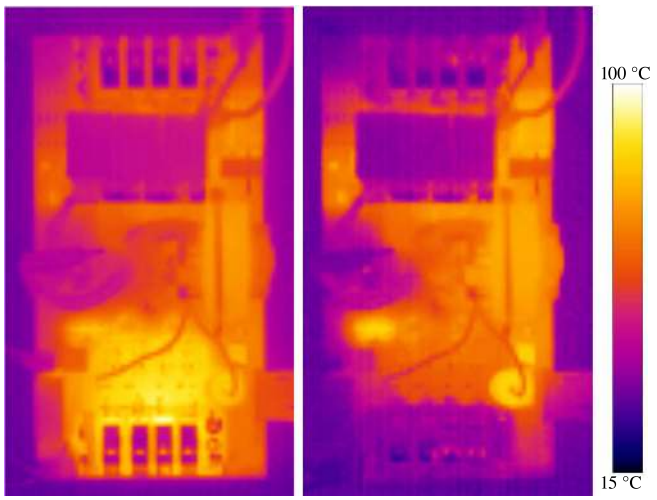


FIGURE 18. Thermography (a) with PSM, (b) with TPS. $V_{IN} = 60\,V$, $V_{OUT} = 400\,V$, $P_{OUT} = 150\,W$. Output, high-voltage side switches on the bottom.

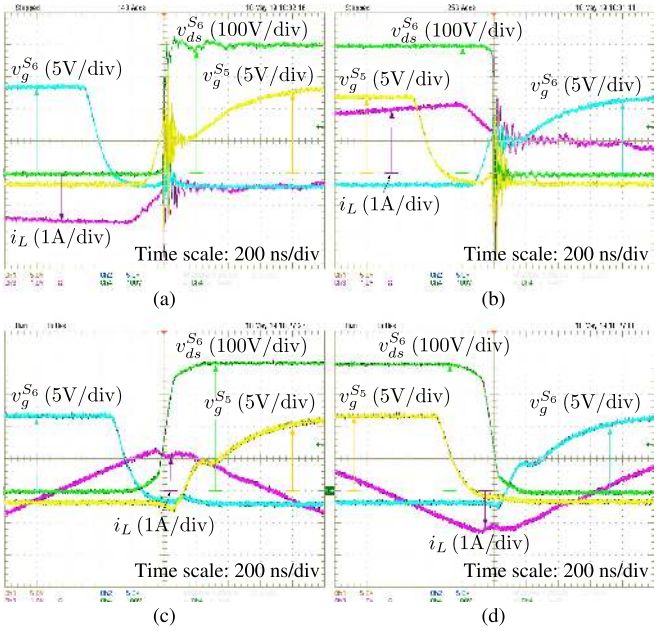


FIGURE 19. Waveforms at turn-on of S_5 and S_6. (a)-(b) with PSM; (c)-(d) with TPS. $V_{IN} = 60\,V$, $V_{OUT} = 400\,V$, $P_{OUT} = 150\,W$. Notably, (a)-(b) report hard switching transitions, (c)–(d) report soft switching transitions.

improvements can be noticed; for example, with $V_{IN} = 60\,V$, $V_{OUT} = 400\,V$, the efficiency increases up to 94%, starting from an initial sub-optimal value of 91.82%. Remarkably, the final efficiency values practically reach the estimated boundary curves of the prototype, which proves the optimality of the found modulation parameters. In general, the approach achieves final efficiencies close to the boundaries attained by brute-force exploration. Fig. 21 also shows the same properties considering operation with reversed power flow. The achieved efficiencies of the above mentioned operating points are summarized in Table 7.

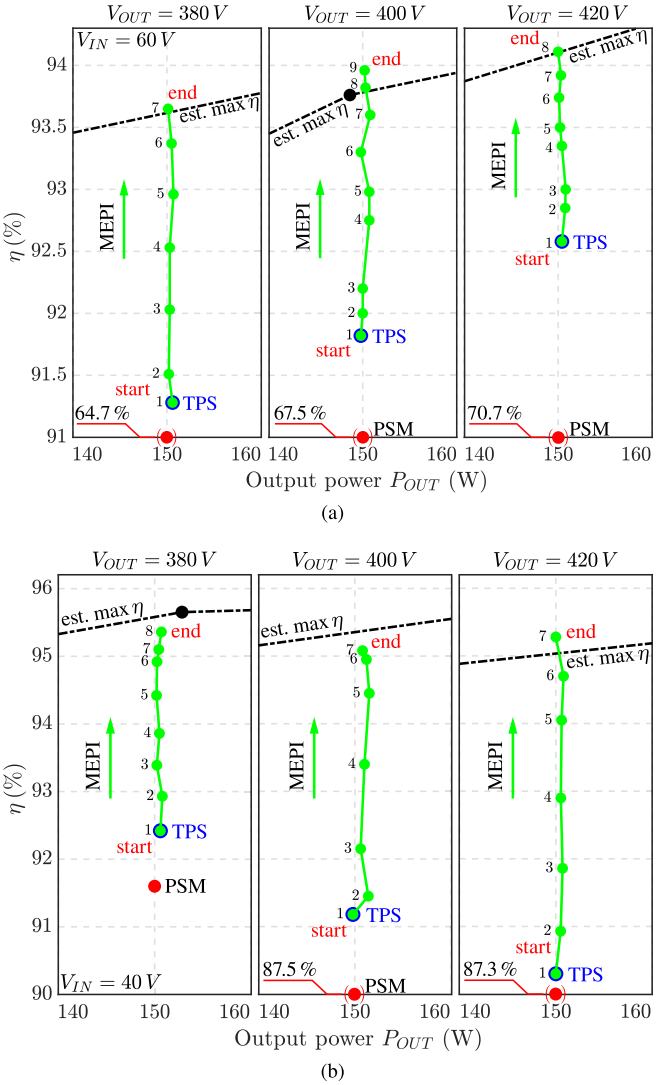


FIGURE 20. Measured efficiency points obtained by the MEPI technique described in Section VI with different output voltage values. $P_{OUT} = 150\,W$ and (a) $V_{IN} = 60\,V$, (b) $V_{IN} = 40\,V$. Modulation parameters from the TPS in Section IV are considered as initial values. Final values approximate the estimated maximum efficiency boundary curve.

TABLE 7. Efficiency Values Related to Fig. 20 and Fig. 21

V_{IN} (V)	V_{OUT} (V)	P_{OUT} (W)	Efficiency (%) PSM	TPS	MEPI	Est. opt.
60	380	150	64.70	91.28	93.65	93.65
	400		67.50	91.82	93.96	93.80
	420		70.70	92.58	94.11	94.16
40	380	150	91.62	92.42	95.36	95.60
	400		87.50	91.18	95.08	95.40
	420		87.30	90.30	95.28	95.10
60	400	-150	56.50	91.18	93.27	93.49
50			92.93	93.05	93.60	93.66
40			88.40	88.94	95.05	95.14

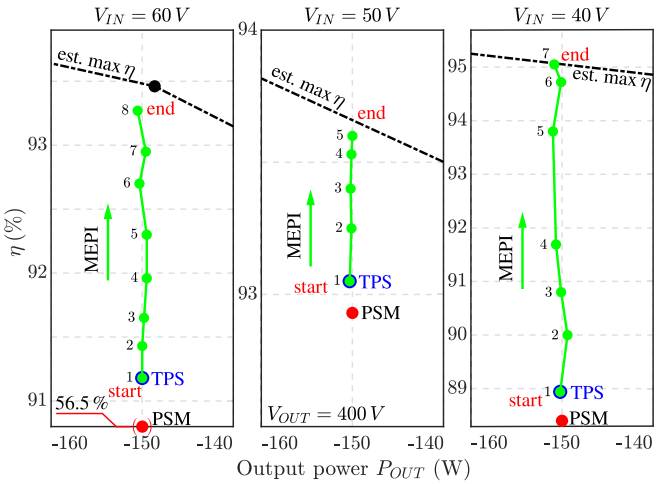


FIGURE 21. Measured efficiency points with different values of input voltage. $P_{OUT} = -150\,W$, $V_{OUT} = 400\,V$.

TABLE 8. Efficiency Values With $V_{IN} = 60V$, $V_{OUT} = 400\,V$

Power Level (W)	Efficiency (%) PSM	TPS	MEPI	Est. opt.
50	47.30	80.50	87.30	87.05
150	67.50	91.82	93.96	93.80
250	77.70	94.38	95.16	95.22
350	83.50	94.47	95.70	95.77
450	87.20	95.20	95.70	95.82
650	91.00	94.32	95.38	95.5
800	92.83	94.89	95.34	95.35

TABLE 9. Efficiency Values With $V_{IN} = 40V$, $V_{OUT} = 400\,V$

Power Level (W)	Efficiency (%) PSM	TPS	MEPI	Est. opt.
50	68.70	78.86	90.82	90.70
150	87.50	91.18	95.08	95.40
250	92.42	94.49	96.40	96.60
500	95.64	96.01	96.20	96.30
600	95.33	95.71	95.87	96.10
800	95.53	95.68	95.70	95.75

Additional operating points were considered in the experimental validation. The most representative results with PSM, TPS, and the proposed MEPI are summarized in Table 8 and Table 9 for $V_{IN} = 60\,V$ and $V_{IN} = 40\,V$, respectively, also indicating the measured optimal efficiencies estimated by brute-force. Notably, final efficiencies practically match the optimal ones and are achieved by the algorithm described in Section VI, which does not rely on the knowledge of converters parameters, and, therefore, it is robust against parameters uncertainties or models discrepancies. Still, slight differences between the actual values found by the MEPI approach and the estimated maximum efficiencies are present, mainly due to unavoidably non-identical test conditions (e.g., temperatures,

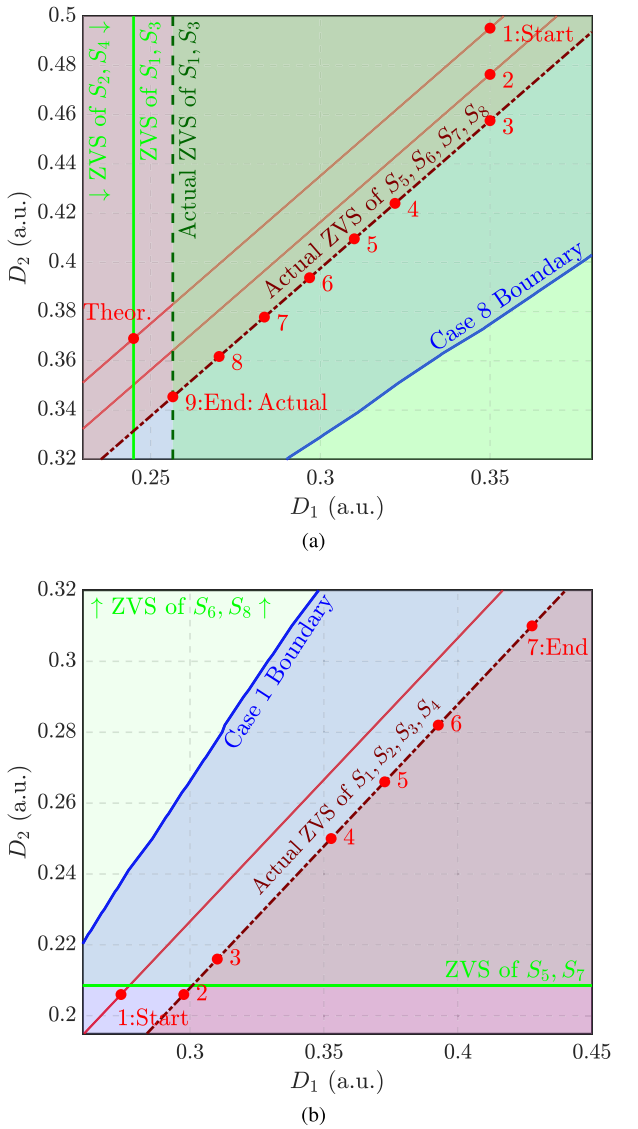


FIGURE 22. Trajectories in the D_1, D_2 modulation plane resulting form the efficiency maximization approach described in Section VI for $P_{OUT} = 150\,W$, $V_{OUT} = 400\,V$ and (a) $V_{IN} = 60\,V$, (b) $V_{IN} = 40\,V$. Modulation parameters from the TPS in Section IV are considered as initial values. (a) and (b) refer to the central subfigure of Fig. 20(a) and Fig. 20(b), respectively.

input/output voltages) between the estimation phase and the MEPI validation phase.

It is finally reported that, even though the initial points for MEPI initialization considered herein are those given by the TPS in Section IV, the authors have verified that convergence to the found optimal points is achieved even considering arbitrary points within the identified Cases, displayed in Fig. 7. Such points might be potentially given by other approaches in the literature that compute TPS modulation values on the basis of off-line converter information (see, e.g., [28], [29] in light-load conditions).

VIII. CONCLUSION

In this paper, the efficiency maximization of a DAB based on minimal converter models is considered. First, the converter

inductor current waveforms have been computed and analyzed considering all the possible order of activation of the switches with the aim of identifying those switching patterns that minimize rms currents while keeping ZVS. Then, the corresponding TPS modulation parameters have been computed numerically. By using only some fundamental converter parameters, the approach attains significant efficiency improvements with respect to the classical phase-shift modulation, especially in light-load operation. Still, optimal operation depends on component characteristics, parasitics, and non idealities. To tackle this issue, a maximum efficiency point identification technique, called MEPI algorithm, has been presented that maximizes converter efficiency by refining the TPS modulation parameters. This approach is based on the analytical description of the switching currents within the identified optimal switching patterns. The optimized modulation parameters are obtained by straight trajectories on the modulation planes, which ensures a precise and prompt procedure. The approaches were validated considering an experimental prototype, obtaining efficiency values practically equivalent to the measured optimal ones found by a brute-force approach. The proposed approach can be executed on-line for loss minimization or it can be exploited for the fast identification of close-to-optimal modulation parameters before deployment. The reported results give insight into the main loss contributions at light-load operation and show a technique capable of attaining close-to-optimal operation considering DAB topologies, which can be exploited in future works also considering multi-port converters.

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