Research Article

A Low Complexity All-Digital Background Calibration Technique for Time-Interleaved ADCs

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A low complexity all-digital background calibration technique based on statistics is proposed. The basic idea of the statistics calibration technique is that the output average energy of each channel of TIADC will be consistent ideally, since each channel samples the same input signal, and therefore the energy deviation directly reflects the mismatch errors of channels. In this work, the offset mismatch and gain mismatch are calibrated by an adaptive statistics calibration algorithm based on LMS iteration; the timing mismatch is estimated by performing the correlation calculation of the outputs of subchannels and corrected by an improved fractional delay filter based on Farrow structure. Applied to a four-channel 12-bit 400 MHz TIADC, simulation results show that, with calibration, the SNDR raises from 22.5 dB to 71.8 dB and ENOB rises from 3.4 bits to 11.6 bits for a 164.6 MHz sinusoidal input. Compared with traditional methods, the proposed schemes are more feasible to implement and consume less hardware resources.

1. Introduction

Modern signal processing applications emerging in the telecommunications and instrumentation industries need high-speed and high-resolution analog-to-digital converters (ADCs). The time-interleaved ADCs (TIADCs) provide an effective way to achieve high sampling rate maintaining high resolution. However, the fabrication errors result in a variety of mismatch errors, constricting the conversion precision of the TIADC. Among them, the main mismatches are offset, gain, and timing mismatches [1, 2].

In recent years, many research institutes and universities have carried out researches on calibration technology for mismatch errors among channels of TIADC. The calibration of offset and gain mismatches is fairly straightforward, which can be done by adders and multipliers [3, 4], but the timing mismatch presents much more challenge due to its frequency dependent detection. The drawbacks of the presented calibration methods mainly are reflected in the following aspects: the normal TIADC working needs to be interrupted [5, 6], the calibration methods cannot applied to any number of channels of TIADC [7], the input signal bandwidth of TIADC is limited [8–10], and the calibration algorithms are more complex and consume large hardware resources [11, 12].

In this brief, low complexity calibration algorithms are designed to mitigate the impact of the three main channel mismatches. All calibration algorithms are in digital domain. The calibration method is effective and capable of reducing all three mismatches errors. The rest of this brief is organized as follows: Section 2 introduces the principle and mismatches in TIADC. Section 3 describes the proposed complete calibration algorithms. Section 4 provides the simulation results. Lastly, Section 5 states the conclusion.

2. Time-Interleaved ADC

A block diagram and a timing diagram of a TIADC are shown in Figure 1; each subchannel ADC alternately samples the analog input which is on the front end and converts the analog signal into a digital signal and then through a synthesis module converts the outputs of multiple channels into a digital output. If the clock cycle of each channel ADC is T_{sub}, the sampling interval of the adjacent channel ADC
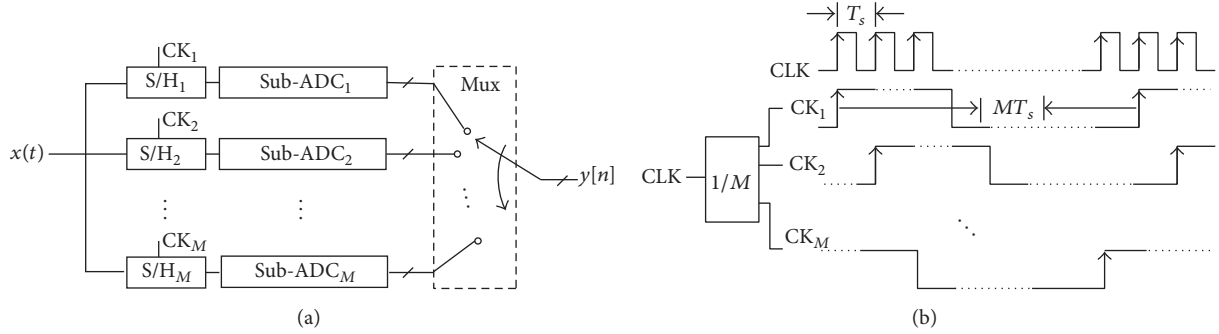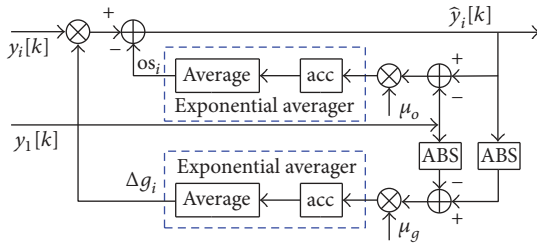
FIGURE 1: The block diagram for an M-channel TIADC.

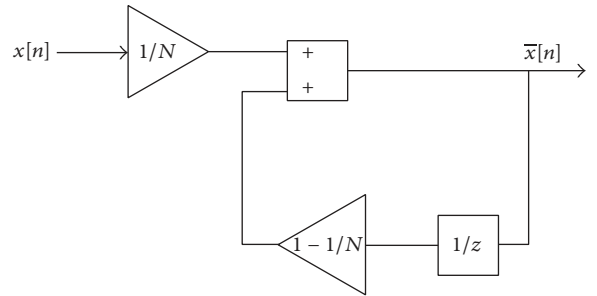FIGURE 2: Cascaded calibration of offset and gain mismatch scheme based on LMS iteration.

FIGURE 3: Exponential smoothing filter.

is $T_s = T_{sub}/M$, and the input signal sampling frequency of TIADC system is $f_s = M \cdot f_{sub}$ ($f_s = 1/T_s$; $f_{sub} = 1/T_{sub}$), which increases M-fold relative to the single-channel ADC. However, the performance of TIADC is sensitive to mismatches among channels. Mismatches between the channel ADCs cause spurious components in the spectrum degrading the signal-to-noise-and-distortion ratio (SNDR).

3. Proposed Calibration Techniques

3.1. An Adaptive Statistics Calibration Scheme Based on LMS Iteration for Offset and Gain Mismatches Calibration. The offset mismatches are mainly caused by the offsets of operational amplifiers and comparators, which are the results of the mismatches of the devices and the asymmetric circuit structures and the fabrication errors. The gain mismatches are mainly due to the capacitor mismatches in the circuits and the parasitic capacitors of MOS transistors and operational amplifiers. The offset voltage of each sub-ADC can be obtained by a cumulative average calculation of the digital outputs of sub-ADCs, and the differences between them are the offset mismatches of TIADCs, while the gain of each sub-ADC can be obtained by a cumulative average calculation of the absolute values of the digital outputs of sub-ADCs. In this work, the calibration of gain mismatch and offset mismatch is cascaded in a scheme as shown in Figure 2, where ABS is the absolute function. We take the first channel as a reference channel; a Least Mean Square (LMS) algorithm is introduced to estimate the offset and gain mismatches between the ith

channel and the reference first channel, which can be written as follows:

$$
\begin{aligned}
os_i(k) &= os_i(k-1) + \mu_o \cdot \left[\widehat{y}_i(k-1) - y_1(k-1)\right], \\
\Delta g_i(k) &= \Delta g_i(k-1) + \mu_g \\
&\quad \cdot \left[\left|\widehat{y}_i(k-1)\right| - \left|y_1(k-1)\right|\right],
\end{aligned}
\tag{1}
$$

where $y_1[k]$ is the kth digital output of the first channel sub-ADC, $y_i[k]$ is the kth digital output of the ith ($i = 2, 3, \ldots, M$) channel sub-ADC, μ_o is the iterative step of offset error, μ_g is the iterative step of gain error, os_i is the offset mismatch within the ith channel, $\Delta g_i = g_1/g_i$ is the gain mismatch between the ith channel and the first channel, and $\widehat{y}_i[k]$ is the calibrated output of the ith channel sub-ADC. After calibration, the output of the i-channel sub-ADC is

$$
\widehat{y}_i(k) = \Delta g_i \cdot y_i[k] - os_i,
\tag{2}
$$

where os_i and Δg_i are the offset and gain mismatches of the ith channel, respectively. In the proposed calibration scheme, an exponential averager is introduced to operate the arithmetic average. Compared with the traditional arithmetic averager, the hardware structure of the exponential averager is simpler; it needs only one adder, two multipliers, and a register as shown in Figure 3. In addition, by using the exponential averager, the gain and offset mismatches error convergence curve can be more smooth and has less output volatility, which will greatly improve the calibration accuracy. Figure 4 shows the response of the exponential averager with different

(a)

(b)

(c)
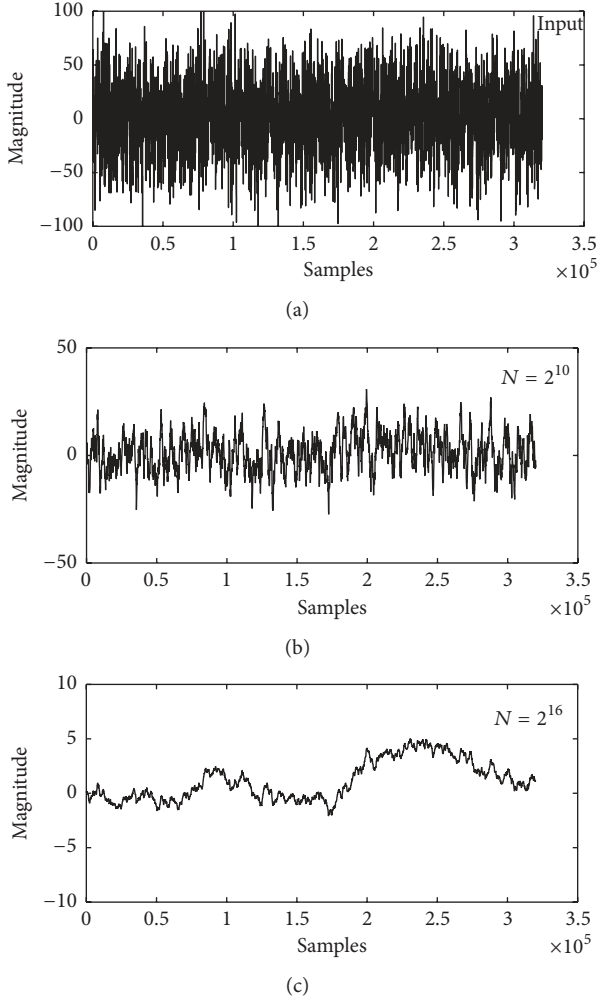
FIGURE 4: Response of exponential averager with different N.

N, where N represents the accumulating point. From top to bottom, they are the input signal and $N = 2^{10}$ and $N = 2^{16}$ output response. It can be seen that, with the increase of N, the output of the exponential averager changes slowly and smoothly.

3.2. Timing Mismatch Calibration Based on an Improved Farrow Filter.

The overall framework of the proposed timing mismatch calibration scheme is shown in Figure 5, where $\downarrow M$ is the downsampling times, $x[n]$ is the digital output of the M-channel TIADC required to be calibrated, and $y[n]$ is the output after calibration. The mismatch estimation module is realized by performing the correlation calculation of the subchannels' outputs. $H_\alpha(z)$ is the improved fractional delay filter based on Farrow structure, whose coefficients change along with the estimated time mismatch to achieve a real-time error correction.

3.2.1. Timing Mismatch Estimation.

Figure 6 shows the time domain description of nonuniform sample in a two-channel TIADC. Ideally, when there is no timing mismatch between
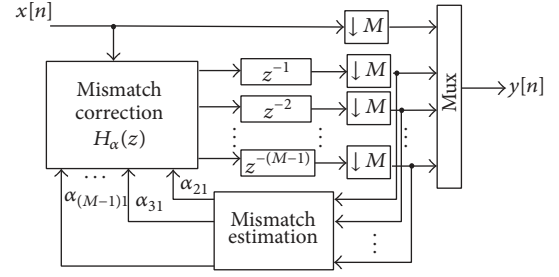

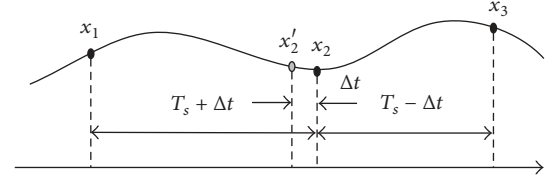FIGURE 5: Block diagram of the proposed calibration scheme.

FIGURE 6: Time domain description of nonuniform sample in a two-channel TIADC.

these two channels, the sampled points of channel 1 and channel 2 are, respectively, x_1 and x_2'. When a timing mismatch Δt occurs, their sampled points change to x_1 and x_2. To illustrate the relationship between the sampled values with the timing mismatch Δt, one can subtract the outputs of channels to get $x_3 - x_2$ and $x_2 - x_1$, where x_3 is the sampled point of the next cycle of channel 1. From a statistical point of view, when the size of samples is large enough, the average difference between $|x_3 - x_2|$ and $|x_2 - x_1|$ is proportional to Δt [15], as shown in the following equation:

$$E\left(\left|x_3 - x_2\right| - \left|x_2 - x_1\right|\right) \propto \Delta t. \tag{3}$$

According to (4), a Least Mean Square (LMS) algorithm can be used to estimate the timing mismatch between the two channels, which can be written as follows:

$$\alpha[n+1] = \alpha[n] \\ + \mu\left(\left|x_3[n] - x_2[n]\right| - \left|x_2[n] - x_1[n]\right|\right), \tag{4}$$

where α ($\alpha = \Delta t/T_s$; T_s is the sampling period of TIADC) is the timing mismatch between the two channels, μ is the iterative step, $x_1[n]$ and $x_2[n]$ are the digital outputs of channel 1 and channel 2, respectively, and $x_3[n]$ is the output of channel 1 of the next cycle with $x_3[n] = x_1[n + 2T_s]$. The specific estimation scheme for a two-channel time-interleaved ADC is shown in Figure 7, where z^{-1} and z^{-2} are both delay units, abs is the absolute function, acc is an accumulator, and $y_n[n]$ is the calibrated output.

Assuming that a four-channel TIADC is considered, we choose channel 1 as a reference channel and calibrate the timing mismatches of channels 2, 3, and 4 with respect to channel 1. The error extraction steps are as follows:

(1) The mismatch errors between channel 3 and channel 1 are firstly estimated, and the estimated error is proportional to $|x_5 - x_3| - |x_3 - x_1|$.
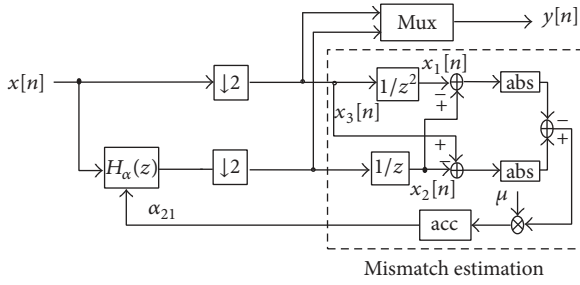
FIGURE 7: Time mismatch calibration technique for a two-channel TIADC.

(2) When channel 3 is calibrated, it can be considered as a reference channel, and the mismatch errors of channel 2 and channel 4 can be estimated. The estimated errors are proportional to $|x_3 - x_2| - |x_2 - x_1|$ and $|x_5 - x_4| - |x_4 - x_3|$, respectively.

So the estimation formula of a four-channel TIADC can be written as

$$
\begin{aligned}
&\alpha_{21}\,[n+1] \\
&\quad = \alpha_{21}\,[n] + \mu\left(\left|x_3\,[n] - x_2\,[n]\right| - \left|x_2\,[n] - x_1\,[n]\right|\right), \\
&\alpha_{31}\,[n+1] \\
&\quad = \alpha_{31}\,[n] + \mu\left(\left|x_5\,[n] - x_3\,[n]\right| - \left|x_3\,[n] - x_1\,[n]\right|\right), \\
&\alpha_{41}\,[n+1] \\
&\quad = \alpha_{41}\,[n] + \mu\left(\left|x_5\,[n] - x_4\,[n]\right| - \left|x_4\,[n] - x_3\,[n]\right|\right),
\end{aligned}
\tag{5}
$$

where α_{21}, α_{31}, and α_{41} are the timing mismatch of channels 2, 3, and 4 with respect to channel 1, respectively. $x_i[n]$ ($i = 1, 2, 3, 4$) corresponds to the output of channel i. $x_5[n]$ is the output of the next cycle of channel 1 with $x_5[n] = x_1[n + 4T_s]$.

3.2.2. Timing Mismatch Correction. Since the parallel alternate sampling time delay of TIADC cannot be precisely controlled, the timing mismatch errors have been a major system error. Commonly, a method that uses a programmable delay line or PLL can realize a precise clock delay adjustment, but this is not enough to meet the ps level clock precision for GHz sampling frequency. In this work, the timing mismatch correction is realized by an all-pass digital filter. Timing mismatch correction uses the delay characteristic of filter to achieve timing mismatch compensation.

Considering only the timing mismatch, the Fourier transform of the output of TIADC is

$$
\begin{aligned}
Y(\omega) = {} &\frac{1}{MT_s} \sum_{i=0}^{M-1} \sum_{k=-\infty}^{\infty} X\left(\omega - k\frac{\omega_s}{M}\right) \\
&\cdot e^{-j(\omega - k(\omega_s/M))\alpha T_s} e^{-jki2\pi/M},
\end{aligned}
\tag{6}
$$

where M is the number of channels of TIADC, α is the timing mismatch between channels, and $Y(\omega)$ is the Fourier
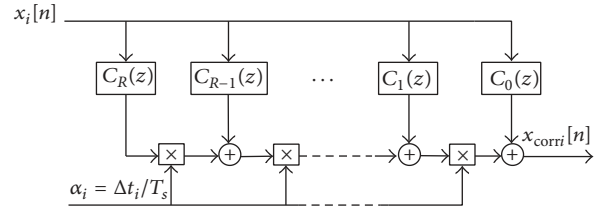

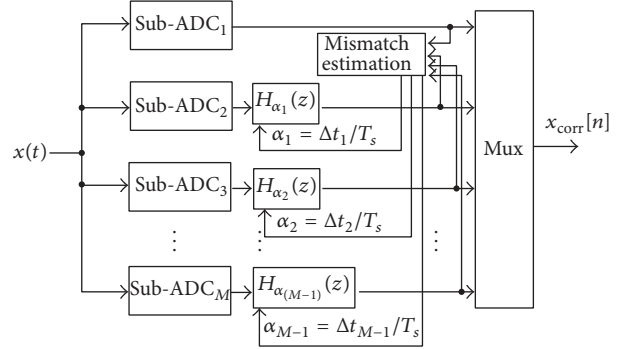FIGURE 8: Block diagram of a filter based on Farrow structure.

FIGURE 9: The traditional calibration scheme with the Farrow filter.

transform of the input signal $x(t)$. Assume that the input signal $x(t) = e^{j\omega_0 t}$, and its Fourier transform is

$$
X(\omega) = 2\pi\delta\left(\omega - \omega_0\right).
\tag{7}
$$

Finally, the Fourier transform of the output of TIADC is

$$
\begin{aligned}
Y(\omega) = {} &\frac{1}{MT_s} \sum_{i=0}^{M-1} \sum_{k=-\infty}^{\infty} 2\pi\delta\left(\omega - \omega_0 - k\frac{\omega_s}{M}\right) \\
&\cdot e^{-j\omega_0 \alpha T_s} e^{-jki2\pi/M}.
\end{aligned}
\tag{8}
$$

Formula (8) shows that the effect caused by the timing mismatch can be corrected by multiplying $Y(\omega)$ with $e^{-j\omega_0 \alpha T_s}$ which can be realized by an ideal all-pass filter. In this design, a filter based on Farrow structure is used to approximate the ideal all-pass filter. Compared with other filters, the order of a Farrow filter will not be required to be very high. It uses the timing mismatch error as one of the filter inputs; even if the timing error changes, it does not need to update the filter order or filter coefficients. The transfer function of a fractional delay filter based on Farrow structure [13] can be realized in the following equation:

$$
H_\alpha(z) = \sum_{k=0}^{p} C_k(z)\, \alpha^k.
\tag{9}
$$

According to the above formula, the filter is divided into many subfilters $C_k(z)$, $k = 0, 1, \ldots, p$. In the meantime, α is made variable; a fractional delay filter based on Farrow structure can therefore be easily implemented as shown in Figure 8.

However, the traditional calibration scheme with the Farrow filter as shown in Figure 9 which has the filter
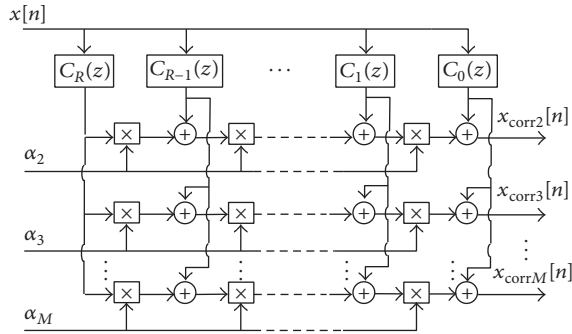
Figure 10: Block diagram of the proposed improved Farrow filter $H_\alpha(z)$.

Table 1: Hardware comparison of the traditional filter and the improved filter.

Channel	The traditional scheme [13]			The proposed scheme		
Channels of TIADC	2	4	8	2	4	8
Adder units	30	90	210	30	40	70
Multiplier units	35	105	245	35	45	75

placed in each subchannel of TIADC tends to have poor calibration effect when the input signal frequency exceeds the subchannel Nyquist sampling rate. In addition, the number of the filters increases with the channels of TIADC, which will consume large hardware resources. Taking into account the identity of these filters, one solution is based on the sharing of the Farrow filter by adopting some extra adders and multipliers. The structure of the improved fractional delay filter is shown in Figure 10. The filter is placed on the digital output of TIADC, α_i ($i = 2, 3, \ldots, M$) is the timing mismatch between channel i and channel 1, $x[n]$ is the digital output of TIADC without calibration, and $x_{\text{corr}i}[n]$ represents the output of TIADC, where channel i is calibrated. Table 1 shows the comparison of the hardware consumption of the traditional filter and the proposed filter. The orders of them are both five. It can be seen that the hardware consumption of the two schemes is almost the same in a two-channel TIADC case. However, with the increase of channel number, the hardware consumption of the proposed structure is much less compared with the traditional one. In addition, since the filter is put at the output of TIADC, the bandwidth of the input signal will be greatly improved.

4. Simulation Results

In order to verify the effectiveness of the calibration algorithms, we implemented them in a 12-bit 4-channel TIADC model in MATLAB platform. The sampling frequency, f_s, is 400 MHz, subchannel S/H frequency is 100 MHz, the input signal is 164.6 MHz, $\mu_o = 2^{-10}$, $\mu_g = 2^{-10}$, and $\mu_t = 2^{-12}$.

Table 2: The channel mismatches of TIADC.

Channel	Channel 1	Channel 2	Channel 3	Channel 4
Offset mismatch	0	0.2	−0.1	0.05
Actual gain	1	0.95	1.03	0.96
Gain mismatch	1	1.053	0.971	1.042
Timing mismatch	0	2% T_s	1% T_s	−1.5% T_s

The accumulating point, N, of the exponential averager is 2^{-16}, the order of the calibration filter is 5, and the coefficients of the filter are calculated through Lagrange interpolation algorithm. The channel mismatches of TIADC are shown in Table 2 (where the first channel is set as the reference channel).

The mismatch convergence process is shown in Figure 11. With the first channel set as the reference channel, only the mismatch errors of the other three channels are calibrated. The proposed calibration method allows estimating the three mismatch errors accurately and fast in about 1.0×10^4 samples. Figure 12 shows the TIADC output spectrum before and after calibration. Before calibration, the distortions caused by channel mismatches appear at frequencies ($f_s/4 \pm f_{\text{in}}$), $f_s/4$, and ($f_s/2 - f_{\text{in}}$), limiting the signal-to-noise-and-distortion ratio (SNDR) of the TIADC to 22.5 dB. After calibration, the distortions due to mismatches are minimized, and the SNDR is improved to 71.8 dB; ENOB is improved to 11.6 bits.

Figure 13 shows the SNDR performance versus the normalized input frequency of TIADC with offset and gain mismatches before and after calibration. Before calibration, the SNDR is dropped around 24 dB, and SNDR has no relation with the input frequency and is nearly constant in the whole Nyquist frequency. When the calibration is enabled, the proposed calibration scheme based on LMS iteration is able to compensate the offset and gain errors. The SNDR is much close to the situation without mismatch errors in the entire Nyquist frequency range. Figure 14 shows the SNDR performance versus the normalized input frequency of TIADC with the same timing mismatch before and after calibration. Before calibration, the SNDR is inversely proportional to the input signal frequency as the timing mismatch has more influence for higher input frequencies. When the input signal frequency approaches Nyquist frequency, the SNDR decreases to 30 dB. When the timing mismatch calibration is enabled, the proposed scheme is able to compensate the timing errors. After calibration, the spurious spectrum is greatly disappeared, and SNDR improves. A good calibration effect with a normalized input frequency from 0 to $0.4 f_s$ with SNR above 72 dB can be seen. With the continued increase of the normalized input, the proposed calibration scheme still can enhance the SNDR; however, the calibration effect is not so good as before. The reason for the decline is that the proposed Farrow filter is realized by the Lagrange interpolation approximation; the interpolation effect will be reduced when the input signal frequency approaches the Nyquist frequency.

Previous analyses are based on a single-frequency input signal, since the nature signal is not of single frequency
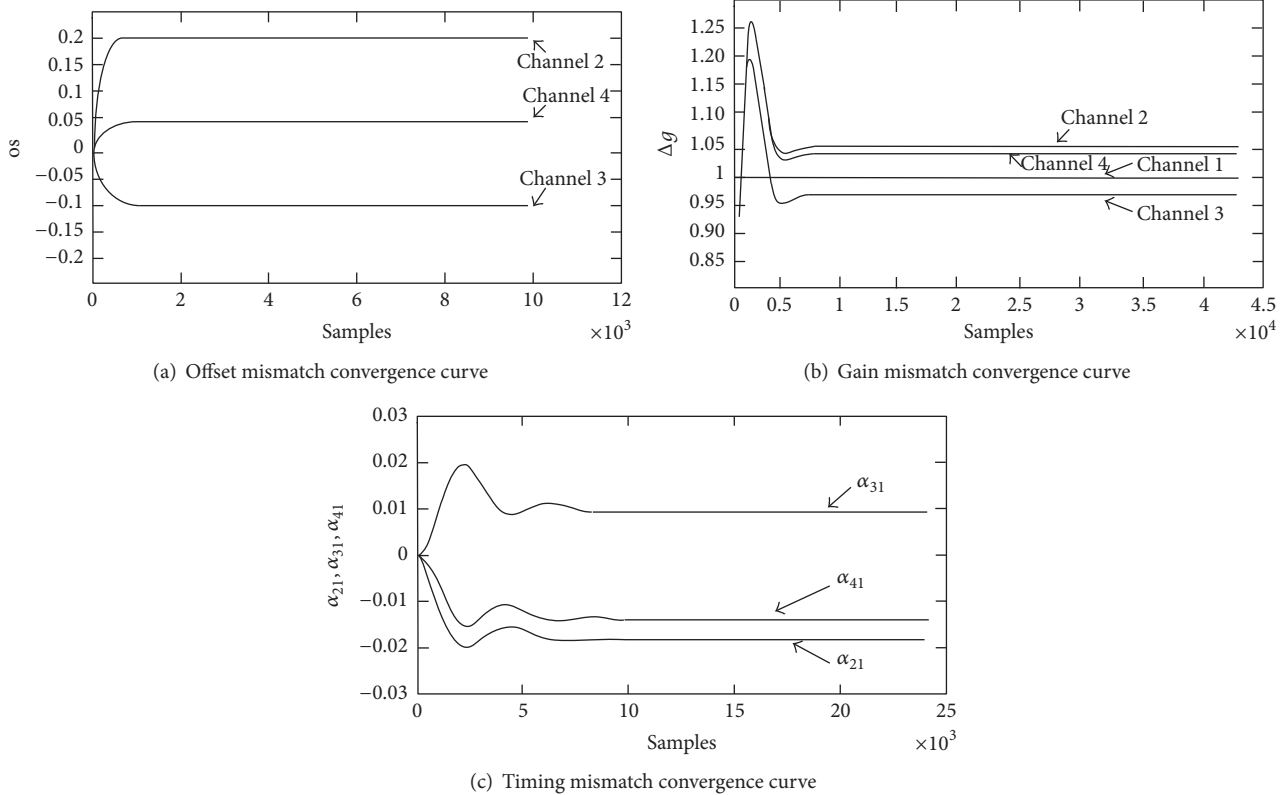
(a) Offset mismatch convergence curve

(b) Gain mismatch convergence curve

(c) Timing mismatch convergence curve

FIGURE 11: Convergence curves of the proposed calibration method.

(a) Before calibration
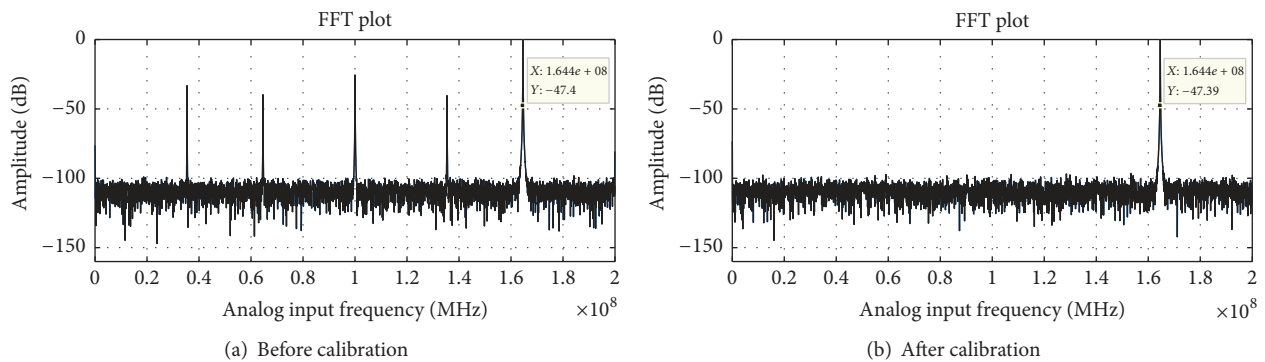

(b) After calibration

FIGURE 12: Dynamic analysis results with single-frequency input signal.

and is often complicated by a number of different frequency components. Here, we further verify the proposed calibration techniques with a multifrequency input signal. The multifrequency input signal is composed by several noramlized frequencies: 0.064, 0.129, and 0.194. In order to prevent exceeding the ADC conversion range, the input signal magnitude is reduced to 0.9. Figure 15 is TIADC output spectrum before and after calibration. It can be clearly seen that the spurs caused by channel mismatch errors of TIADC have been greatly depressed after calibration.

Table 3 compares the performance of this work with other systems; this work uses fewer resources, and the convergence time is also shorter than that in other references.

5. Conclusion

In this paper, we focus on all-digital calibration structures and algorithms to mitigate the impact of mismatches of TIADC; the presented calibration methods have the merits of low hardware resource consumption and fast calibration.

TABLE 3: Performance comparison.

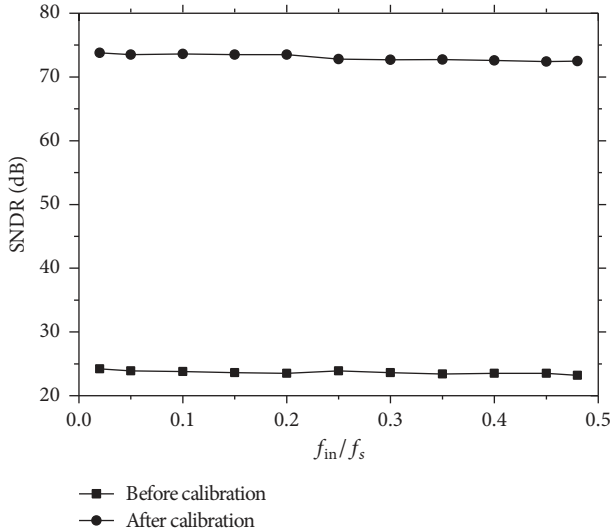|	[13]	[14]	[8]	This work
Channels	4	4	16	4
Mismatch types	Timing	Gain, timing	Gain, offset, timing	Gain, offset, timing
Filter (taps)	11	82	31	**5**
Adders	100	/	10^6	49
Multipliers	125	/	10^6	53
Convergence time (samples)	4×10^4	10^5	10^5	1.0×10^4

FIGURE 13: SNDR versus normalized input frequency (with offset and gain mismatches).
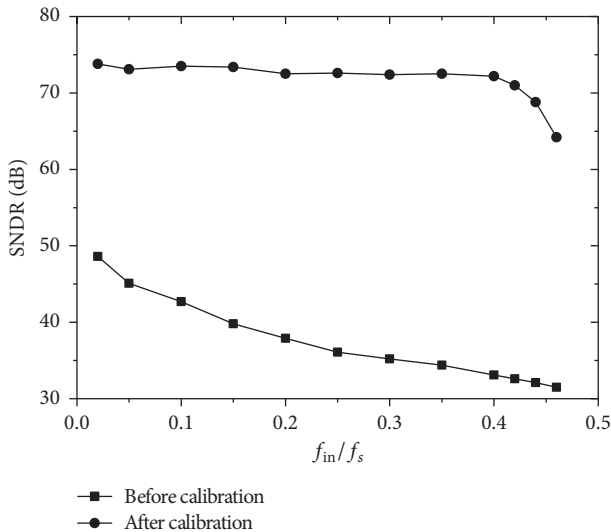

FIGURE 14: SNDR versus input frequency (with timing mismatch).

Simulation results show that the performance of TIADC is enhanced significantly by using the proposed calibration technique.
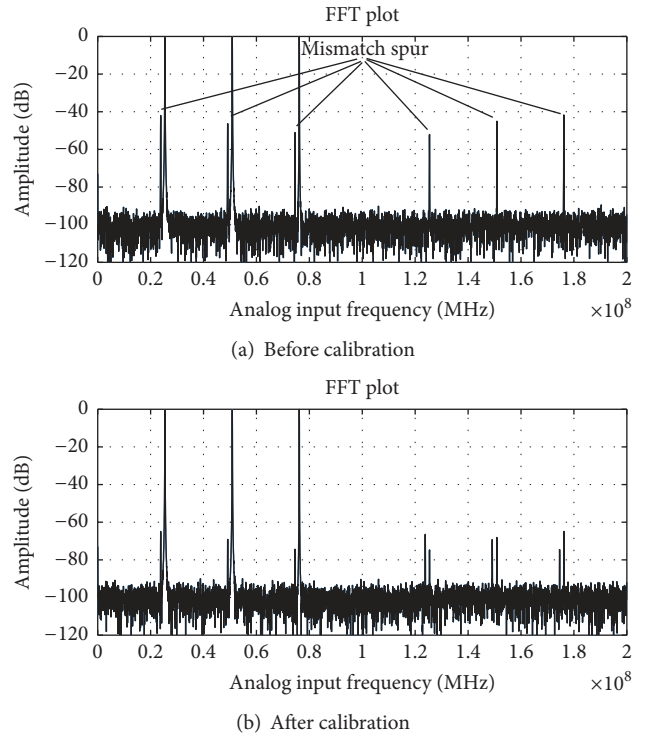

(a) Before calibration

(b) After calibration

FIGURE 15: Dynamic analysis results with multifrequency input signal.

Competing Interests

The authors declare that they have no competing interests.

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