A Low-Consumption Regulated Gate Driver for Power MOSFET

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***Abstract*—Driving power MOSFET at high switching frequency may induce significant switching power losses. A gate driver with low energy consumption is proposed for power MOSFET in switching power conversion applications. The proposed gate driver regulates the output gate driving voltage for minimizing the loss of charging and discharging the gate capacitor. No extra off-chip components are required, and hence, the proposed approach can be completely designed on chip. A 40 V/0.5 μm CMOS technology is utilized and experiments on a boost converter are performed. The power dissipation of the proposed gate driver, compared with the conventional gate driver, can be reduced up to 15.5% and 55.4% under 15 V and 30 V supply voltage, respectively.**

***Index Terms*—Gate driver, high frequency, power MOSFET, switching loss.**

I. Introduction

GENERALLY speaking, to decrease the size and weight of a switching power converter is a common target for power supply design. One effective way to reduce the volume and weight of the passive bulky inductor and capacitor is to increase the switching frequency. However, to operate a switching power supply at high switching frequencies, the switching loss is of great concern. The switching loss is mainly generated from the power MOSFET and the output rectifier. Though the power loss may be reduced by selecting better components with lesser power-consuming characteristics, the cost will usually increase as well.

Another way to decrease the switching loss is to modify the gate driving method for the power MOSFET. There have been several gate drive schemes which use resonant techniques to reduce the driving power loss. A typical resonant gate driver, as shown in Fig. 1, uses a bulky capacitor $C_{\rm o}$ in series with inductor L_r [1]. The charges stored in C_g during turn-ON could be recovered to $C_{\rm o}$ while turning OFF. The off-chip devices, such as inductors and capacitors in the gate driver circuit, are undesirable as far as the weight and volume issues are concerned.

Another approach that limits the supply voltage of the gate driver to achieve a better overall efficiency is proposed [2], [3]. A supply-voltage-limited-type driving circuit [2], shown in Fig. 2(a), requires additional components M_1, $C_{\rm OUT}$, and a bias circuit compared with the conventional gate driver. The bias circuit regulates $V_{\rm bias}$, which is set by the reference voltage $V_{\rm ref}$

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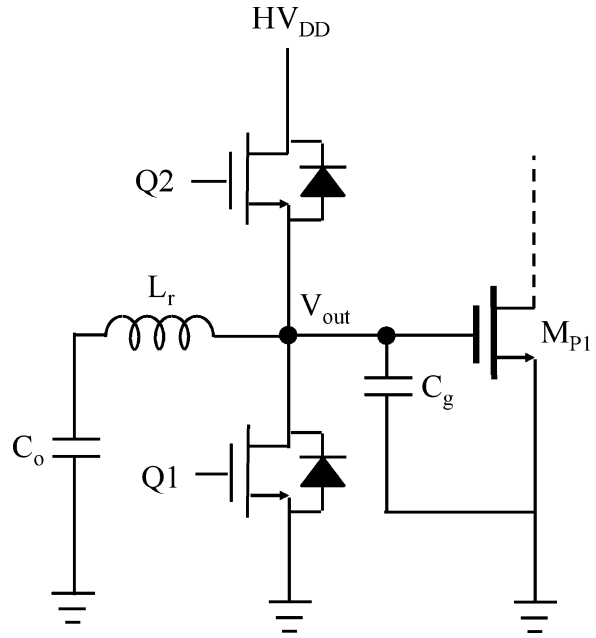


Fig. 1. Resonant gate driver.

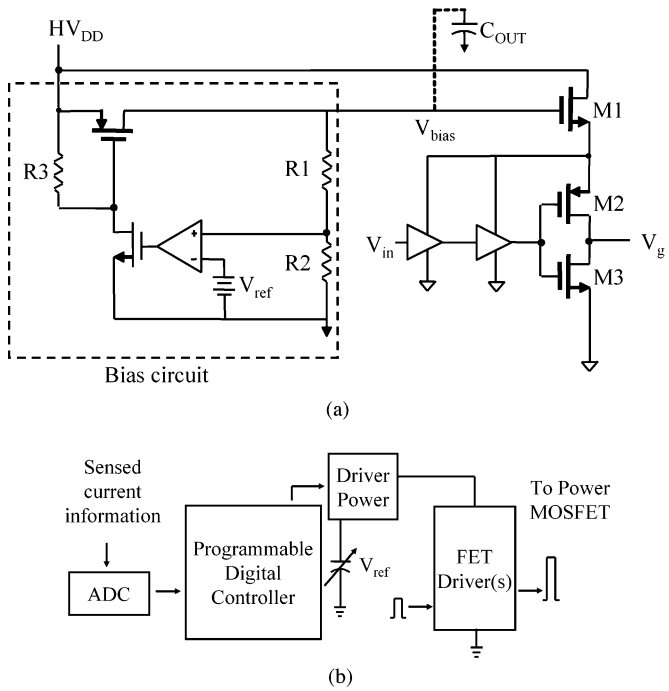


Fig. 2. Supply-voltage-limited-type gate driver. (a) Gate driver with wide operating voltage range. (b) Drive voltage optimizer controller.

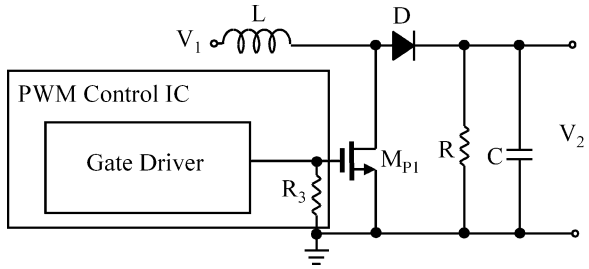


Fig. 3. Boost-type switching converter.

and the ratio of R_1 and R_2. The drain to source voltage of M_{10} is adjusted by the negative feedback loop which is made of R_3, M_{20}, and the error amplifier such that $V_{\rm bias}$ remains regulated. In this way, the maximum voltage of V_g is limited by $V_{\rm bias}$ and the gate to source voltage of M_1. Therefore, V_g can be regulated to a desired value to reduce P_C. The capacitor $C_{\rm OUT}$ is added in order to hold $V_{\rm bias}$. However, $C_{\rm OUT}$ would occupy a huge chip area if built on chip. While off-chip, it would also require additional board size. The drive-voltage-optimizer (DVO) controller [3], shown in Fig. 2(b), was proposed in a similar, but digital, way. It receives the sensed current information and converts to a digital signal for the digital controller. The driver power circuit accepts the controller command and regulates the supply voltage to the gate driver. With lower supply voltage, the switching loss is thus reduced.

However, the DVO-type controller with the stack structure on the gate driver may result in significant power consumption during switching. A gate-charge modulation control circuit is presented in [4] to control the ON-time duration of the pull up/down device in the gate driver. The desired voltage value of the gate driver output can be obtained. Only simulation is provided and the design of the ON-time duration control circuit is not mentioned. In addition, the driver in [5] combines the principles proposed in [1] and [4] to increase the efficiency and is implemented by chip design. However, a gate-charge-recycling controller is needed in order to integrate the resonant driving technique in [4], but the controller is not described in detail. Moreover, combining the resonant driving technique requires a build-in inductor for the resonant, which would occupy a huge silicon area.

In this paper, a new gate driver circuit with complete analysis is proposed to reduce the switching loss and part of the idea has been presented at the IEEE Applied Power Electronics Conference [6]. Experimental results show that the efficiency of the regulated gate driver is improved by 55.4% with 30 V supply voltage compared with the nonregulated gate driver.

II. Strategies for Improving the Gate Driver Power Loss

The presented gate driver can be used in different topologies of power conversion system and Fig. 3 gives an example of a simple boost-type switching power supply system. In this system, the pulsewidth modulation control IC includes a gate driver to turn ON/OFF the power MOSFET M_{P1} to achieve power conversion from V_1 to V_2. In order to prevent M_{P1} from false turning-ON while the system is not operating, a discharge resister R_3 is connected between the gate terminal of M_{P1} and ground to keep the gate voltage low.

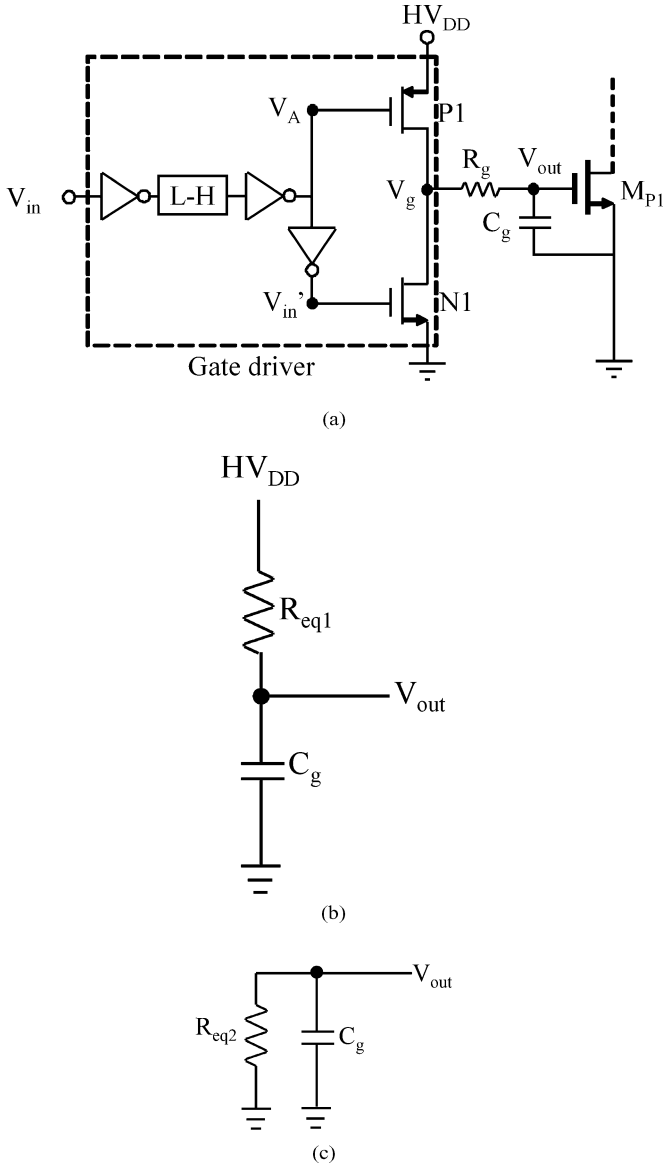


Fig. 4. Gate driver with power MOSFET load and its operation equivalent circuit. (a) The conventional gate driver with power MOSFET load. (b) Charging equivalent circuit. (c) Discharging equivalent circuit.

The gate driver's output is connected to the gate of the power MOSFET and an equivalent parasitic gate capacitor C_g is shown between $V_{\rm out}$ and ground. Equivalent circuits for the charging and discharging operations of the conventional gate driver in Fig. 4(a) [1], [7] can be modeled as simple *RC* circuits shown in Fig. 4(b) and (c), respectively. In the charging period, $\rm HV_{DD}$ supplies the charging current flowing through the $R_{\rm eq1}$, which is the equivalent of the P_1 ON-resistance in series with R_g, to C_g, and during the discharging period, C_g is discharged through the $R_{\rm eq2}$, the equivalent of the N_1 ON-resistance plus R_g.

The total power loss in driving a power MOSFET can be expressed by the following equation [7]:

$$P_C = \mathrm{HV}_{\mathrm{DD}}^2 C_g f. \tag{1}$$

In the proposed gate driver, the driver output V_{out} will be regulated and may not be as high as $\mathrm{HV}_{\mathrm{DD}}$. Power consumption for charging and discharging C_g can be derived from the following steps. First, in the charging period, C_g is charged by $\mathrm{HV}_{\mathrm{DD}}$, as shown in Fig. 4(b). Therefore, the current from $\mathrm{HV}_{\mathrm{DD}}$ can be shown as

$$I dt = C_g dV_{\mathrm{out}} \tag{2}$$

where I is the current provided by $\mathrm{HV}_{\mathrm{DD}}$. Therefore, the total charges Q can be derived by integrating both sides of (2) as

$$Q = It = C_g V_{\mathrm{out}}. \tag{3}$$

Therefore, the energy consumed from $\mathrm{HV}_{\mathrm{DD}}$ is equal to $Q \times \mathrm{HV}_{\mathrm{DD}}$ in the charging period.

As the discharging period is considered, P_1 is cut OFF and N_1 is turned ON by $V_{\mathrm{in}'}$. The stored energy on C_g is totally discharged to ground. Therefore, by averaging the energy consumed in each switching period T, the power P_C provided by $\mathrm{HV}_{\mathrm{DD}}$ is given by

$$P_C = \frac{Q}{T}\mathrm{HV}_{\mathrm{DD}} = \mathrm{HV}_{\mathrm{DD}} V_{\mathrm{out}} C_g f. \tag{4}$$

To reduce P_C, there are three possible factors that can be controlled. They are $\mathrm{HV}_{\mathrm{DD}}$, V_{out}, and C_g. In normal off-line ac-to-dc switching power converters, $\mathrm{HV}_{\mathrm{DD}}$ usually comes from an auxiliary winding. It varies with the loading conditions and usually cannot be controlled precisely. Furthermore, C_g, the equivalent parasitic gate capacitor, is majorly determined by the fabrication process technology and the physical die size of the power MOSFET. It is not adjustable after production. Nevertheless, adjustment of V_{out} to decrease P_C seems to be a more convenient way to minimize the switching loss. Circuit design techniques provide the capability of V_{out} regulation.

To provide a feasible gate drive voltage, characteristics of the power MOSFET turn-ON resistance under different gate driving voltages needs to be investigated. The turn-ON properties of some commonly used high-voltage power MOSFETs is shown in [8]–[13]. The required turn-ON voltage for driving a power MOSFET is about 10 V and R_{ON} of the power MOSFET is not reduced significantly by increasing the gate drive voltage. A typical gate driver directly applies $\mathrm{HV}_{\mathrm{DD}}$ to drive C_g and $\mathrm{HV}_{\mathrm{DD}}$ usually varies from 15 to 30 V in normal operations. Therefore, the turn-ON voltage can be lowered for decreasing P_C.

III. Principle and Operation of the Proposed Regulated Gate Driver

The proposed regulated gate driver circuit is shown in Fig. 5. It consists of a pull-up circuit, a gate resistance R_g, a pull-down circuit, and a feedback circuit. The purpose of the feedback loop is to regulate V_B to be equal to V_{in}. When the input voltage V_{in} is logic high, V_B is regulated and V_g is set equal to

$$V_g = \left(1 + \frac{R_1}{R_2}\right) V_{\mathrm{in}}. \tag{5}$$

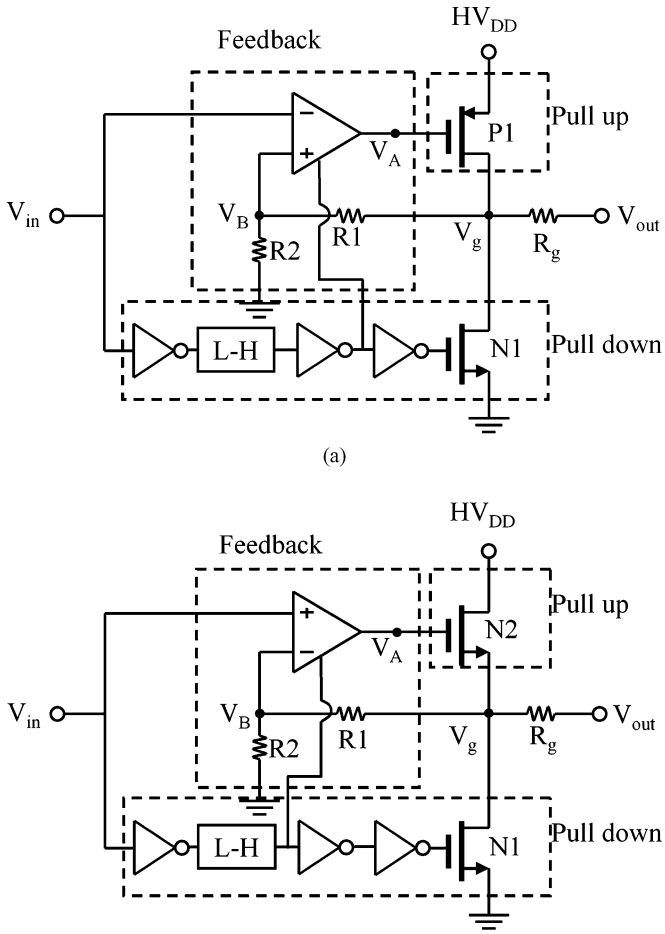


Fig. 5. Proposed regulated gate driver circuit. (a) p-type pull-up gate driver. (b) n-type pull-up gate driver.

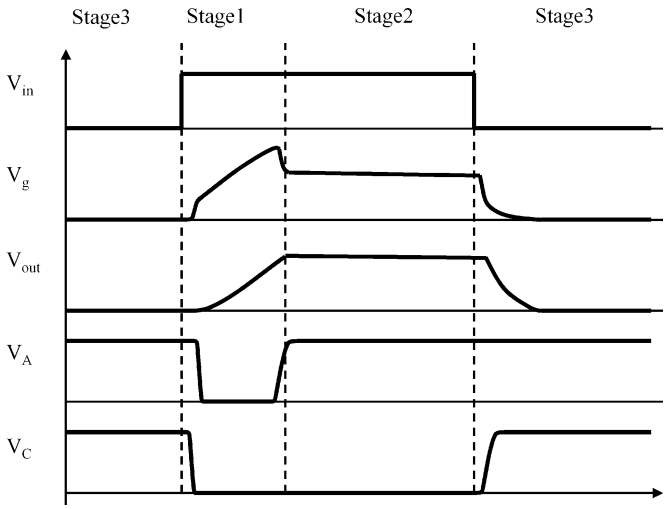


Fig. 6. Some key waveforms of the proposed driver.

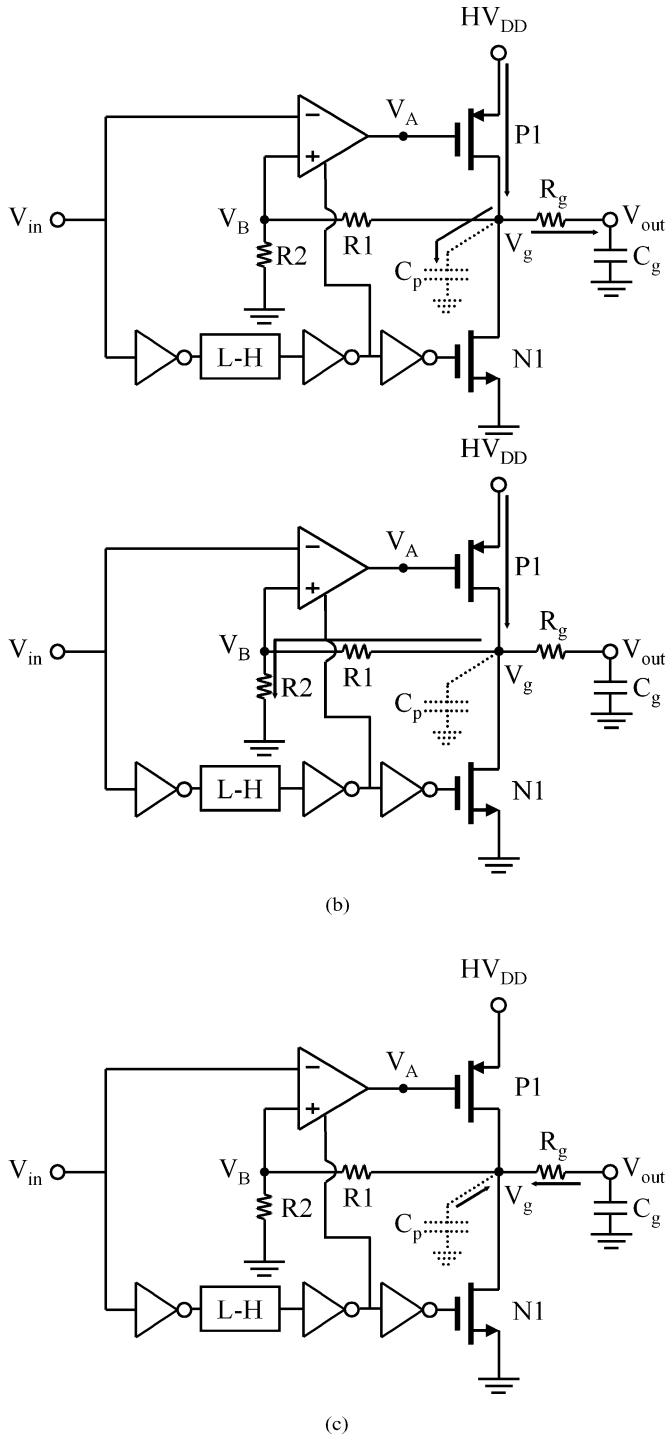


Fig. 7. Operation modes of the proposed p-type pull-up gate driver. (a) Stage1. (b) Stage2. (c) Stage3.

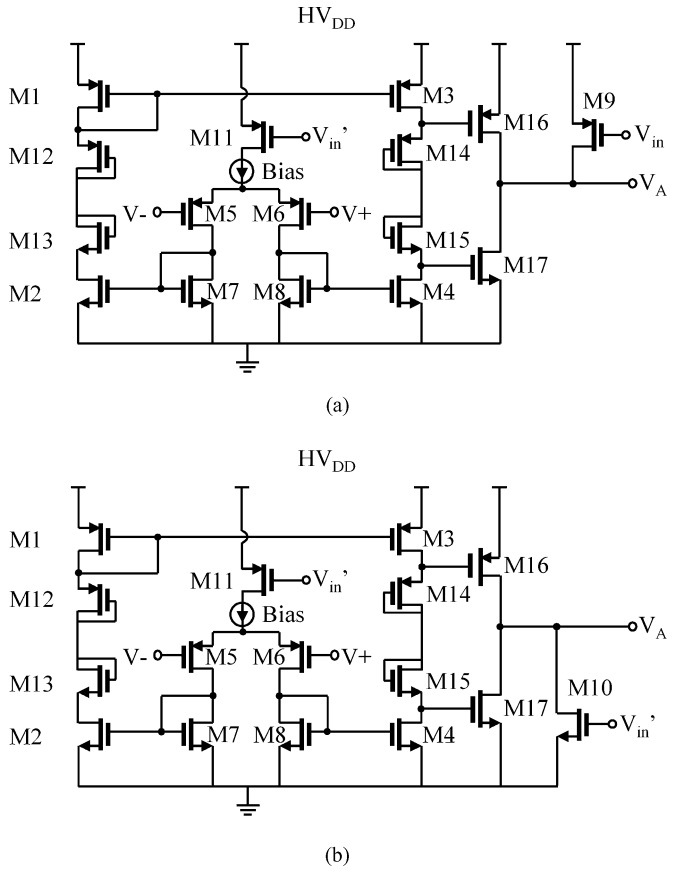


Fig. 8. Schematics of the error amplifiers for the proposed gate driver circuit. Schematic of the OpAmp for: (a) p-type pull-up gate driver, and (b) n-type pull-up gate driver.

Hence, the proposed gate driver can adjust the gate voltage supplied by the output node for different applications. The feedback resistors R_1 and R_2 can be implemented either on-chip or off-chip. The circuit operations will not be affected. It could be set off-chip to increase the design flexibility to meet the various input voltage levels of driver in real applications. R_3 in Fig. 3 can be eliminated as the feedback resistors R_1 and R_2 in Fig. 5 can perform the role of discharging. Moreover, the power dissipation of the proposed gate driver is less than the gate driver with a wide operating range shown in Fig. 2(a), because it requires additional feedback resistors.

A circuit design of the proposed gate driver is given in Fig. 5(a). The pull-up circuit is implemented by PMOS and the pull-down circuit by NMOS with an inverter. The feedback circuit consists of R_1, R_2, and an error amplifier, which may be a comparator or an operational amplifier (OpAmp). It should be noticed that the pull-up circuit can also be implemented by NMOS, as shown in Fig. 5(b). Since NMOS has better driving capability, the physical die size may be smaller. However, for normal operations, the lowest $\mathrm{HV_{DD}}$ should be higher than the p-type pull-up driver for the N_2 gate-to-source threshold voltage.

The proposed gate driver can significantly reduce the chip area since it only uses one transistor for the pull-up circuit, instead of two in the circuit of Fig. 2(a). Moreover, it does not require an additional reference voltage because it uses the input logic level as the reference. The complexity of the proposed driver circuit is slightly increased by adding an error amplifier compared to a conventional gate driver. The extra chip area caused by the error amplifier is less than 10% in our implementation. In order to analyze the operation of the proposed gate driver, Fig. 6 provides qualitative time-scale representations of voltages at important nodes and the corresponding steady-state operation modes are

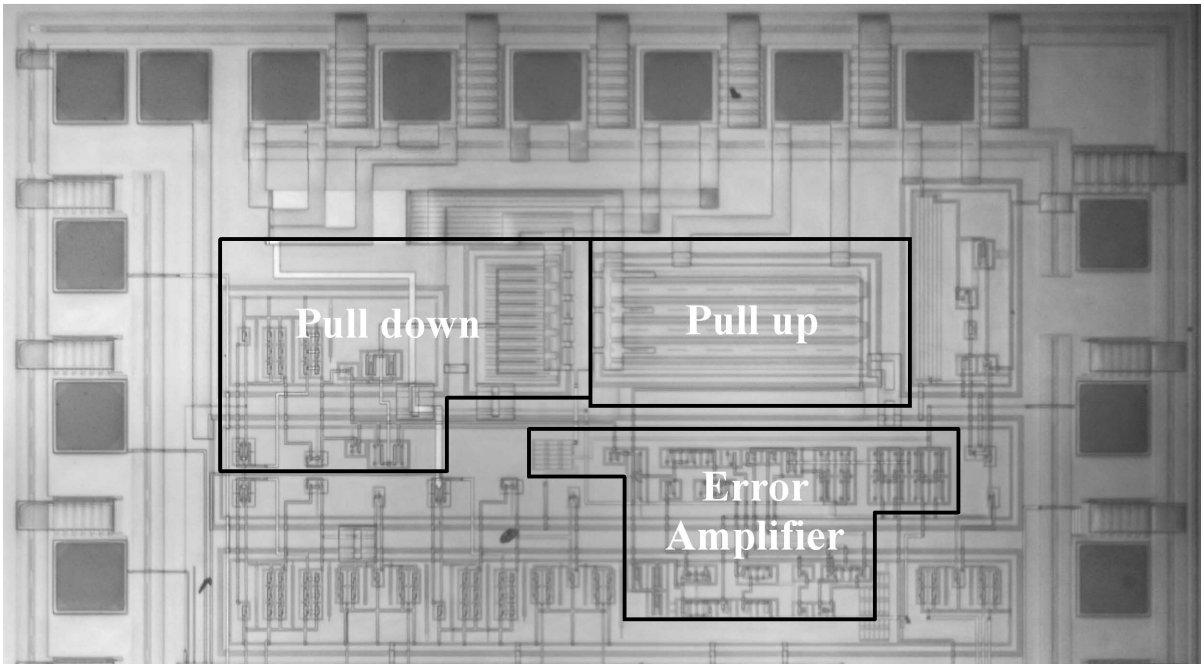


Fig. 9. Chip microphotograph of the proposed driver.

shown in Fig. 7. The steady-state operation is divided into three stages as follows:

A. Stage 1

Fig. 7(a) shows the circuit operation during this stage. At the beginning of this stage, $V_{\rm in}$ turns to logic high and V_A decreases. Therefore, P_1 is ON and most of the current I_{P1} flows through the parasitic capacitance C_P such that V_g is pulled up. C_g is charged until V_B reaches $V_{\rm in}$.

B. Stage 2

Fig. 7(b) shows the circuit operation when V_B equals V_i. When a comparator is utilized as the error amplifier, P_1 is turned OFF and C_g provides the current through R_1 and R_2 to ground. Therefore, $V_{\rm out}$ and V_g will slightly decrease. On the other hand, if an OpAmp is used as the error amplifier, the feedback loop would set V_B equal to $V_{\rm in}$. $V_{\rm out}$ and V_g are fixed at this stage.

C. Stage 3

Fig 7(c) shows the circuit operation when $V_{\rm in}$ switches to logic low. V_A is pulled up to $\rm HV_{DD}$ to turn OFF P_1 and the gate voltage of N_1 is pulled high to turn ON N_1. C_g is discharged through R_g and N_1.

However, care should be exercised when $V_{\rm in}$ is low. As $V_{\rm in}$ is low and N_1 is turned ON, V_g would be pulled down to ground level. The output voltage of the error amplifier is not well defined since both inputs of the error amplifier, $V_{\rm in}$ and V_B, are near the ground level. Malfunction might appear due to ground noises. To avoid N_1 and P_1 being turned ON at the same time, a protection mechanism in the utilized error amplifier is designed. In Fig. 8(a), M_9 pulls the output voltage of the error amplifier to $\rm HV_{DD}$ as $V_{\rm in}$ is low to avoid the possible malfunction. In the n-type pull-up gate driver, M_{10} is added to ensure that the pull-up circuit would be shut down when $V_{\rm in}$ is low, as shown in Fig. 8(b). Also, M_{11} is added to turn OFF the bias current of the error amplifier when $V_{\rm in}$ is low so as to further reduce the power consumption of the error amplifier.

IV. Experimental Results

For experimental verification, the proposed gate driver is designed and fabricated using a 40 V/0.5 μm CMOS technology. An OpAmp is adopted for the error amplifier. Fig. 9 shows the chip microphotograph of the p-type pull-up gate driver. The chip area is 1.2 mm $\times$ 0.6 mm.

The power consumption of the proposed gate driver is compared with a nonregulated gate driver which is built by adjusting the scaling resistors R_1 and R_2 of the p-type gate driver in Fig. 5(a). In this way, the gate voltage is not regulated and charged to $\rm HV_{DD}$ when $V_{\rm in}$ is logic high. In order to measure the reduced power dissipation of the regulated gate driver, a switching boost-type power stage, as shown in Fig. 1, is constructed. The regulated gate voltage is set to 13 V and the logic voltage is 5 V. The feedback resistors R_1 and R_2 are designed to be 40 kΩ and 25 kΩ in the driver according to (5). In the following experiments, the Infineon SPP20N60C3 [11] is used for M_{P1} to verify the regulated function and measure the power consumption of switching loss and conduction loss. A pulse generator is adopted as the input to the driver.

The input and output waveforms of the gate driver are shown in Fig. 10, in which $V_{\rm in}$ changes from 0 to 5 V and back to 0 V as a square wave with a turn-ON time of 8.4 μs. The supply voltage $\rm HV_{DD}$ is set to 15 V in Fig. 10(a), 20 V in Fig. 10(b), and 30 V in Fig. 10(c), respectively. When $V_{\rm in}$ is 5 V, $V_{\rm out}$ is charged and regulated to 12.7 V in steady state. With higher

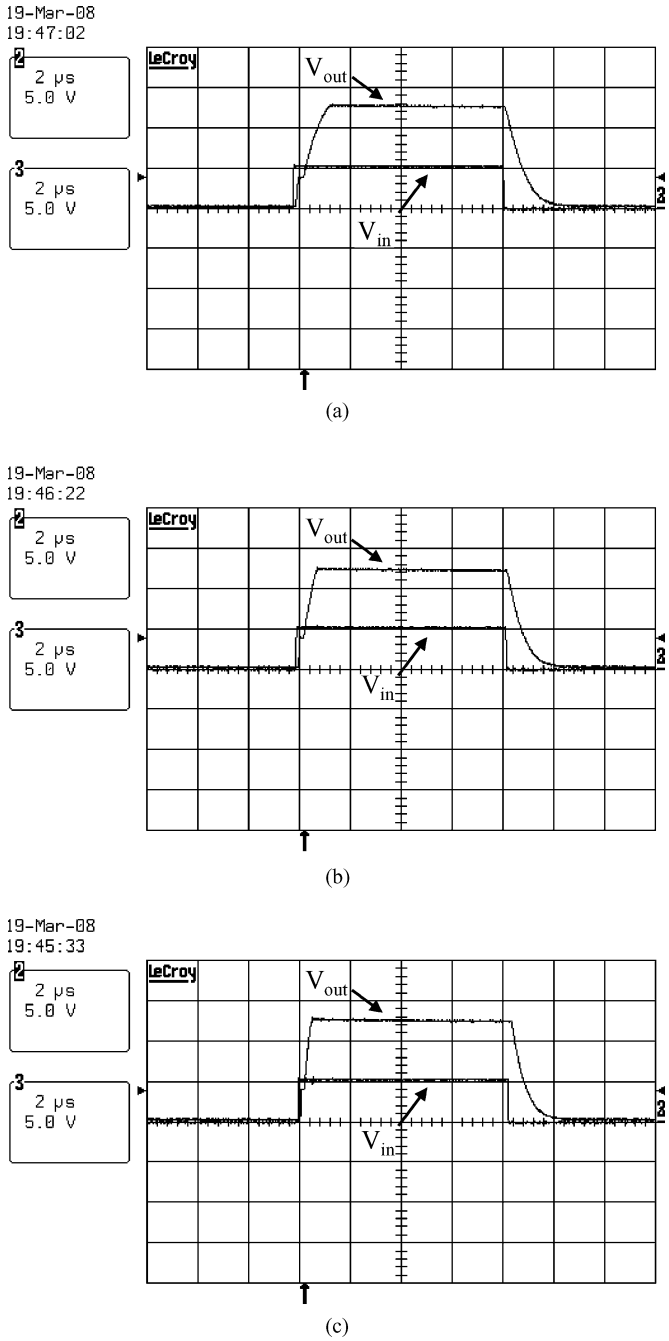


Fig. 10. Input and output waveforms of the regulated gate driver. (a) 15 V HV_{DD}. (b) 20 V HV_{DD}. (c) 30 V HV_{DD}.

HV_{DD}, the driving capability of the gate driver is improved so that the rise time of the gate driver output voltage is shorter, as shown in Fig. 10(a)–(c).

Fig. 11 shows the total power consumption of the proposed gate drivers versus the switching frequency from 20 to 160 kHz and the HV_{DD} is set to 15 V. The solid line is the power consumption of the proposed gate driver and the dashed line is the power consumption of the nonregulated gate driver. For the proposed gate driver, the power consumption increases from 25.37 to 242.5 mW as the frequency increases from 20 to 160 kHz. For the nonregulated gate driver, power consumption changes from

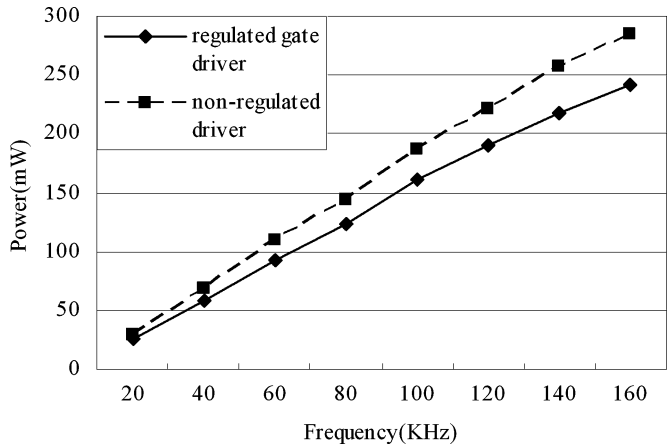


Fig. 11. Power consumption at different frequencies with 15 V HV_{DD}.

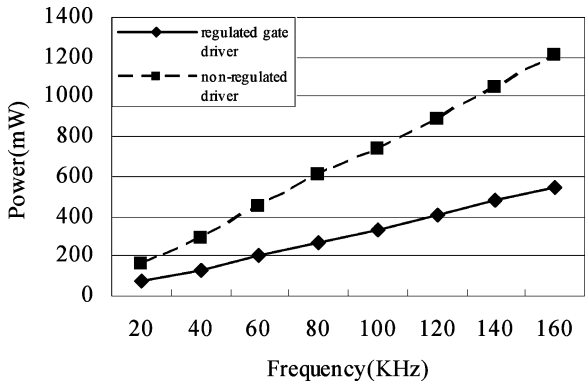


Fig. 12. Power consumption at different frequencies with 30 V HV_{DD}.

30 to 285 mW. As a result, the power consumption dissipated by the proposed gate driver can be reduced by 15.5% under 15 V HV_{DD}. Fig. 12 shows the power consumption under 30 V HV_{DD}. The power consumption increases from 72 to 546 mW for the proposed regulated gate driver and 156 to 1205 mW for the nonregulated gate driver. The power consumption dissipated by the gate driver can be reduced by 55.4% under 30 V supply voltage. To express the efficiency improvement, the power saving ability η is defined

$$\eta = \frac{P_{\text{nonregulated}} - P_{\text{regulated}}}{P_{\text{nonregulated}}} \times 100\%. \tag{6}$$

This index gives a quantitative picture of power consumption reduction of the proposed regulated gate driver. Fig. 13 shows the power saving ability relationship with switching frequency and supply voltage. Obviously, the changes of supply voltage affect the η more than the switching frequency. It is clear that the supply voltage play a more significant role.

In addition to the power consumption on charging/discharging gate capacitance, the total loss of a power MOSFET should include turn-ON/OFF switching and the conduction loss, as shown in Fig. 14. Regulating the driver output voltage would also affect the turn-ON/OFF loss and the loss of charging/discharging gate capacitance. When the driver output translates from low to high, the regulated gate driver would suffer

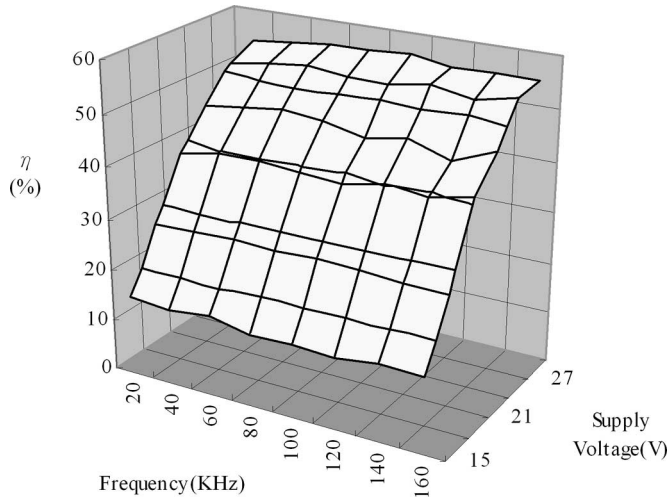
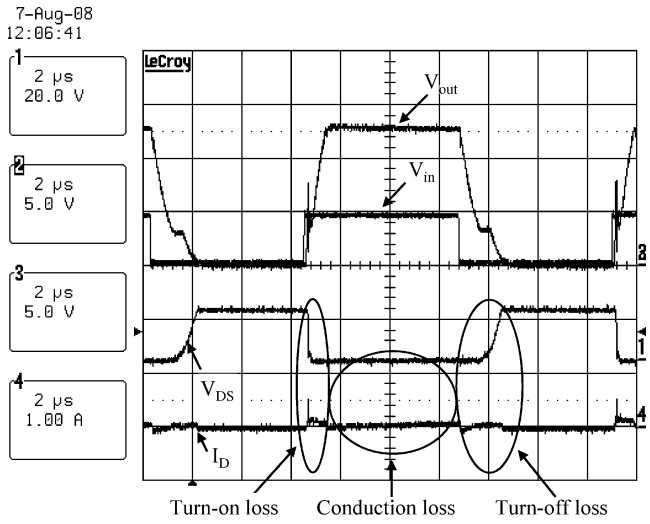
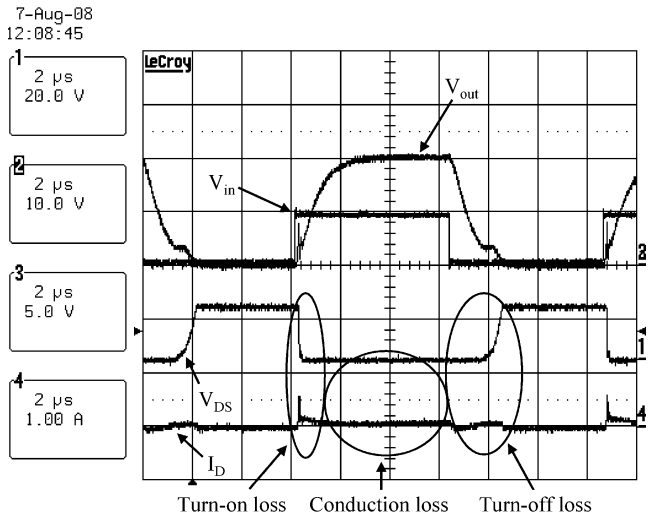


Fig. 13. Power saving ability at different supply voltages.



(a)



(b)

Fig. 14. Gate driver and the power MOSFET waveforms with 80-KHz switching frequency. (a) Regulated gate driver. (b) Nonregulated gate driver.

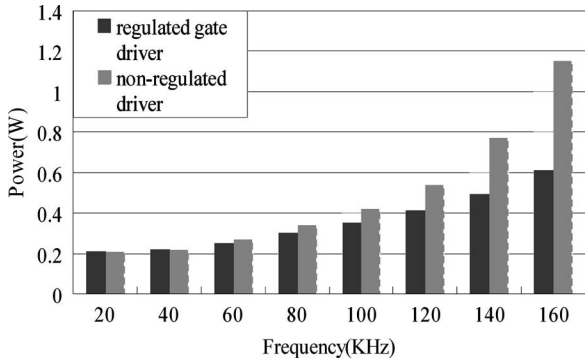


Fig. 15. Turn-ON/OFF and conduction loss of power MOSFET.

TABLE I
INPUT CAPACITANCE AND THRESHOLD VOLTAGE OF POWER MOSFET

Power MOSFET Type	Cg (pF)	Vth (V)
I ST P4NK60ZFP	510	3.75
II FSR SSS4N60B	710	3
III ST P60NF06	1810	3
IV Infineon SPP20N60C3	2400	3
V ST W20NK50Z	2600	3.75
VI ST W8NC90Z	3550	4

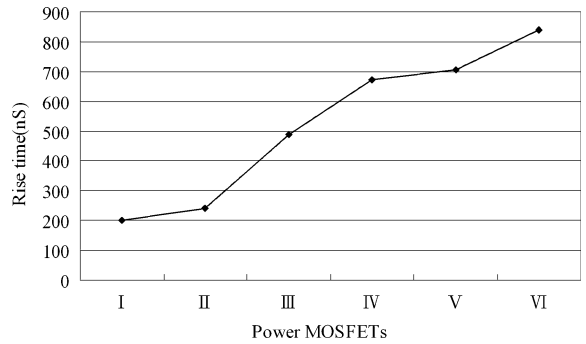


Fig. 16. Risetime of power MOSFETs in Table I.

a little more turn-ON loss than nonregulated drivers due to the slightly slower charging speed while traversing through the linear operation region upon regulation. However, when the driver output translates from high to low, the lower gate voltage of proposed driver would be pulled to ground sooner. This would reduce the turn-OFF loss. Fig. 15 shows the total turn-ON/OFF switching and conduction losses with 20 V $\mathrm{HV_{DD}}$ and constant load. The result shows that the nonregulated driver consumes more power. However, it might not be fair to calculate the power saving ability of the power consumption in Fig. 15 as the conduction loss would vary with different loads.

To observe the effect of variation of the input capacitance C_g and threshold voltage V_{th} on the turn-ON speed of M_{P1}, six

different power MOSFETs [8]–[13] listed in Table I are utilized for experiments. Fig. 16 shows the risetime of each power MOSFET in Table I. The $V_{\rm th}$ of power MOSFET usually ranges from 3 to 5 V and it would be quickly overtaken when the driver begins to charge C_g. The C_g value would be the parameter that dominates the turn-ON speed, as shown in Fig. 16. The larger C_g results in the longer risetime.

V. Conclusion

A low-consumption gate driver for power MOSFET in switching power supplies has been proposed. The total power consumption of the proposed gate driver can be divided to static and dynamic power loss. The static loss includes the error amplifier power and the power consumption of $R_1 + R_2$ during the turn-ON period. The major part of the dynamic loss is the pull-up and pull-down losses, mainly due to charging and discharging of the equivalent parasitic gate capacitance. In high-frequency switching power applications, the dynamic loss may dominate because it grows as the switching frequency increases. The proposed gate driver eliminates unnecessary gate driving voltage to reduce the dynamic loss. The efficiency can, therefore, be improved.

The proposed gate driver is completely designed on chip and does not need extra off-chip components. Moreover, it is simpler than other efficient gate drivers in the literature. The proposed gate driver has been designed and fabricated using a 40 V/0.5 μm CMOS technology. Experiments are performed on a simple boost converter with the regulated gate driver. Compared with the nonregulated gate driver, the power dissipation of the proposed gate driver can be reduced up to 15.5% and 55.4% under 15 V and 30 V supply voltage, respectively.

References

[1] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE Appl. Power Electron. Conf.*, 1991, pp. 527–532.

[2] J. D. Jeong and R. P. Verdes, "Gate driver output stage with bias circuit for high and wide operating voltage range," U.S. Patent 0 258 495 A1, Nov. 2005.

[3] J. A. Abu-Qahouq, W. Al-Hoor, Y. Liangbin, and I. Batarseh, "Drive voltage optimization controller to improve efficiency," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2006, pp. 2277–2280.

[4] M. D. Mulligan, B. Broach, and T. H. Lee, "A constant-frequency method for improving light-load efficiency in synchronous buck converters," *IEEE Power Electron. Lett.*, vol. 3, no. 1, pp. 24–29, Mar. 2005.

[5] M. D. Mulligan, B. Broach, and T. H. Lee, "A 3MHz low-voltage buck converter with improved light load efficiency," in *Proc. Int. Solid State Circuits Conf.*, San Francisco, CA, 2007, vol. 620, pp. 528–529.

[6] R. H. Tzeng, C. C. Hung, and C. L. Chen, "High efficiency regulated gate driver for power MOSFET," in *Proc. IEEE Appl. Power Electron. Conf.*, 2008, pp. 621–626.

[7] T. López, G. Sauerlaender, T. Duerbaum, and T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, vol. 2, pp. 873–878.

[8] *600 V N-Channel Zener-Protected SuperMESH Power MOSFET, STP4NK60ZFP Data Sheet*, STMicroelectronics, Inc., Lexington, MA, 2003.

[9] *600 V N-Channel MOSFET, SSS4N60B Data Sheet*, Fairchild Semiconductor, Inc., South Portland, ME, 2002.

[10] *60 V N-Channel STripFET Power MOSFET, STP60NF06 Data Sheet*, STMicroelectronics, Inc., Lexington, MA, 2002.

[11] *CoolMOS Power Transistor, SPP20N60C3 Data Sheet*, Infineon Technologies, Inc., Concord, MA, 2003.

[12] *500 V N-Channel Zener-Protected SuperMESH Power MOSFET, STW20NK50Z Data Sheet*, STMicroelectronics, Inc., Lexington, MA, 2003.

[13] *900 V N-Channel Zener-Protected SuperMESH III MOSFET, STW8NC50Z Data Sheet*, STMicroelectronics, Inc., Lexington, MA, 2000.

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