A Low-Cost Uncooled Infrared Microbolometer Detector in Standard CMOS Technology

Deniz Sabuncuoglu Tezcan, *Member, IEEE*, Selim Eminoglu, *Member, IEEE*, and Tayfun Akin, *Member, IEEE*

***Abstract*—This paper reports the development of a low-cost uncooled infrared microbolometer detector using a commercial 0.8 μm CMOS process, where the CMOS n-well layer is used as the infrared sensitive material. The n-well is suspended by front-end bulk-micromachining of the fabricated CMOS dies using electrochemical etch-stop technique in TMAH. Since this approach does not require any lithography or infrared sensitive material deposition after CMOS fabrication, the detector cost is almost equal to the CMOS chip cost. The n-well has a TCR of 0.5–0.7%/K, relatively low compared to state-of-the-art microbolometer materials; however, it has negligible $1/f$ noise due to its single crystal structure. The use of polysilicon interconnects on the support arms instead of metal reduces the overall pixel TCR to 0.34%/K, but provides a better performance due to improved thermal isolation. Measurements show that such a fabricated pixel with 74 μm $\times$ 74 μm pixel area provides a thermal conductance of 0.62 μW/K, a thermal time constant of 21 ms, a dc responsivity of 9250 V/W, and a detectivity of 2.0 $\times$ 10^9 cmHz$^{1/2}$/W with a total noise of 0.82 μV for a 4 kHz bandwidth. Based on this pixel, a 16 $\times$ 16 prototype focal plane array (FPA) with 80 μm $\times$ 80 μm pixel size and 13% fill factor has been implemented, where built-in diodes are used to simplify array scanning, at the expense of reduced overall pixel TCR of 0.24%/K. The n-well microbolometer array with a simple readout scheme provides a responsivity of 2000 V/W, a detectivity of 2.6 $\times$ 10^8 cmHz$^{1/2}$/W, and an estimated NETD of 200 mK at 0.5 Hz frame rate. Considering that this performance can be further improved with low noise readout circuits, the CMOS n-well microbolometer is a cost-effective approach to implement very low-cost uncooled infrared detector arrays with reasonable performance.**

***Index Terms*—CMOS infrared detectors, low-cost infrared detectors, microbolometers, uncooled infrared detectors.**

I. Introduction

UNCOOLED infrared detectors have recently gained wide attention for infrared imaging applications, due to their advantages such as low cost, low weight, low power, large spectral response, and long term operation compared to those of photon detectors. Worldwide effort is still continuing to implement very large format arrays at low cost for use in various applications, including commercial applications like driver's night vision enhancement and fire fighting. One of the main issues for achieving low-cost detectors is their monolithic integration and compatibility with CMOS technology.

The most widely used uncooled detector approach is to implement microbolometers using surface micromachined bridges on CMOS processed wafers, where infrared radiation increases the temperature of a material formed on the thermally isolated and suspended bridge, causing a change in its resistance related to its temperature coefficient of resistance (TCR) [1]–[9]. Currently, there are microbolometer arrays with 640 $\times$ 480 array formats and 25 μm $\times$ 25 μm pixel sizes with performance approaching that of cooled photon detectors [1]. However, these detectors require deposition of some high TCR materials after CMOS fabrication and complicated post-CMOS surface micromachining processing, increasing its cost and limiting its use for ultra low-cost commercial applications. For example, vanadium oxide (VO_x), which is the most widely known and used microbolometer material, has a high TCR of about 2–3%/K [2]; however, VO_x is not a standard material in IC fabrication and requires dedicated expensive equipment to prevent contamination of the CMOS line. In addition, it exhibits large $1/f$ noise due to its noncrystalline structure. There are efforts to implement surface micromachined microbolometers using IC compatible materials such as amorphous silicon [3], amorphous silicon carbide [4], and polycrystalline silicon–germanium [5]; and these materials also have high TCR values of 2.5%/K, 4–6%/K, and 2–3%/K, respectively. However, these materials require high temperature annealing to reduce their residual stress, which is not suitable for post-CMOS processing for monolithic integration. In addition, they exhibit even higher $1/f$ noise than VO_x, due to their noncrystalline structures. Another high TCR microbolometer material that is recently used is YBaCuO, which is deposited at room temperature, however, these detectors also require complicated and expensive post-CMOS surface micromachined processes [6], [7]. There are also microbolometers implemented with IC compatible metal films [8], [9], however, these detectors still require deposition and lithography steps after CMOS and their performances are low due to low TCR of metal films. Therefore, although surface micromachined microbolometers are very cheap compared to photon detectors, their price is still high for many commercial applications due to extra processes required for their fabrication.

Low-cost infrared detectors can be implemented with front or back-end bulk-micromachining of CMOS fabricated wafers, and this approach has mostly been used to implement CMOS thermopile arrays [10], [11]. However, thermopile arrays have low responsivity values (5–15 V/W) and large pixel sizes ($\geq$250 μm $\times$ 250 μm), limiting their use for large detector arrays. In addition, these detectors also require extra processing

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steps to form silicon islands [10] or electroplated gold lines [11] for thermal isolation between the pixels when back-end bulk-micromachining is used.

Recently, a new bulk-micromachining approach has been emerged, where silicon p-n diodes are used as uncooled infrared detectors. Up to now, two such approaches have been reported. One of them uses a suspended single p-n diode implemented in a 100 μm × 170 μm pixel area and fabricated using a dedicated in-house process technology [12], however, this approach does not seem suitable for large format arrays, due to its large pixel size and its large thermal time constant [13]. The other diode microbolometer approach uses suspended multiple series diodes with 40 μm × 40 μm pixel sizes implemented in a SOI CMOS process, and successful implementation of a 320 × 240 FPA has been reported [14]. Although this approach has very good potential for low-cost high performance uncooled detectors, the fabrication is based on a dedicated in-house SOI process, limiting its cost reduction. For ultra low-cost applications, the best approach would be to implement the detector arrays together with their readout circuitry fully in a standard CMOS process, using some simple post-CMOS etching steps where neither lithography nor detector material deposition is needed.

This paper reports the implementation of such an ultra low-cost bulk-micromachined uncooled microbolometer, where the CMOS n-well layer is used as the active sensor material [15]. The suspended n-well structure is obtained by post-CMOS anisotropic silicon etching. Since this fabrication approach does not require any lithography or advanced detector material deposition, the detector cost is almost equal to the CMOS chip cost. The performance of the n-well microbolometer is acceptable when its TCR and noise are considered together. The n-well layer has a TCR of 0.5–0.7%/K that is lower than that of deposited high TCR materials; however, it has negligible $1/f$ noise due to its single crystal nature, which is a clear advantage over amorphous materials with large $1/f$ noise. Using n-well detectors, various prototype FPAs with 16 × 16 array sizes have been implemented in standard CMOS processes [16]–[18]. These studies show that the n-well microbolometer approach allows easy implementation of ultra low cost and highly reproducible CMOS integrated microbolometer FPAs with reasonable performance for commercial infrared imaging applications.

II. n-Well Microbolometer Structure

Fig. 1 shows the perspective view of the n-well microbolometer that can be obtained with a standard n-well CMOS process. Infrared radiation heats the absorbing layer on the thermally isolated n-well region, increasing its temperature, which in turn results in a change in its resistance related to its TCR value. The bulk silicon under the n-well is etched away to reduce detector's thermal conductance and to increase its responsivity. This thermally isolated suspended structure is obtained by front-end bulk-micromachining of fabricated CMOS dies, while the n-well is protected from etching by the electrochemical etch-stop technique [15], [19], [20]. The required etch openings are formed without any post-CMOS lithography step, by placing various CMOS layers on top of each other, including active, contact, via, and passivation opening layers [21]. The absorber layer for the detector is formed with various dielectric layers available in CMOS [22]. In summary, the n-well microbolometer structure can be obtained with simple wet etching and without needing any lithography or deposition steps after CMOS fabrication, resulting in very low-cost detectors monolithically integrated with readout electronics.

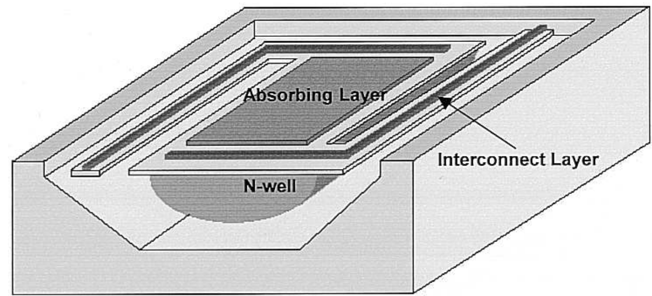


Fig. 1. Perspective view of the n-well microbolometer that can be obtained with a standard n-well CMOS process.

TABLE I
Thermal Conductivity and Heat Capacity of the Various Layers in a 0.8 μm CMOS Process Based on the Data in Literature [23]–[25]

	N-well	Dielectric	Poly Si	Metal-1
Thermal Conductivity (W/mK)	141	1.22	24	194
Heat Capacity (J/cm^{3}K)	1.63	1.74	1.6	2.23
Density (gr/cm^3)	2.33	2.38	2.33	2.70

The performance of the n-well microbolometer is affected by a number of design parameters and material characteristics, including pixel size, fill factor, opening width, support arm width, interconnect layer on the support arms, and the absorbing layer. The most important design parameters are the thermal isolation and effective pixel TCR. The use of metal interconnects on the support arms provides a better effective pixel TCR approaching that of n-well, however, it results in poor thermal isolation. In contrast, the use of polysilicon interconnects results in much better thermal isolation and responsivity, even though it reduces the effective pixel TCR.

The performance and structure of the n-well microbolometers are optimized using detailed simulations with various programs. Table I shows the thermal conductivity and heat capacity values of the various layers in a 0.8 μm CMOS process based on the data in literature [23]–[25]. CoventorWare simulations show that the thermal conductance and thermal time constant of the pixel with 74 μm × 74 μm pixel size and 15% fill factor are 5.10 μW/K and 3.6 ms, respectively, when metal interconnect is used. The thermal conductance decreases to 1.16 μW/K, and thermal time constant increases to 14.3 ms, when polysilicon interconnects are used. These simulations verify that the polysilicon interconnects provide about five times improvement in thermal isolation. It should be noted that polysilicon interconnect provides a larger electrical resistance and therefore in-

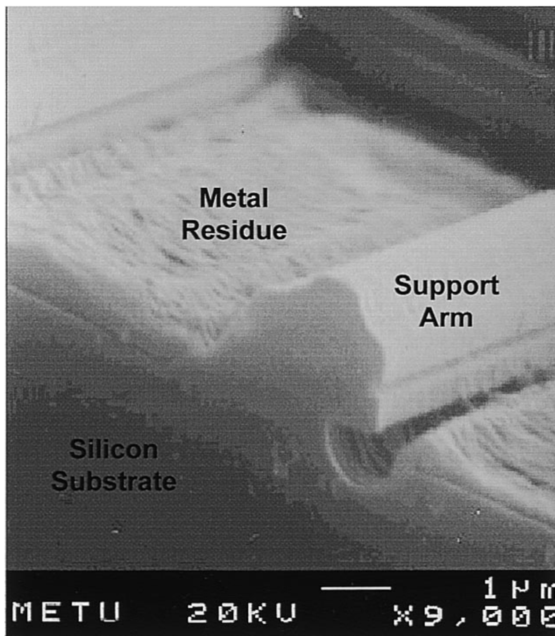
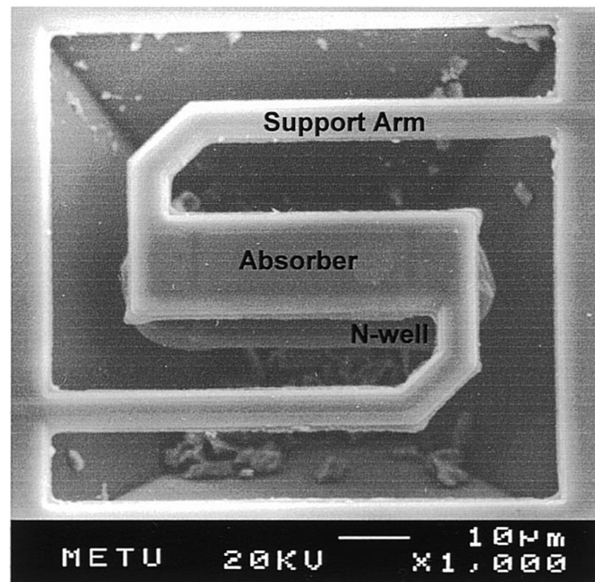


Fig. 2. SEM photograph of one opening just after the CMOS process, where the aluminum residue is clearly visible.

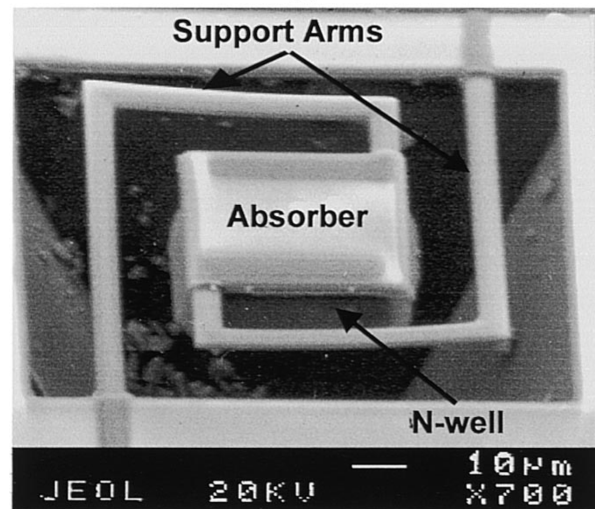
creases the pixel noise, but it is still preferred over metal arms considering the overall pixel performance. Various simulations have also been performed using Kidger Optics Software to estimate the performance of the absorber layer, which is chosen as the oxide-metal-passivation sandwich layer. These simulations verify that the absorptance is in the 8–14 μm band, having a peak at 10.5 μm wavelength. It should be noted that it is possible to implement different absorber structures in CMOS to increase the absorptance of CMOS infrared detectors [22].

III. Detector Fabrication

Various n-well microbolometers with different sizes and structures are designed and sent to fabrication in a standard 0.8 μm CMOS process. After CMOS fabrication, the detectors are suspended and thermally isolated using a post-CMOS process. First, any metal residue in etch openings are removed, so that the silicon etchant can reach and etch the bulk silicon underneath the n-well. The metal residue is left in the narrow opening areas especially in submicron processes due to thicker dielectric and metal layers. Fig. 2 shows an SEM photograph of one opening just after the CMOS process, where the aluminum residue is clearly visible. This residue is removed with a standard aluminum etchant, while bonding pads are protected. In the second step, the die is exposed to an anisotropic silicon etchant, while a four-terminal electrochemical etch-stop technique is used to prevent the etching of the n-well [26]. Among various anisotropic silicon etchants, TMAH has been chosen since it is safe to use and is selective to silicon dioxide. A 5 wt.% TMAH solution at 85 °C is used, while ammonium peroxidisulfate $[(NH_4)_2S_2O_8]$ is added to prevent hillock formation. An additional 1.6 wt.% powder silicon is dissolved to prevent etching of the aluminum pads [27]. The details of this post-CMOS etching process can be found elsewhere [15], [19], [20].



(a)



(b)

Fig. 3. SEM photographs of the post-processed single pixel n-well microbolometers: (a) with 74 μm × 74 μm pixel size and 15% fill factor, and (b) with 100 μm × 100 μm pixel size and 17% fill factor having longer arms to obtain better thermal isolation of the n-well.

Fig. 3 shows SEM photographs of post-processed single pixel n-well microbolometers. Fig. 3(a) shows a pixel with a 74 μm × 74 μm area and 15% fill factor, and Fig. 3(b) shows a pixel with a 100 μm × 100 μm area and 17% fill factor, where longer arms are implemented to obtain better thermal isolation. It should be noted here that the fill factors are low due to 10 μm-wide openings, which are necessary to reduce the undesired metal residue.

IV. Test Results of Single Pixel Detectors

A number of electrical and optical tests are performed to characterize the n-well microbolometers. Electrical measurements show that the sheet resistances of the n-well and polysilicon layers are 1.19 kΩ/sq. and 24 Ω/sq., respectively. The TCR of the n-well and polysilicon layers are measured as 0.58%/K and 0.09%/K, respectively. The effective TCR of a pixel is the

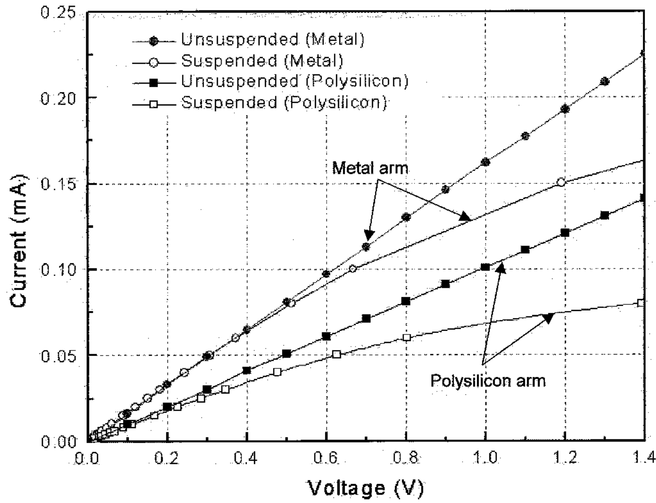


Fig. 4. Resistance variation of two pixels with polysilicon and metal interconnects upon the applied electrical power for the structure shown in Fig. 3(a). The resistance of the suspended n-well microbolometers increase with the applied bias; the I–V curves of the unsuspended pixels remain linear, giving the resistance of pixels with metal and polysilicon interconnect layers as 6.05 kΩ and 10.07 kΩ, respectively.

weighted average of the n-well and interconnect TCR values: it is equal to the TCR of the n-well layer for detectors with metal interconnect and it is lower for detectors with polysilicon interconnect. For example, the TCR of the n-well microbolometer structure given in Fig. 3(a) is measured as 0.34%/K when implemented with polysilicon interconnects.

The thermal conductance of the pixels is measured using self-heating effect of the suspended pixels in vacuum. Fig. 4 shows resistance variation of two pixels with polysilicon and metal interconnects upon the applied electrical power for the structure shown in Fig. 3(a). The graphs in Fig. 4 verify that only the resistance of the suspended n-well microbolometers increase with the applied bias; the I–V curves of the unsuspended pixels remain linear, giving the resistance of pixels with metal and polysilicon interconnect layers as 6.05 kΩ and 10.07 kΩ, respectively. Using the data of the suspended structures and knowing the effective TCR of the pixels, the thermal conductance of the n-well microbolometers with metal and polysilicon interconnects are measured as 4.6 μW/K and 0.62 μW/K at 10 mtorr, respectively. In these measurements, care is taken when determining the amount of power that causes temperature increase. In detectors with metal interconnect, almost all the applied power is dissipated in the n-well, contributing fully on the temperature increase of the pixel. However, in detectors with polysilicon interconnects, the applied power is dissipated both in the n-well and polysilicon arms, reducing the temperature increase of the pixel. Fig. 5 shows the distributed thermal model of the pixel used in the analysis of self-heating upon applied bias. In this model, the suspended n-well is assumed to be a point detector with thermal conductance of G_{th}, and each support arm is divided into N units with thermal conductance of $NG_{th}/2$. The temperature rise of the pixel can be determined using superposition of individual power sources in the distributed model as

$$\Delta T_{n\text{-}well} = \frac{P_{n\text{-}well}}{G_{th}} + \frac{P_{connect}N(N+1)}{2G_{th}N^2} \quad (1)$$

where $P_{n\text{-}well}$ is the power dissipated in the n-well, and $P_{connect}$ is the power dissipated on the support arms. When the number of units (N) goes to infinity, the temperature increase can be found as

$$\lim_{N\to\infty} \Delta T_{n\text{-}well} = \frac{P_{n\text{-}well}}{G_{th}} + \frac{P_{connect}}{2G_{th}}. \quad (2)$$

This result indicates that effective thermal conductance for the support arms actually doubles, resulting in less temperature rise than expected. For example, for the pixel in Fig. 3(a) with polysilicon arm, only 78% of the total applied power effectively contributes to the temperature rise.

Optical tests are performed to determine the responsivity of the detectors. Detector responsivity depends on biasing and readout scheme, and in the case of a simple constant current biasing, it can be given as

$$\Re = \frac{\eta \alpha_{pixel} i_{bias} R_{pixel}}{G_{th}\sqrt{(1+(2\pi f \tau)^2)}} \quad (3)$$

$$\alpha_{pixel} = \frac{\alpha_{connect}R_{connect} + \alpha_{n\text{-}well}R_{n\text{-}well}}{R_{pixel}} \quad (4)$$

$$R_{pixel} = 2R_{connect} + R_{n\text{-}well} \quad (5)$$

where η is absorptance, G_{th} is thermal conductance, τ is the thermal time constant of the pixel, $R_{n\text{-}well}$ is n-well resistance, $R_{connect}$ is interconnect resistance of each arm, R_{pixel} is the total pixel resistance, $\alpha_{n\text{-}well}$ is the TCR of the n-well layer, $\alpha_{connect}$ is the TCR of the interconnect material, α_{pixel} is the total effective TCR of the suspended pixel, f is the modulation frequency of the infrared radiation, and i_{bias} is the applied bias current. As it is seen from (3), responsivity depends on the infrared modulation frequency due to the thermal time constant of the pixel. Using this equation and measuring the responsivity at different modulation frequencies, both the dc responsivity and thermal time constant of the pixels can be measured. For example, Fig. 6 shows the responsivity data for the two structures in Fig. 3 with metal arms measured with respect to infrared modulation frequency, where dc bias currents are selected to provide 2.5 V across the detector pixel. From this data, the dc responsivity and thermal time constant of the pixel in Fig. 3(a) are extracted as 2700 V/W and 6.9 ms, respectively; for the pixel in Fig. 3(b) the same parameters are extracted as 5100 V/W and 22 ms, respectively. Having a high responsivity alone is not that important, instead, detectivity is a more important parameter to evaluate the performance of the n-well microbolometer.

The detectivity (D^*) of the n-well microbolometer can be obtained as

$$D^* = \frac{\Re\sqrt{A_{det}\Delta f_e}}{V_n} \quad (6)$$

where $\Re$ is the responsivity, $A_{\rm det}$ is the active area of the detector, Δf_e is the electrical bandwidth, and V_n is the total rms noise voltage. To determine the detectivity of the n-well microbolometers, their noise values are measured for different structures.

N-well resistor noise principally consists of thermal (Johnson) and $1/f$ noise. Since n-well layer is single crystal, it is expected that $1/f$ noise to be low and thermal noise to be dominant. This is a major advantage of the n-well

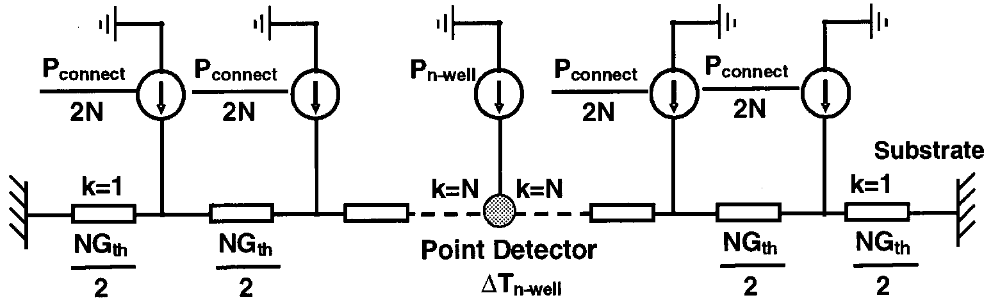


Fig. 5. Distributed thermal model of the pixel used in the analysis of self-heating upon applied bias.

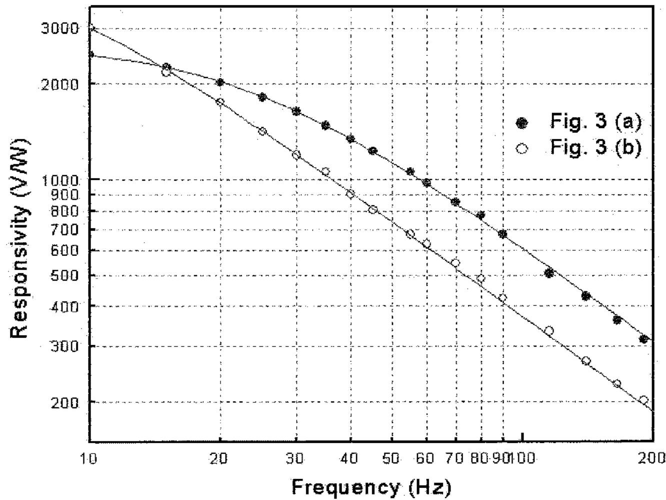


Fig. 6. Measured responsivity of the two n-well microbolometers with metal interconnects shown in Fig. 3 with respect to infrared modulation frequency.

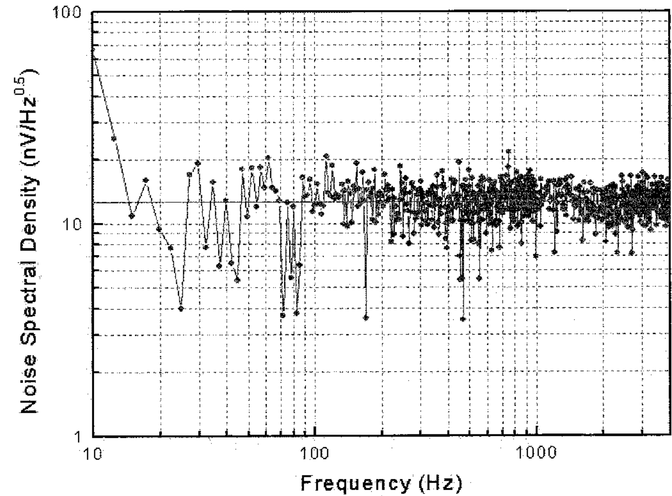


Fig. 7. Measured noise spectral density of the n-well microbolometer with polysilicon interconnect having an average value of 12.8 nV/Hz$^{1/2}$. This value is very close to the thermal noise component, showing that $1/f$ noise of the single crystal n-well is very small.

microbolometer over the other microbolometers implemented with amorphous microbolometer materials. It should be mentioned here that the detector structures with polysilicon interconnect exhibit some $1/f$ noise due to its noncrystalline structure, however, the measurements show that even these structures have negligible $1/f$ noise with a knee frequency below 20 Hz (Fig. 7).

The noise of the n-well microbolometers are measured using HP4395A Spectrum Analyzer through a custom preamplifier that has a gain of 1000 V/V with 3 dB points at 20 Hz and 13.7 kHz. Fig. 7 shows the measured noise spectral density of the n-well microbolometer for the structure in Fig. 3(a) with polysilicon interconnects. The average noise spectral density is measured to be 12.8 nV/Hz$^{1/2}$ and 10.5 nV/Hz$^{1/2}$ for the pixels with polysilicon and metal interconnects, resulting in a total rms noise voltage of 0.82 μV and 0.67 μV for a 4 kHz electrical bandwidth, respectively. These overall noise values are very close to the thermal noise component of the n-well microbolometers, showing that $1/f$ noise component of the single crystal n-well microbolometers are very small indeed. Based on these measurements, the detectivities of the n-well microbolometers with polysilicon and metal interconnect are determined as 2.0×10^9 cmHz$^{1/2}$/W and 7.3×10^8 cmHz$^{1/2}$/W, respectively. Table II shows the summary of the device parameters and performance results of the single-pixel n-well microbolometer structure shown in Fig. 3(a) with metal and polysilicon interconnect layers.

TABLE II
SUMMARY OF THE DEVICE PARAMETERS AND PERFORMANCE RESULTS OF THE n-WELL MICROBOLOMETER STRUCTURE SHOWN IN FIG. 3(a) WITH METAL AND POLYSILICON INTERCONNECT LAYERS

Interconnect Material	Metal	Poly Si
Resistance @ 300K (kΩ)	6.05	10.07
TCR (%/K)	0.58	0.34
Thermal Conductance (μW/K)	4.6	0.62
Thermal Time Constant (msec)	6.9	21
Responsivity (V/W)	2700	9250
Average Noise (nV/Hz$^{1/2}$)	10.5	12.8
D* (cm.Hz$^{1/2}$/W)	7.3x10^8	2.0x10^9

V. ARRAY IMPLEMENTATION

Various 16×16 n-well microbolometer array prototypes have been implemented together with their readout circuitry in a 0.8 μm CMOS process [16]–[18]. Fig. 8 shows the schematic view of the electronic pixel connection inside the array. To

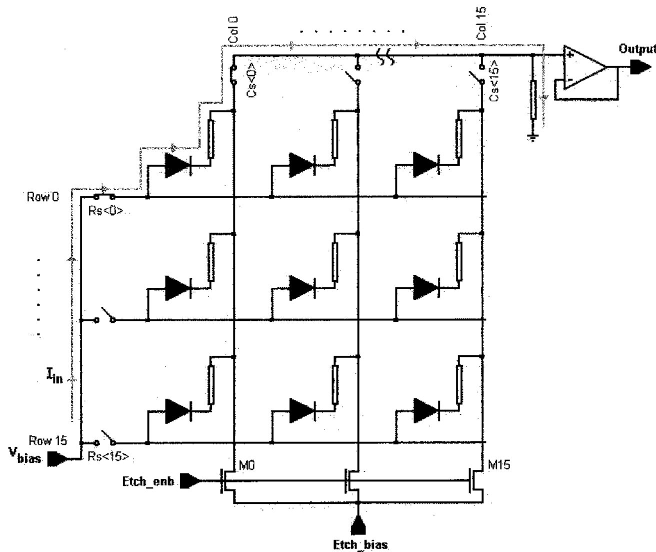


Fig. 8. Schematic view of the electronic pixel connection inside the array and the circuitry used for etching process.

simplify the readout scheme and to reduce the number of interconnects, built-in diodes are used within the pixels instead of MOS switches. Fig. 8 also shows the required etching circuitry that is used to connect all the n-wells in the array to passivation potential during etching. This is achieved by turning on transistors M_0–M_{15} [19]. Under normal operation conditions, transistors M_0–M_{15} are turned off, and each pixel connected to the output by the scanning circuitry, which is monolithically integrated with the detector array. Microbolometer pixels in the array have polysilicon interconnect layers to have better thermal isolation, at the expense of increased noise and reduced pixel TCR.

Fig. 9 shows an SEM photograph of a fabricated and post-processed array die verifying that all n-well structures are suspended and none of the support arms are broken. The suspended structures remain flat without any extra stress-reducing process steps after CMOS fabrication. It should be noted that the bulk silicon regions between the suspended n-wells reduce the thermal cross-talk, eliminating the need for gold stripes or silicon islands between the pixels, which have been used in other low-cost CMOS imagers that use thermocouples as detection mechanism [10], [11].

The array pixel uniformity is determined by measuring the resistance values of the individual pixels. Fig. 10(a) and (b) shows the resistance measurement results and the histogram plot of the 256 pixels, respectively, verifying their high uniformity. The mean value of the pixel resistances is 8.37 kΩ with a standard deviation of 103 Ω and a nonuniformity of 1.23%. This nonuniformity is expected to determine the overall nonuniformity of the arrays, as the other parameters, like the thickness and dimensions of the dielectric absorber layer, are usually very uniform in mature CMOS processes.

The performance of the n-well microbolometers decreases when implemented in an array format, due to the diode that is incorporated inside the pixel. The effective TCR of the pixel

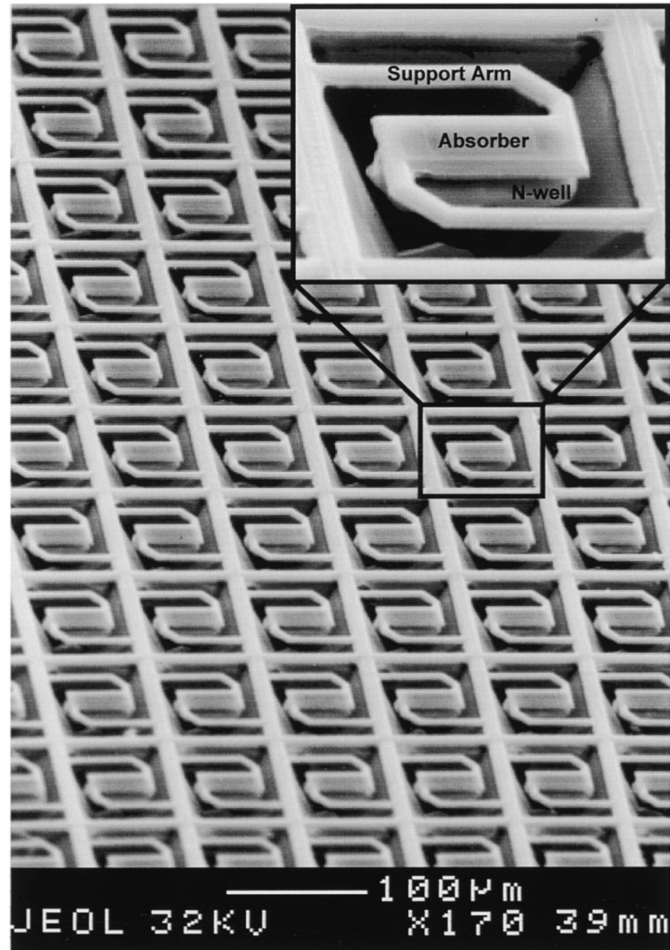


Fig. 9. SEM photograph of a fabricated and post-processed array die verifying that all n-well structures are suspended and none of the support arms are broken. The suspended structures remain flat without any extra stress-reducing process steps after CMOS fabrication.

reduces due the negative TC of the diode, which modifies the effective pixel TCR in (3) and (4) as

$$\alpha_{pixel} = \frac{1}{i_{bias} R_{pixel}} \frac{dV_D}{dT} + \frac{\alpha_{poly} R_{poly} + \alpha_{n\text{-}well} R_{n\text{-}well}}{R_{pixel}} \tag{7}$$

where $R_{n\text{-}well}$ is n-well resistance, R_{poly} is polysilicon resistance in each arm, R_{pixel} is the total pixel resistance, $\alpha_{n\text{-}well}$ is TCR of n-well layer, α_{poly} is TCR of polysilicon layer, i_{bias} is the applied bias current, and V_D is diode voltage. Since the diode term dV_D/dT is negative with a typical value of −2 mV/K, the effective pixel TCR in the array is reduced to about 0.24%/K.

Based on above measurements, the responsivity and detectivity of the n-well microbolometer in the array are determined as 2000 V/W and 2.6 × 10^8 cmHz$^{1/2}$/W, respectively. The overall noise voltage at the array output with the simple readout scheme is calculated as 0.174 μV for 0.5 frames per second scanning rate, considering the pixel and readout circuit noise. The expected NETD value of the array is 200 mK, with $f/1$ optics and an array bias voltage of 5 V. Table III summarizes the device parameters and performance results of the 16 × 16 n-well microbolometer array with a simple readout circuit.

These results show that the performance of the n-well microbolometer FPAs is lower than that of the high-cost high-TCR

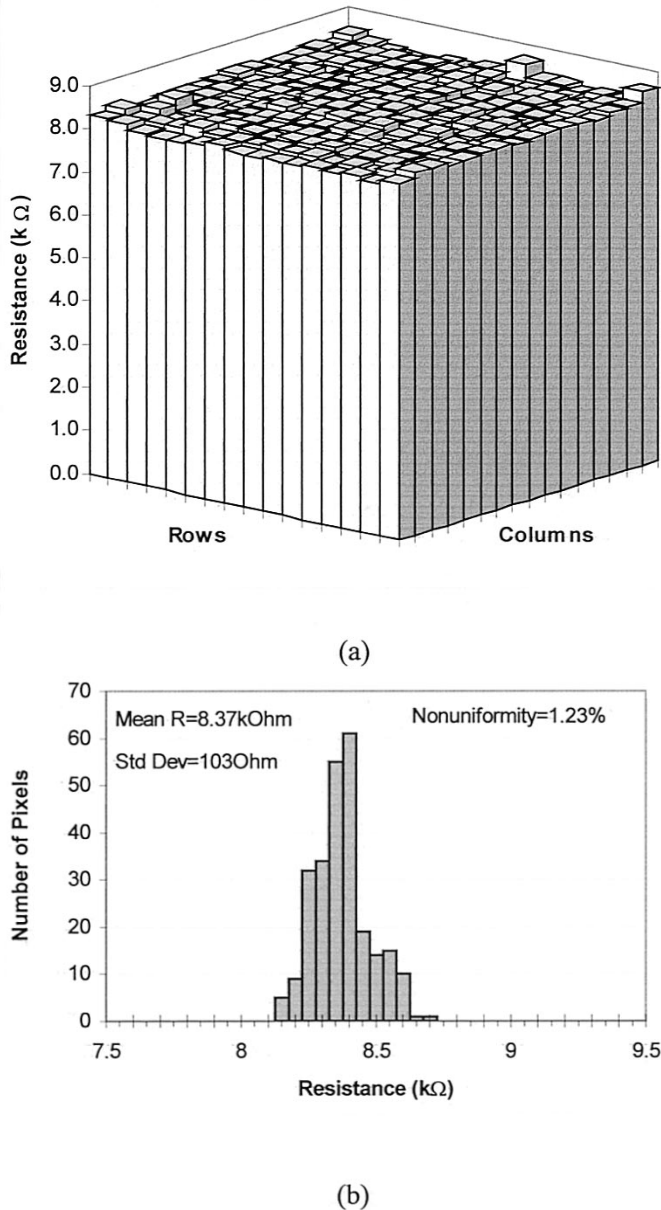


Fig. 10. Measured uniformity results of the 16 × 16 prototype array: (a) resistance measurement results and (b) the histogram plot of the 256 pixels. The mean value of the pixel resistances is 8.37 kΩ with a standard deviation of 103 Ω and a nonuniformity of 1.23%.

TABLE III
COMPARISON OF CMOS n-WELL MICROBOLOMETER DETECTOR ARRAY WITH POST-CMOS BULK MICROMACHINED THERMOPILE ARRAYS

Parameter	Ref. [10]	Ref. [11]	N-well
Process (CMOS)	3μm	1μm	0.8μm
Array Size (# of pixels)	32 x 32	10 x 10	16 x 16
Pixel Size (μm^2)	375 x 375	250 x 250	80 x 80
Chip Size (mm^2)	16 x 16	5.5 x 6.2	2.1 x 2.1
Responsivity (V/W)	15	4	2000
Detectivity ($cmHz^{1/2}/W$)	$1.6x10^7$	$1.56x10^7$	$2.6x10^8$
NETD	500mK*@ 6.7fps	320mK @ 0.5fps	200mK*@ 0.5fps

*Expected.

surface micromachined microbolometers. However, n-well microbolometer FPAs still show a better performance than other very low cost and simple post-CMOS processed infrared detector arrays, like bulk-micromachined CMOS thermopile arrays. Table III shows the comparison of the CMOS n-well microbolometer detector array with post-CMOS bulk-micromachined thermopile arrays reported in literature [10], [11]. The pixel size of the n-well microbolometer is 80 μm × 80 μm, which is much smaller than 375 μm × 375 μm and 250 μm × 250 μm. The responsivity of n-well is 2000 V/W, which is much larger than 15 V/W and 4 V/W, while the detectivity of the n-well is 2.6 × 10^8 cmHz$^{1/2}$/W, which is an order of magnitude larger than the thermopile arrays. The n-well microbolometer array performance can be improved further by using a low noise preamplifier circuit, even at higher scanning rates. Another advantage of the n-well microbolometers is that the pixels are thermally isolated due to front-side bulk-micromachining, however, thermopile detector arrays require extra processing steps to form silicon islands [10] or electroplated gold lines [11] for thermal isolation between the pixels when back-end bulk-micromachining is used. It should be noted here that the main advantage of the thermopiles is that they do not require a thermoelectric temperature stabilizer, but the temperature stabilizers can also be eliminated from microbolometers using temperature compensated readout design or using digital signal processor based temperature compensation [28].

VI. CONCLUSION

Low-cost uncooled infrared microbolometer detectors and FPAs have been developed using a commercial CMOS process without requiring any masking or photolithography steps. The microbolometer uses the CMOS n-well layer as the infrared sensitive material. The n-well layer is suspended by front-end bulk-micromachining of the fabricated CMOS dies, while the n-well region is protected from etching by electrochemical etch-stop technique using a TMAH solution. Various single pixel n-well microbolometers with different pixel sizes and different interconnect layers have been implemented in a 0.8 μm CMOS process. Pixels with polysilicon interconnect provide much better thermal isolation, resulting in a better overall pixel performance, despite the fact that polysilicon interconnect reduces the overall pixel TCR and increases the overall noise and thermal time constant. Such a pixel with a 74 μm × 74 μm pixel size and a fill factor of 15% provides a measured responsivity of 9250 V/W and a detectivity of 2.0 × 10^9 cmHz$^{1/2}$/W. The pixel fill factors are low due to the limitations coming from bulk-micromachining and required wide etch openings. Various 16 × 16 prototype arrays have been implemented, where the pixel size is increased to 80 μm × 80 μm and the fill factor is reduced to 13% due to the routing metals. The effective TCR of the array pixel is reduced to 0.24%/K due to the built-in diode and polysilicon interconnect layer. The array provides a responsivity of 2000 V/W, a detectivity of 2.6 × 10^8 cmHz$^{1/2}$/W, and an estimated NETD of 200 mK at 0.5 Hz frame rate. The CMOS n-well microbolometer performance can be increased significantly by using advanced readout techniques and high fill factor structures which can be obtained with finer CMOS

technologies and different post-CMOS processing approaches. Therefore, the CMOS n-well microbolometer detector is a promising approach to implement very low-cost uncooled infrared detector arrays with reasonable performance.

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