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A low-distortion ΣΔ capacitive microaccelerometer with self-test circuit

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Abstract: A low-distortion ΣΔ interface with self-test circuit is proposed for a closed-loop capacitive microaccelerometer. A fully feedforward architecture is used to reduce integrator output swing and decrease distortions of the ΣΔ interface circuit, resulting in a reduction of power dissipation. A self-test circuit is proposed to measure the distortions of the microaccelerometer without using a vibration table. A fourth-order closed-loop capacitive microaccelerometer is proposed to verify the effectiveness of the technique. The interface circuit is designed and the chip is fabricated using a standard 0.35 µm CMOS process. The capacitive microaccelerometer consumes 10 mW from a 5 V supply with a sampling frequency of 250 kHz. It achieves a noise floor of 9 µg/Hz$^{1/2}$, and the self-test measurement results show that the resulting HD2 and HD3 of the microaccelerometerare −92.28 dB and −99.27 dB, respectively.

Keywords: low-distortion, ΣΔ capacitive microaccelerometer, interface, self-test circuit

Classification: Micro- or nano-electromechanical systems

References

[1] X. W. Liu, H. L. Xu, L. Yin, Z. Gao and M. Ren: IEICE Electron. Express **11** (2014) 20140315. DOI:10.1587/elex.11.20140315

[2] V. P. Petkov and B. E. Boser: IEEE J. Solid-State Circuits **40** (2005) 1602. DOI:10.1109/JSSC.2005.852025

[3] A. Bader and K. Michael: 2014 IEEE Sensors (2014) 1780. DOI:10.1109/ICSENS.2014.6985370

[4] F. Chen, W. Z. Yuan, H. L. Chang, I. Zeimpekis and M. Kraft: 2014 IEEE 27th International Conference on MEMS (2014) 761. DOI:10.1109/MEMSYS.2014.6765752

[5] B. V. Amini, R. Abdolvand and F. Ayazi: IEEE J. Solid-State Circuits **41** (2006) 2983. DOI:10.1109/JSSC.2006.884864

[6] X. W. Liu, H. L. Xu, C. He and M. Y. Ren: IEICE Electron. Express **11** (2014) 20140320. DOI:10.1587/elex.11.20140320

[7] Y. T. Liu, X. W. Liu, Y. Wang and W. P. Chen: Analog Integr. Circ. Sig. Process **72** (2012) 27. DOI:10.1007/s10470-011-9816-1

[8] R. Schreier and G. C. Temes: *Understanding Delta Sigma Data Converters* (Wiley–IEEE Press, New York, 2004).

[9] SF1500 Data Sheet (2005) http://www.colibrys.com.

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Publicized July 21, 2015
Copyedited August 10, 2015

[10] M. Yücetaş, M. Pulkkinen and A. Kalanti: IEEE J. Solid-State Circuits **47** (2012) 1721. DOI:10.1109/JSSC.2012.2191675
[11] B. Amini and F. Ayazi: IEEE J. Solid-State Circuits **39** (2004) 2467. DOI:10.1109/JSSC.2004.837025

1 Introduction

High performance microaccelerometers are becoming popular in consumer market and military applications. A microaccelerometer with ΣΔ modulation technology provides direct digital output which is processed by a post-stage circuit and stored in low power units such as memristors. An important objective for designing a ΣΔ sensor is to implement the digital feedback without compromising the noise performance of the underlying open-loop system. In addition, ΣΔ interface circuits for microaccelerometers are easy to be obtained in CMOS process [1, 2]. A new control structure for an electromechanical ΣΔ modulator based on the dual quantization technique is presented in [3], and the proposed MASH2-0 structure achieved a noise-floor level of −130 dB, which shows its potential as a closed-loop interface for high-performance capacitive MEMS inertial sensors. The authors of [4] reports a novel six-order ΣΔ closed-loop accelerometer with extended bandwidth in vacuum environment, and a noise acceleration value of 1.2 $\mu g/Hz^{1/2}$ is achieved. Most of the published microaccelerometers employ topologies of distributed feedback or that with feedforward paths [1, 3, 4, 5, 6]. These topologies have signal paths bypassing the sensor element, therefore, compensating zeros are determined by feedback coefficients as well as the parameters of sensor, and the position of the zeros are influenced by the variations of sensor's parameters [2]. The uncertain zeros bring the high-order system into stability problem and decrease noise shaping ability. A low-distortion architecture with feedforward summation is presented in [2] to avoid the signal paths bypassing the sensor element. In this way, the position of zeros is determined only by capacitor ratios in the interface circuits. However, this architecture needs a non-inverting switched-capacitor (SC) integrator, a inverting SC integrator and a delay unit, so the circuit is complicated. What is more, there is no measurement result of the harmonic distortion. In this work, an improved topology is proposed. Key difference of the proposed architecture compared with the feedforward topology presented in [2] is that it does not need any delay unit, and only two non-inverting SC integrators are used, therefore, the complexity of circuit implementation is reduced. In addition, the phase compensator locates before the integrators with improved stability, especially for a high quality factor (Q) sensor element. On-chip-test technique is proposed in [6] to measure the distortions of microaccelerometers without using a vibration table. However, this technique is not available for low-distortion architecture. Self-test circuit for a fully feedforward interface is thus proposed in this paper for the verification of low-distortion performance.

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2 Proposed ΣΔ microaccelerometer

A distributed feedback architecture for a single-loop fourth-order ΣΔ microaccelerometer is presented in [7]. The signal paths bypassing the sensor element influence the position of compensating zeros, which do not track the variations in the sensor transfer function. A single-loop fourth-order ΣΔ microaccelerometer with feedforward summation architecture is proposed in [2]. Two additional electronic integrators are cascaded with the micromachined sensing element to form a fourth-order loop filter. This architecture does not contain signal paths bypassing the sensor element, so the position of the zeros is determined only by capacitor ratios in the interface circuits, avoiding the influence from the parameter variations of sensor element. However, this topology has a phase compensator inserted between the summation unit and comparator, which limits the input range of the sensor [7]. In addition, an additional unit delay is needed, which breaks the settling path of the amplifiers at the point of the second integrator, and a non-inverting integrator and a inverting integrator are needed, which complicate the implementation of the circuit.

The proposed fourth-order ΣΔ microaccelerometer is presented in Fig. 1. A fully feedforward summation topology is employed, and a lead compensator is inserted before the integrators. This architecture also avoids the signal paths bypassing the sensor element, resulting in a certain position of zeros. Compared with distributed feedback architecture, it increases the low frequency loop gain, thus reducing the output swing of integrators and relaxing the requirements for the operational amplifier in the integrators. The key difference of the proposed architecture compared with the ΣΔ microaccelerometer presented in [2] is that it does not need any delay unit, and only two non-inverting SC integrators are used. Therefore, the proposed ΣΔ microaccelerometer reduces the complexity of the circuit implementation and avoids the circuit nonidealities of the extra delay unit. In addition, a phase compensator locating before the integrators can compensate the large phase shift in advance, thus resulting in a more stable high-order system. Moreover, the lead compensation in this work increases the input range of the sensor [7]. However, a fully feedforward summation topology has a severe stability problem due to a very large loop gain in low frequency. To solve this issue, a heavy lead compensator is used to increase the phase shift before the integrators with a compensation factor $\alpha = 0.9$, and the stability is improved by positioning the zeros closer to the open-loop poles of the filter. Secondly, the loop gain is scaled down by the gain factors of the first and second integrators. Thirdly, a large feedforward summation factor A is applied to reduce the signal energy passing the integrator paths. Scaling integrator gain can reduce integrator's output range, which saves power dissipation and improves the stability of the closed-loop system. For an electrical modulator, a large sampling capacitance is required to achieve a high SNR if a relatively low OSR is applied. Increasing the sampling rate is an effective way to make the desired specifications more readily achievable [8]. However, it is not necessary for an microaccelerometer. The sampling capacitance of the first integrator could be relatively small due to the noise suppression by the front-end block. The values of the coefficients in the feedforward summation are $A = 0.8$, $B = 0.1$ and $C = 0.1$, and the gain factors of the integrators are $k1 = 1/5$,

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k2 = 1/4, respectively. The signal transfer function (STF) and noise transfer function (NTF) of the proposed ΣΔ microaccelerometer are given as

$$STF(z) = H_{mz}(z)K_{x/V}(z-\alpha)[A(z-1)^2 + Bk_1(z-1) + Ck_1k_2]/\{z(z-1)^2 + H_{mz}(z)K_{x/V}(z-\alpha)[A(z-1)^2 + Bk_1(z-1) + Ck_1k_2]\} \quad (1)$$

$$NTF(z) = z(z-1)^2/\{z(z-1)^2 + H_{mz}(z)K_{x/V}(z-\alpha) \times [A(z-1)^2 + Bk_1(z-1) + Ck_1k_2]\} \quad (2)$$

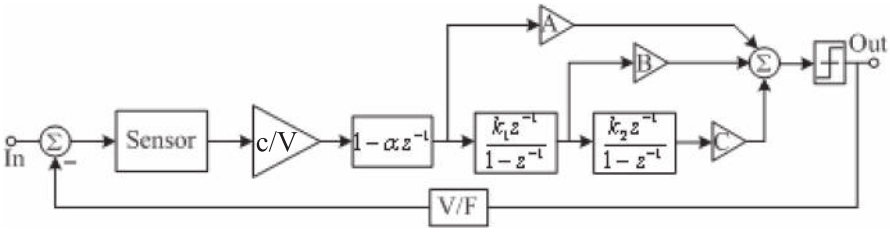

Fig. 1. Proposed fourth-order ΣΔ microaccelerometer

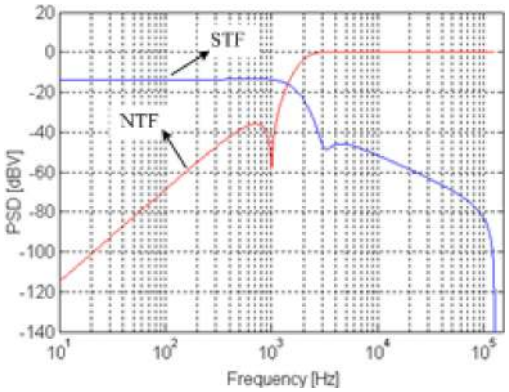

Fig. 2. STF and NTF of the proposed ΣΔ microaccelerometer

where H_{mz} is the transfer function of the sensor element in z-domain, and $K_{x/V}$ is the gain of displacement-to-voltage. The sensor element has a fundamental frequency of 1 kHz, and the Q value is larger than 20. There has a peak at the fundamental frequency in the open-loop frequency response for a high-Q sensor element, and it will introduce complex poles which may bring the risk of instability to the closed-loop circuit and ringing in the step response. Fig. 2 illustrates the simulated plots of STF and NTF of the closed-loop microaccelerometer in Matlab. The frequency response peaking is eliminated by using a phase compensator and closed-loop operation. The zero positioned at 1 kHz improves the noise shaping ability of the high-order system. The simulation results of integrator output histograms for a conventional distributed feedback ΣΔ microaccelerometer presented in [7] and for the proposed one are shown in Fig. 3. The fully distributed feedback microaccelerometer is inherently stable and has signal paths bypassing the sensor element with no feedforward paths. The histograms indicate that the first integrator output is scaled down by nearly 90 percent, while that of the second integrator output is about 50 percent. Compared with a conventional topology, the proposed

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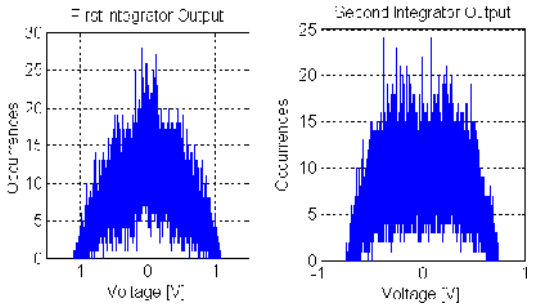
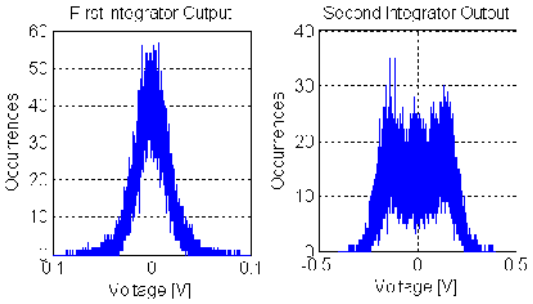
architecture is advantageous in decreased integrator output swings. The significant decrease of output swings will lead to a reduction of integrator nonlinearity, which is helpful to achieve a low-distortion microaccelerometer.



(a)



(b)

Fig. 3. Integrator output histograms (a) Conventional topology (b) Proposed topology

3 Circuit implementation and measurement results

The closed-loop interface circuit diagram for the proposed fourth-order low-distortion microaccelerometer is presented in Fig. 4. Fig. 5 presents the main timing diagram of the interface. The target performance of the proposed micro-accelerometer is to achieve a overall noise floor of lower than 10 $\mu g/Hz^{1/2}$, sensing range of larger than ± 1.5 g, low power dissipation of lower than 15 mW, DR of larger than 100 dB and bandwidth of larger than 300 Hz, respectively. Additionally, we want to obtain a self-test circuit with distortion of lower than -90 dB [1, 6]. Fig. 4 shows that the complexity of the circuit implementation is relaxed compared with that in [2]. The low-noise charge sensitization circuit in the front-end is based on a correlated-double-sampling (CDS) technique [1]. The charge amplifier is followed by the sampling and hold (S&H) circuit, and the low frequency $1/f$ noise and offset of the amplifier is reduced. The operational amplifier (OPA) in the charge sensitization circuit is the most important module for the interface. The OPA is realized using a PMOS-input folded-cascode topology, which dissipates 0.8 mA current from a single 5 V supply. The OPA has a dc gain of 89 dB and closed-loop bandwidth of 15 MHz with an integration capacitance of 20 pF. A smaller integration capacitance is useful for the reduction of circuit noise, while a larger capacitance is necessary to stabilize the high-order system. A two-stage PMOS-

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input folded-cascode OPA is employed in the S&H circuit with a 6 MHz bandwidth, which has a dc gain of larger than 80 dB to increase the settling precision, and its power dissipation is 1 mW. A lead compensator, operated as a passive filter to minimize the power dissipation, is presented in Fig. 4. The compensation factor is designed to be C_2/C_1, and C_2 is equal to C_3. The OPA dc gains of the non-inverting integrators are 65 dB and 55 dB, respectively. The sampling capacitances in the first and second integrators are 1 pF and 0.3 pF, respectively. The closed-loop bandwidth of the first integrator is 14 MHz, and that of the second integrator is 16 MHz. The first integrator dissipates 400 µA current and that of the second integrator is 180 µA with a scaled down capacitance load. The summation capacitances C_{a1}, C_{a2} and C_{a3} are 1.6 pF, 0.2 pF and 0.2 pF, respectively. Due to the small integrator output, a high-precision comparator is needed. The reference voltages $+V_S$ and $-V_S$ are 5 V and 0 V, respectively. The interface and layout are implemented in a standard CMOS process.

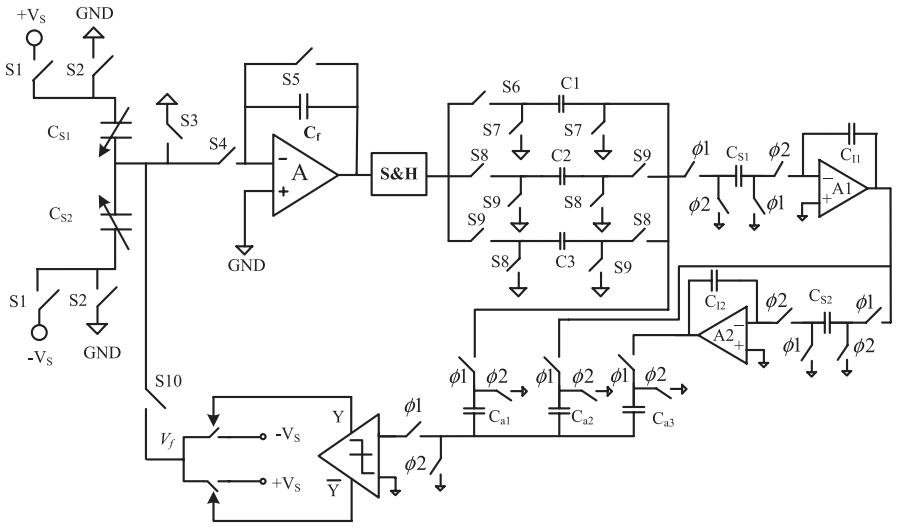

Fig. 4. Proposed interface circuit for the ΣΔ microaccelerometer

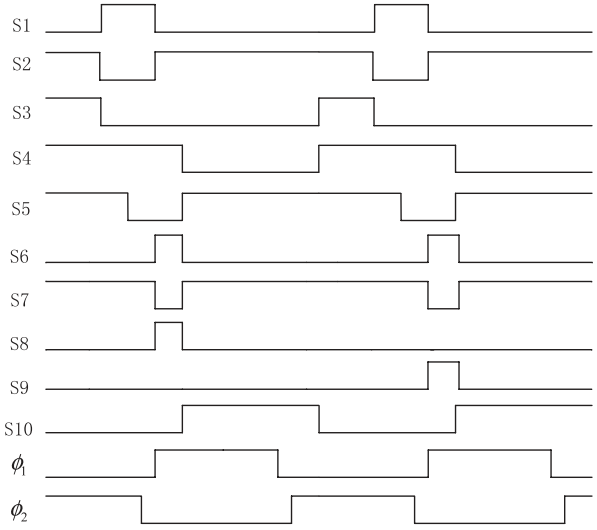

Fig. 5. Main timing diagram of the interface

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A vibration table produces harmonic distortions and decreases measurement resolution, therefore, an on-chip-test technique is proposed in [6] to measure the distortions of the microaccelerometer. However, this on-chip-test circuit is not available for a fully feedforward summation topology in this work due to the large gain of the feedforward path. Self-test circuit for a fully feedforward interface is thus proposed in this paper for the verification of low-distortion performance. A self-test circuit is presented in Fig. 6 to measure the harmonic distortion of the microaccelerometer. In Fig. 6, V_{st_in} is the input of the self-test signal, and V_{cp_out} is the output of the lead compensator in Fig. 4. The output signal V_{st_out} is followed by the input of the modulator. The self-test signal V_{st_in} can be performed as a input acceleration, and the electrostatic feedback force caused by the self-test signal leads to the displacement of the proof mass, and thus the dynamic performance of the microaccelerometer can be tested. On-chip test circuit presented in [6] achieved a HD3 lower than −100 dB and HD2 lower than −110 dB, respectively. A similar signal is applied to the input of self-test circuit proposed in this work, and the simulation result is shown in Fig. 7. The simulation results obtained in [6] and this work ignored the non-ideal conditions, such as the mismatch and interference. A HD2 of −131 dB and HD3 of −124 dB are achieved in this work, respectively. The results are better than that in [6], which indicates that the proposed architecture has low distortion characteristic.

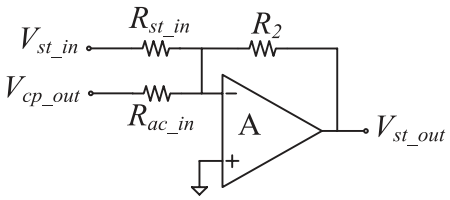

Fig. 6. Self-test circuit for the microaccelerometer

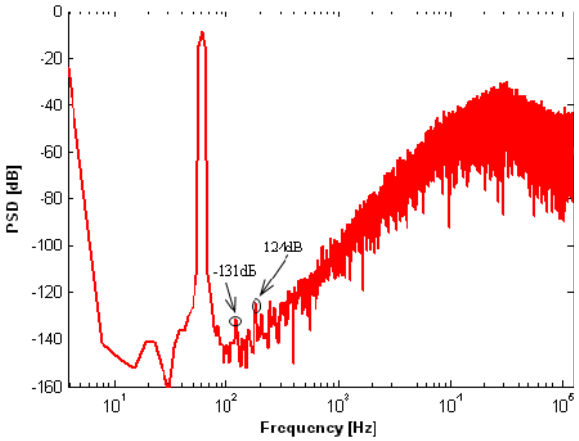

Fig. 7. Self-test simulation result

The microphotograph of the interface IC is shown in Fig. 8, and the critical individual blocks are highlighted. A silicon accelerometer is used and wire-bonded to the interface chip, and the total power dissipation is 10 mW [9]. A mass-spring shock absorption system is used to reduce the environment vibration, and the

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experiment is carried out in the underground. A rate table was used to test the linearity of the accelerometer. The output of the accelerometer was filtered by an analog filter, and a measured sensitivity of 0.5 V/g was attained. With a 1 g sinusoidal signal input centered at 10.01 Hz, the digital output is captured and calculated in a Matlab program. The measured output spectrum of the proposed microaccelerometer is shown in Fig. 9. The measurement result indicates that it achieves a second harmonic distortion (HD2) of −92.28 dB and a third harmonic distortion (HD3) of −99.27 dB, respectively. The harmonic distortions could be caused by the mismatch of the layout and the nonlinear electrostatic feedback force. The noise floor of the measured data is lower than $-115\,\mathrm{dBV/Hz^{1/2}}$. Referring to the achieved sensitivity, the sensor obtains a resolution of $9\,\mu\mathrm{g/Hz^{1/2}}$. The performance comparison is shown in Table I in a fundamental FOM [10], and the chip area does not include the area of MEMS devices. Table I shows overall noise floor and mechanical noise floor, respectively, and overall noise floor includes mechanical noise floor of the MEMS and electronic noise floor of the interface. The noise comparison results presented in Table I show that the electronic noise floor is dominant in all the sensors.

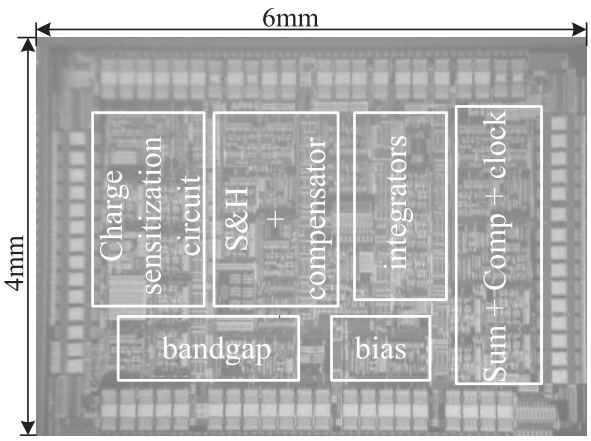

Fig. 8. Chip microphotograph

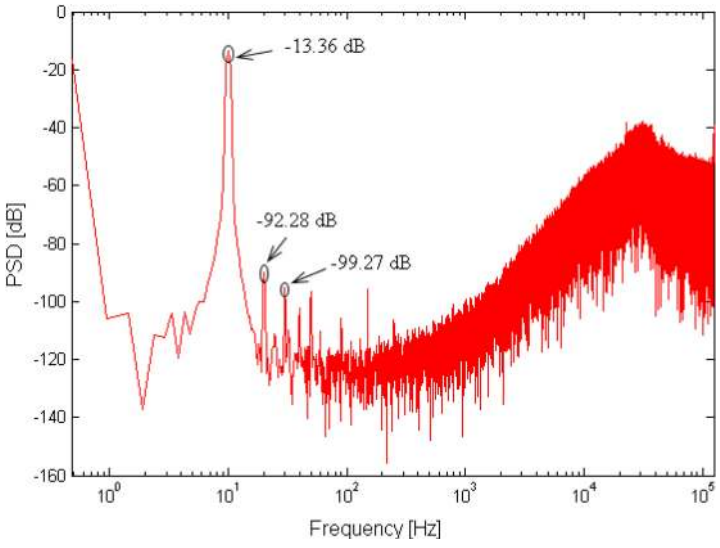

Fig. 9. Measurement result of the proposed ΣΔ microaccelerometer

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Table I. Performance comparison

Parameter	[5]	[10]	[11]	This work
Supply/Range	3 V/±0.1 g	3.6 V/±1.15 g	2.5 V/±1 g	5 V/±2 g
Power	4.5 mW	3.6 mW	6 mW	10 mW
BW (Hz)	500	200	75	400
DR (dB)	88	115	80	107
Chip area	36 mm^2	6.66 mm^2	4 mm^2	24 mm^2
Sensitivity	30 V/g	0.495 V/g	0.5 V/g	0.5 V/g
Overall noise floor /Mechanical noise floor ($\mu g/Hz^{1/2}$)	4/1	2/0.5	110/1	9/0.5
$FOM = \frac{P}{BW \times 10^{DR/20}}$	358 pW/Hz	32 pW/Hz	8 nW/Hz	112 pW/Hz

The complexity of circuit implemented in this work is relaxed compared with that in [2] and [10], but [5] and [11] have achieved an excellent work with more reduction of circuit complexity. Reference [5] achieved a large sensitivity with a relatively low power dissipation, but the chip area and range are not preponderant. Reference [10] has a small size of chip area, and the bandwidth and sensitivity are small. Reference [11] shows a small chip area, but the bandwidth, DR and overall noise floor are not satisfying. This work has more power dissipation due to high sampling frequency and power supply, which requires wide amplifier bandwidth, so the useful bandwidth and range are relatively larger. This work is advantageous in DR, resulting in a better FOM, when compared with [5] and [11]. However, the performance of [10] is more excellent due to a larger DR and lower power dissipation. The advantage of this work is that self-test circuit is proposed and low distortion result is achieved, which is not shown in the references. The overall noise floor and power dissipation of this work can be improved in the future research.

4 Conclusion

A low-distortion ΣΔ microaccelerometer is presented. The fully feedforward architecture uses a heavy lead compensator, in combination with the scaling factors, to form a stable system, which results in decreased integrator output swings. Based on the presented architecture, a low power dissipation interface circuit is designed and fabricated. The microaccelerometer consumes 10 mW from a 5 V supply and achieves a noise floor of 9 $\mu g/Hz^{1/2}$. The resulting HD2 and HD3 are −92.28 dB and −99.27 dB, respectively.

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