A Low-Dropout Regulator for SoC With Q-Reduction

Sai Kit Lau, *Member, IEEE*, Philip K. T. Mok, *Senior Member, IEEE*, and Ka Nang Leung, *Member, IEEE*

***Abstract*—A low-dropout regulator for SoC, with an advanced Q-reduction circuit to minimize both the on-chip capacitance and the minimum output-current requirement down to 100 μA, is introduced in this paper. The idea has been implemented in a standard 0.35-μm CMOS technology ($V_{\mathrm{THN}} \approx 0.55$ V and $|V_{\mathrm{THP}}| \approx 0.75$ V). The required on-chip capacitance is reduced to 6 pF, comparing to 25 pF for the case without Q-reduction circuit. From the experimental results, the proposed regulator-circuit implementation enables voltage regulation down to a 1.2-V supply voltage, and a dropout voltage of 200 mV at 100-mA maximum output current.**

***Index Terms*—Low-dropout regulator, power management, Q-reduction.**

I. Introduction

POWER management utilizing multiple local on-chip voltage regulators to power-up system sub-blocks individually, as shown in Fig. 1, is a very promising approach in system-on-a-chip (SoC) development [1]. In addition to the advantage of tailor-making supply voltages for optimizing performance of different circuits separately, power-line cross-talk problem can also be lessened. This approach is especially suitable for portable systems, since lower usage of PCB space and fewer off-chip components are advantageous to production. Of all the types of voltage regulators, low-dropout regulator (LDO) is regarded as a suitable choice for local on-chip voltage regulation in SoC, due to its fast transient response and low-noise advantages. However, an off-chip capacitor at LDO output, generally about 0.47 μF to 10 μF for a 200-mA LDO, is necessary to provide good dynamic performance and simultaneously ensure the regulator's stability [2]–[6]. On-chip capacitance, for example, the 0.6-nF decoupling capacitance in [6], consumes huge silicon area and is undoubtedly an obstacle in the SoC development.

Currently, many researchers and companies have been developing LDOs which do not need off-chip load capacitor for stability and performance. Many approaches, such as using non-standard technology-based approach, (for example, DMOS in [7]), and circuit-level-based pole-splitting approach [8], have been proposed with good performance. The conceptual figure of a LDO, based on pole-splitting method, is shown in Fig. 2. The LDO is viewed as a three-stage amplifier compensated by pole-splitting frequency compensation. The power dissipated at the power transistor increase its transconductance (g_{mp}). A higher g_{mp}, due to moderate output current, results in higher nondominant complex-pole frequencies. When the nondominant complex poles locate far higher than the unity-gain frequency (UGF) in the open-loop frequency response, the LDO is stable [9].

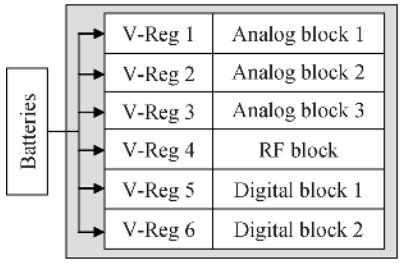

Fig. 1. An example, simplified power distribution of SoC.

However, as illustrated in Fig. 3, when the output current is low, the nondominant complex poles have a large Q (or small damping factor) and locate near UGF. A large Q causes a sharper phase change at the angular corner frequency. The LDO will then be unstable due to the magnitude peaking near UGF [9]. The minimum output current requirement of the pole-splitting-based LDO is in the range of several milli-ampere and should be further reduced for voltage regulation in a wider current range. One method to reduce the minimum output current level is to increase the on-chip compensation capacitance for lowering the UGF, since the UGF is inversely proportional to the compensation capacitance, as shown in Fig. 3 [9]. However, the larger on-chip capacitance consumes more chip area, and therefore, is not a good solution. Further development, focusing on minimizing the output current condition by advanced Q-reduction methods to control the nondominant complex poles, is one of the design directions of LDOs for SoC applications.

In this paper, a LDO targeted for SoC will be proposed. The key feature is to reduce required on-chip capacitance with the proposed Q-reduction circuit. Advanced circuit implementation of the Q-reduction circuit will then be introduced and discussed. Finally, experimental results will be given to verify the theory.

II. Proposed LDO Structure

The schematic of the proposed LDO is shown in Fig. 4. M01, M02, M03, and M04 form the first stage and the proposed current buffer (formed by M03 and M04 and C_{cf}), while M05, M06, M07, and M08 form the second noninverting gain stage. MPT is the power pMOSFET forming the third stage, and C_{gd}

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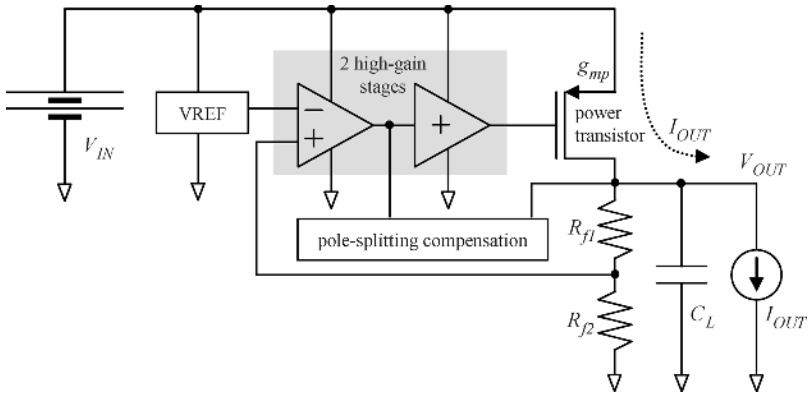

Fig. 2. Conceptual structure of the LDO in [8].

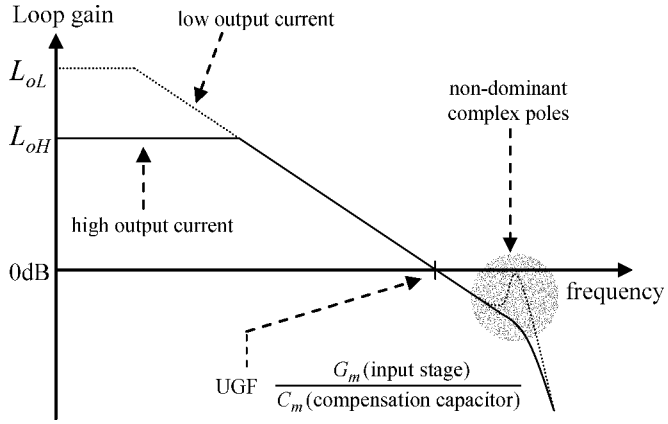

Fig. 3. Loop gains of pole-splitting-based LDO at different output currents.

is its gate-drain parasitic capacitance. M01, M03, and M08 form the feed-forward transconductance stage. C_{m1} and C_{cf} are the required on-chip capacitance of the proposed structure. R_{f1} and R_{f2} construct the feedback resistive network. R_L and C_3 model the equivalent load resistance and load capacitance at the power line. Fig. 4 shows that the bias current of the current buffer is, in fact, the bias current of the input stage. The high-gain property of the amplifier enforces the bias current of M03 and M04 to be nearly equal. Therefore, the proposed circuit implementation is simpler and consumes less power. Moreover, the small-signal current signals from input stage and from C_{cf} can be summed together to generate v_1.

A smaller g_{mcf}, which is the transconductance of M03, is needed to reduce Q. This is achieved by a small aspect size ratio of M03 and M04. This design requirement helps to reduce the random offset voltage of the input stage due to the mismatch of the threshold voltage of pMOS so that the LDO output voltage has less error due to process variations in mass production [10]. The feed-forward transconductance stage is formed by M01, M03 and M08. Both M06 and M08 form a push-pull stage such that the gate capacitance of the power pMOSFET can be charged and discharged more effectively for fast load transient responses.

The proposed LDO in Fig. 4 can be modeled by Fig. 5 in open-loop domain. The structure is basically composed of three gain stages (not including the Q-reduction circuit), where the third stage is the power pMOSFET in common-source configuration. Since the transistor size of the power pMOSFET is large, its gate-drain capacitance (C_{gd}) is also large and should be included for detailed analysis. The corresponding transconductance, output resistance and lumped output parasitic capacitance of each stage are denoted by g_{mi}, R_i and C_i (for $i = 1, 2,$ and 3), respectively. A compensation capacitor C_{m1} enables pole-splitting effect [9]. The proposed Q-reduction circuit is formed by C_{cf} and a current buffer (where the transconductance, input resistance, and input capacitance are g_{mcf}, $R_{cf} \approx 1/g_{mcf}$, and C_p, respectively). In this analysis, the current buffer is assumed to have ideal frequency response, which is valid in LDO design since the parasitic capacitances due to the current buffer are much smaller than those from the power transistor. As will be discussed, a feed-forward transconductance stage (g_{mf1}) is used to generate a left-half-plane (LHP) zero to improve both LDO stability and slewing at the gate of the power pMOSFET. Moreover, C_3 is the parasitic capacitance due to the power line in SoC and is generally larger than the internal nodal capacitances C_1, C_2, and C_p. The signal transfer function of the proposed LDO structure, regarded as loop-gain frequency response of a feedback circuit $L(s)$, is given by (1), shown at the bottom of the page. Since the output current of a LDO will change (so as g_{m3} will change), the stability of the proposed LDO should be considered at different load conditions. In this analysis, the stability of LDO is considered when the feedback factor defined by the feedback resistors is 1 (i.e., $V_{\rm OUT} = V_{\rm REF}$). This guarantees that the proposed LDO is stable when $V_{\rm OUT} > V_{\rm REF}$ in

$$L(s) = \frac{v_o(s)}{v_i(s)} \approx \frac{-g_{m1}g_{m2}g_{m3}R_1R_2R_3\left\{1+s\left(C_{cf}R_{cf}+\frac{C_{m1}g_{mf1}}{g_{m1}g_{m2}}-\frac{C_{gd}}{g_{m3}}\right)-s^2\left[\frac{C_{m1}(C_{gd}+C_2)}{g_{m2}g_{m3}}+\frac{C_{gd}C_{cf}R_{cf}}{g_{m3}}\right]\right\}}{(1+sC_{m1}g_{m2}g_{m3}R_1R_2R_3)\cdot\left[1+s\frac{C_{m1}C_{gd}(g_{m3}-g_{m2})+C_{cf}C_3g_{m2}+C_{m1}C_{cf}g_{m2}g_{m3}R_{cf}}{C_{m1}g_{m2}g_{m3}}+s^2\frac{(C_{gd}+C_2+C_{cf})C_3}{g_{m2}g_{m3}}\right]} \quad (1)$$

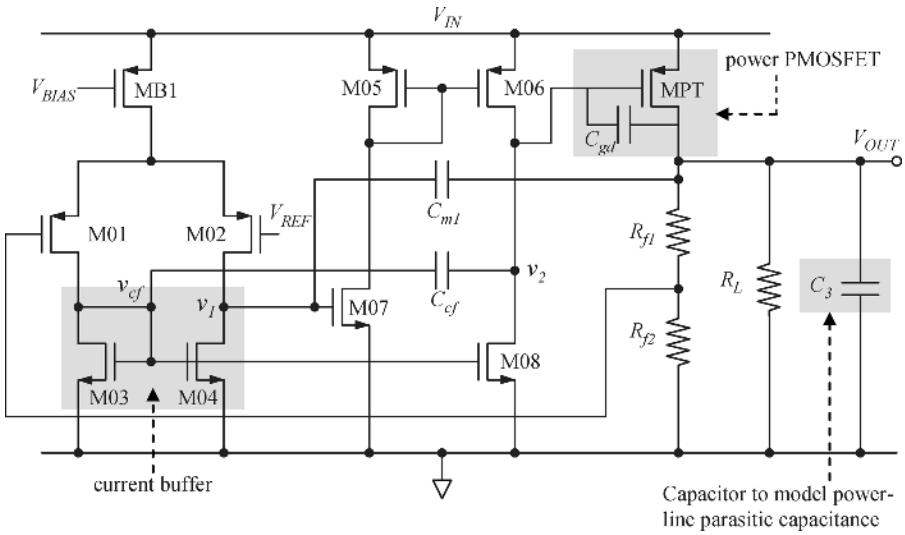

Fig. 4. Schematics of the proposed CMOS LDO.

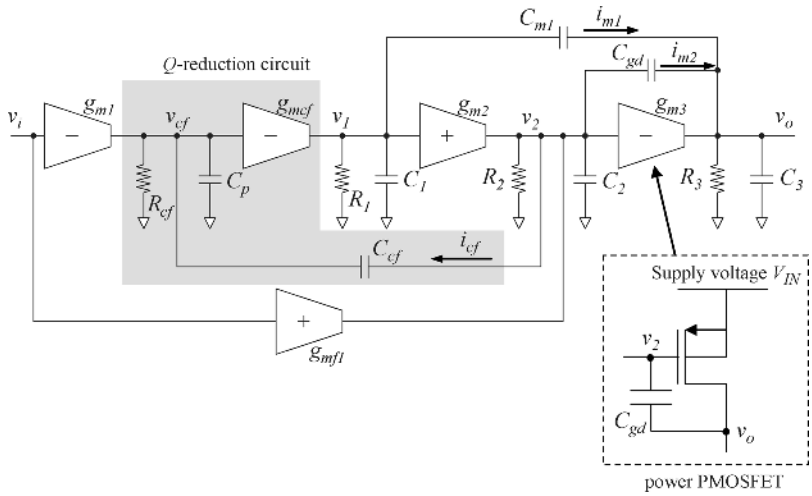

Fig. 5. Proposed LDO structure (open loop).

general operations. There are three cases to consider when C_3 is due to the parasitic capacitance of the power line and is not large.

Case 1: Moderate to Maximum Output Current (i.e., g_{m3} is Much Larger Than g_{m1} and g_{m2}): The transfer function in (1) is approximated as given in (2), shown at the bottom of the page. The second-order function at the denominator of (2) gives two separate poles when the condition $(4(C_{gd}+C_2+C_{cf})\cdot C_3)/g_{m3} \le (C_{gd}+C_{cf})^2/g_{m2}$ holds. That condition happens when the output current is high so that g_{m3} is very large. At this condition, there are three poles and one zero, given by $p_1 = 1/C_{m1}g_{m2}g_{m3}R_1R_2R_3$, $p_2 = g_{m2}/(C_{gd}+C_{cf})$, $p_3 = ((C_{gd}+C_{cf})\cdot g_{m3})/((C_{gd}+C_2+C_{cf})\cdot C_3)$ and $z_1 = g_{m1}g_{m2}/C_{m1}g_{mf1}$, respectively. With a large g_{m3}, p_3 locates at a high frequency and has no effect on LDO stability. When z_1 is used to cancel p_2, there is effectively one pole and the proposed LDO is stable for any resistive feedback factor with a theoretical phase margin of 90°.

Case 2: Low to Moderate Load Current (i.e., g_{m3} is Larger Than g_{m1} and g_{m2}): The transfer function is the same as (1).

$$L(s) \approx \frac{-g_{m1}g_{m2}g_{m3}R_1R_2R_3\cdot\left(1+\dfrac{sC_{m1}g_{mf1}}{g_{m2}g_{m3}}\right)}{(1+sC_{m1}g_{m2}g_{m3}R_1R_2R_3)\left[1+s\dfrac{(C_{gd}+C_{cf})}{g_{m2}}+s^2\dfrac{(C_{gd}+C_2+C_{cf})C_3}{g_{m2}g_{m3}}\right]} \tag{2}$$

There is a pair of complex poles since the coefficients of (1) have the following relationship when g_{m3} is not much larger than g_{m1} and g_{m2}:

$$\left[\frac{C_{m1}C_{gd}(g_{m3}-g_{m2})+C_{cf}C_3g_{m2}+C_{m1}C_{cf}g_{m2}g_{m3}R_{cf}}{C_{m1}g_{m2}g_{m3}}\right]^2 \leq 4\frac{(C_{gd}+C_2+C_{cf})C_3}{g_{m2}g_{m3}}. \quad (3)$$

By solving (1), there are one pole ($p_1 = 1/C_{m1}g_{m2}g_{m3}R_1R_2R_3$), one pair of complex poles, and one zero ($z_1 = g_{m1}g_{m2}/C_{m1}g_{mf1}$). The pole frequency of the complex poles is given by

$$\omega_O \approx \sqrt{\frac{g_{m2}g_{m3}}{(C_{gd}+C_2)\cdot C_3}} \quad (4)$$

and its Q is given by (5), shown at the bottom of the page, where k_1, k_2, k_3, and k_4 are constants dependent on load-current level. From (4), a higher output current, hence a larger g_{m3}, results in a higher ω_O and the stability of the proposed LDO will be improved. More importantly, from (5), the proposed Q-reduction circuit decreases Q linearly by a larger C_{cf} and a smaller g_{mcf} of the current buffer. Therefore, the minimum output current of the proposed LDO can be reduced effectively by controlling C_{cf} and g_{mcf} separately. As a reference, for the same circuit structure and transistor parameters ($g_{m1} = 120$ μA/V, $g_{m2} = 480$ μA/V, $g_{m3} = 1.5$ mA/V, $C_{gd} = 6.4$ pF, $C_3 = 100$ pF), the Q factors with Q-reduction technique ($C_{m1} = 5$ pF and $C_{cf} = 1$ pF) and without ($C_{m1} = 25$ pF and $C_{cf} = 0$, note that in this case, a larger C_{m1} is needed for stable loop gain) is 2.2 and 7.4, respectively. There is about 3.4 times reduction on the Q factor and hence a smaller C_{m1} can be used when the proposed Q-reduction technique is employed. The phase margin (PM) of the LDO in this case can be evaluated by [11], [12]

$$\begin{aligned}\mathrm{PM} &= 180^\circ - \tan^{-1}\left(\frac{\mathrm{UGF}}{p_1}\right) - \tan^{-1}\left\{\frac{\mathrm{UGF}/\omega_O}{Q\left[1-(\mathrm{UGF}/\omega_O)^2\right]}\right\} + \tan^{-1}\left(\frac{\mathrm{UGF}}{z_1}\right)\\ &= 90^\circ - \tan^{-1}\left\{\frac{\mathrm{UGF}/\omega_O}{Q\left[1-(\mathrm{UGF}/\omega_O)^2\right]}\right\} + \tan^{-1}\left(\frac{\mathrm{UGF}}{z_1}\right) \quad (6)\end{aligned}$$

where $\mathrm{UGF} = g_{m1}/C_{m1}$. From (6), there are a few important implications for design.

1) The critical phase reduction is due to ω_O. Therefore, a lower UGF by a larger C_{m1} can help to increase the phase margin.
2) A smaller g_{mcf} and a larger C_{cf} help to reduce Q, as shown in (5). This can help to reduce the negative phase shift for more phase margin.
3) The parameter g_{mf1} is very useful to control the position of z_1 for positive phase shift. Since, according to (4), ω_O is low when g_{m3} is low (or light load). The position of z_1, in terms of g_{mf1}, should be designed in light-load condition.

Case 3: Very Light Output Current: When the load current is very small, the small g_{m3} will result in an unstable LDO. The boundary between stable and unstable regions of the proposed LDO is addressed here. It is well-known that right-half-plane (RHP) pole causes unstable negative feedback system [10]. From the denominator of (1), RHP poles can be avoided when the s term in the second-order function is positive. Therefore, the necessary condition is given by

$$C_{m1}C_{gd}(g_{m3}-g_{m2})+C_{cf}C_3g_{m2}+C_{m1}C_{cf}g_{m2}g_{m3}R_{cf} > 0. \quad (7)$$

By rearranging the term, the minimum g_{m3} is

$$g_{m3(\min)} = \frac{\left(\frac{C_{cf}+C_3}{C_{m1}+C_{gd}}\right)\cdot g_{m2}}{1-\left(\frac{C_{cf}}{C_{gd}}\right)\cdot g_{m2}R_{cf}}. \quad (8)$$

Therefore, the minimum load current that the LDO is stable can be found indirectly from $g_{m3(\min)}$. In general, it requires a current higher than the bias current of the resistive feedback network that passing through the power pMOSFET.

A loop-gain simulation of the proposed LDO in Fig. 6 has been performed to study the stability. The simulation is with a BSIM3v3 0.35-μm CMOS model from Austria Mikro System Group, Austria (AMS). The capacitance C_3 at power line is assumed to be 100 pF in the simulation. From the simulation results in Fig. 6, the stability of the proposed LDO is better when the output current is higher, as expected according to the stated theory. The nondominant poles locate separately in frequency domains at higher output current, while a pair of complex poles with a higher Q is generated at lower output current. Based on the proposed structure and implementation, the minimum output current is about 100 μA when an on-chip C_{cf} of only 1 pF is used. Moreover, the effect due to process and temperature variations is also studied by simulations. The proposed LDO is loaded with a current of 100 μA. Corner transistor models provided by the foundry are used to investigate the impact to sta-

$$\begin{aligned}Q &= \sqrt{\frac{(C_{gd}+C_2)C_3}{g_{m2}g_{m3}}}\cdot\left[\frac{C_{m1}g_{m2}g_{m3}}{C_{m1}C_{gd}(g_{m3}-g_{m2})+C_{cf}C_3g_{m2}+C_{m1}C_{cf}g_{m2}g_{m3}\cdot(1/g_{mcf})}\right]\\ &\propto \frac{k_1}{k_2+[C_{cf}\cdot(k_3+k_4/g_{mcf})]} \quad (5)\end{aligned}$$

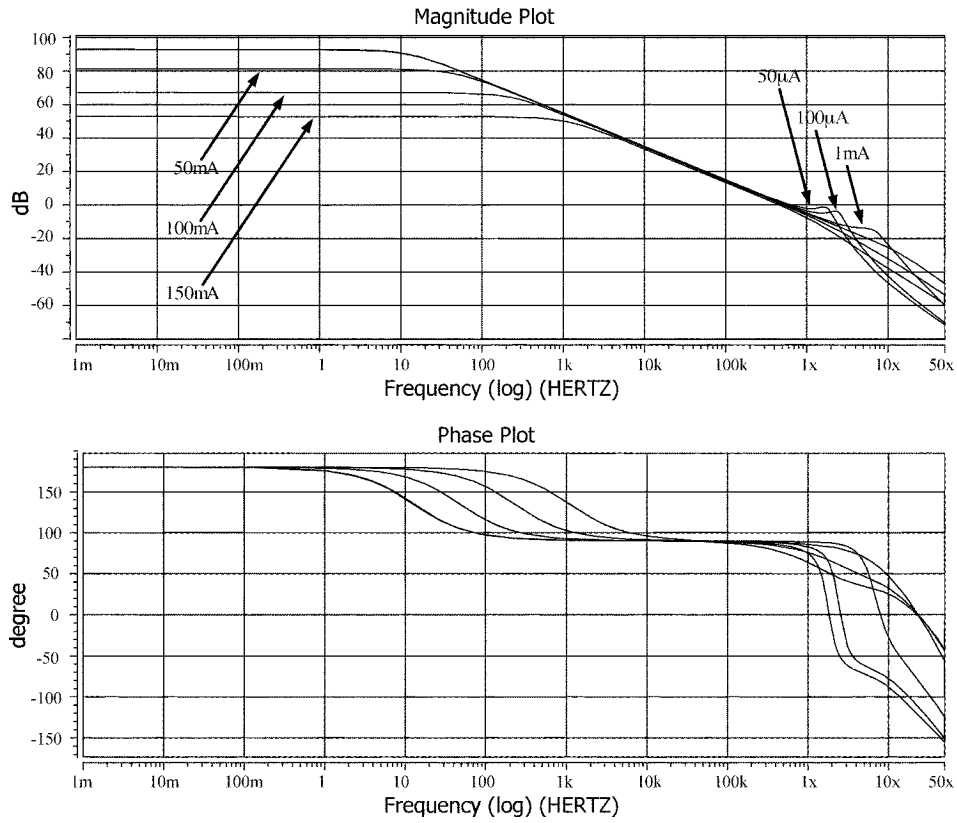

Fig. 6. Loop-gain simulation ($V_{\rm IN} = 1.2$ V and $V_{\rm OUT} = 1$ V).

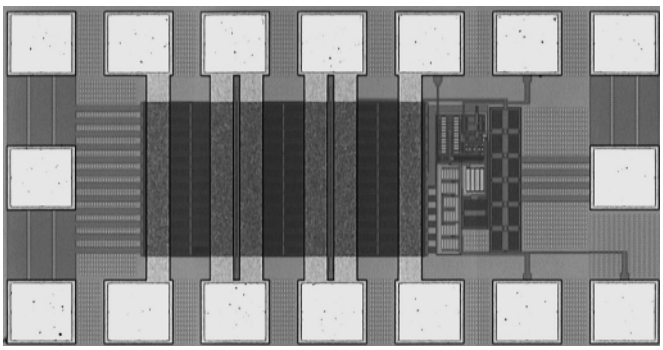

Fig. 7. Micrograph of proposed LDO (testing pads included).

TABLE I
CORNER-MODEL SIMULATIONS OF THE PROPOSED LDO

Conditions: At V_{DD} = 1.2 V, V_O = 1.0 V, I_{OUT} = 100 μA

Temp = 25°C

Corners	tm	wo	wp	ws	wz
UGF (Hz)	595k	495k	650k	469k	630k
PM (degree)	86.6	87.8	86.1	87.9	86.1

Temp = 85 °C

Corners	tm	wo	wp	ws	wz
UGF (Hz)	659k	582k	527k	596k	285k
PM (degree)	84.9	86.2	81.9	85.1	96.8

Temp = -40 °C

Corners	tm	wo	wp	ws	wz
UGF (Hz)	514k	355k	588k	335k	575k
PM (degree)	88	89.5	87.6	89.8	87.5

where tm = typical mean; wo = worst one; wp = worst power;
ws = worst speed and wz = worst zero.

bility. From the simulated results in Table I, the proposed LDO retains stable at different corners.

III. EXPERIMENTAL RESULTS

The proposed LDO has been implemented in AMS double-poly triple-metal 0.35-μm CMOS technology. The threshold voltages of nMOSFET and pMOSFET are 0.55 V and −0.75 V, respectively. The chip micrograph is shown in Fig. 7, and the active silicon area is 236 μm × 529 μm, excluding the testing pads. The LDO can operate down to 1.2 V with a preset output voltage of 1 V. The dropout voltage at output current of 100 mA is 200 mV. The maximum ground current is about 100 μA at $V_{\rm IN} = 3.3$ V. The measured results are in Table II.

Load transient response with no off-chip capacitor (the estimated parasitic capacitance $C_3 = 100$ pF) at $V_{\rm IN} = 1.2$ V and $V_O = 1$ V has been tested to verify the stability of the proposed LDO. As shown in Fig. 8, the LDO output voltage has no oscillation when the load current changes from 100 μA to 100 mA in 1 μs, or vice versa. It is proven that the minimum output-current requirement for pole-splitting type LDO is reduced by the proposed Q-reduction circuit. Moreover, the proposed LDO is

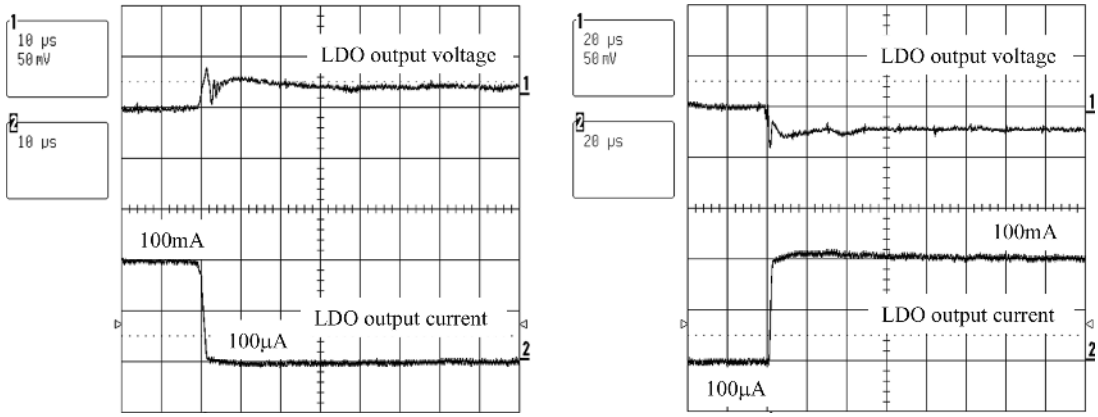

Fig. 8. Measured load transient responses at $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 1$ V, $C_3 = 100$ pF.

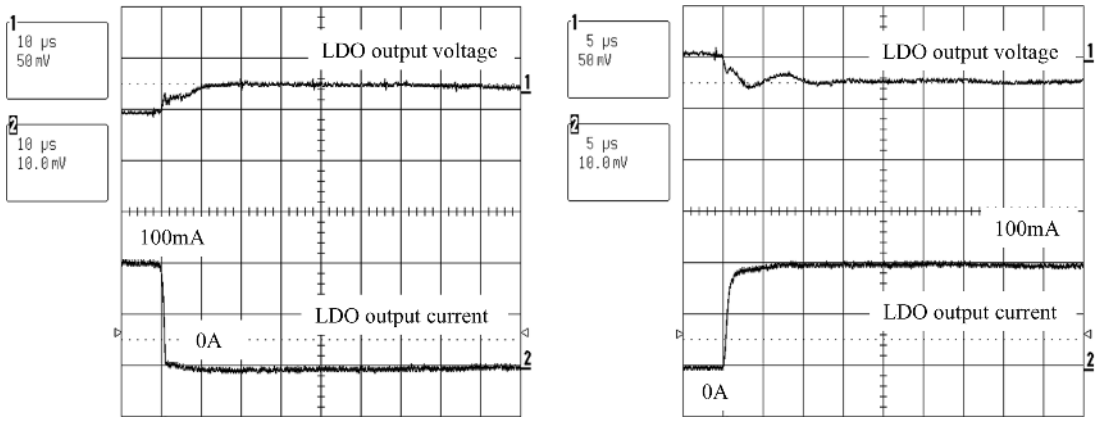

Fig. 9. Measured load transient responses at $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 1$ V, $C_L = 10\,\mu$F.

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED LDO

Technology	AMS 0.35-µm CMOS 2P 3M
Threshold Voltage	V_{THN} ⊕0.55 V and $\|V_{THP}\|$ ⊕0.75 V
Input Voltage (V_{IN})	1.2 V to 3.3 V
Preset Output Voltage (V_O)	1.0 V
Output Current	100 µA to 100 mA
Dropout Voltage	200 mV@100 mA
Line regulation	344 μV/V@100 mA
Load Regulation	–338 μV/mA@V_{IN} = 1.2 V
On-chip capacitance	$C_{m1} + C_{cf} = 6$ pF
Power-line load capacitance modeling	$C_3 = 100$ pF
Active Chip Area	236 µm x 529 µm (excluding testing pads)

also stable when an off-chip capacitor is used. The equivalent series resistance of the off-chip capacitor creates a LHP zero for pole-zero cancellation to achieve LDO stability. Fig. 9 shows the load transient responses when a 10-μF off-chip capacitor is used.

IV. CONCLUSION

A LDO for SoC has been introduced, supported by circuit-modeling analysis and experimental results. The proposed LDO structure and the proposed Q-reduction circuit, as well as its circuit implementation enable a smaller chip area and lower minimum output current requirement, which are very important for future SoC on chip, local voltage regulations.

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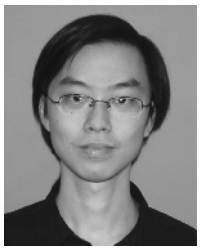

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