A Low Jitter 1.6 GHz Multiplying DLL Utilizing a Scrambling Time-to-Digital Converter and Digital Correlation

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Abstract

This paper presents a 1.6 GHz multiplying delay-locked loop (MDLL) that leverages time-to-digital conversion and a digital correlation technique to achieve low deterministic jitter while still maintaining low random jitter. A proposed time-to-digital converter consists of a ring oscillator that is gated on and off to accurately measure time and scramble the measurement's residual error. Using a 50 MHz reference, the prototype system has measured reference spurs less than -59 dBc and an overall measured jitter of 1.41 ps.

Keywords: MDLL, delay offset, deterministic jitter, reference spur, correlation, TDC, scrambling, noise shaping.

Introduction

Multiplying delay-locked loops (MDLL) have been proposed in recent years as an alternative to PLLs for generating high speed clocks [1, 2]. An MDLL drastically reduces phase noise of its ring oscillator by periodically multiplexing a clean edge from the reference, as seen in Fig. 1, thereby removing the jitter accumulated since the last reference edge. However, the resulting improvement in random jitter is typically accompanied by deterministic jitter due to misalignment between the VCO edge and the reference edge that replaces it. As shown in Fig.1, the deterministic jitter takes the form of periodic changes in the output period that occur at each reference edge.

Reduction of deterministic jitter in MDLL circuits has recently been a topic of active research [3]. Previously proposed approaches have been analog in nature, and are limited by mismatch issues that introduce offsets within the analog feedback loop. In contrast, techniques borrowed from newly proposed digital PLL architectures [4] offer the possibility of eliminating such analog issues. Unfortunately, straightforward use of a classical time-to-digital converter (TDC) [4] for this application would still lead to offset issues and would also be prone to large limit cycles. To overcome these limitations, we present a digital correlation technique that largely eliminates the offset issue, and a time-to-digital converter that removes the limit cycle issue.

Proposed Correlation Technique

Fig. 2 illustrates the proposed correlation technique to largely eliminate offset issues for improved deterministic jitter suppression. Rather than trying to directly measure the offset once every reference period by using a phase detector, as shown in Fig. 1, we instead take two measurements every reference period and *infer* the offset by subtracting those two measurements, as shown in Fig. 2. By using the same TDC for each of the measurements, offset is virtually eliminated and the deterministic period change of the MDLL output, Δ,

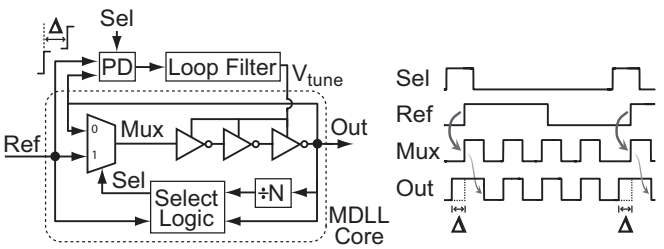

Fig. 1 Classical MDLL and its timing diagram

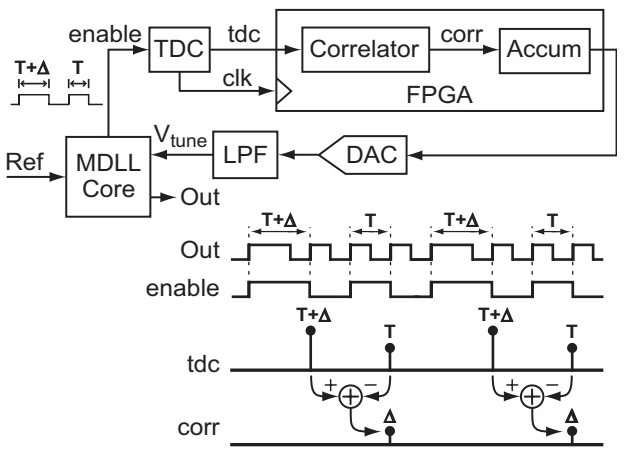

Fig. 2 Proposed MDLL implementation and its timing diagram showing the proposed digital correlation

is accurately measured. This measurement technique is essentially the digital equivalent of popular correlated double-sampling techniques that have been applied in numerous analog applications.

As with a classical MDLL structure, the resulting error signal, Δ, is used to tune the delays of the ring oscillator elements such that its output edge becomes aligned with the reference edge that replaces it. The resulting feedback circuit consists of both digital and analog components. It includes a digital accumulator (Accum), a 16-bit digital-to-analog converter (DAC), and a first-order analog low-pass filter (LPF). In the prototype, the digital operations are implemented using an FPGA that is clocked by the TDC output clock, which runs at twice the reference frequency. The MDLL core and TDC are custom chips implemented in 130 nm CMOS, and the DAC is an off-the-shelf discrete component.

Proposed Time-to-Digital Converter

Fig. 3 illustrates a classical TDC structure in which time is measured with accuracy set by the delay through one buffer cell. Unfortunately, the resulting resolution is typically limited to tens of picoseconds (ps), which is far larger than the sub-ps resolution desired in this application. Since an

MDLL requires an integer-multiple relationship between its output and reference frequencies, the resulting residue will not be scrambled and the resolution cannot be significantly improved through averaging. In fact, the placement of such a TDC within the MDLL feedback loop will lead to large limit cycles that introduce significant jitter in the MDLL output.

By scrambling the TDC residue, the effective measurement resolution is substantially improved with averaging [5] and, moreover, limit cycles are ideally eliminated when the TDC is placed in a feedback loop. Here we propose a simple and compact TDC architecture that achieves scrambling of the residue through use of a gated ring oscillator (GRO). As shown in Fig. 4, the oscillator is enabled during the measurement time (when Enable = 1), and disabled otherwise. A counter tracks the number of oscillator edge transitions for each sample, which relates directly to the length of the enable pulse. Since the internal oscillator state is held after each sample, the starting point for the next sample corresponds to the stopping point of the last sample. As a result, the residue essentially becomes scrambled and, interestingly, is first order noise shaped.

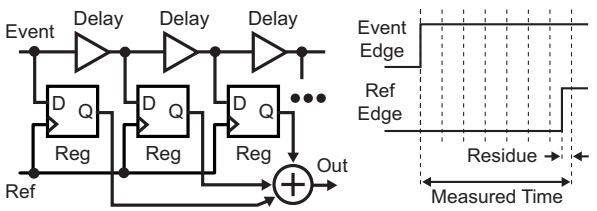

Fig. 3 Classical TDC architecture

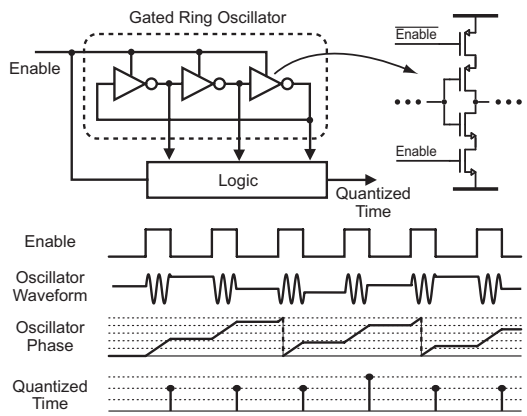

Fig. 4 Proposed digital GRO-TDC architecture

Measurement Results

Fig. 5 shows chip micrographs for the MDLL core and GRO-TDC, implemented in a 130 nm process with core areas of 150×250 μm^2 and 120×172 μm^2, respectively. At the highest reference frequency of 100 MHz, the chip cores consume 5 mA and 2 mA for the MDLL core and GRO-TDC, respectively. Table 1 lists performance summary for an output frequency of 1.6 GHz using a reference of 100 MHz and 50 MHz (divided down from 100 MHz on-chip).

For a 50 MHz reference, the measured reference spur of the proposed MDLL is -59.6 dBc, as seen in Fig. 6 showing a snapshot from an HP8595E spectrum analyzer. Based on this measurement and Fourier series analysis, the resulting deterministic jitter is calculated to be less than 0.7 ps peak-to-peak (p-p). The measured overall jitter, using an Agilent 86100A oscilloscope, is 1.41 ps (rms) and 11.7 ps (p-p), as shown in Fig. 6.

However, it is important to recognize that the oscilloscope has a trigger jitter specification of more than 1.2 ps (rms) and, therefore, is inadequate for sub-picosecond jitter measurement. As an alternative method to estimate the random jitter, the MDLL output phase noise was measured using an Agilent E5052 signal analyzer. The random jitter was calculated by integrating the measured phase noise from 1 kHz to 40 MHz, resulting in 0.54 and 0.36 ps (rms) for the 50 and 100 MHz references, respectively.

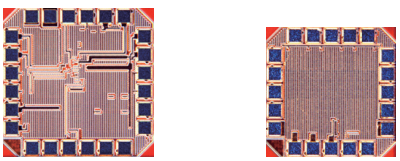

Fig. 5 Chip microphotographs for the MDLL core and GRO-TDC

Table 1 Performance Summary for 1.6 GHz Output

Process	130 nm CMOS
Core area	MDLL : 150 × 250 μm^2, GRO: 120 × 172 μm^2
Core Power	MDLL: 5 mA, GRO: 2 mA (100 MHz) @ 1.2V
Reference Spur	-59.6 dBc (50 MHz) and -61.6 dBc (100 MHz)
Deterministic Jitter (peak-to-peak)	< 0.7 ps (50 and 100 MHz), as calculated from measured reference spurs
Random Jitter (rms)	from integrated phase noise (1 kHz to 40 MHz): 0.54 ps (50 MHz) and 0.36 ps (100 MHz)
Overall Jitter	1.41 ps (rms) and 11.7 (p-p) for a 50 MHz reference, measurement limited by oscilloscope's internal jitter

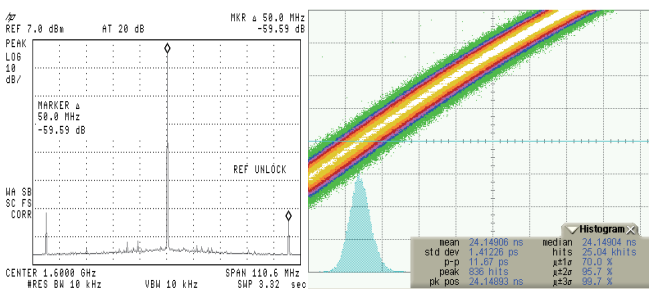

Fig. 6 Measured Reference Spur and Overall Jitter (at 50 MHz)

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