A Low-jitter 2.5-to-10 GHz Clock Multiplier Unit in CMOS

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Abstract— **This paper demonstrates a low-jitter clock multiplier unit [1] that generates a 10 GHz output clock from a 2.5 GHz reference clock. An integrated 10 GHz LC-oscillator is locked to the input clock, using a simple and fast phase detector circuit. This phase detector overcomes the speed limitation of a conventional tri-state Phase Frequency Detector, by eliminating an internal feedback loop. A frequency detector guarantees PLL locking without degenerating jitter performance. The clock multiplier is implemented in a standard 0.18μm CMOS process and achieves a jitter generation of 0.22 ps while consuming 100 mW power from a 1.8 V supply.**

Keywords— **Clock Multiplier Unit, Frequency Synthesis, Oscillator, Phase Locked Loop, Phase Detector, CMOS, jitter.**

High-speed low-jitter serial optical transmitters rely on a high-performance clock multiplier unit (CMU) to convert a parallel-input clock signal into a serial-output clock signal. For SONET/SDH compliant systems, the CMU in the transmitter typically consumes a large part of the power budget, as multi-GHz operation combined with sub-picosecond jitter is required. The trend in serial communication circuits is the increase in frequencies of the parallel input clock and of the serial output clock signals. At this moment, the state-of-the-art CMU implemented in a standard CMOS technology [2] operates with a parallel input signal of 622 MHz and outputs a signal with a frequency of 10 GHz. It can be anticipated, however, that next-generation serial transmitters will operate with parallel, or reference frequency, signals of the order of 2.5 GHz and will require the CMU to produce output signals in the 10 and 40 GHz frequency range.

We present a 10 GHz CMU, implemented in 0.18μm CMOS, that works with reference frequencies in excess of 2.5 GHz, with significantly better jitter and power dissipation performance than reported in CMOS so far [2]. To achieve the high reference frequency, we used a fast linear Phase Detector (PD) in combination with a Frequency Detector (FD). Figure 1 shows the top-level block diagram of the CMU with the proposed PD and FD.

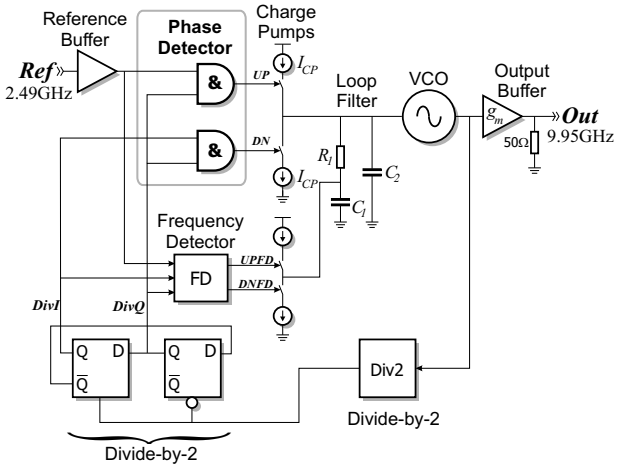


Fig. 1
ARCHITECTURE OF THE CLOCK MULTIPLIER UNIT.

The speed of a conventional tri-state Phase Frequency Detector (PFD) is limited due to the internal reset loop needed to asynchronously reset the logical circuitry that generates the *UP* and *DN* pulses for the Charge Pump (CP) [3]. Due to the absence of this slow reset loop in the proposed PD, it can run at much higher frequencies. Simulations show a speed improvement of at least a factor 4, in a 0.18μm CMOS technology. The fast PD can be seen as a step toward the realization of OC-768 transmitters (40 Gbps) in CMOS. To achieve low jitter operation, the detector generates CP signals, thus inheriting the favor-

able noise and spurious injection properties of CP based PLLs.

The operation of the PD is illustrated in Figure 2. It exploits the readily available quadrature signals of the last divider stage (*DivI* and *DivQ*) to generate *UP*/*DN* pulses using two AND-gates. Note that the width of the *UP* pulse responds *linearly* to the time overlap of *DivQ* and *Ref*. The width of the *DN* pulse depends on the time-overlap of *DivQ* and *DivI*. In lock, with coinciding rising edges of *Ref* and *DivI*, the *UP* pulse has the same width as the *DN* pulse, in which case the CP current sources cancel, resulting in low output spurs. When in phase-lock, the *UP*/*DN* signals have a duty-cycle of about 25%, so that a potential dead-zone in the transfer function of the PD/CP combination can be easily avoided.

Figure 3 demonstrates that the locking position and the gain of the PD/CP combination are insensitive to the quadrature accuracy of the *DivI* and *DivQ* signals, and to the duty cycle of the reference signal. These properties do influence the extremes of the linear operation input range of the PD, which for perfect conditions ranges from $-\pi/2$ to $+\pi/2$.

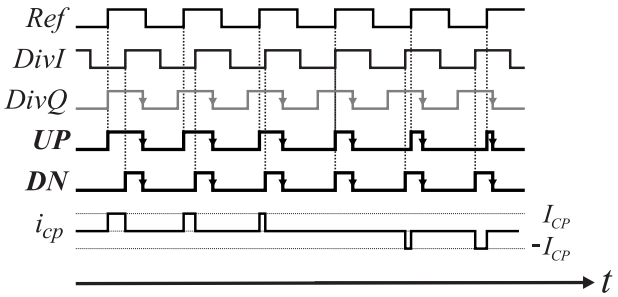
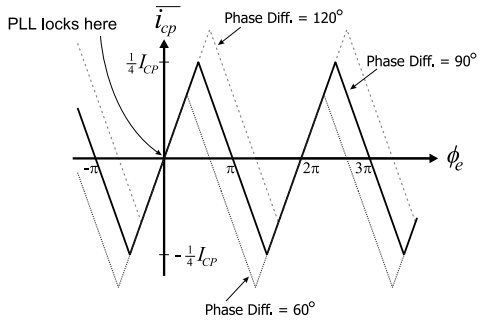
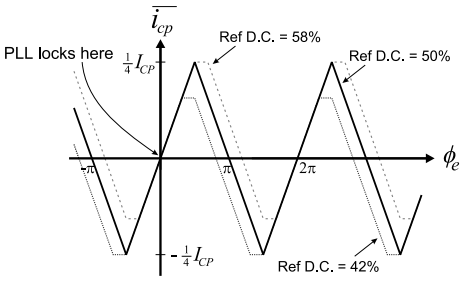


Fig. 2
RESPONSE OF THE PD.



(a)Imperfect quadrature



(b)Reference Duty Cycle

Fig. 3
INFLUENCE OF IMPERFECT QUADRATURE AND REFERENCE DUTY CYCLE ON PD/CP RESPONSE.

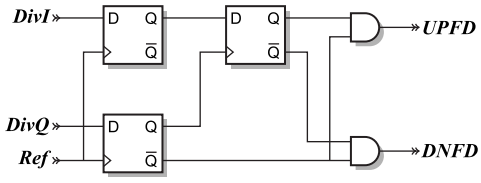


Fig. 4
IMPLEMENTATION OF THE FREQUENCY DETECTOR.

Because of the limited pull-in range of the PD, a frequency detector (FD) as shown in Figure 4 was added to ensure correct locking of the PLL over the entire tuning range of the VCO. The FD is similar to the architecture presented in [4], with two AND-gates added to generate CP compatible signals (*UPFD* and *DNFD*). The FD works reliably up to much higher frequencies than the conventional PFD architecture, as the flip-flops in this FD have an output frequency that is equal to the difference between the reference frequency and the divided VCO frequency. Also, the flip-flops do not need to be reset asynchronously, which makes their design easier and faster. A further strong point of the proposed detector is its inactivity when frequency lock has been achieved, eliminating the need for a lock detector. The PD and FD work in parallel without the FD disturbing the loop when in phase-lock.

The 2.5 GHz reference frequency allowed by this PD/FD combination will lower the frequency division ratio of the loop as compared to that of a lower reference frequency PLL. This in turn will lower the close-in phase noise and the integrated output jitter. Because the optimum loop bandwidth will increase due to the lower close-in phase noise, the loop filter capacitor sizes will decrease, thus significantly reducing chip area.

The CMU was realized in a standard 0.18μm CMOS process with a substrate resistivity of 10 Ω·cm. It provided 5 metallization layers, but not the possibility of triple well isolation. The frequency dividers and logic elements of the IC were implemented using Current Mode Logic (CML) to ensure both low sensitivity to and low generation of supply and substrate noise. The CPs use low-voltage mirrors to enable rail-to-rail operation at the output node and to in-

crease the CP output resistance. The 10 GHz LC VCO is constructed around a negative *Gm*-cell implemented as a cross-coupled NMOS differential pair. The VCO uses an inductor with a patterned ground shield to decrease substrate losses, achieving a measured Q of 17 at 10 GHz [5]. The PLL loop bandwidth was optimized with respect to jitter performance, using noise simulations combined with VCO noise measurements. The IC draws a current of 55 mA from the 1.8 V power supply (99 mW), including the output buffer.

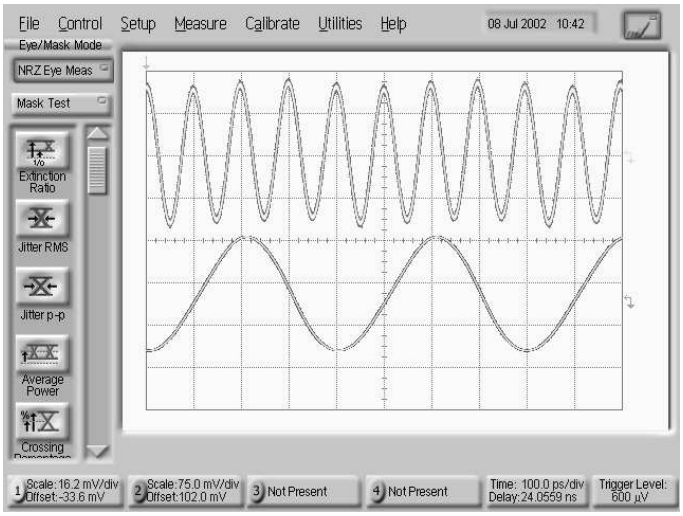


Fig. 5
OSCILLOSCOPE SCREENDUMP OF THE 2.5 GHZ REFERENCE INPUT SIGNAL AND THE 10 GHZ PLL OUTPUT.

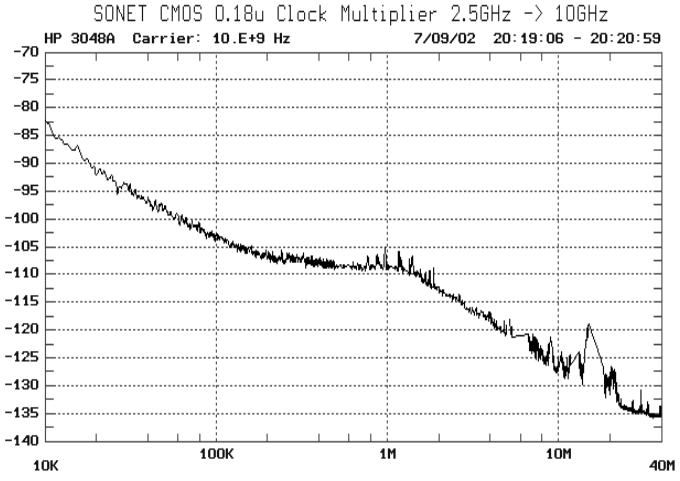


Fig. 6
PHASE NOISE MEASUREMENT RESULTS.

The measured time-domain operation of the CMU is presented in Figure 5. The 2.5 GHz input signal was derived from a Marconi 2042 signal generator. The jitter generation of the CMU was measured with a HP3048A phase noise measurement setup in PLL-configuration. The phase noise spectrum of the 10 GHz output signal is shown in Figure 6. Integration of the phase noise spectrum using the integration limits defined for OC-192 SONET systems (50 kHz up to 80 MHz), yields an rms-jitter of 0.8^o (equivalent to 2.2 mUI rms), which is almost a factor 5 lower than the SONET recommendation of 10 mUI rms. A usual rule-of-thumb can be used to predict a peak-to-peak jitter of 2.2 ps (22 mUI rms). The table in Figure 7 summarizes the IC performance. Comparing to the state-of-the-art [2] we realized an approximate factor 3 improvement in peak

Property	Value
Output Frequency	9.953 GHz
Reference Frequency	2.488 GHz
Technology	0.18µm standard CMOS
Jitter Generation (RMS)	0.8^o rms, equiv. to 0.22 ps rms
Jitter Generation (peak-to-peak)	2.2 ps (SONET spec. = 10 ps)
Supply Voltage	1.8 V
Chip Size	0.83 x 0.86 mm^2
Power Consumption	99 mW 81 mW without output buffer

Fig. 7
CMU PERFORMANCE SUMMARY

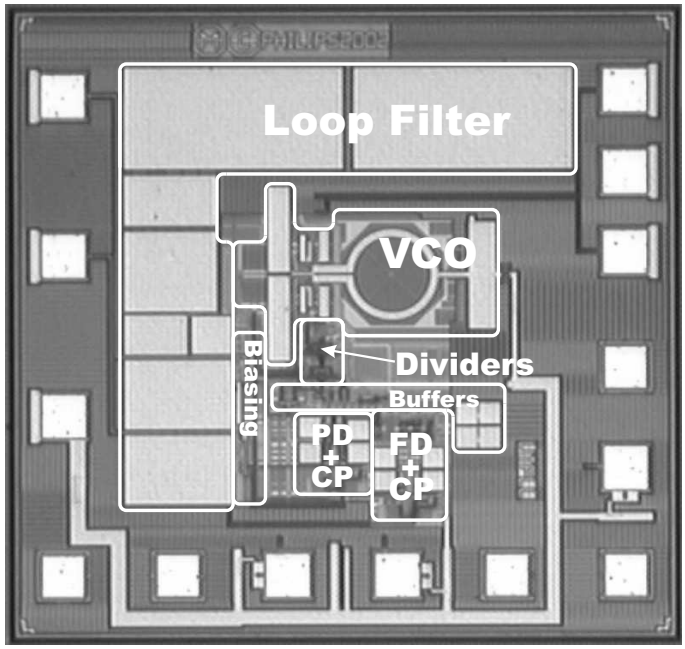


Fig. 8
CHIP MICROGRAPH

jitter performance, for around 2 to 3 times less power dissipation in a comparable technology. Figure 8 shows the chip micrograph.

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