A Low-Loss 77 GHz Sub-Sampling Passive Mixer Integrated in a 28-nm CMOS Radar Receiver

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***Abstract* — This paper demonstrates that using sub-sampling mixer topology can be the right choice to implement a millimeter-wave (mmW) receiver. In a 77 GHz radar receiver, it allows to reduce the burden of a 77 GHz LO distribution chain, in term of area and consumption, while preserving RF performances. Demonstration is done from two topologies of ×3 sub-sampling mixers implemented in 28-nm FD-SOI CMOS technology. The best proposed passive mixer exhibits a -2.1 dB conversion gain (G_{cv}), a 1dB input-referred compression power (ICP1dB) of +3.5 dBm, and a 16.8 dB Single Side Band Noise Figure (NF_{SSB}). The mixer LO signal shaping consumption is 32 mW on a 1.2 V supply while the passive mixer core does not require any DC power.**

Keywords — Millimeter-wave, Sub-harmonic, FD-SOI.

I. Introduction

By preventing crashes and identifying potential dangers even under low visibility conditions, the 77 GHz automotive radar drastically improves driving safety. Using mm-wave frequencies enables a good circuit integration and a fine range resolution, thanks to wide modulation bandwidths. Nevertheless, using a 77 GHz frequency often requires complex and power-hungry LO distribution chains. Conventional radar architectures are mostly based on a 38.5 GHz VCO followed by a frequency doubler and high consumption 77 GHz drivers [1],[2]. At the scale of a full chip including several receivers, this approach is complex and results in extra power consumption and extra circuit area. A sub-sampling mixer driven with a LO frequency sub-multiple of the RF frequency ($f_{LO} \approx f_{RF}/n$ with n a natural integer) would drastically simplify the picture. Passive sub-sampling mixers as described in [3] are popular for low frequency receivers as the sub-harmonic down-conversion is performed with low conversion losses and high linearity. The aim of this paper is to demonstrate that it can be extended to mmW frequencies. Hence, a ×3 sub-sampling mixer is proposed and implemented with a LNA in a 77 GHz receiver showing that this solution is compliant with the high requirements of automotive radar application. Section II introduces the sub-sampling mixer principle. Then, two mixer topologies relying on different mixer cores and associated 26 GHz LO signal shapers are detailed in section III. Measured performances of the 28-nm FD-SOI CMOS test chips validating this topology are given in section IV. Finally, section V draws the conclusions of this work.

II. Sub-Sampling Mixer Principle

In an ideal sampling operation, every RF signal close to a sampling frequency harmonic ($n.f_{LO}$) is converted at a f_{IF} of $|f_{RF}-n.f_{LO}|$ without any conversion losses. Consequently, using sub-sampling with $f_{LO} \approx f_{RF}/n$ appears as a good solution to perform a frequency conversion with a LO frequency sub-multiple of the RF frequency without prohibitive conversion losses.

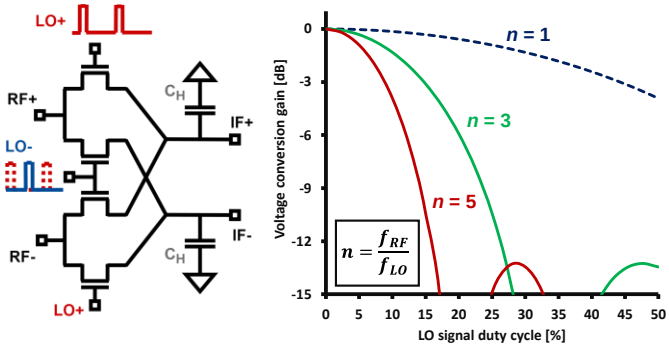

Fig. 1. sub-sampling mixer topology and conversion gain.

Fig.1 illustrates the sub-sampling mixer principle in a double-balanced configuration. When loaded by a hold capacitor (C_H) and driven by a low duty cycle LO signal, the passive mixer acts as a voltage sampler. The voltage conversion gain (G_{cv}) of the mixer of fig.1 is calculated with a similar approach as in [4] and represented versus the LO signal duty cycle (D) for different odd ratios $n = f_{RF}/f_{LO}$. Even n ratios are not considered because the double balanced topology rejects RF signals around the even LO harmonics resulting into a zero-conversion gain. Fig.1 shows that passive sub-sampling mixer allows a sub-harmonic frequency conversion with low conversion losses when D is low enough. Furthermore, passive mixers are highly linear as long as transistors switching time remains small [5]. Thus, driving mixing transistors with a LO signal having sharp transitions results in a high linearity.

Fig.1 highlights that G_{cv} drastically decreases when increasing either n or D. Because the generation of duty cycles below 15% becomes difficult when frequencies are increasing, a n ratio of 3 has been chosen to keep the conversion gain above -3 dB. Therefore, the 77 GHz sub-sampling mixer will use a 26 GHz LO frequency. The proposed sub-sampling mixer implementation in 28-nm FD-SOI CMOS will be detailed in the next section.

III. Circuit Description and Implementation

A. 26 GHz LO pulse shaper based on AND logic gates

Using a 26 GHz LO frequency in conjunction with the 28-nm FD-SOI technology, providing high speed CMOS transistors, open the way to a digital approach for the pulse shaper as presented in fig.2.a. In the differential pulse shaper of fig.2.a, number of stages between inverter chains A/C and B/D are different to create the required time delay between output square signals. Then, the AND gate turns both out of phase square signals into a pulsed signal. Inverters and AND gates are specifically designed for the application. The high body effect in FD-SOI technologies (about 85mV/V), enables to tune the threshold voltage (V_{th}) of transistors by setting the body voltage. This feature is used to implement a duty cycle tuning to the pulse shaper.

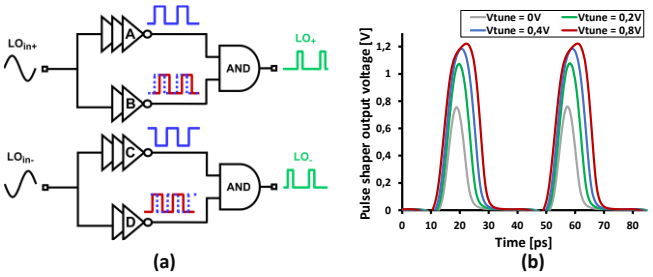

Fig. 2. (a) 26 GHz pulse shaper (b) simulated LO waveforms.

In each inverter, a tuning voltage (V_{tune}) is applied to the body of NMOS and PMOS transistors with opposite sign leading to a variation of the inverter time delay. From this variation, the duty cycle of LO pulsed signals, at the output of AND gates, is tuned as it can be depicted in Fig.2.b.

The LO pulse shaper supply voltage V_{DD} is 1.2 V. This value gives the necessary LO swing for a good mixer linearity. In logic gates, the V_{GS} stays low (no current) when V_{DS} is high, so the transistor does not enter in high Hot Carrier Injection and stays in a safe operating area even under a 1.2 V supply. Transient simulation of the pulse shaper output voltage LO_+ is given in fig.2.b for different V_{tune} ranging from 0 to 0.8 V. A duty cycle range from 19% to 33% is thus available without decreasing the LO voltage swing below 1.1 V. The AND gate fall time is the limiting factor to address duty cycles lower than 19%".

B. Implementation of a 77 GHz sub-sampling mixer

The double balanced passive sub-sampling mixer described in fig.1 has been implemented with the 26 GHz LO pulse shaper of fig.2 in a 28-nm FD-SOI CMOS test chip. The test chip is depicted in fig.3.a and fig.3.b is a microphotograph of the manufactured chip. The circuit area is 0.81 mm × 0.54 mm. The chip is sticked and wire-bonded on a PCB test board supporting DC supplies and IF outputs while the RF and LO signals are provided by RF probes. As a differential 77 GHz signal synthesizer was not available, a passive balun is implemented on the RF access. This balun also provides a 50 Ω matching and exhibits a voltage gain of 8.1 dB corresponding to the voltage transformation ratio.

Two Op-amp in follower configuration (0-dB gain) are implemented as an output IF buffer, providing a high resistive impedance R_{IF} (10kΩ) in parallel with C_H to preserve the sampling operation ($1/(2.\pi.R_{IF}.C_H) << f_{RF}$). A mixing transistor size of W/L = 15 µm / 30 nm is set to get the best noise/linearity trade-off for the mixer. This sizing ensures a good linearity since LO signal rising and falling edges are not significantly soften by a too high mixing transistor gate capacitance.

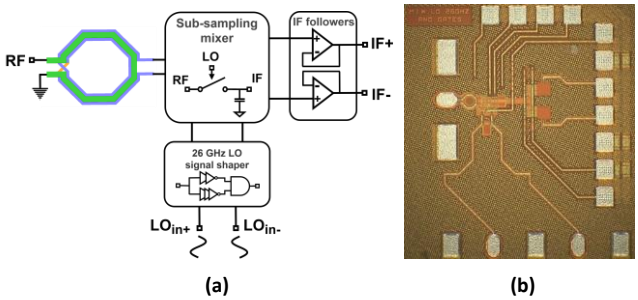

Fig. 3. (a) Block diagram of the test chip (b) manufactured chip.

At the same time, the ON-state resistor r_{on} of transistors remains low enough to limit the thermal noise contribution. Finally, the hold capacitor value C_H is set to 300 fF to properly store the signal sampled value without limiting the circuit bandwidth. Fig.4 shows the layout of the sub-sampling mixer core with the 26 GHz LO pulse shaper. The circuit area is 90 µm x 70 µm. It can be noticed that this sub-sampling mixer remains very compact as it does not require inductors on the LO chain.

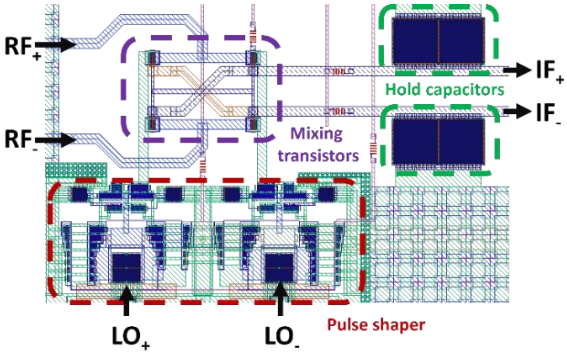

Fig. 4. Layout of the sub-sampling mixer.

Stand-alone mixer performances (excluding RF balun and output buffer) are summarized in table 1. They result from an harmonic balance and a non-linear noise simulation. f_{RF} and f_{LO} are respectively set to 78.02 GHz and 26 GHz.

TABLE I. SUB-SAMPLING MIXER SIMULATED PERFORMANCES

f_{RF} / f_{LO} [GHz]	G_{cv} [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	P_{dc} [mw]
78 / 26	-3.5	+3	13.3	36

As previously stated, the sub-sampling mixer conversion gain is limited by the LO signal duty cycle lower values resulting from the use of AND gates in 26 GHz pulse shapers (fig.2). An implementation getting rid of the AND gates is proposed as an alternate solution in the next section.

C. Co-integration of LO AND gates and mixing transistors

To overcome the AND gate fall time limitation, the AND function can be merged with the mixing function. This solution is presented in fig.5. The implementation of this innovative mixer has been presented in [6] with the associated simulated performances. Present paper provides additional details, as well as measurement results validating all simulations. Its aim is to compare this approach with the more conventional solution relying of the 26 GHz pulse shaper integrating AND logic gates.

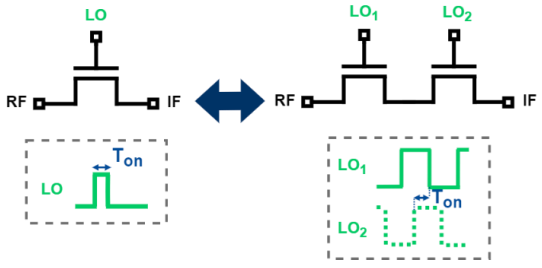

Fig. 5. Co-integration of the AND function and mixing transistors.

When a mixing transistor driven by a low duty cycle LO signal (fig.1) is replaced by two series transistors directly driven by time delayed square waves (fig.5) the sub-sampling mixer operating principle remains the same. The conversion gain is the same with both solutions as soon as the ON-time (T_{ON} in fig.5) of mixing transistors is similar. On the other hand, the co-integration depicted in fig.5 allows to remove the AND gates. Consequently, lower duty cycles can be reached leading to a better conversion gain. The sub-sampling mixer based on this co-integration of the AND function and the mixing function has been implemented in a test chip similar to the one of fig.3. The time delay tuning between LO_1 and LO_2 generated square waves is also available in this second version. In the following sections the mixer presented in III.B is referred as mixer 1. The mixer co-integrating the AND function to the mixer core as described in III.C is called mixer 2. For both mixers, the sizing of the mixing transistors stays similar. Nevertheless, the two series mixing transistors on each mixer path are implemented following a specific layout strategy as illustrated in fig.6.

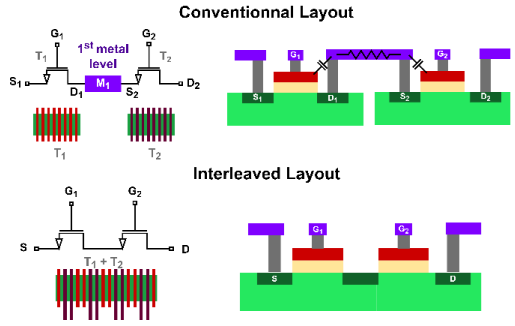

Fig. 6. Layout of the NMOS interleaved series mixing transistors

Using an interleaved layout for series mixing SOI CMOS transistors rather than a conventional approach enables to merge their source and drain. This way, parasitic capacitors and resistors coming from the connection between both transistors via first metal level (M_1) are removed. Simulated performances of this version of the stand-alone sub-sampling mixer are reported in table 2.

TABLE II. SUB-SAMPLING MIXER 2 SIMULATED PERFORMANCES

f_{RF} / f_{LO} [GHz]	G_{cv} [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	P_{dc} [mw]
78 / 26	-2.5	+3	14.4	36

Compared to mixer with AND gates (mixer 1), the simulation results in table 2 confirm that the co-integration of AND gates and mixing transistors allows to reach a lower LO duty cycle resulting in a higher conversion gain. The next section presents measured performances of both sub-sampling mixers.

IV. MEASUREMENT RESULTS

The measurements presented in this section are performed with a 0-dBm LO input power and include the RF input balun and the output buffer performances. The measured consumption of the LO shaping circuit on a 1.2V supply is 32 mW for both mixers. The duty cycle tuning integrated to inverter chains is used to set the best conversion gain. All measurements corresponding to the sub-sampling mixer test chip of fig.3 (mixer 1) are reported in fig.7.

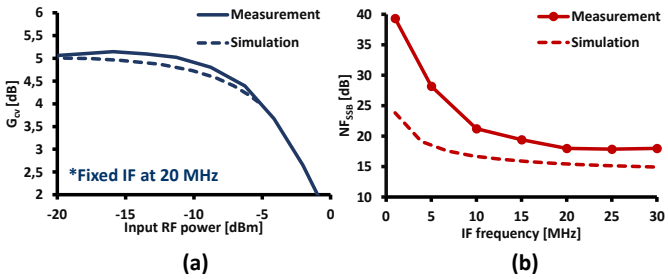

Fig. 7. Mixer with AND gates (a) Measured G_{cv} compression curve at a f_{RF} of 78 GHz (b) Measured NF_{SSB} at a f_{RF} of 78 GHz.

The G_{cv} compression obtained versus RF input power is plotted in fig.7.a. f_{RF} and f_{LO} are respectively set to 78.02 GHz and 26 GHz. The extracted G_{cv} and ICP1dB are respectively 5.1 dB and -5.3 dBm. If the simulated voltage transformation ratio of the RF input balun contribution (8.1 dB) is removed from measurements, G_{cv} becomes equal to -3 dB with an ICP1dB of + 2.8 dBm. Fig.7.b shows the NF_{SSB} with f_{LO} of 26 GHz and the IF frequency ranging up to 30 MHz. The measured value of the NF_{SSB} is 17.9 dB at an IF offset of 30 MHz. When the noise contribution of the output stage is removed, the NF_{SSB} of the mixer, including the input balun, is 16.9 dB.

The same measurements are performed on the mixer with co-integration AND/mixer (mixer 2). Corresponding results are presented in fig.8. The input RF balun implemented with this second mixer is different than in mixer with AND gates and presents a voltage gain of 4.8 dB. With the previous approach, overall measurements of G_{cv} and ICP1dB are 2.7 dB and -1.5 dBm, respectively. It translate into a G_{cv} of -2.1 dB and an ICP1dB of +3.3 dBm for the standalone mixer, after balun de-embedding. Fig.8.b shows the NF_{SSB} in the same conditions as in fig.7.b. For this version of the mixer, measured values are close to simulated ones above 20 MHz. The measured value of NF_{SSB} is 18.4 dB at an IF offset of 30 MHz. Removing the noise contribution of the output stage results in a NF_{SSB} of 16.8 dB.

For both mixers, the measured NF_{SSB} is higher than the simulated one at low frequencies, highlighting an extra $1/f$ noise. In [7], the influence of various noise sources on a CMOS inverter is discussed showing that the noise coming from the inverter input and voltage supply is amplified, resulting in an important output jitter. In the presented LO signal shaper, at least five stages are included in each inverter chain. Since simulations do not consider noise for the LO source and voltage supplies, large discrepancies between simulated and measured NF_{SSB} values can be observed.

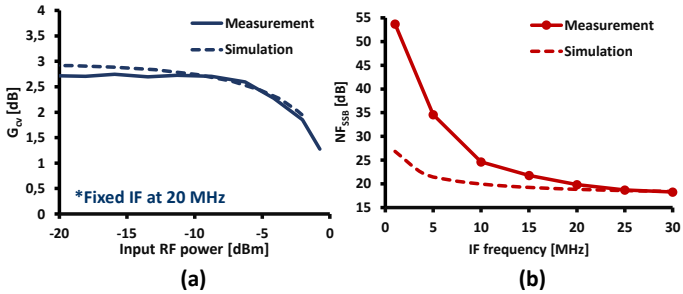

Fig. 8. Mixer with co-integration AND/mixer (a) Measured G_{cv} compression curve (b) Measured NF_{SSB} , at a f_{RF} of 78 GHz.

TABLE III. MEASURED PERFORMANCES FOR BOTH VERSIONS OF THE SUB-SAMPLING MIXER

Mixer	f_{RF} / f_{LO} [GHz]	G_{cv} [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	P_{dc} [mW]
Mixer 1	78 / 26	-3	+2.8	16.9	32
Mixer 2	78 / 26	-2.1	+3.3	16.8	32

The table III sums up the measured performances for the two versions of the sub-sampling mixer. They both show very low conversion losses, especially when considering that they are passive and subharmonic mixers, as well as a good linearity. The second mixer, which is merging the AND function and the mixing one, presents the best performances, as expected since lower duty cycles are achievable. Simulated NF_{SSB} values in fig.7 and fig.8 exceed those reported in table I and II because they include input balun losses which are difficult to extract.

Because stand-alone sub-harmonic passive mixers are not reported in the literature related to CMOS 77 GHz radar receivers, a meaningful comparison between the proposed mixers and other existing solutions is a bit difficult. To do so, both proposed sub-sampling mixers have been implemented with a variation of the LNA presented in [8] in a 77 GHz front-end (LNA / mixer). As a result, a proper comparison with the state of the art can be provided. The measured front-end performances are summarized and compared with other radar receivers in table IV. The receiver front-ends including mixer 1 and mixer 2 will be respectively called Rx_1 and Rx_2.

TABLE IV. COMPARISON WITH THE STATE OF THE ART.

	f_{RF} / f_{LO} [GHz]	G_{cv} [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	Area [mm²]	P_{dc} [mW]
Rx_1	78 / 26	8.9	-11	11.9	0.2	42
Rx_2	78 / 26	9.5	-12	11.5	0.2	42
[1]	78 / 78	16	-7.8	8.7	NA	NA
[2]	78 / 78	18/60	-7/-30	20/11	Rx 0.3 LO 0.4	Rx 31 LO 58
[9]	78 / 39	14.5	-29	10.5	0.58	57
[10]	78 / 39	16	-20	13	2.33	28.5

The 77 GHz radar receivers in [1] and [2] are based on a conventional architecture using a 38.5 GHz VCO followed by a frequency doubler and 77 GHz LO drivers. [1] shows the best characteristics of this table but the LO power consumption and the circuit area dedicated to the LO chain are not given. However, [2] gives an idea of the power consumption of a conventional LO chain (about 60 mW) and allows to estimate the related chip area (0.4 mm2). Receivers based on sub-sampling mixers can use a 26 GHz LO VCO without requiring a frequency tripler and 77 GHz drivers. The mixer is also very compact as it does not require inductors. Consequently, proposed receivers based on sub-sampling mixers save DC power and silicon area while keeping decent performances when compared to conventional radar receivers. Finally, the comparison between this work and radar receivers based on sub-harmonic Gilbert cells in [9] and [10] highlights that using sub-sampling mixers lead to better overall performances with a higher ratio between f_{RF}/f_{LO}.

V. CONCLUSION

A 3x sub-sampling passive mixer is proposed as a solution for a 77 GHz receiver implementation in a 28 nm FD-SOI CMOS. To overcome frequency limitations due to the complexity of AND gates required for the OL pulse shaper, an innovative solution based on the co-integration of the AND function and the mixing function is used.

Measurements demonstrate that a good conversion gain associated to a high linearity can be obtained using sub-harmonic passive mixers based on a sub-sampling operation. A higher f_{RF}/f_{LO} ratio than other sub-harmonic receivers is observed, also. Furthermore, when compared to conventional radar receivers, the LO chain is greatly simplified, saving area and reducing power consumption, while good performances are kept.

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