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A low-noise CMOS front-end for TOF-PET

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ABSTRACT: An analogue CMOS front-end for triggering and amplification of signals produced by a silicon photomultiplier (SiPM) coupled to a LYSO scintillator is proposed. The solution is intended for time-of-flight measurement in compact Positron Emission Tomography (TOF-PET) medical imaging equipments where excellent timing resolution is required ($\approx 100\ ps$). A CMOS 0.13 μm technology was used to implement such a front end, and the design includes preamplification, shaping, baseline holder and biasing circuitries, for a total silicon area of 500x90 μm. Waveform sampling and time-over-threshold (ToT) techniques are under study and, hence, the front-end provides fast and shaped outputs for time and energy measurements. Post layout simulation results show that, for the trigger of a single photoelectron, the time jitter due to the pre-amplifier noise can be as low as 15 ps (FWHM), for a device with a total capacitance of 70 pF. The very low input impedance of the pre-amplifier ($\approx 5\ \Omega$) allows a 1.8 ns peaking time, at the cost of 10 mW of power consumption.

KEYWORDS: Front-end electronics for detector readout, Analogue electronic circuits, PET PET/CT, Solid state detectors .

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Contents

1. Introduction

Recent developments of highly compact solid-state photodetectors have created the potential for scaling down the coincidence timing resolution of PET scanners to the deep sub-nanosecond range, needed for time-of-flight (TOF) measurements. However, the TOF capability requires the use of very high speed electronics, very sensitive to the rising edge of a signal produced by the particle detector and, thus, capable to extract temporal information with a resolution down to 25 ps.

The work reported here focuses on the development of a new front-end amplifier, suitable to be used for time and charge measurements of signals produced by the SiPM detector. Based on data provided by manufacturers, a simple electrical model for the SiPM will be used in analytical studies and simulations, where the optical input for the photodetector is produced by the scintillation of a L(Y)SO:Ce crystal hit by a γ ray. The pre-amplification, shaping, baseline holder and biasing building blocks were implemented in a standard mixed-mode 130nm CMOS process technology.

2. Characteristics of the SiPM electrical signal

The SiPM is a recently introduced solid state photodetector, with a very high gain and sensitivity to single photon hits.[11] Its fast rise time and good timing characteristics makes it suitable to extract the TOF information of two photons originating from the same positron annihilation on a PET detector.

A SiPM is an array of solid-state photodiodes operating in Geiger mode, sharing the same substrate, and a network of quenching resistors. The SiPMs are seen as an attractive solution for low energy photon detection in medical imaging, as they have important advantages with respect to the photomultiplier tube (PMT) or avalanche photodiode (APD). Besides having a very low form

factor (less than $2.5 \times 2 \times 1$ *mm* for a S10362-1-0xxP Hamamatsu device), the SiPM is immune to magnetic fields, as the path traveled by the charge carriers is short. The advantage of this characteristic is in allowing the possibility to be integrated in multi-modal PET-MRI equipment. The work in [6] provides experimentally supported conclusions on the effect of static, gradient and RF magnetic fields on the performance of SiPMs. It uses significantly lower bias voltages ($25-50\ V$) than the other solutions and, nonetheless, achieves a high gain, similar to that of the PMTs. This high gain, typically of the order of 10^5, is much higher than that achievable (within the $100-500$ range) with APDs. It is a robust and compact alternative, with excellent time resolution and quantum efficiency, and also low sensitivity to temperature and bias variations. n the event of a group of photons being incident simultaneously, the current pulses generated by each photodiode of the dense array sum up, since all cells are connected in parallel. Likewise, the integral of the current pulse is nearly proportional to the intensity of the incident light pulse of finite duration. This proportionality only applies if moderate light intensity is considered, since it does not account for the probability of multiple incidences within the microcell recovering time. When n microcells fire simultaneously, then a total current of $I_{out}(n) = n \cdot i_{pix}$, where i_{pix} is the avalanche pulse current generated by a single microcell hit by an incoming photon.

Electrical models for SiPMs were extensively depicted by Corsi et al.[2], Pavlov et al.[8] and Badoni et al.[1], among others. Similarly, the authors have proposed experimental set-ups to extract the relevant electrical parameters. The use of an electrical model that is able to relate the device output response to the number of fired cells, or that takes into account second order effects due to the stray inductances does in fact increase the accuracy of the simulations. However, as far as a validation of the front-end topology in terms of its dynamic range is concerned, a current mode stimulus with known damping factors is seen as an adequate model from the perspective of an electronic circuit designer. It can be approximated by the convolution of the bi-exponential function of the SiPM response to a Dirac pulse and the exponential decay characteristic of the scintillator. If, instead, one aims to characterize the front-end response to a single pixel firing, then it must be taken into account that avalanches in single diodes transfer charge into the array of n parallel microcells. Hence, the voltage signal produced at the output of the device can be approximated by the value of the overdrive voltage (above breakdown) divided by the total number of pixels of the array [9].

The dense array of the SiPM is responsible for a total parallel capacitance C_d, which accounts not only for the grid capacitance C_g (due to the grid parallel interconnection) but also the pixel capacitance $C_{pixel} = C_d + C_q$, a sum of the junction capacitance and the parasitic C_q (nomenclature on the models proposed by [2] and [8]). Therefore, C_d depends on the number of cells in the array, thus the active area, and may be in the range of $35-320\ pF$, respectively concerning 1 mm^2 and 9 mm^2 devices.

3. Analogue front-end electronics

The goal of the analogue front-end design reported in this work is to validate an architecture suitable to be used with waveform sampling, time-over-threshold or multi-threshold based signal processing schemes. Two outputs must hence be produced in order to achieve the required flexibility: a

fast current pulse, appropriate for timing measurements and the amplified voltage signal with an integration constant that maximizes signal-to-noise ratio, from which the charge of the input signal can be extracted. The current produced by the SiPM, proportional to the input charge for the readout electronics, is substantial and thus not much amplification is needed.

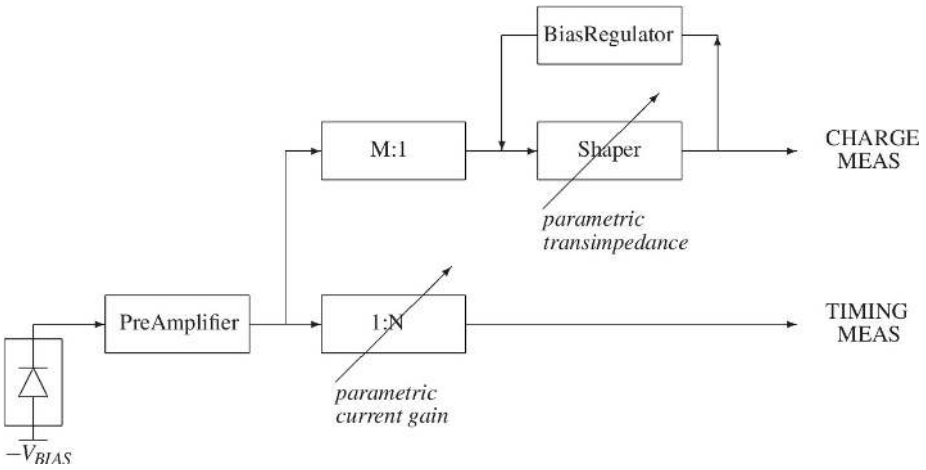

Figure 1. Block diagram representation of the front-end electronics.

The overall channel architecture is represented by the block diagram in Figure 1. The proposed circuit comprises two distinct signal paths for both timing and charge measurements, whose common input is a buffered current-mode replica of the signal from the photomultiplier. For the charge measurement circuitry, the current is scaled down by a fixed factor of M, whereas for time extraction a multiplication ratio of $N = \{1,2\}$ provides a fast replica of the input current signal. Feeding the shaper with higher currents would not only increase the overall power, unnecessarily, but also require a higher value of the feedback capacitance in order to keep the time constant of the integrator, as the transresistance, hence R_F, would be made smaller. A set of PMOS and NMOS current mirrors scales down the current buffer output current by a (fixed) factor of $k = 32$. This strategy, however, lowers the amplifier sensitivity G_0 at least by the same order. Since a delta pulse of charge Q_δ produces a voltage output of amplitude ΔV_{out}, then an equivalent noise charge (ENC) can be defined as the delta charge $Q_{\delta ENC}$ at the input that produces an output ΔV_{outENC} which is equal to the total output *rms* noise voltage of the amplifier, $V_{no\ rms}$, or (with convenient units conversion)[1]:

$$ENC\ (e^-) = 6250 \cdot \frac{V_{no\ rms}\ (mV)}{G_0\ (mV/fC)} \tag{3.1}$$

One can thus anticipate an ENC that is, at least, k times superior to what is found in literature for low gain photodetector amplifiers. Hence, the ENC is not an even-handed benchmark of comparison, in the knowledge that the input referred noise will also be decreased by the same amount.

The SiPM produces, typically [7], a negative current signal, as suggested by the representation of the n-type cathode at the output port of the device. Thus, the input port of the current buffer collects electrons, which is to say, the input signal presented to the pre-amplifier is a negative current pulse. The need for a current buffer as first stage is due to the high value of the stray capacitance

[1] $1\ e^- = 1.6 \cdot 10^{-19}\ C$

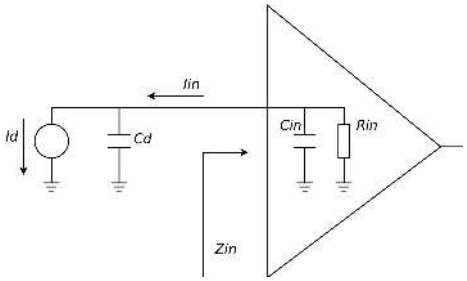

Figure 2. Front-end amplifier input impedance and internal poles: effect on amplifier bandwidth.

C_d at the terminals of the device. In fact, considering a generic amplifier with an input impedance Z_{in}, the frequency response of the amplifier is affected by the pole with a time constant given by $\sigma_1 = Z_{in} \cdot C_d$. Considering the expected upper limit for the SiPM terminal capacitance (more than 300 pF for a 9 mm^2 device) and an input impedance of 50 Ω (DC), then the amplifier would be plagued by a dominant pole around 15 ns ($\approx$ 10 MHz). This value is of the same order of τ_1 and τ_2, defined by equation 3.2, which describes the transfer function of a general transimpedance function with two poles.

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{R_{TIA}}{(1+s\tau_1)(1+s\tau_2)} \tag{3.2}$$

Consequently, the shaping function would no longer be well defined, as the position of its poles should drift with the value of C_d. A buffer placed before the shaper serves the purpose of removing the dependence of $V_{out}(s)/V_{in}(s)$ on the value of the photodetector capacitance. The output of the current buffer feeds the shaping stage, which limited frequency response is used to optimize the signal-to-noise ratio for the energy measurement.

3.1 Pre-Amplifier

It has been predicted that the excessive parasitic capacitance at the terminals of the SiPM could pose severe bandwidth constraints in the design of the front-end amplifier. That is easily confirmed by inspection of Figure 2, which shows the relevant capacitive elements of a general signal equivalent model of the photodetector and the input amplifier.

Although a first order system is a simplistic approach to the input impedance of the amplifier, it serves the purpose to demonstrate the contribution of the SiPM capacitance to the input node related time constant; an adequate design of the amplification chain will likely make this pole dominant. Defined by the input resistance of the amplifier and the node capacitance, $\tau_{in} = R_{in}(C_d + C_{in})$, then the amplifier input current is given by Equation 3.3:

$$I_{in}(s) = \frac{1}{1+s\tau_{in}} I_d(s) \tag{3.3}$$

Likewise, the voltage variation of the input node is described by equation 3.4:

$$Z_{in} = \frac{\Delta V_{in}}{\Delta I_{in}} \Leftrightarrow \Delta V_{in} = Z_{in}\Delta I_{in} \tag{3.4}$$

A low input impedance not only moves τ_{in} to higher frequencies but also reduces the bounce of the input node voltage due to the large current output of the photodetector. This is of utmost

importance since the SiPM, which is DC coupled to the input node, has its gain strongly dependent on the voltage bias applied.

A pre-amplification stage capable to convey a current from a low-Z input port into a high-Z output port, is implemented with the gm-boosted common-gate (RGC) input shown in Fig. 3.

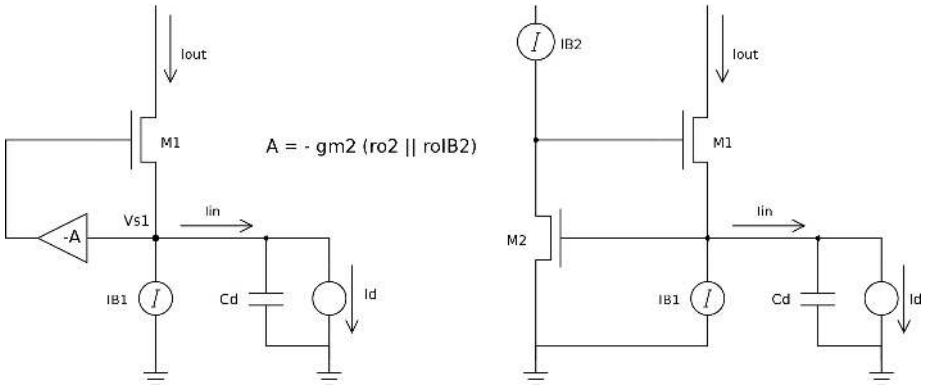

Figure 3. The RGC circuit diagram: regulation gain schematic (left) and its implementation with a common-source amplifier of gain $-A$ (right).

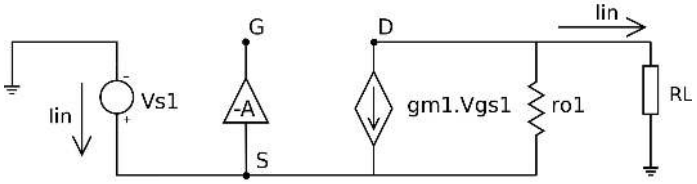

Figure 4. The RGC circuit small-signal equivalent: the load R_L has ideally a zero small signal impedance, corresponding to an ideal power source biasing the drain of the input transistor.

Straightforward analysis of the small-signal model, represented in Fig.4, reveals the node equation 3.5:

$$-I_{in} + g_{m1}V_{s1}(A+1) + \frac{V_{s1} - I_{in}R_L}{r_{o1}} = 0 \tag{3.5}$$

From Eq. 3.4, equation 3.5 can be rewritten as:

$$-1 + Z_{in}\left(g_{m1}(A+1) + \frac{1}{r_{o1}}\right) - \frac{R_L}{r_{o1}} = 0 \tag{3.6}$$

Considering a typical value for $r_{o1} = 20\ k\Omega$ ($g_{ds1} = 50\ \mu S$); if the drain of M1 is a diode-connected PMOS load with high transconductance, then the value of R_L is indeed very low and given by $R_L = \left(\frac{1}{g_m}\right)||r_o \approx \frac{1}{g_m}$. In any standard deep submicron technology, a saturated wide PMOS ($W/L > 500$) will exhibit a resistance down to some hundred ohm (assuming $R_L = 250\ \Omega$). The above premises imply that $\frac{R_L}{r_{o1}} << 1$.

Moreover, with a transconductance of 5 mS and a feedback loop gain of 80 ($A >> 1$), then $g_{m1}(A+1) >> \frac{1}{r_{o1}}$. Equation 3.6 can suitably be simplified to:

$$Z_{in} = \frac{1}{Ag_{m1}} \tag{3.7}$$

The regulated cascode (RGC) effectively enhances the transconductance of the input stage as its input resistance is diminished by a factor A, when compared to the common-gate (CG) topology. Furthermore, as a result of a smaller variation at the input node, the drain current I_{ds} of M1 remains steadier, yielding an output resistance that is increased by the same amount of the regulation gain, thus becoming $Z_{out} = Ag_{m1}r_{o1}$. It is worth mentioning that the latter would already impose a small Z_{in}, since a current input into the source of an NMOS transistor sees a resistance which is given by the inverse of its transconductance, $R_{in} = g_m^{-1}$. However, given that the input transistor of a CG circuit is the predominant source of noise, its g_m can only be increased with the penalty of increasing the transistor current noise.

If the regulation gain of the RGC is implemented with a common-source amplifier, the amount of feedback is given by the voltage gain A:

$$A = g_{m2}(r_{o_{M2}} || r_{o_{IB2}}) \tag{3.8}$$

which is equivalent to :

$$A = g_{m2}\frac{1}{g_{ds_{M2}} + g_{ds_{IB2}}} \tag{3.9}$$

The values of ro_{M2} and ro_{IB2} are, respectively, the g_{ds}^{-1} of the common-source M2 and the PMOS current mirror IB2. From the transistor-level design, the feedback gain can be derived: $A = g_{m2}/(g_{dsM2} + g_{dsIB2}) = (14.2m)/(153\mu + 23\mu) = 81$.

With $g_{m1} = 5.8\ mS$, using Equation 3.6 results in:

$$Z_{in} = \frac{1}{Ag_{m1}} = \frac{1}{81 \cdot 5.8m} = 2.1\ \Omega \tag{3.10}$$

which is in good agreement with what was measured by schematic-level simulations ($R_{in} = 2.1\ \Omega$). Unavoidably, this low input impedance is for low frequencies only, since the regulation gain rolls-off for higher frequency. As a result of the total parasitic capacitance at the input node, the frequency response of the regulation loop will show the effect of such capacitive load: a larger fraction of the high frequency spectra of the input current signal is rejected, enlarging the rise time of the buffered replica at the output. More than a decrease of A at high frequencies, the stability of the feedback loop is also affected with C_{tot} (a sum of the total device capacitance and those of the local signal path parasitics). Predictably, higher values of C_{tot} increase the phase margin of the loop, since the dominant pole is pushed towards zero and hence the zero-gain crossover happens earlier in frequency.

In the RGC circuit, the newly introduced regulation transistor adds a new source of thermal noise. Its contribution becomes dominant to the total *rms* output noise voltage, which can be driven down with higher transconductance values of M2.

3.2 Shaper

The charge measurement and signal shaping are performed by a transimpedance amplifier (TIA) with variable gain, whose high-level representation is shown in Figure 5 (right). As the input charge, replicated by the *PreAmplifier* circuit, is transferred to the capacitor C_F, a voltage across it is developed. Consequently, the output node suffers a potential increase that is proportional to the

charge deposited in the capacitor and, hence, $V_{out} \propto Q_{in}$. In this context, the circuit is commonly designated as a charge sensitive amplifier (CSA),as it performs a charge-to-voltage conversion. The circuit integrates the input current, with a shaping constant τ_F given by $R_F C_F$. The output voltage signal is thus an amplified (and inverted, due to the OA topology) and shaped function of the input charge.

If the OA gain is very high, then the transimpedance gain approaches the value of the feedback resistor R_F. A buffer (with high input impedance and low output impedance) needs to be included such that the OA experiences no significant gain loss (cf. with Figure 5 (left)).

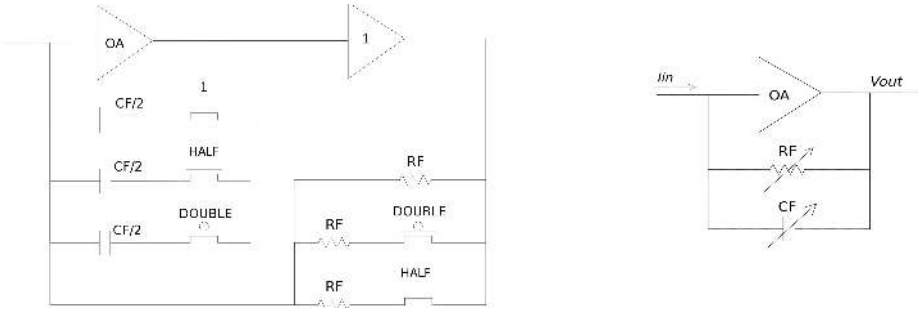

Figure 5. Implementation of the TIA variable gain, switching controlled by external signaling (left), and the generic transimpedance amplifier with variable gain (right).

Should the feedback resistor R_F load directly the high output impedance output of the OA, then an open-loop gain drop, more severe if the transimpedance gain was set lower, should be observable. The buffer not only solves this issue, it also isolates the feedback capacitor from the parasitic capacitances of the output node.

Nominal values of the feedback resistance and capacitance components are 95 $k\Omega$ and 175 fF, yielding $\tau_F = 17\ ns$. The use of a smaller feedback capacitor could leave the transfer function more susceptible to process biases. In other words, if C_F was set lower than 100 fF, then its value would become of the same order of that of the parasitic capacitances (which can be estimated after layout netlist extraction). Although the value of the shaping constant τ_F is fixed, the transimpedance gain has to be programmable. A proof-of-concept with a dynamic range of $G_{max}/G_{min} = 4$ was implemented, consisting of a two-bit gross gain control based on CMOS transmission gates.

3.3 Baseline Holder

The design of a 2-stage architecture requires both AC coupling (high-pass filtering) between stages and a baseline stabilization able to avoid the unwanted amplification of any offset voltage appearing at the output of the pre-amplifier. The DC operation point at the input of the shaping stage is forced by a baseline stabilization block, commonly used in particle detector systems due to its ability to correct baseline drifts with pulse rate [5, 4].

An external analogue signal $Vbaseline$ is sampled and compared to the output baseline voltage, producing a voltage difference which is fed to a transconductor, which current output is injected to the input of the transimpedance amplifier. This results in a virtual short-circuit between the inputs

Vbaseline and *Vo_TIA*, thus keeping the external output node DC value at a fixed programmable voltage level. The transconductance function must reject variations caused by the fast signals at the output of the shaper, which is accomplished with a slew rate limited buffer. The block diagram of such low-pass transconductor is shown in Figure 6, where the non-inverting unitary gain buffer is implemented with a source-follower [10].

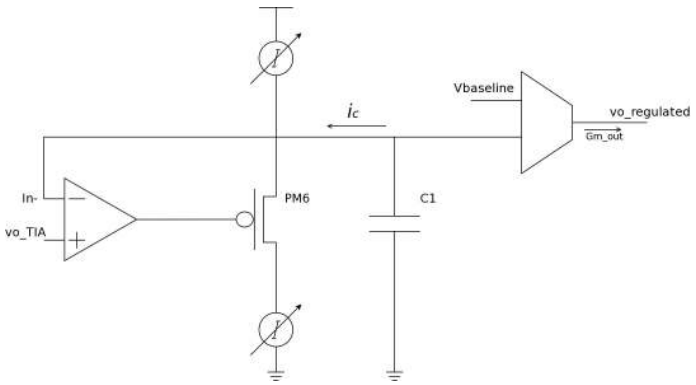

Figure 6. Block diagram of the *BiasRegulator*

4. Post-layout simulation results

Figure 7 shows the top hierarchy of a single-channel design, whose pitch will allow to abut vertically the amplifiers in a multi-channel chip. The performance of the amplifier in terms of amplitude (hence charge) measurements takes into account the realistic input stimulus (including SiPM rise time and LYSO decay) that has been proposed. Such a test assesses the shaping characteristics of the output signal and measures the ratio between the peak output voltage and the total *rms* output noise voltage on the same node. For the minimum input signal of interest, this ratio must be higher than 15-20. Alternatively, the energy information can be extracted by measuring the leading trailing edges of the shaped output, so that ToT window can be correlated with the pulse amplitude.

The timing measurement requirement include gain and noise specifications, from which the additional time jitter introduced by the circuit is calculated. Testing the amplifier to extract these parameters implies the use of a delta function as input. Otherwise, the test would be addressing not only the pulse shape and noise characteristics of the amplifier, but also the sum of jitter due to the SiPM, photoelectron statistics and the characteristics of the scintillation (rise and decay time).

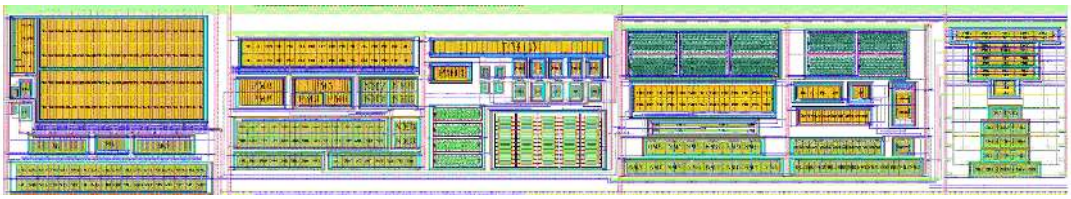

Figure 7. Layout ($493 \times 87 \mu m^2$) of the *Full_channel* block (top hierarchy)

The validation testbench is based on post-layout netlisting, which includes a model of the chip I/O parasitics (a standard quad flat plastic packaging option with inductive and resistive effects due to the routing redistribution layer and pin, as well as the capacitive coupling to substrate. Figure 8 plots the two voltage outputs, revealing the delay introduced by the physical layout parasitic capacitances on the transient response. We inspect the performance of the front-end for timing and

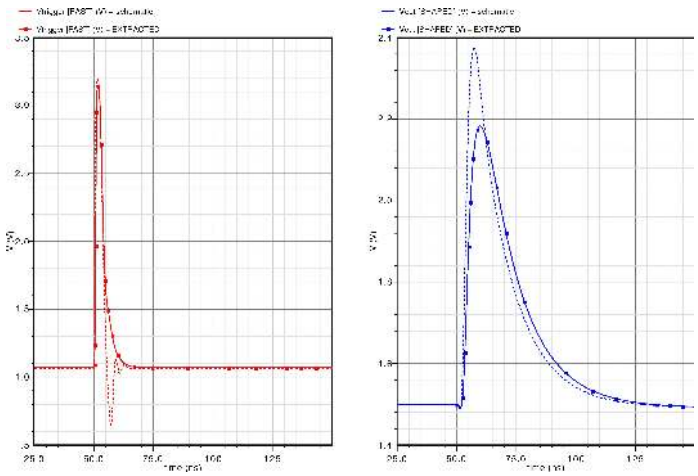

Figure 8. Transient waveforms of shaped (right) and trigger (left) signals for schematic level (dashed lines "schematic") and post-layout (solid lines "EXTRACTED") simulations Dirac pulse stimulus).

energy measurement; the corresponding voltage signals are hereinafter mentioned as trigger and shaped ouptuts.

Since the design goals of TOF-PET detectors emphasize the possibility of having precise time stamps, we focus on the degradation of such measurements due to excessive electronic noise. A time stamp of the event will be obtained by feeding a discriminator with a very fast triggering pulse, produced by the high-bandwidth pre-amplifier stage. The output *rms* noise voltage of the signal output appears as an input to the discriminator, and will be translated as an uncertainty on its transition region, leading to jitter and thus deteriorating the timing measurement accuracy. Assuming a noiseless comparator with infinite gain, then its transfer curve is affected by the variation σ_t, which is a function of the voltage noise at the input V_{in}. If the transition region (of the comparator) is centered at a given threshold V_{th}, then the slope of the signal $[\delta_v/\delta_t]_{v_{in}=V_{th}}$ must be maximized in order to mitigate the voltage fluctuations caused by the unwanted random electronic noise. That is to say, given the total *rms* noise voltage σ_v and the slope $[\delta_v/\delta_t]_{V_{in}=V_{thX}}$, then the contribution of the electronics noise (superimposed to V_{in}) to the degradation of the timing resolution is given by:

$$\sigma_t\ (ps) = \frac{\sigma_v}{\left[\frac{\delta_v}{\delta_t}\right]_{v_{in}=V_{th}}} \left[\frac{mV}{mV \cdot ns^{-1}}\right] \tag{4.1}$$

Figure 9 shows a graphical insight into the problem. The effect of the electronics noise on the time resolution of a particle detection system can be isolated from the influence of the photon arrival time fluctuations, as it is considered that the contribution to the jitter due to the variance introduced by the SiPM itself and scintillation is statistically independent from that of the electronics. This variance includes changes in the shape of the scintillation pulse, as well as the time drift inherent following the electron-hole (e-h) pair generation in the SiPM.

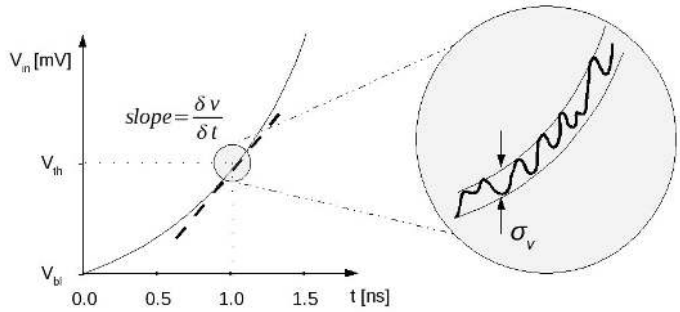

Figure 9. Detail of the input electronic noise at the threshold level, where the derivative of V_{in} is calculated.

Each incident photon creates an e-h pair, producing a finite amount of charge that sums in time with that produced by the preceding photoelectron (p.e.). Thus, the contribution of each phototoelectron increases, arithmetically, the slope of the signal produced at the output of the SiPM. It is equivalent to say that the slope of the SiPM current output due to the simultaneous arrival of n photons is n times steeper to that produced by a single photon. From this postulate, and according to Equation 4.1, it is foreseeable that a higher comparator threshold and thus higher signal slope would improve time measurements.

However, since the time of arrival of these photons is weakly correlated to t_0, the statistical time distribution of the arriving photons (number of photoelectrons per time unit) is reflected as a fluctuation in the shape of the rising edge of the output signal. In this regard, an optimum threshold corresponding to the inflection of the coincidence resolving time (CRT) curve will dictate a trigger around 2-5 photoelectrons [11]. Therefore, a good time measurement implies a discriminator that is able to detect the arrival of these first photoelectrons, within the first nanosecond after the event.

Having measured a total output noise voltage $\sigma_v = 2.3\ mV$ and re-writing equation 4.1 as to define the time resolution in terms of FWHM:

$$\sigma_{tF} = 2.35 \frac{\sigma_v}{\delta_{[th]}} \tag{4.2}$$

Considering the ability to set the trigger threshold between 1 and 3 photoelectrons, then table 1 summarizes the findings for the fast trigger output in terms of the analogue electronics noise contribution to the total timing jitter.

No. of photoelectrons	Q_{th} (fC)	ΔV (mV)	V_{th} (V)	$\delta_{[th]}$ (Vs^{-1})	σ_{tF} (ps)
0.5 (min)	60	24	1.09	3.7E8 (@50.3ns)	15
2.5 (typ)	300	120	1.19	1.1E9 (@50.4ns)	5

Table 1. FWHM time resolution for *Vtrigger [FAST]*, $C_d = 70pF$, $\sigma_v = 2.3mV$, $V_{bl_{FAST}} = 1.070\ V$

From what has been predicted for the total pulse charge at the amplifier input, the transient response of the amplifier is plotted in figure 10 for a sweep of the input charge. The input signal is

a realistic model for a LYSO+SiPM pulse, where a charge of 22 *pC* (average charge for the scintillation of a 511 *keV* photon) corresponds to a 550 μA peak current of the exponential pulse. Having a shaped voltage output, which amplitude is a direct function of the input charge, allows the use of waveform sampling techniques with reasonably low analogue-to-digital conversion frequency. The fast derived signal is thus not suitable to be used with such technique. For time-over-threshold measurements, a measure of the time window between the leading and falling edges of either the shaped or trigger signal will be used to extract the pulse amplitude and thus its energy.

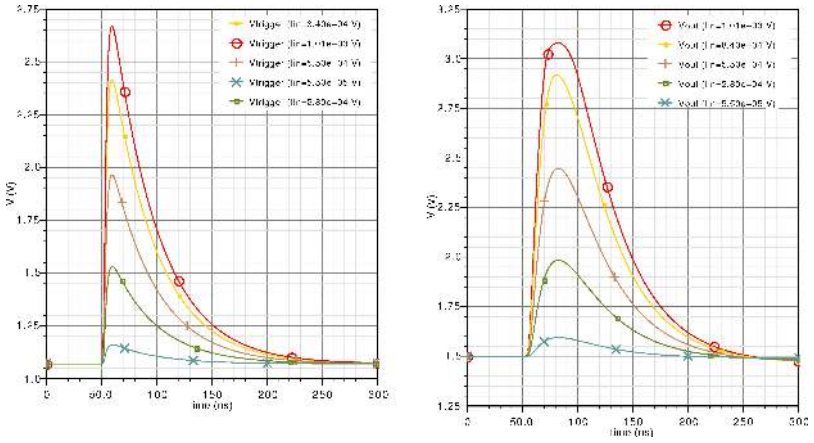

Figure 10. Transient waveforms of trigger (left) and shaped (right) outputs, when the input charge is swept between 2.2 *pC* and 40.3 *pC*.

5. Ongoing and future work

A very low-noise front-end has been proposed, and post-layout simulations have provided important results for a revised design of the pre-amplifier stage. Table 5 compares some benchmarks of the current design with a referenced solution. Results after layout parasitics extraction show an input resistance which is more than doubled than what was predicted by analytical estimates and schematic-level simulations. The causes have been identified and the layout floorplan of the input stage will be revised in order to reduce this discrepancy.

The feedback topology of the front-end is clearly a drawback in terms of bandwidth, but is crucial to substantially reduce the noise of the input transistor and its input resistance. A differential regulation amplifier will substitute the simple common-source feedback amplifier and provide fine adjustment of the input node DC voltage, hence allowing a fine control of the SiPM gain.

	TOF-PET ASIC	BASIC
Parameter		
Tech. node	0.13 μm	0.35 μm
Input impedance (DC)	5.3 Ω	17 Ω
Bandwidth	60 MHz	250 MHz
Dynamic range (waveform sampling)	2 - 40 pC	50 pC
Power consumption	10 mW	6.6 mW
Peaking time	1.8 ns	0.4 ns
Electronic jitter	5.0 ps (@2.5 p.e.)	70 ps

Table 2. Summary of results for the work here reported (TOF-PET ASIC) and the solution proposed by Corsi et al. on [3]

References

[1] D. Badoni et al, *SiPM: characterizations, modelling and VLSI front-end dedicated development*, nuovo cimento- societa italiana di fisica, sezione c, vol. 30, nr. 5, pp. 503-514, 2007

[2] F. Corsi et al., *Electrical Characterization of Silicon Photomultiplier Detectors for Optimal Front-End Design*, IEEE Nuclear Science Symp. Conf. Record, N30-222, 2006

[3] Francesco Corsi et al., *ASIC development for SiPM readout*, JINST 4 P03004, Issue 03, March 2009

[4] G. De Geronimo, P. O' Connor, J. Grosholz, *A CMOS Baseline Holder (BLH) for Readout ASICs*, IEEE Trans. Nuclear Science, vol. 47, no. 3, June 2000

[5] Larry V. East, *Baseline Stabilization in Direct Coupled Counting Systems* doi:10.1063/1.1684780, Rev. Sci. Instrum. 41, pp. 1245-6, 1970

[6] Rob Hawkes et al., *Silicon Photomultiplier Performance Tests in Magnetic Resonance Pulsed Fields*, IEEE Nuclear Science Symp. Conf. Record, M18-118 , 2007

[7] HAMAMATSU, *MPPC Technical Information* 20 pages, May 2009

[8] N. Pavlov et al., *Gamma Spectroscopy using a Silicon Photomultiplier and a Scintillator*, IEEE Nuclear Science Symp. Conf. Record, N9-3, 2005

[9] F. Powolny et al., *Time-Based Readout of a Silicon Photomultiplier (SiPM) for Time of Flight Positron Emission Tomography (TOF-PET)*, Nuclear Science, IEEE Transactions on , vol.58, no.3, pp.597-604, June 2011

[10] Angelo Rivetti, Paolo Delaurenti, *A fast large dynamic range shaping amplifier for particle detector front-end*, Nuc. Instr. and Meth. A, Vol. 572, Issue 1, pp. 392-393, March 2006

[11] S. Seifert et al., *Ultra Precise Timing with SiPM-Based TOF PET Scintillation Detectors*, IEEE Nuclear Science Symp. Conf. Record, J01-4, 2009