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A Low-Noise Multi-GHz CMOS Multiloop Ring Oscillator With Coarse and Fine Frequency Tuning

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***Abstract*—A 7-GHz CMOS voltage controlled ring oscillator that employs multiloop technique for frequency boosting is presented in this paper. The circuit permits lower tuning gain through the use of coarse/fine frequency control. The lower tuning gain also translates into a lower sensitivity to the voltage at the control lines. Fabricated in a standard 0.13-μm CMOS process, the proposed voltage-controlled ring oscillator exhibits a low phase noise of −103.4 dBc/Hz at 1 MHz offset from the center frequency of 7.64 GHz, while consuming a current of 40 mA excluding the buffer.**

***Index Terms*—CMOS, coarse/fine tuning, gigahertz (GHz), multiloop, phase noise, ring oscillator, voltage-controlled oscillator (VCO).**

I. Introduction

As BOTH optical and data link systems move towards high-data rate application, low noise high frequency voltage-controlled oscillators (VCOs) are becoming more important in the design of the receiver and transmitter blocks in optical communications systems or the systems-on-chip (SOCs) with read channel and interface circuits such as Serial Advanced Technology Attachment (SATA) in data link/storage systems [1]. Ring oscillator has long been perceived as capable of permitting easy implementation and occupying much smaller die area as compared to its inductance-capacitance (LC) counterpart. Due to the low-power supply voltage as the technology scales down, a conventional tuning scheme will result in excessive VCO voltage-to-frequency gain (K_{VCO}) and this increases the noise sensitivity of the oscillator. To avoid such problem, various methods have been developed, such as to implement a coarse/fine frequency tuning in the LC-tuned and ring oscillators, to maintain the wide tuning range as well as a moderate tuning gain. For *LC*-tuned oscillators, the digitally switched varactor banks are usually adopted to provide the coarse tuning along with the continuous fine frequency tuning [2]–[5]. Most ring oscillators, however, implement the coarse/fine-tuning through controlling the tail current of the whole circuit [6]. This unfortunately increases the risk of up-conversion of the $1/f$ noise from the tail current source transistors.

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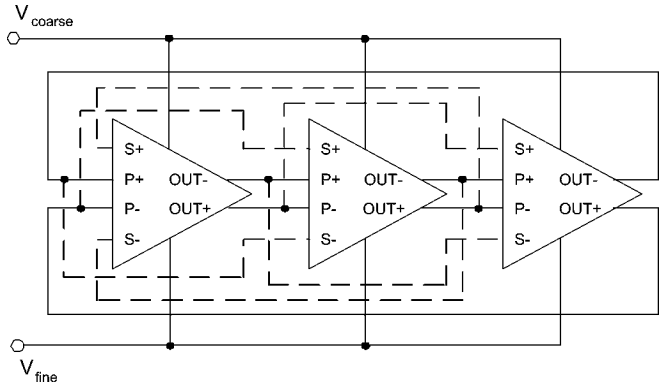

Fig. 1. Three-stage multiple-loop ring oscillator. The solid line represents the primary loop while the dashed line represents the secondary loop.

In this paper, a new delay cell that is equipped with both coarse- and fine-tunings is proposed. The multiloop technique is adopted to push the circuit's operating frequency to the maximum [7], [8]. Fine-tuning is implemented by adjusting the current flowing through the positive feedback cross-coupled nMOS pair that is included for self-balancing. Since the positive feedback latch transistors are sized very small, the drain current (and the drain current noise) is significantly reduced [9]. Therefore, their noise up-conversion makes a negligible impact on the noise performance of the whole circuit.

The design of the circuit is described in Section II. The small signal analysis in terms of frequency tuning as well as phase noise characteristics are both discussed in Section III. Lastly, the experimental results are presented in Section IV.

II. Design of Circuit

As mentioned in Section I, the proposed ring oscillator delay cell utilizes the multiloop technique. A general architecture of a three-stage multiloop ring oscillator is illustrated in Fig. 1. Two operating loops, a primary (solid line) and a secondary (dashed line), are involved in the ring oscillator. The primary loop works as a normal differential ring oscillator, while the secondary loop provides an additional entry to the input-output transfer function. This extra entry can help to decrease the slew time of the output nodes, from low to high, since the secondary inputs are fed from the outputs that are a few stages prior to the current stage. The circuit schematic of the proposed delay cell is depicted in Fig. 2. In this circuit, nMOS N1 and N2 form the input pair of the primary loop, while pMOS P5 and P6 serve as the input pair of the secondary loop. PMOS P1/P2 forms the load of the delay cell. When V_{P+} is lower than V_{tn}, transistor N1 shuts off. Since the input voltage at V_{S+} is earlier than V_{P+},

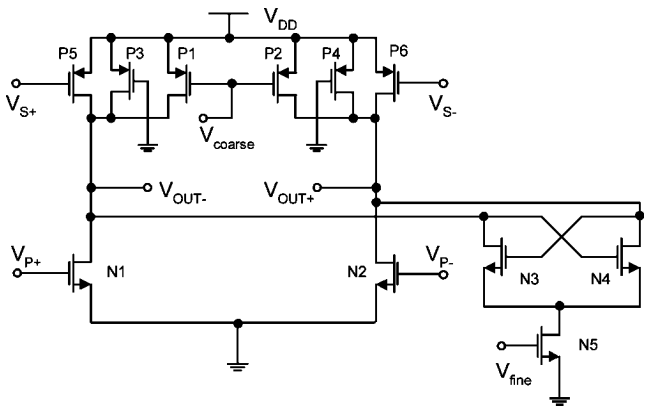

Fig. 2. Proposed delay cell for the multiple-loop ring oscillator.

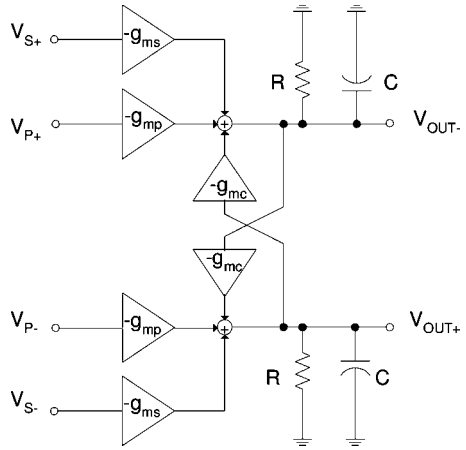

Fig. 3. First-order approximation of the proposed oscillator gain stage.

the secondary input transistor P5, will already be conducting its source current to the load capacitor at the output node $\mathrm{OUT}-$. As a result, the time for the output node to rise from low to high is decreased.

The tail current source transistors are avoided in this delay cell so as to maximize the signal swing, which is beneficial for signal-to-noise ratio (SNR). In order to avoid the loss of oscillation at the extreme cases of frequency tuning, extra pMOS loads, P3 and P4, are added in shunt with the controllable load P1 and P2. In this design, the gates of P3 and P4 are connected to G_{ND} to bias the transistors into the triode region of operation. Coarse-tuning is accomplished by varying the load through changing the gate voltage of P1/P2. On the other hand, fine-tuning can be achieved by adjusting the amount of tail current flowing through the positive feedback latch, N3 and N4.

III. Small Signal Analysis

The design of the ring oscillator is a tradeoff process that involves power, frequency, area, and noise performance. A qualitative analysis is essential for oscillator design since it provides the designer insight into the circuit and helps the designer to make informed decisions on the tradeoffs that are involved in the ring oscillator in terms of power, frequency, and noise. While the ring oscillator is actually experiencing large signal operation, it becomes extremely difficult to analyze its frequency and noise characteristics due to the nonlinearity and complexity. In this section, brief qualitative analysis of both the oscillator frequency tuning and phase noise performance are provided.

A. Frequency Tuning Issues

Assuming the oscillation amplitude to be small and the waveform shape is sinusoidal, the first-order small signal model of the gain stage in the proposed ring oscillator is presented in Fig. 3. g_{mp} and g_{ms} represent the transconductances from the primary input and the secondary input to the outputs, implemented by using N1/N2 and P5/P6. g_{mc} represents the transconductance between the differential outputs, which is constructed by the cross-coupled pair. R and C are the equivalent resistive and capacitive load seen at the output node, respectively. If θ is defined as the phase difference between the output node and the primary input node, and ϕ as that between the output node and the secondary input node, then for each half stage, the following equations may be derived:

$$V_{\mathrm{OUT}-} = V_{P+}e^{-j\theta} \tag{1}$$

$$V_{\mathrm{OUT}-} = V_{S+}e^{-j\phi} \tag{2}$$

$$V_{\mathrm{OUT}-} = V_{\mathrm{OUT}+}e^{-j\pi}. \tag{3}$$

Use KCL at the output node $\mathrm{OUT}-$

$$V_{\mathrm{OUT}-} = \frac{R}{1+j\omega RC}(-g_{mp}V_{P+} - g_{ms}V_{S+} - g_{mc}V_{\mathrm{OUT}+}). \tag{4}$$

Following the calculation procedure presented in [7], the relationship between the oscillation frequency and the small-signal model's parameters can be obtained, where

$$\omega = \frac{\tan\theta}{RC} + \frac{g_{ms}(\cos\phi\tan\theta - \sin\phi)}{C} - \frac{g_{mc}\tan\theta}{C}. \tag{5}$$

From the equation, it is noted that the first term represents the primary loop operating frequency, and is determined by the time constant and the number of delay stages n, since θ is defined by n as $\theta = (n+1/n)\pi$, considering the fact that θ is the sum of a dc phase shift of π and an ac phase shift of π/n. The second term in the equation illustrates the effect of the oscillation frequency, attributed by the secondary loop. In order to improve the oscillator speed, the term $\cos\phi\tan\theta - \sin\phi$ has to be positive. Because $\pi < \theta \leq 3\pi/2$ (i.e., $\theta = 3\pi/2$ when $n = 2$, $\theta = 4\pi/3$ when $n = 3$ and θ approaches π when n increases), which implies that $\tan\theta$ is always a positive value, the secondary loop has to be properly connected to ensure that the second term is positive.

The third term in (5) corresponds to the frequency change that is contributed by the cross-coupled nMOS pair. We can see that the introduction of the cross-coupled pair slows down the circuit speed by a factor that is proportional to the transistor transconductance. Hence, decreasing the transistor size or the drain current will reduce the slowdown effect. The cross-coupled nMOS pair can also be viewed as a latch, which makes it more difficult for both the differential outputs to change their status. Although this pair slows down the circuit operating speed, it is still essential since they can help to prevent the differential outputs

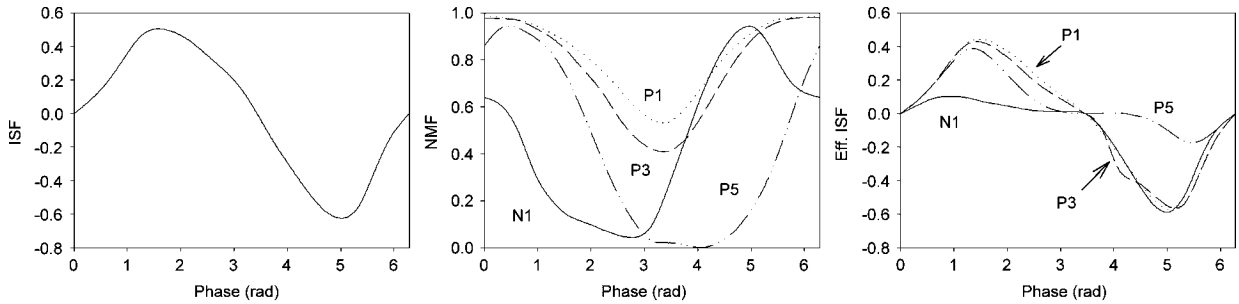

Fig. 4. (a) Calculated; (b) ISF, NMF; and (c) effective ISF of transistors N1, P1, P3, and P5.

from converging at the same voltage level. The positive feedback caused by the cross-coupled pair also reduces the slew time of the output nodes, for both the low to high and high to low transitions, yielding better oscillator phase noise performance [9].

B. Phase Noise Characteristics Analysis

The phase noise of the ring oscillator is analyzed based on the theory proposed in [9]. In [9], the phase noises of an oscillator in the regions of $1/f^3$ and $1/f^2$ are defined in (6) and (7), respectively

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log\left(N \cdot \frac{\Gamma_{\rm rms}^2}{q_{\max}^2} \cdot \frac{\frac{\overline{i_n^2}}{\Delta f}}{4 \cdot \Delta\omega^2}\right) \tag{6}$$

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log\left(N \cdot \frac{c_0^2}{q_{\max}^2} \cdot \frac{\frac{\overline{i_n^2}}{\Delta f}}{8 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right) \tag{7}$$

where $q_{\max}$ is the maximum charge at the output node of interest, $\Gamma(x)$ is the *Impulse Sensitivity Function (ISF)*, and N is the number of noise stages, i.e., $N = 6$ for a three-stage differential ring oscillator since the analysis is based on each half-stage. The quantity $\Gamma_{\rm rms}$ is the $\rm rms$ value of the ISF, c_0 is twice the dc value of the ISF function and is defined as $1/\pi \cdot \int_0^{2\pi} \Gamma(x)dx$. The ISF can be plotted by measuring the excess phase shift a few tens of cycles after injecting a current impulse into the node of interest across one period of the oscillation. The duration of the impulse should be set small enough so as to improve on the accuracy of the calculated ISF. $\overline{i_n^2}/\Delta f$ is the noise current *Power Spectral Density (PSD)* of the active devices. Meanwhile, the *Noise Modulation Function (NMF)* is also defined since the noise sources involved in the oscillator appear to be cyclostationary noise and can be treated as a stationary noise that is applied to the system with an effective ISF given by

$$\Gamma_{\rm eff}(x) = \Gamma(x) \cdot \alpha(x) \tag{8}$$

where $\alpha(x)$ is the NMF obtained from device noise characteristics. By substituting (8), (6) and (7) can be rewritten as

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log\left(N \cdot \frac{\Gamma_{\rm rms,eff}^2}{q_{\max}^2} \cdot \frac{\frac{\overline{i_{n0}^2}}{\Delta f}}{4 \cdot \Delta\omega^2}\right) \tag{9}$$

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log\left(N \cdot \frac{c_{0,\rm eff}^2}{q_{\max}^2} \cdot \frac{\frac{\overline{i_{n0}^2}}{\Delta f}}{8 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right). \tag{10}$$

The calculated ISF, NMFs, and effective ISFs are all illustrated in Fig. 4. Since N3/N4 and the tail transistor N5 contribute much less noise than the rest of the transistors, they are neglected in our analysis. The noise current PSD of the active devices in the ring oscillator can be modeled as

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{\overline{i_{n,d}^2}}{\Delta f} + \frac{\overline{i_{n,g}^2}}{\Delta f} = 4kT\gamma g_{d0} + 4kT\delta g_g \tag{11}$$

where $\overline{i_{n,d}^2}$ and $\overline{i_{n,g}^2}$ represent the channel noise and gate induced noise of the MOS devices, respectively. γ and δ are the bias-dependent noise factors and $\delta = 2\gamma = 3$ is used for calculation of this work in 0.13-μm process. The relationship between the gate conductance g_g and the channel conductance at zero drain-source bias g_{d0} can be expressed as [10]

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}}. \tag{12}$$

It has been proven that $\overline{i_{n,d}^2}$ is in general frequency-independent and increased when the channel length is decreased, while the induced gate noise is proportional to f^2, where f is the operating frequency [11]. Although both the noise sources contribute to the total noise at high frequency, the dominant contribution still comes from the channel thermal noise.

From our calculation, the largest transistor N1 is found to contribute to nearly half of the thermal noise and N1 has to be large enough to provide sufficient gain for the delay stage so as to maintain oscillation at high frequency.

C. Design Implications and Discussions

To summarize the previous analysis on frequency and phase noise, some design implications are given as follows.

1) The differential input nMOS transistors (N1/N2 in this work) contribute a significant portion of thermal noise as compared to the rest of the circuit. However, a larger dimension is necessary if higher frequency is desired. Hence, there is a tradeoff involving phase noise performance and operating frequency.

TABLE I
TRANSISTOR SIZES OF THE PROPOSED 3-STAGE RING OSCILLATOR DELAY CELL (IN MICROMETERS)

	N1	N3	N5	P1	P3	P5
W/L	35/0.13	5/0.13	20/0.4	15/0.13	15/0.13	15/0.13

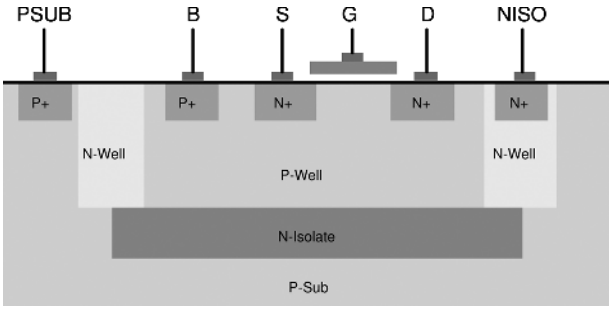

Fig. 5. Simplified cross-sectional view of nMOS transistor in triple-well technology.

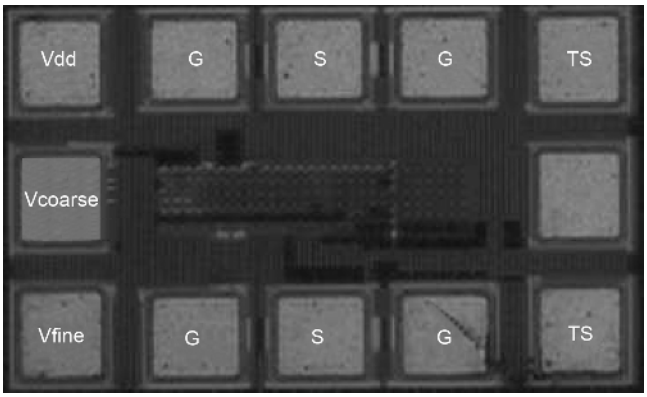

Fig. 6. Die photograph of the ring oscillator.

2) If cross-coupled latches are introduced, the slowdown impact on the entire circuit operation can be reduced by decreasing the transconductance, i.e., by reducing the W/L or the drain current.
3) Once the sizes of the input differential nMOS transistors and cross-coupled latch are determined, the g_m of pMOS load transistors (P1/P3 in this work) has to be larger than a specific value in order to meet the minimum required dc gain, so as to ensure the kick-start of the oscillation.
4) If a large coarse tuning range is desired, the size ratio of P1/P2 to P3/P4 can be increased, i.e., to reduce W/L of P3/P4 and increase that of P1/P2.

According to the previous analysis, the transistors are sized as shown in Table I. The length of the tail current transistor of the cross-coupled latch is increased to 0.4 μm to minimize the $1/f$ noise up-conversion.

Buffer has also been designed to drive the bondpads and the probe. An inverter buffer stage is inserted between the VCO and the 50-Ω output buffer to isolate the ring oscillator stages from the output load.

IV. EXPERIMENTAL RESULTS

To validate the performance of the proposed ring oscillator, the circuit was fabricated in a standard one-poly six-metal

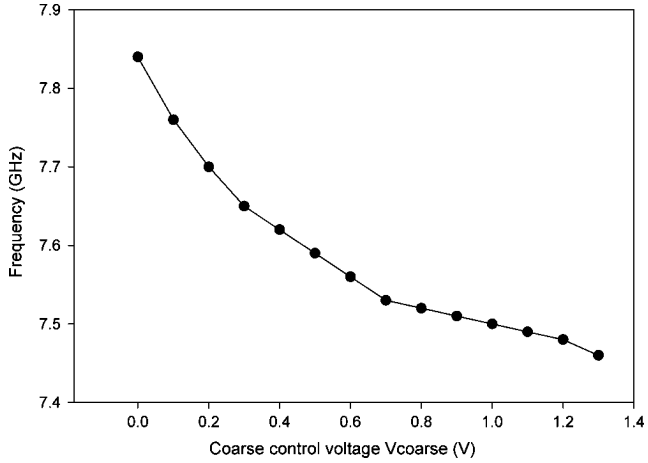

Fig. 7. Measured coarse frequency tuning characteristics of the ring oscillator when $V_{\rm fine}$ is fixed at 0 V.

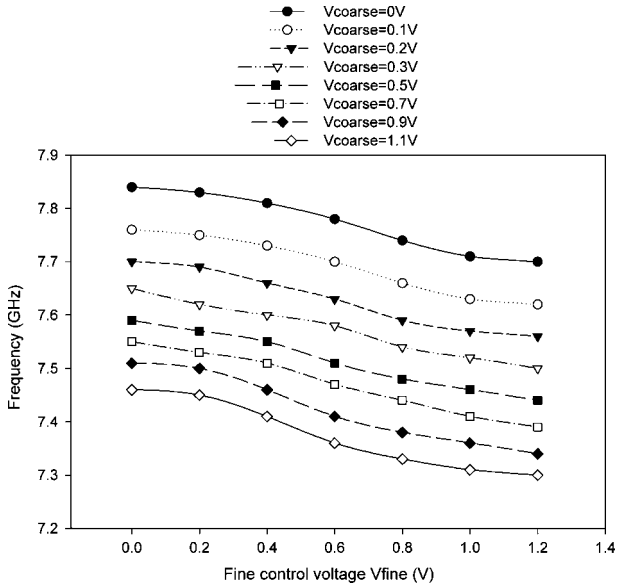

Fig. 8. Measured fine frequency tuning characteristics of the ring oscillator.

0.13-μm triple-well digital CMOS technology. The cutoff frequency f_T of nMOS transistor in this technology is over 90 GHz. The triple well process offers a better performance in terms of noise isolation and bulk control as compared to conventional p-well technology. As illustrated in the simplified cross-sectional view in Fig. 5, the buried deep n-well isolates the bulk of nMOS from the common P-substrate, thereby effectively minimizes the noise coupling from p-substrate to nMOS bulk. Fig. 6 shows the die photograph of the fabricated oscillator with a chip dimension of 500 μm $\times$ 320 μm (including the pad frame). The core oscillator occupies only 180 μm $\times$ 50 μm. On-wafer probing was performed for the measurement.

Two additional pads (marked as TS in Fig. 6) were added to cater to troubleshooting in the event of failure, for example, to kick start its oscillation. Two differential internal nodes of the VCO are connected to these two pads at the cost of a lower operating frequency since additional parasitic capacitances introduced by the pads into the oscillator loop make an influential impact on the circuit's operating frequency.

TABLE II
COMPARISON WITH OTHER RING OSCILLATOR DESIGNS

Reference	Tuning Range (GHz)	Technology	Power (mW)	Phase Noise	FOM (dBc/Hz)
[1]	3.2-10	0.12-μm CMOS	15	-90 dBc/Hz@1MHz from 6.4 GHz	-154
[6]	2.4	0.35-μm CMOS	-	-97 dBc/Hz@1MHz from 2.4 GHz	-
[8]	0.75-1.2	0.6-μm CMOS	30	-117 dBc/Hz@600KHz from 906 MHz	-165.8
[12]	0.1-3.5	0.18-μm CMOS	16	-106 dBc/Hz@4MHz from 3.5 GHz	-153
[13]	9.8-11.5	30 GHz BiCMOS	75	-94.3 dBc/Hz@2MHz from 11.5 GHz	-151
[14]	4.3-6.1	0.18-μm CMOS	80	-85 dBc/Hz@1MHz from 5 GHz	-140
This Work	7.3-7.86	0.13-μm CMOS	60	-103.4 dBc/Hz@1MHz from 7.64 GHz	-163.3

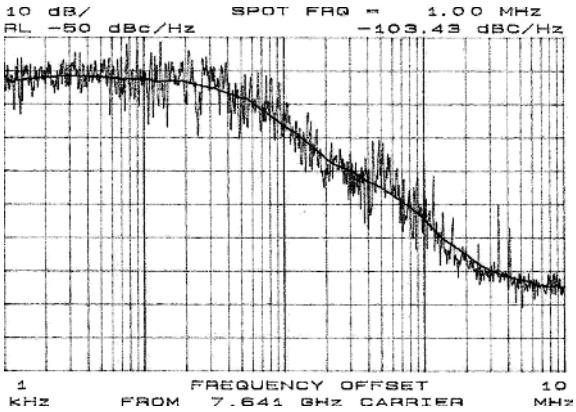

Fig. 9. Phase noise measurement result at 7.64 GHz.

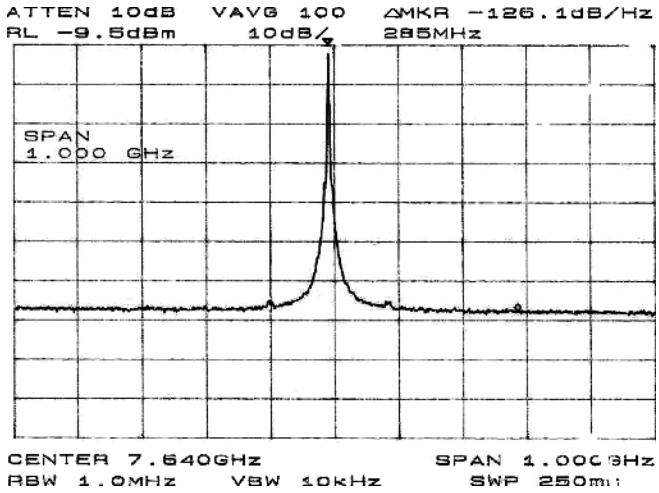

Fig. 10. Output power spectrum at the frequency of 7.64 GHz.

The coarse- and fine-tuning characteristics were measured and the results are plotted in Figs. 7 and 8, respectively. As seen in Fig. 7, the oscillator is able to operate from 7.44 to 7.86 GHz when V_{fine} is fixed at 0 V and with V_{coarse} tuned. The coarse tuning range shifts to 7.3 to 7.7 GHz when V_{fine} is fixed at 1.2 V, where the cross-coupled latch is turned on. It is noted from Fig. 7 that the coarse frequency tuning gain is about 380 MHz/V when $V_{\text{fine}} = 0$ V. Fig. 8 illustrates the fine tuning characteristics with varied coarse control voltages. A lowered fine frequency tuning sensitivity is found to be around 115 MHz/V. The fine tuning sensitivity can be further reduced by using the cross-coupled latch with smaller g_m. In contrast, the coarse tuning gain can be increased by using larger W/L sizes of transistors P1/P2.

TABLE III
PERFORMANCE SUMMARY OF THE FABRICATED VCO

Technology	0.13-μm CMOS
Die Size	500 μm $\times$ 320 μm
Tuning Range	7.3 - 7.86 GHz
Tuning Sensitivity	Coarse: 380 MHz/V Fine: 115 MHz/V (average)
Supply Voltage	1.5 V
Current Consumption	61 mA (40 mA by VCO core)
Phase Noise at 1 MHz offset	-103.4 dBc/Hz (from 7.6 GHz)

The phase noise measurement is characterized on-wafer using the HP8563E spectrum analyzer. Fig. 9 presents a typical phase noise measurement result of -103.4 dBc/Hz at 1 MHz offset from the 7.64 GHz operating frequency, at $V_{\text{coarse}} = 0.2$ V and $V_{\text{fine}} = 0.5$ V. The corresponding output power spectrum is plotted in Fig. 10. The power dissipation of the total chip is 91 mW, of which 60 mW is consumed by the VCO core, with a supply voltage of 1.5 V. As a comparison, the calculated minimum achievable phase noise of CMOS ring oscillator at same frequency with same power consumption is evaluated to be -105.3 dBc/Hz at 1 MHz offset. This is less than 2 dB better than the results achieved in this work. The calculation shown below is based on the theory reported in [15] in that

$$\mathcal{L}_{\min}(\Delta f) = 10\log\left[\frac{7.33kT}{P_{\min}}\left(\frac{f_0}{\Delta f}\right)^2\right] \tag{13}$$

where $P_{\min}$ is the minimum power dissipation of ring oscillator that is proportional to the parasitic capacitance value and the square of the bias voltage.

Some other ring oscillator designs have been listed in Table II for comparison. The figure-of-merit (FoM) of the VCO is expressed as [13]

$$FoM = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{mW}}{1\,\text{mW}}\right) \tag{14}$$

where $\mathcal{L}(\Delta f)$ is the measured phase noise in dBc/Hz at a frequency offset of Δf from the carrier frequency f_0 and P_{mW} is the measured power dissipation of the oscillator in milliwatts. From the table, it is evident that our proposed design is able to achieve good results that are comparable to some of the recently

reported ring oscillator designs. The measured results demonstrate the capability of the proposed coarse- and fine-tuning VCO to operate at high frequencies with low phase noise. The performance of the ring oscillator is summarized in Table III.

V. Conclusion

Coarse- and fine-tuning can be used to decrease the VCO tuning sensitivity without impairing the tuning range. A novel delay cell of coarse/fine-controlled ring oscillator has been proposed to reduce the tuning sensitivity and the low-frequency noise up-conversion. A fully integrated implementation in a 0.13-μm CMOS one-poly six-metal process demonstrates a frequency tuning range of 7.3 to 7.86 GHz, with average fine tuning sensitivity of 115 MHz/V. This oscillator can be used in phase-locked loops that engage frequency-training loop. In this case, the fine tuning of the VCO is driven by the phase-locking loop while the coarse tuning is derived from the frequency-training loop. Since the frequency loop remains relatively quiet after phase lock, the high sensitivity of coarse control does not lead to high jitter.

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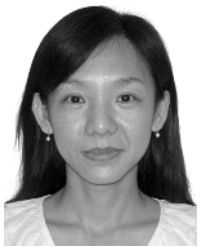

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