A Low-Phase Noise, Anti-Harmonic Programmable DLL Frequency Multiplier With Period Error Compensation for Spur Reduction

Qingjin Du, Jingcheng Zhuang, and Tad Kwasniewski

***Abstract*—A low phase noise, delay-locked loop-based programmable frequency multiplier, with the multiplication ratio from 13 to 20 and output frequency range from 900 MHz to 2.9 GHz, is reported in this brief. A new switching control scheme is employed in the circuit to enable the capability of locking to frequencies either above or below the start-up frequency without initialization. To reduce the spurious output power level, a low-bandwidth auxiliary loop [period error compensation loop (PECL)] is employed to compensate for the output period error caused by the phase realignment errors. This frequency multiplier is implemented in TSMC 0.18-μm CMOS technology and measured with a synthesized frequency source. A significant reduction of the output spurs from −23 to −46.5 dB at 1.216 GHz is achieved by enabling the PECL. The measured cycle-to-cycle timing jitter at 2.16 GHz is 1.6 ps (rms) and 12.9 ps (pk-pk), and the phase noise is −110 dBc/Hz at 100-kHz offset with a power consumption of 19.8 mW at a 1.8-V power supply.**

***Index Terms*—Delay-locked loop (DLL), frequency multiplier, in-lock error, phase noise, phase-locked loop (PLL), spurious power level.**

I. Introduction

THE frequency multiplier is an important building block in communication systems and its performance parameters including the phase noise and spurious power level are very critical. The phase-locked loop (PLL) architecture is dominant in the field of frequency synthesis for many years. However, compared with the delay-locked loop (DLL) counterpart, it suffers from phase noise accumulation in the voltage-controlled oscillator (VCO) induced by the power supply and substrate noise. In recent years, the DLL-based clock synthesis is under exploration [1]–[7], due to its superior phase noise performance, while relatively high output spurs limit its wide use. To date, two typical implementations of DLL-based frequency multiplication are reported. One is based on a voltage-controlled delay line (VCDL) and an edge combiner [1], [2], [6], [7] and the other one is based on a VCO-like VCDL [3], [4]. Two main sources of spurious output of the first approach are the mismatches of the VCDL/edge combiner and the loop in-lock error. The mismatches are minimized in the second approach because the reference signal always circulates in the same delay stage, but the phase realignment errors, in the process of injecting the clean reference edges into the VCDL, might even enlarge the total period errors, which cannot be effectively minimized by optimizing the charge pump (CP) and the phase and frequency detector (PFD). This brief presents a multiplying DLL frequency multiplier with a period error compensation loop (PECL) to achieve both low phase noise and low spurious power level. To prevent the loop from locking to harmonic reference edges, a switching control logic circuit and a resetable dynamic frequency divider are proposed.

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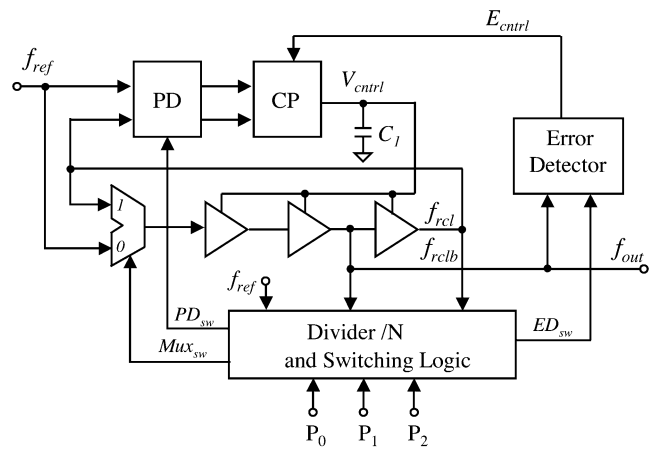

Fig. 1. Proposed architecture of the DLL frequency multiplier with period error compensation loop.

II. Proposed DLL Frequency Multiplier With a PECL

The block diagram of the proposed frequency multiplier is shown in Fig. 1. It comprises of a PFD, a CP, a MUX, a divide-by-N divider, a switching logic (SL) circuit, an error detector (ED), a VCO-like VCDL, and a loop filter (C_1). The reference edges are injected into the VCDL by setting the MUX to position "*1*" and the edges propagates in the VCDL, or circulates in the ring consisting of 3 invertors and a MUX, until the MUX is switched to "*0*." Comparing with a conventional VCDL, which physically consists of multiple delay stages, the VCO-like VCDL eliminates the stage mismatch and the use of edge combining circuit. In addition, it can be easily programmable. By comparing the phase of the VCDL output ($f_{\rm rcl}$), which is the delayed reference edge after circulating in the ring

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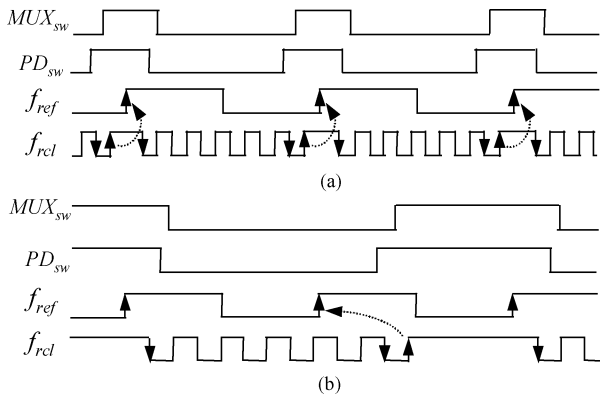

Fig. 2. Timing of the frequency multiplier for the cases of the initial frequency is (a) higher and (b) lower than the desired frequency.

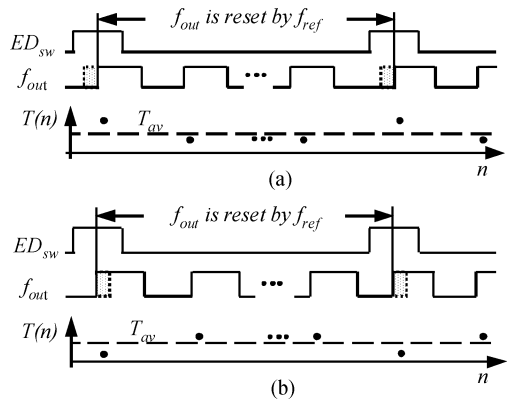

Fig. 3. Period errors when the loop is in lock with positive period error (a) and negative period error (b).

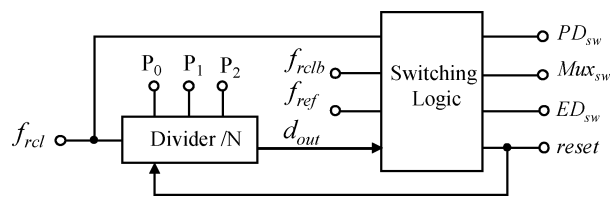

Fig. 4. Frequency divider and the SL circuit.

for N cycles, with that of the next reference edge, the delay of the VCDL is tuned so that the total delay ($N \cdot T_{\rm out}$) equals to the reference period ($T_{\rm ref}$). In other words, the output frequency is N times the reference frequency.

However, employing a VCO-like VCDL may cause the phase detector compares the phase of $f_{\rm rcl}$ with that of the harmonic reference edge, the loop may fail in locking if an initial frequency is lower than the desired one [3]. This design employs a novel switch scheme to solve this problem. Fig. 2 shows two cases where the initial frequency is higher and lower than the desired frequency with an example $N = 6$. After a reference edge is injected to the VCDL, the frequency divider is reset and the $\rm MUX_{sw}$ goes low so that the reference edge can circulate in the VCDL. After five output cycles, the $\rm MUX_{sw}$ goes high and the VCDL is connected to the reference signal until a new reference rising edge is injected. The $\rm PD_{sw}$ goes high at the fifth output rising edge so that the PFD captures the last output rising edge. The PFD is based on a conventional 3-state PFD controlled by $\rm PD_{sw}$, which only controls the comparison path of $f_{\rm rcl}$ and resets the PFD when its falling edge comes and a new reference edge is injected. This proposed switching scheme ensures the phase comparison is always done between the last output rising edge and the reference rising edge next to the previously injected one as illustrated in the dotted arrows. Consequently, the DLL can always acquire lock without initializing the VCDL control signal and avoid harmonic locking.

Due to the mismatches in the feedback path including the PFD/CP combination and the realignment error introduced while the new reference edge is injected into the VCDL every N output cycles [5], the N-th cycle always has its period different from periods of the previous $N - 1$ cycles even when the loop is in lock and large output spur is thus resulted. As illustrated in Fig. 3, there are N output cycles within one reference period, and each corresponding period is plotted at the bottom of the figure. One period among the N periods may be always larger or smaller than other $N - 1$ periods as shown in Fig. 3(a) and (b), respectively. This static error is referred as the period error in the remaining of this brief. To minimize the error, the output $f_{\rm out}$ is applied to an ED to extract this error and compensate it by tuning the charge pump current. The ED compares the period of the Nth output cycle $T_{\rm out}(n)$ with the average period ($T_{\rm av}$). The difference between $T_{\rm out}(n)$ and $T_{\rm av}$ is amplified and its polarity is determined. The comparison offset is self-cancelled in the ED so that it can provide more precise error information than the PFD, where the offset of the phase comparison cannot be self-cancelled. In addition, the error information provided by the ED corresponds to the total period error appearing at output of the frequency multiplier while the error provided by PFD only corresponds to part of the period error. In this design, besides the loop governed by the PFD, which dynamically compensates for the period error, a low bandwidth PECL, governed by the ED, is used to compensate for the static period error to significantly reduce the output spurious level.

III. CMOS Implementation

A. VCO-Like VCDL

The high output frequency is generated in the VCO-like VCDL, which consists of three inverting delay cells and a MUX controlled by the SL circuit. Since the frequency multiplier output f_{rclb} or $f_{\rm out}$ is derived from a fixed node (the output of the second delay cell), the stage mismatch among the three delay cells does not result in spurious output even with a MUX placed at the input of the first stage. Current starved inverters are employed in the delay cells and two CMOS pass gates are used to form the *2* to *1* MUX.

B. Frequency Divider and SL Circuit

The frequency divider and the SL circuit shown in Fig. 4, coordinate the frequency multiplier operation by providing three signals $\rm MUX_{sw}$, $\rm PD_{sw}$, and $ED_{\rm sw}$. The programmable frequency divider counts the high frequency output $f_{\rm rcl}$ to achieve a programmable multiplication ratio. After a reference edge is injected in the VCDL, the frequency divider is reset by a reset signal from the SL and starts to count from zero again. In this design, the frequency divider comprises of three stages of divide-by-2,3 dividers connected in series and three NOR gates

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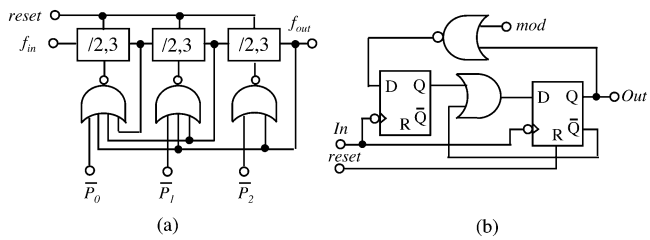

Fig. 5. (a) Divider-by-N divider. (b) Divide-by-2,3 divider .

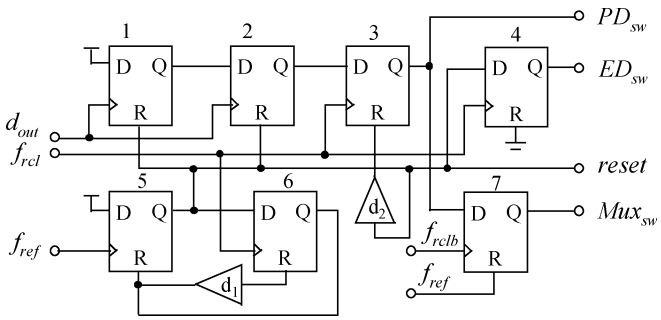

Fig. 6. Schematic of the SL circuit.

as shown in Fig. 5(a). By programming P_0, P_1 and P_2, multiple division ratios can be obtained and the ratio is calculated as

$$N = \sum_{i=o}^{i=2} 2^i \cdot P_i + 2^{i+1}. \tag{1}$$

From the equation, the frequency division ratios are integers from 8 to 15. Due to the delay from the VCO output, the divider and the SL, to the $\mathrm{MUX_{sw}}$, the actual division ratios of the frequency multiplier are from 13 to 20.

Fig. 5(b) shows the schematic of the divide-by-2,3 divider. It consists of two D flip-flops (DFFs) and two logic gates. For the normal mode operation when $\mathrm{mod} = 1$, the output Q of the shaded DFF is always 0 and the second one is in a toggle configuration working as a divide-by-2 divider. When $\mathrm{mod} = 0$, the second one remains high for an extra clock cycle before setting back to 0 and toggles again, resulting in dividing by 3. The extended true-single-phase-clock (E-TSPC) logic is employed in the divider to reduce the transistor count, power consumption and achieve high-speed operation.

The SL circuit consists of seven resetable FFs and two delay elements as shown in Fig. 6. One of the four inputs, d_{out}, is from the frequency divider, and its second rising edge after the divider is reset indicates when the counting-to-N is reached. DFF1 and DFF2 form a count-to-2 circuit and the output Q of the DFF2 goes high at the second rising edge of the d_{out}. The operation after $Q2$ goes high is illustrated in Fig. 7. Signal $\mathrm{PD_{sw}}$ is obtained by sampling Q2 at the rising edge of the f_{rcl}. The $\mathrm{MUX_{sw}}$ is generated by sampling the $\mathrm{PD_{sw}}$ at the rising edge of f_{rclb}. The *reset* signal appears at the first rising edge of f_{rcl} after the rising edge of the f_{ref}. The ED_{sw} is obtained by sampling the *reset* signal at the rising edge of f_{rcl}, and it is a positive pulse with the width equal to one output period.

C. Phase Detector and Charge Pump

The schematic of the phase detector is shown in Fig. 8(a). It is based on a dual FF PFD controlled by $\mathrm{PD_{sw}}$ generated from

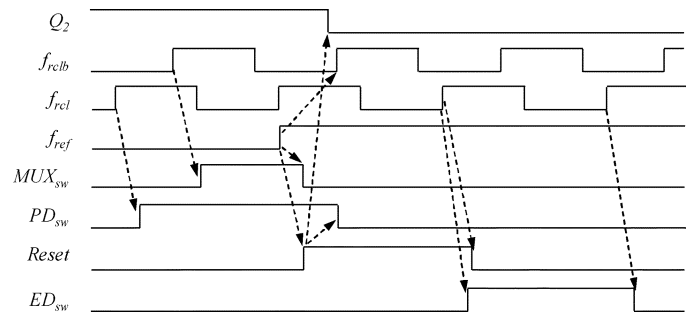

Fig. 7. Operating principle of the SL circuit.

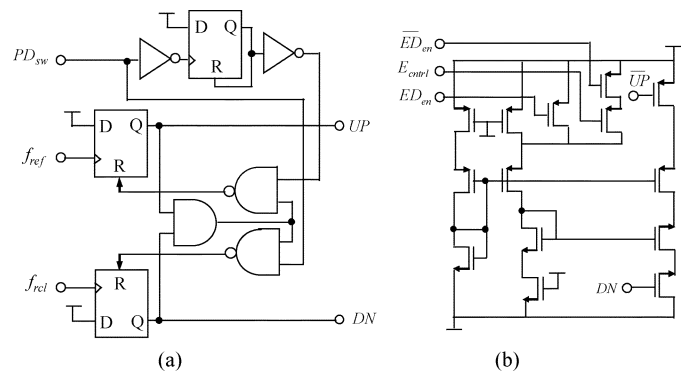

Fig. 8. Schematic of PFD (a) and CP (b).

the SL circuit. The signal *DN* goes high at rising edge of f_{rcl} only if $\mathrm{PD_{sw}}$ is high, while the *UP* signal always goes high at the reference rising edge. Similar to a conventional PFD, the UP and DN are reset once both of them are high. At the following edge of $\mathrm{PD_{sw}}$, the PFD is reset so that correct comparison can be guaranteed. This reset signal is a narrow pulse generated by DFF 3 with its output connected to its reset input.

In the charge pump as shown in Fig. 8(b), the *UP/DN* signals control a charge current and a discharge current respectively. Normally speaking, the two currents are equally matched by the current mirrors so that the zero net charge is achieved when *UP/DN* have the equal width. Any current mismatch in this approach results in in-lock error. In this design, a dynamic compensation technique is used to reduce the in-lock error as well as other injection errors and a current tuning capability is implemented in the charge pump. Since the relative error itself between the charge current and the discharge current is of importance, only charge current is finely tuned with the PECL while the discharge current is fixed in this design.

D. Error Detector

The ED is the main part of the PECL. It compares the average period of the signal f_{rcl} and the period of each nth cycle, whose period may be different from the other cycles. The mathematic model of the ED is shown in Fig. 9. From the figure, all VCO periods are subtracted by their average period value, which is determined by an internal feedback loop, and the subtracted results are amplified and their polarities are examined to produce the error output whenever the ED_{sw} is high.

The schematic of the ED is shown in Fig. 10 and its operation, for the case of positive period error, is illustrated in

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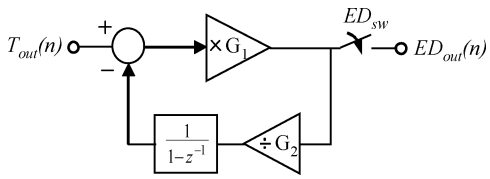

Fig. 9. Mathematic model of the ED.

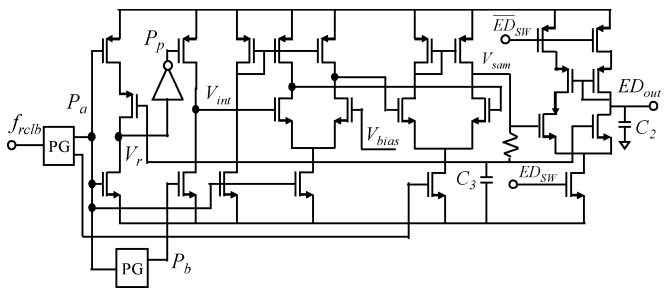

Fig. 10. CMOS implementation of the ED.

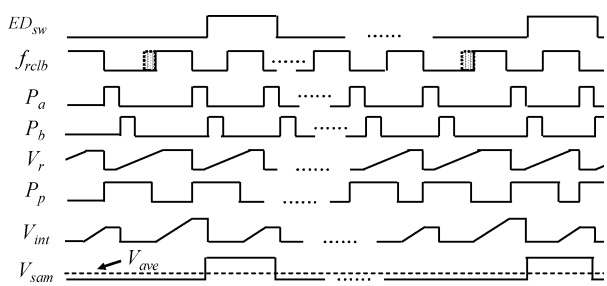

Fig. 11. Operation of the ED.

Fig. 11. At each falling edge of the input signal f_{rclb}, the pulse generator (PG) generates a narrow pulse (P_a), and its width is then increased by an amount corresponding to the average period duration. The resulted pulse train (P_p) is inverted and integrated by a high-gain integrator whose output ($V_{\rm int}$) is sampled and then reset before the next pulse coming. Those sampled results ($V_{\rm sam}$), corresponding to the VCO periods, drive the internal feedback, so that the average value ($V_{\rm ave}$) of the sampled results can be dynamically maintained by the internal feedback at a certain level determined by $V_{\rm bias}$. When signal $ED_{\rm sw}$ is high, a comparator is switched on to compare the samples ($V_{\rm sam}$) with its average ($V_{\rm ave}$) to generate the error output signal. The internal feedback loop compares $V_{\rm ave}$ with a pre-defined value ($V_{\rm bias}$) and adjusts the width increase amount of signal P_a accordingly. With the internal loop, a large integrator gain can be used to achieve high period error resolution. The bias voltage ($V_{\rm bias}$), which determines $V_{\rm ave}$, is set to be approximately $V_{DD}/2$ to ensure the integrator works in its high-gain region.

The output of the ED is to finely tune the charging current in the charge pump after it is low-pass filtered to compensate the period error. The functionality of the ED can be observed from signal $V_{\rm cntrl}$ and $E_{\rm cntrl}$ during the locking process from the post-layout simulation result as shown in Fig. 12. The shaded region expanded on the right shows the details how $E_{\rm cntrl}$ changes $V_{\rm cntrl}$ after the loop is in lock. When the main loop is in lock, $V_{\rm cntrl}$ is stable, and the ED detects in-lock errors based on the output $f_{\rm out}$. Accordingly, the period compensation loop tunes

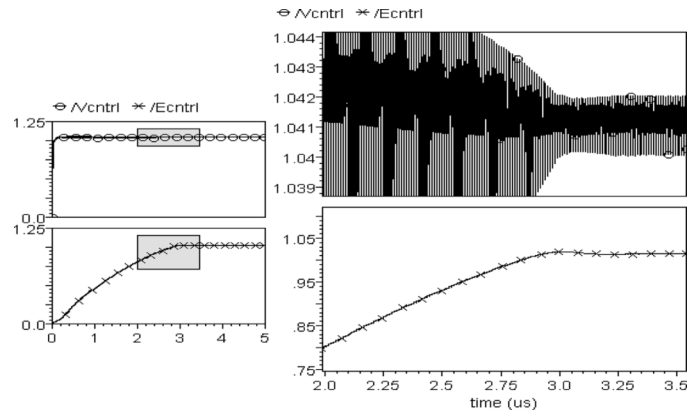

Fig. 12. Signal $V_{\rm cntrl}$ and signal $E_{\rm cntrl}$ signal from post-layout simulation.

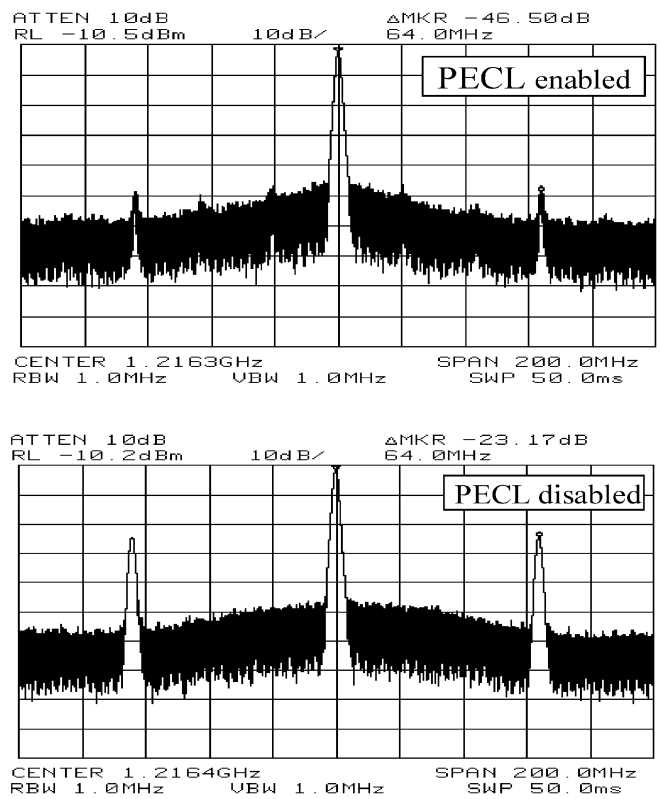

Fig. 13. Measured spurious power level at 1.216 GHz with PECL enabled and disabled.

$E_{\rm cntrl}$ to increase or decrease the charging current of the charge pump, making a small change in $V_{\rm cntrl}$. $V_{\rm cntrl}$ is decreased by about 2 mV as shown in the figure, and the large current spikes are also reduced, resulting in an edge jitter reduction from 28 to 3.2 ps (peak to peak). All these significantly contribute to the output spurs reduction.

IV. Measurement Results

The circuit is implemented in CMOS 0.18-μm technology and tested with a synthesized reference signal from an RF signal generator. Fig. 13 presents the measured output spurious power level with a carrier frequency of 1.2 GHz. With the compensation loop disabled and enabled, the spurious tones at the reference frequency of 64 MHz are −23.17 and −46.5 dBc, respectively, and a significant spur reduction of 23 dB is obtained.

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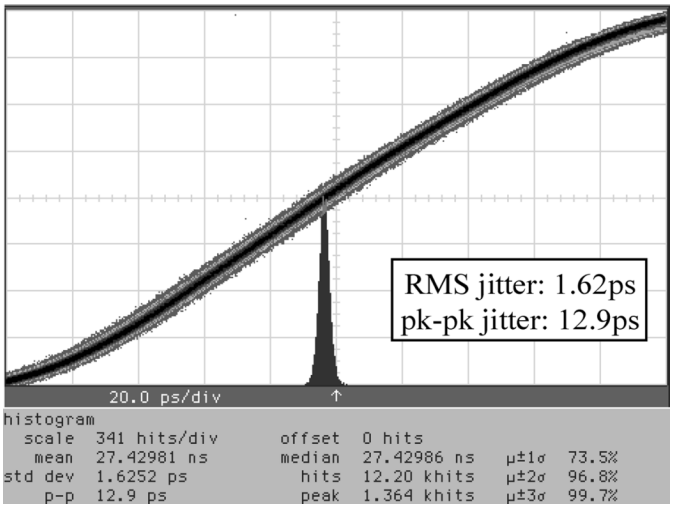

Fig. 14. Measured cycle-to-cycle timing jitter at 2.16 GHz.

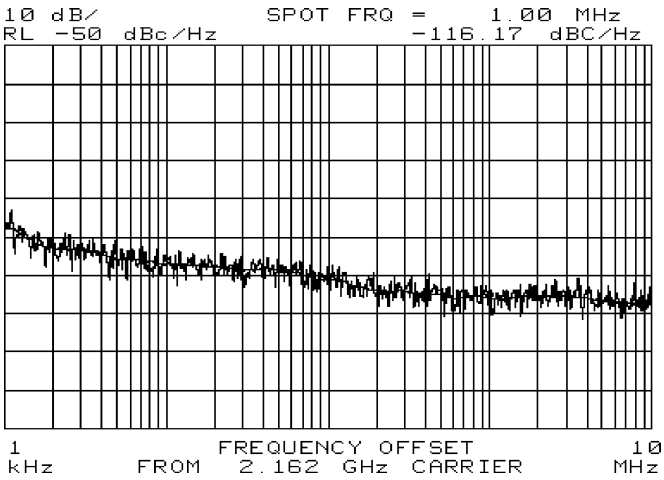

Fig. 15. Measured phase noise at 2.16 GHz.

Fig. 14 shows the jitter histogram with the in-lock error reduction technique enabled. The cycle-to-cycle rms edge jitter is 1.6 ps and the peak-to-peak value is 12.9 ps at the 2.16-GHz output frequency with the division ratio of $N = 20$. The phase noise of the output is shown in Fig. 15. The measured phase noise is -110 dBc/Hz at 100-kHz offset while the reference phase noise is -135 dBc/Hz at 100 kHz. This output phase noise is mainly limited by the reference signal due to the nature of the DLL. The measured phase noise does not change much when the compensation loop is enabled. Similar results are achieved for other frequencies tested. Supplied by a 1.8-V dc source, the circuit consumes less than 20 mW, and the output frequency range is from 900 MHz to 2.9 GHz. The measured performances of the circuit are listed in the comparison with state of the art as shown in Table I. Fig. 16 shows the die microphotograph.

V. Conclusion

A programmable DLL-based frequency multiplier with a period error compensation loop is presented. The proposed in-lock error reduction technique can effectively reduce the output spur by more than 20 dB, and an rms timing jitter of 1.6 pS at 2.16 GHz is achieved. By implementing the proposed SL circuit and the resetable divider, the circuit can lock to any frequencies either above or below the start-up frequency without initialization and avoid harmonic locking.

TABLE I
Measured Performance Comparisons

Items	REF[3]	REF[7]	THIS WORK
Supply voltage	1.8 V	3.3 V	1.8 V
Division ratios	4, 6, 8, 10	1- 8	13 - 20
Output (Hz)	200M - 2G	120M - 1.8G	900 M ~ 2.9 G
Phase noise (dBc/Hz)	N/A	N/A	-116 @ 2.16 G, 1MHz offset
Timing jitter (ps, rms) (ps, pk-pk)	1.62 at 2 G 13.1 at 2 G	1.8 13.2	1.61 at 2.16 G 12.9 at 2.16 G
Spurious tones	-37 dB at 2GHz	N/A	-46.5 dB at 1.2 GHz
Loop capacitor	N/A	N/A	C_1: 2 pF
Power (mW)	12 at 2GHz	86 at 1.6GHz	19.8 at 2GHz
Active area	0.05 mm^2	0.07 mm^2	0.07 mm^2
Technology	0.18 μm	0.35 μm	0.18 μm

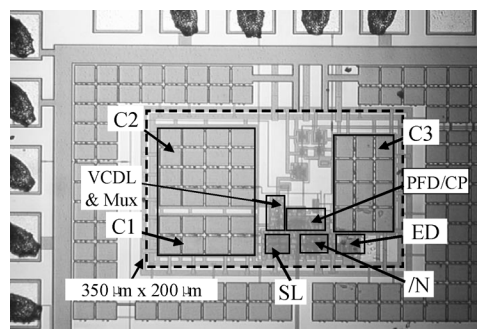

Fig. 16. Die microphotograph.

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