A Low-Power 22-bit Incremental ADC

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***Abstract*—This paper describes a low-power 22-bit incremental ADC, including an on-chip digital filter and a low-noise/low-drift oscillator, realized in a 0.6-μm CMOS process. It incorporates a novel offset-cancellation scheme based on fractal sequences, a novel high-accuracy gain control circuit, and a novel reduced-complexity realization for the on-chip sinc filter. The measured output noise was 0.25 ppm (2.5 μV_{RMS}), the DC offset 2 μV, the gain error 2 ppm, and the INL 4 ppm. The chip operates with a single 2.7–5 V supply, and draws only 120 μA current during conversion.**

***Index Terms*—Analog-to-digital conversion, CMOS analog integrated circuits, delta-sigma modulation, incremental data converters, low-power electronics, mixed analog-digital integrated circuits, oversampling A/D converters, switched-capacitor circuits.**

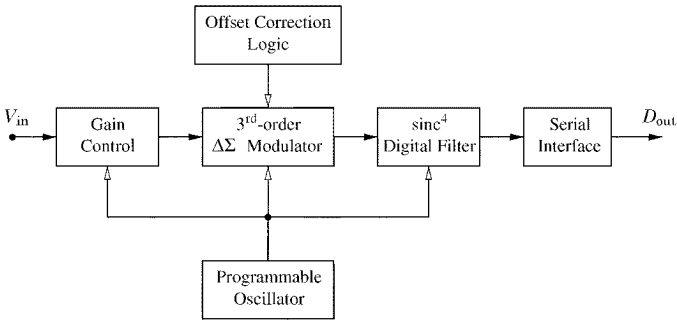

Fig. 1. System diagram of the incremental data converter.

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) used in instrumentation and measurement (I&M) applications often require very high absolute accuracy and linearity, and very low offset and noise. Low power is also an important consideration. On the other hand, the frequency band of the input signal is usually very narrow; often, it is only a few hertz wide. Typical applications include weight scales, as well as smart humidity, pressure or temperature sensors, and digital voltmeters.

Such I&M specifications are not easily satisfied with conventional delta-sigma ADCs, since these do not provide accurate gain control and low offset, and require complex and power-hungry digital filters for high-accuracy performance [1]. Dual-slope ADCs, on the other hand, are capable of low-offset and accurate gain operation, and do not need elaborate digital filters, but require a very long conversion time, and are sensitive to analog element nonidealities.

The properties of incremental data converters (IDCs) [2] are, by contrast, well matched to the requirements of I&M. They can be considered to be delta-sigma ADCs operated in a transient mode. They provide very precise conversion with accurate gain, high linearity and low offset, and the conversion time can be relatively short. IDCs need only simple digital postfilters, and they can readily be multiplexed between multiple channels.

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In contrast to the conventional delta-sigma ADC, which converts a waveform operating continuously, the IDC converts individual input samples. It operates for a predetermined number N of clock periods (usually, N is 1000–10 000), and is then reset. The reader is referred to [2]–[5] for detailed explanation of the underlying theory.

Earlier works described a first-order [2] and a second-order [3] IDC. The design theory of higher order IDCs was discussed in [4], which also discussed the tradeoffs between various realizations. However, the theory was not corroborated by experimental evidence until now.

This paper describes a third-order IDC fabricated in a 0.6-μm CMOS process based on the theory described in [4]. It also incorporates some novel features, such as "fractal" offset cancellation, a novel signal-scaling circuit, and a novel realization of the on-chip digital filter. The measured data confirmed 22-bit performance, with an INL below 4 ppm, an input-referred noise below 2.5 μV_{RMS}, and a gain error typically around 2 ppm.[1] The measured DC offset was around 2 μV.

In Section II of the paper, the overall architecture and operation of the implemented IDC are discussed. Section III describes the delta-sigma modulator, including the gain control stage at its input port. Section IV discusses the fractal offset compensation used in the modulator. Section V describes the digital filter used to process the digital output of the modulator, and Section VI the implementation of the integrated IDC, along with the results of the measurements verifying its performance. Finally, Section VII summarizes the design techniques and experimental results.

II. Architecture and Operation

Fig. 1 shows the system diagram of the IDC. The input signal V_{in} is sampled and scaled by the precision gain control block, and then entered into a third-order low-distortion single-bit delta-sigma loop [6]. The output bit stream enters a fourth-order

[1]Note that in the paper we defined error in ppm as $10^6 \cdot \text{error}/2V_{ref}$, as usual in the literature on I&M data converters.

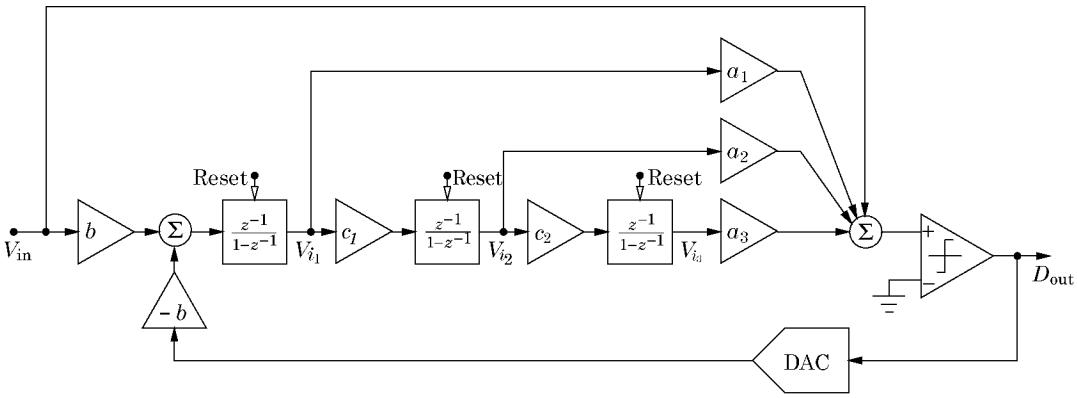

Fig. 2. Block diagram of the delta-sigma loop.

sinc filter [4]. The 24-bit output of the filter (22 bits of data plus two overflow bits) is the desired digital equivalent of V_{in}. Note that the IDC is functional only for a limited number N of clock cycles. The minimum value of N is determined by two conditions: the first insures the required accuracy of the delta-sigma modulator output signal, and the second requires the filling of the registers of the sinc filter with valid data [4]. The first condition can be understood from the block diagram of the delta-sigma loop (Fig. 2). As can be seen from the figure, the difference between the analog input V_{in} and the reconverted digital output D_{out} is integrated three times in the loop to yield V_{i_3}, the output of the third integrator. Hence, after n clock periods

$$V_{i_3}[n] = c_2 c_1 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} (V_{\text{in}}[k] - d_k V_{\text{ref}}) . \qquad (1)$$

Here, the d_k are the single-bit output samples in D_{out}.

If the loop is stable, all voltages can be kept smaller than the reference voltage V_{ref} used in the internal converters. Assuming also that V_{in} does not change during the conversion, it follows that V_{in} may be estimated from

$$\frac{V_{\text{in}}}{V_{\text{ref}}} \approx \frac{3!}{(n-2)(n-1)n} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k. \qquad (2)$$

The error of the estimation is $V_{\text{LSB}}/2$, where

$$V_{LSB} \approx \frac{2 \cdot 3!}{(n-2)(n-1)n} \frac{1}{c_2 c_1 b} V_{\text{ref}}. \qquad (3)$$

From (2) and (3), it follows that V_{in} can be obtained from the triple summation of the digital output over n clock periods, with a worst-case error given by (3). Comparing V_{LSB} with the permissible error, a minimum number N of clock periods needed for sufficiently accurate conversion can be estimated.

The second condition insures that the registers of the digital decimation filter (which are reset after each conversion cycle) are fully filled with new data after N clock periods. For an Lth-order sinc filter with a transfer function

$$H(z) = [1 + z^{-1} + z^{-2} + \ldots + z^{-M+1}]^L / M^L = \left(\frac{1}{M} \frac{1 - z^{-M}}{1 - z^{-1}} \right)^L \qquad (4)$$

which requires $N \geq L \cdot M$. Hence, N must satisfy both conditions; (4) is usually the decisive one. After N cycles, the output word is stored, and the system is reset. In our ADC, $L = 4$, $M = 512$, and $N = 2048$ were chosen.

The crucial offset compensation function is controlled by the offset correction logic (Fig. 1). This controls the switches in the switched-capacitor (SC) integrators of the delta-sigma loop so as to implement a fractal sequence. As discussed later, this involves the periodic inversion of the offset polarity in the loop filter, and results in the accurate cancellation of the input offset after N cycles.

The sinc filter uses a novel implementation of the familiar Hogenauer structure [7], which contains a cascade of integrating, differentiating and scaling stages. In our implementation, the differentiating stages are replaced by a programmable counter [8]. This reduces the complexity of the filter hardware.

The clock signals are provided by an on-chip relaxation oscillator, with digital frequency and temperature coefficient control. It consumes only around 50 μW power.

The operation and circuitry of the main blocks of the system are discussed in the following sections.

III. Delta-Sigma Modulator and Gain Control

Fig. 3 shows the simplified schematic diagram of the third-order delta-sigma modulator, without the gain- and offset-control circuits. It uses a low-distortion configuration, in which the SC integrators (ideally) do not carry the input signal, so that the required linearity of the operational amplifiers (opamps) is reduced [6, ch. 3]. Since the input signal of an IDC is effectively DC, the oversampling ratio (OSR) was defined as the ratio of the loop's clock frequency f_s divided by the main notch frequency f_n of the sinc filter. Hence, by (4), OSR $= M$, which was 512 in our circuit. In this converter, the main notch can be selected as either $f_n = 50$ Hz or 60 Hz for line noise suppression (or $f_n = 55$ Hz for simultaneous rejection). As discussed earlier, the circuit requires $4 \cdot \text{OSR} = 2048$ clock periods for converting an input sample.

One of the key specifications for the design is related to the differential input-signal range, which must extend from $-V_{\text{ref}}$ to $+V_{\text{ref}}$. Thus, to prevent the overloading of the delta-sigma loop, the input signal needs to be attenuated by a suitable factor. Since the IDC (unlike most conventional delta-sigma ADCs)

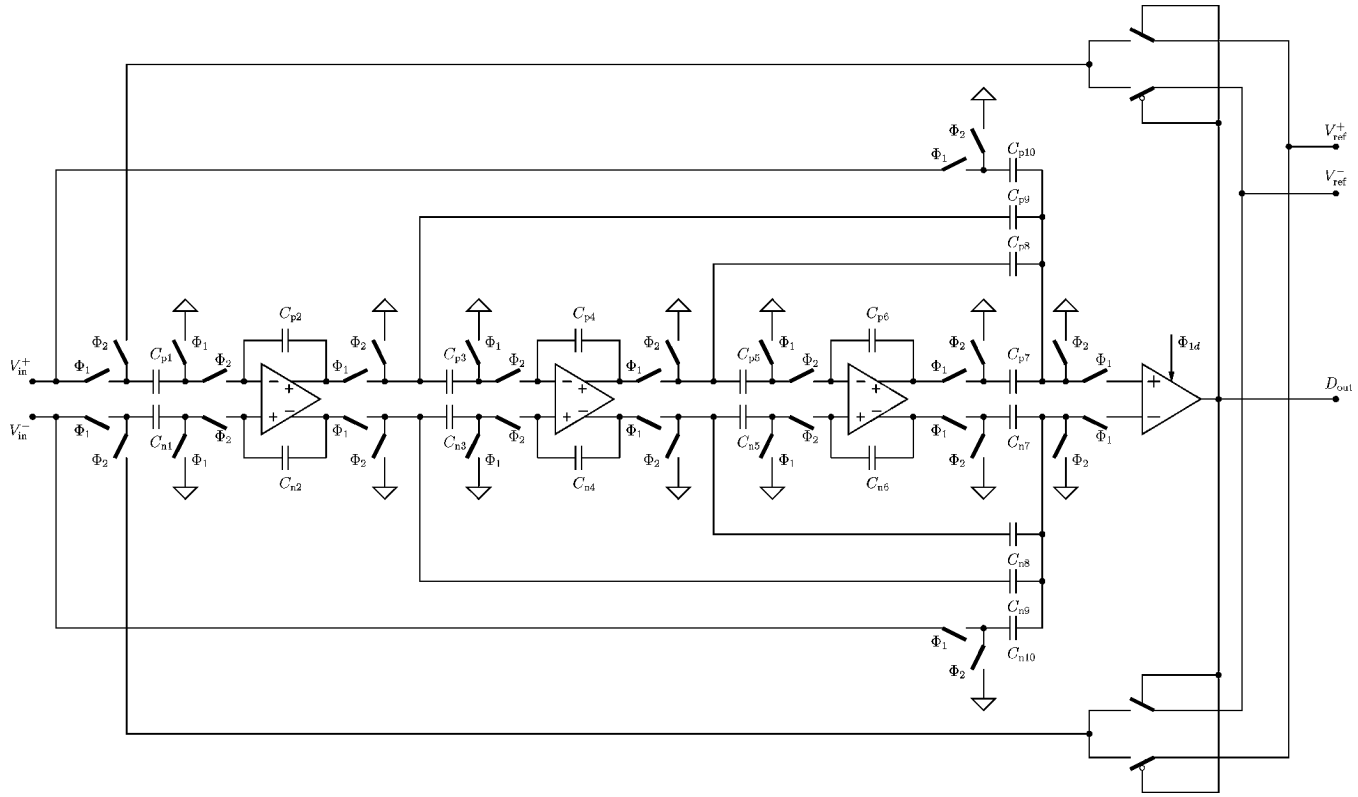

Fig. 3. Simplified schematic diagram of the delta-sigma loop.

must provide accurate gain along with high linearity, the gain reduction must be realized by a circuit which is insensitive to the inaccuracy of its components. The actual circuit, used as the first integrator in the delta-sigma loop, is illustrated in Fig. 4, along with its clock waveforms. In a full clock period, all three capacitors in each input branch deliver a charge proportional to the DAC voltage $V_{\rm dac}$, but only two deliver a charge proportional to $V_{\rm in}$. The differential input charge delivered to the integrating capacitors is then given by

$$Q_{\rm in} = C_{\rm in}\left(\frac{2}{3}V_{\rm in} - V_{dac}\right). \tag{5}$$

Hence, this circuit provides a scaling factor of 2/3, which can be later compensated in the digital domain, to restore the validity of the digital output.[2] The role of the three capacitors is rotated in every clock period, thus converting the effects of mismatch errors from a gain error into an out-of-band periodic noise.

This "rotating capacitor" scheme was shown to limit the gain error to a few ppm (U.S. patent pending.) It is also possible to introduce any rational scale factor n/m (with $m > n$) by using m capacitors in each input branch in the manner described. However, for some values of n and m, the resulting periodic noise may not be out of band. In addition, if the total number of samples is not an integer multiple of m, a small gain error will remain. Although the described implementation does not satisfy this condition (i.e., $N = 2048$ is not an integer multiple of 3), it uses a sufficiently large number of samples, thus making the residual error negligible.

IV. Offset Correction

The inherent offset of the delta-sigma loop must be corrected with a very high accuracy, so that the residual offset is less than 10 μV. This cannot be achieved using chopper stabilization, which is only effective for a first-order loop. Also, correlated double sampling would have required an extra clock phase in this application. Hence, the offset correction used in this device was a generalized version of chopper stabilization, which we named "fractal sequencing" [9]. The fractal sequence contains only $+1$ or -1 elements. A -1 in the sequence represents an inversion in the propagation path of the DC offset, while a $+1$ indicates no inversion. The signal is always integrated without any inversion. The first-order fractal sequence S_1 is simply an alternation $+1, -1, +1, -1, \ldots$, which can be represented by the symbol $(+-)$ for convenience.[3] The second-order sequence is then $S_2 = ((+-)(-+))$, and the third-order one is $((+--+)(-++-))$. In general, an $(m+1)$st order sequence S_{m+1} is obtained from an mth-order one S_m by concatenating S_m and its complement $\overline{S_m}$ in which $+$ and $-$ are interchanged. It can be proven that by determining the offset propagation polarities in a cascade of m integrators according to sequence S_m, the offsets at the outputs of all integrators will be cancelled after the N clock periods needed for the conversion, if $N/2^m$ is

[2]Since the original stability range at the input of the modulator is slightly larger than 2/3 of the full-scale range, this scaling factor also offers overrange capability for the converter, a useful feature for closed-loop applications with large input signals. Simulations predicted that a second-order loop would only marginally meet the 20-bit requirements for the oversampling ratio of 512.

[3]This is the sequence used in the conventional chopper stabilization technique.

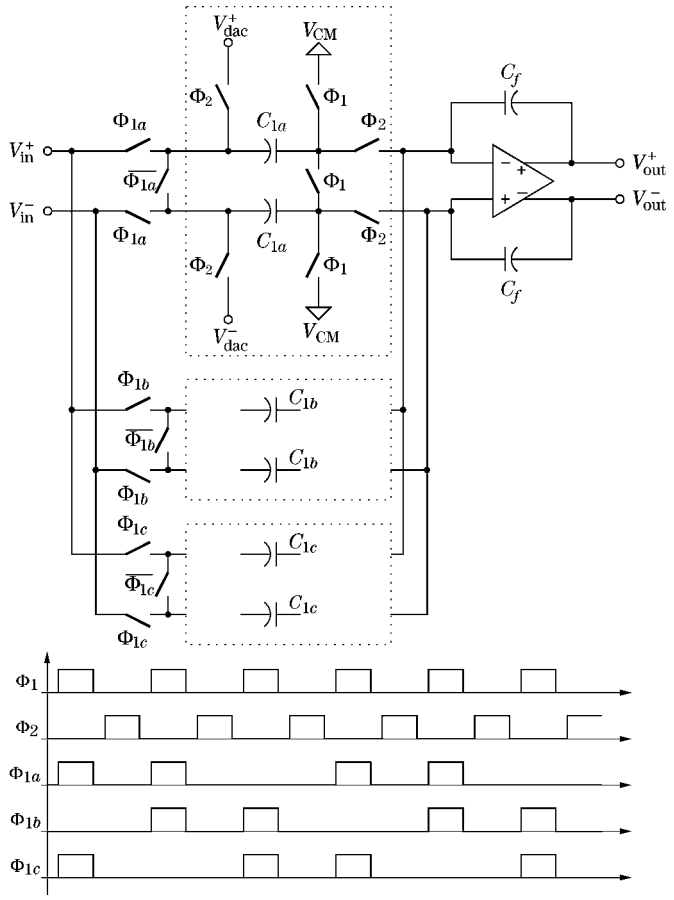

Fig. 4. Gain control stage. The dotted boxes containing C_{1b} and C_{1c} are replicas of the box containing C_{1a}.

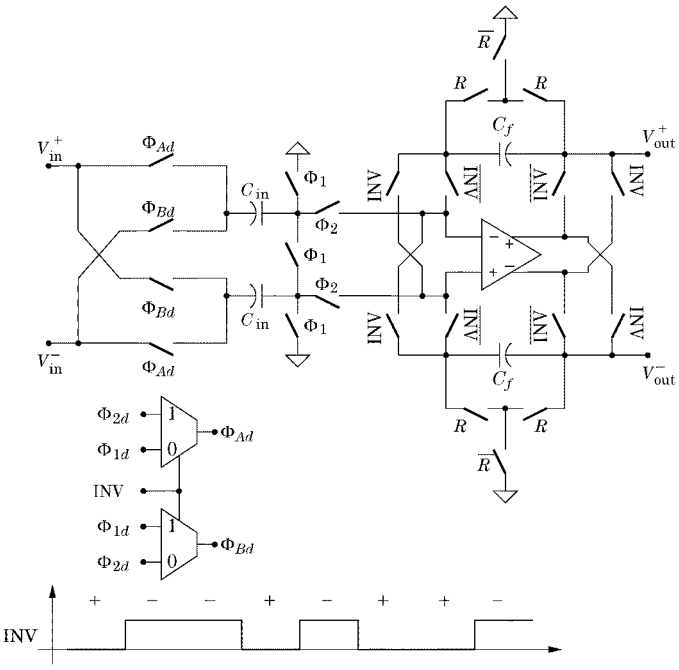

Fig. 5. Switched-capacitor integrator with signal inversion and reset switches. Subscript d indicates delayed clock phases.

an integer. (Appendix A discusses the properties of fractal sequencing in more detail.) Fig. 5 illustrates how the inversions

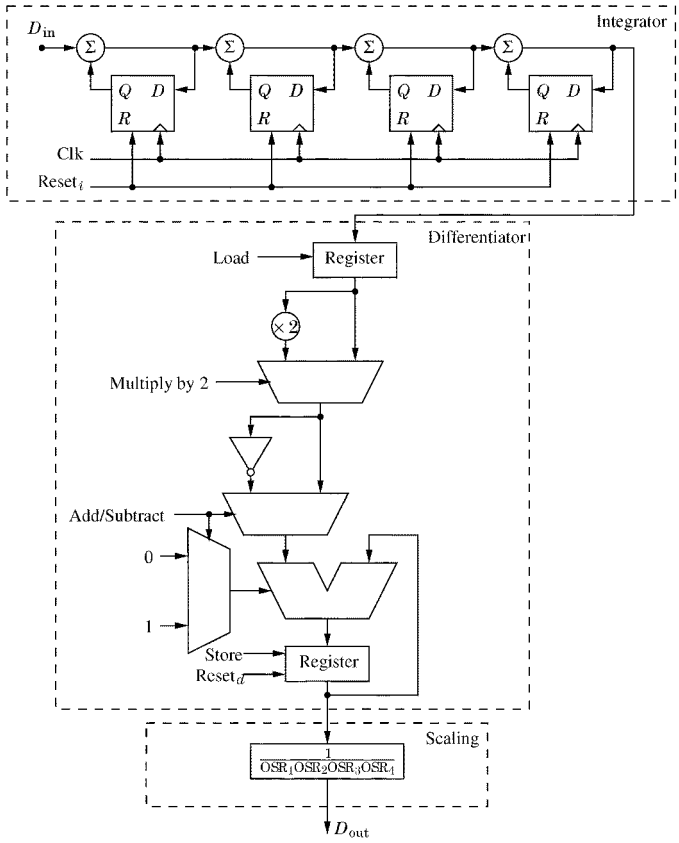

Fig. 6. Block diagram of the digital post filter.

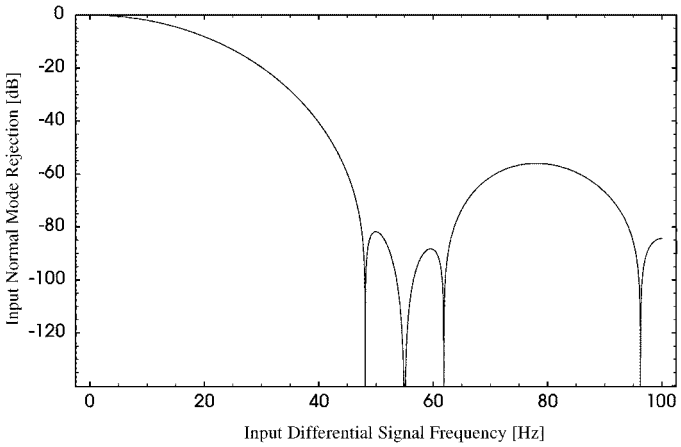

Fig. 7. Gain response of the narrowband digital filter.

in the offset path can be carried out in a differential integrator by swapping the polarities of the input and output opamp terminals whenever the logic signal INV (controlled by S_m) is high. To keep the signal flow unchanged, the nonoverlapping phases Φ_{Ad} and Φ_{Bd} of the four input switches are also interchanged when INV is high. The figure also shows the switches (operated by phase R) required for resetting the circuit after the Nth period.

In this device, the third-order fractal sequence S_3 was used, with each polarity held for 64 clock periods between inversions. The resulting $8 \cdot 64 = 512$ element pattern was repeated four times during the 2048 clock periods of operation.

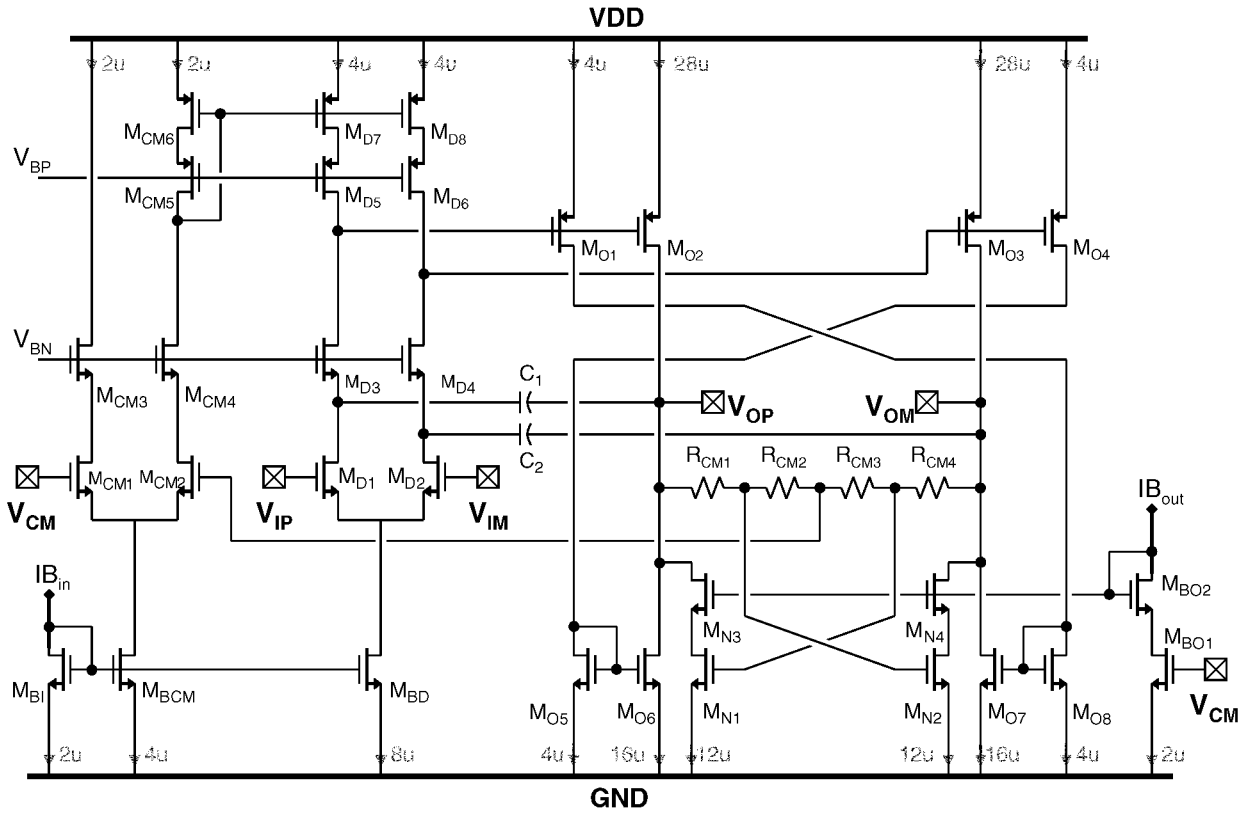

Fig. 8. Opamp circuit diagram. The annotated currents are for the first integrator.

V. Digital Filter

The fourth-order digital sinc filter used in the chip uses multiple staggered zeros around each notch frequency, to allow for drift in the clock rate or the line frequency. It has a modified transfer function including the staggered zeros, and uses a novel implementation [8] which differs from the familiar Hogenauer structure [7]. In this implementation, the four cascaded differentiators needed in the Hogenauer scheme are replaced by a programmable counter (which selects the location of the zeros) and by a simple adder. These perform the differentiation operations. Thus, with very little added complexity, the filter can be programmed to offer different line frequency rejection schemes using, e.g., narrow notches with high rejection, or wide notches with lower rejection. The block diagram of the filter is shown in Fig. 6. Appendix B discusses the details of the filter implementation. Fig. 7 shows the gain response of the filter programmed for simultaneous rejection of both 50 and 60 Hz tones.

VI. Implementation and Measurement Results

In the following, the design details of the implemented device will be discussed. To satisfy the stringent thermal noise requirements, the capacitors used in the input stage of the modulator loop were chosen to be 2.5 pF each. As described in Section III, the input gain-control stage uses two capacitors to sample the input signal and three capacitors for the DAC feedback signal, corresponding to a total of 5 and 7.5 pF, respectively. These capacitors were connected in an anti-parallel scheme in order to cancel their first-order voltage coefficients and to obtain better linearity.

The integrators were implemented with fully differential two-stage opamp topologies, with rail-to-rail output operation. Fig. 8 shows their transistor-level circuit diagram. Most of the DC gain was provided in the first stage by a telescopic cascode configuration (M_{D1} to M_{D8}), using nMOS input devices.

The common-mode feedback (CMFB) circuit operates in continuous time, using a resistive network (R_{CM1} to R_{CM4}) to generate the average of the outputs, and a simple error amplifier (M_{CM1} to M_{CM6}) to keep it near the common-mode voltage, $V_{CM} = V_{\rm DD}/2$. The resistive network causes a reduction in the load impedance of the second stage, thus degrading its differential gain. Larger resistor values would improve the gain but would reduce the speed of the CMFB loop. Therefore, the gain reduction was minimized by adding a negative conductance (formed by transistors M_{N1} to M_{N4}) in parallel with the resistors. The transistors M_{N1} and M_{N2} were designed to stay in the linear region over the full output voltage range.

Two-stage opamps need some form of compensation to maintain stability. The capacitors C_1 and C_2 are connected to the cascoded nodes of the input pair, in the Ahuja compensation style [10]. This allows for a good stability behavior while using smaller capacitance values than those needed by the conventional Miller compensation technique.

For design and layout simplicity, the same opamp configuration was used in all three integrator stages, but with different device sizes and bias currents to accomodate the different gain and bandwidth requirements. The opamp used in the first integrator (with the most stringent requirements) was designed to have a nominal DC gain of 140 dB and a unity-gain bandwidth

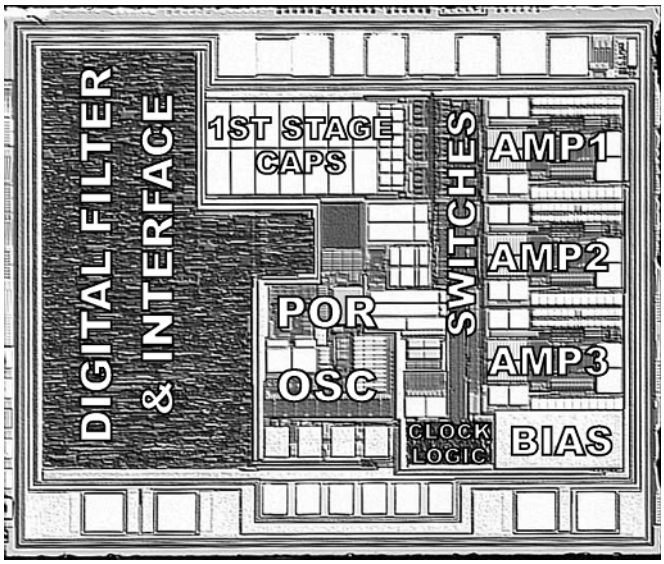

Fig. 9. Chip microphotograph. (POR: Power-On-Reset.)

of 3 MHz. To achieve this performance, the first opamp required only 76 μA of supply current at $V_{\rm DD} = 5$ V. For the second- and third-integrator stages, the opamps were designed for 120-dB DC gain and 1.5-MHz unity-gain bandwidth.

Three different versions of the complete ADC were implemented in a 0.6-μm CMOS technology. The first one has a slow maximum data rate (13.75 Hz), and includes a digital filter which rejects both 50 and 60 Hz with a wide multiple notch at 55 Hz. It has low output noise (0.25 ppm). The second chip also has a slow data rate (12.5 or 15 Hz), a main notch at either 50 or 60 Hz, with greater rejection (at least 120 dB within a 3% variation from the selected line frequency), and also low output noise (0.25 ppm). The third chip has a maximum data rate of 60 Hz, a notch at 240 Hz, and an elevated (0.8 ppm) output noise. These three versions differed in the oversampling ratios, and in the locations of the zeros implemented by the digital filter. As discussed in Section III, the modulator sampling frequency and the conversion time depend on the notch frequency. For the version with the 60-Hz notch and OSR $= 512$, the sampling frequency is 30.72 kHz, and the conversion time is 66.7 ms.

The chip photo is shown in Fig. 9. Note that there are double guard rings between the input capacitors and the digital section, which reduce the digital noise coupling into the sensitive input stage. The chip occupies an area of 1.59×1.31 mm^2. Typical measurement results are shown in Fig. 10 for the output noise, Fig. 11 for integral nonlinearity (illustrating the very small temperature coefficient), and Fig. 12 for the supply current. Figs. 13 and 14 show the distributions of the offset and gain errors, respectively, obtained from measurements performed on 50 parts at different temperatures. As Fig. 13 illustrates, the offset is typically around 2 μV. This is consistent with the 22-bit resolution. As a comparison, some chopper-stabilized instrumentation amplifiers achieved 0.2 μV input-referred offset voltage [11]. However, chopper-stabilized delta-sigma ADCs have typically much higher offset values (ranging from 10 μV in [12] to 1.5 mV in [13]). The measured performance is summarized in Table I.

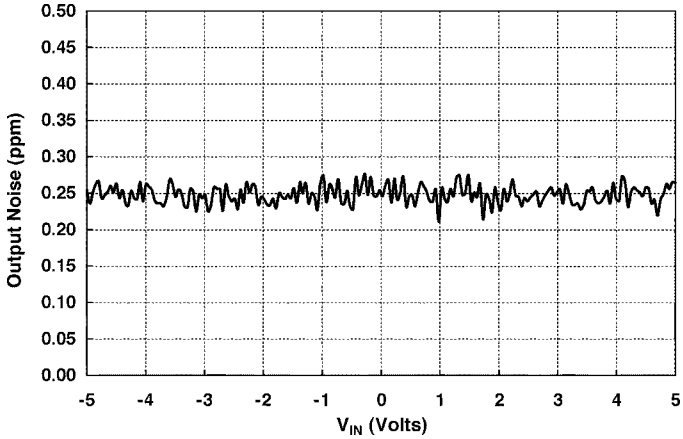

Fig. 10. Measured output noise versus input signal voltage.

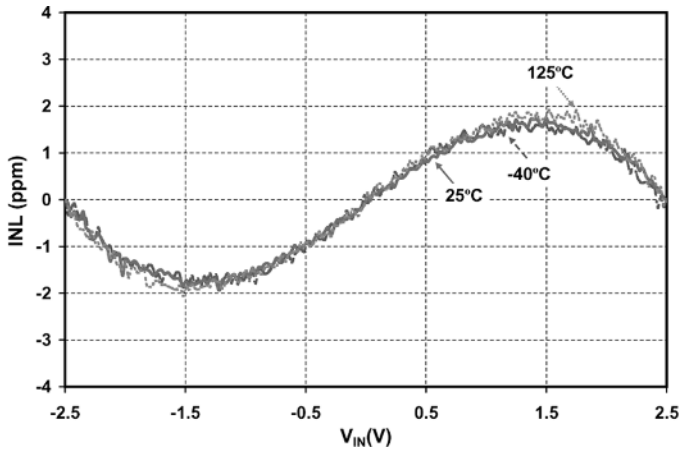

Fig. 11. Measured integral nonlinearity.

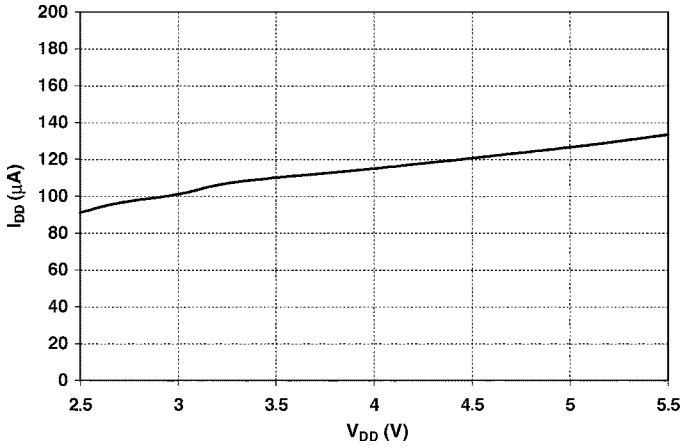

Fig. 12. Measured supply current.

It is of interest to compare the performance of the device described above with that of the second-order MASH IDC discussed in [3]. The IDC of [3] was a 15-bit ADC which did not reject line frequency. The conversion time was 10 ms, the power consumption of the analog part 0.325 mW. The ADC presented here has a 22-bit resolution, and provides line-frequency rejection. A conversion requires about 67 ms, the power consumption (total) is 0.6 mW. The earlier chip consumed 3.25 μJ energy per

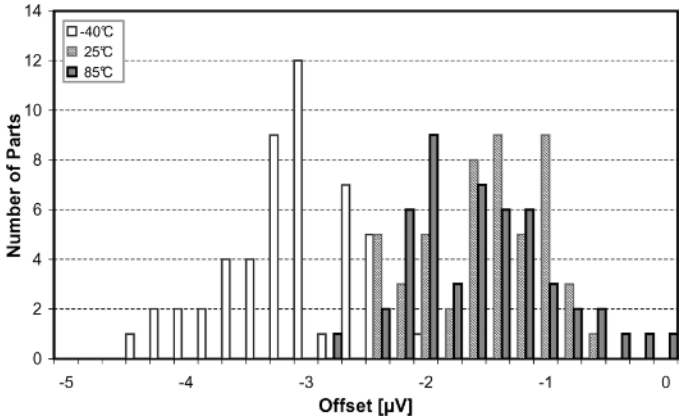

Fig. 13. Offset distribution versus temperature (50 parts).

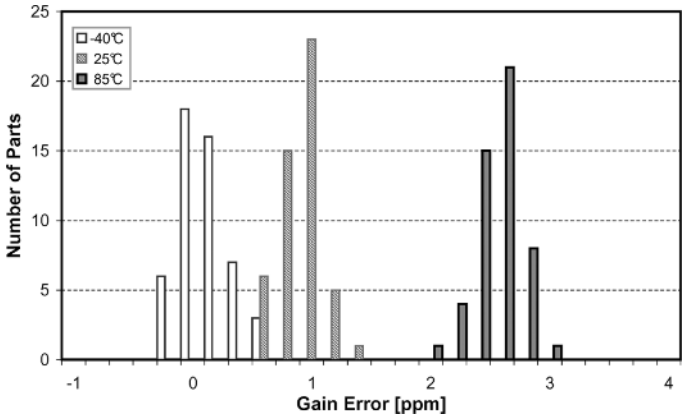

Fig. 14. Gain error distribution versus temperature (50 parts).

TABLE I
SUMMARY OF THE MEASURED PERFORMANCE OF THE INCREMENTAL ADC

Parameter	Performance
Conversion time	
typ.	66.7 ms
DC offset	
typ.	2 μV (1.7 LSB)
max.	10 μV (8.4 LSB)
Gain Error†	
typ.	2 ppm (8 LSB)
max.	10 ppm (40 LSB)
INL†	
$V_{\rm ref} = 2.5$ V	max. 4 ppm (16 LSB)
$V_{\rm ref} = 5$ V	max. 10 ppm (40 LSB)
Supply Current	
Shutdown mode	max. 1 μA
Op. mode $V_{\rm DD} = 5$ V	typ. 120 μA
Op. mode $V_{\rm DD} = 3$ V	typ. 100 μA
CMRR‡ @ 50/60 Hz	at least 135 dB
DC PSRR‡	
$V_{\rm DD} = 2.5 \sim 6$ V	at least 120 dB
Output Noise†	
$V_{\rm ref} = 5$ V	0.25 ppm (2.5 $\mu V_{\rm RMS}$, or 1 LSB)
$V_{\rm ref} = 2.5$ V	0.48 ppm (2.4 $\mu V_{\rm RMS}$, or 2 LSB)
Oscillator frequency variation over $V_{\rm DD}$ and temperature range	$\pm 0.5\%$

† ppm of $2V_{\rm ref}$. 1 ppm = 4 LSB
‡ $V_{\rm in}^+ = V_{\rm in}^- = V_{\rm ref}/2$

conversion, the new one 40 μJ. The energy per LSB is 32.5 pJ for the earlier device, and 20 pJ for the present one. One important difference between the two devices is the offset compensation method. The IDC of [3] used a simpler scheme based on the subtraction of offsets from two half conversions. The resulting offset was 12.5 μV, while the fractal compensation scheme used in the present chip reduces the offset to 2 μV.

VII. CONCLUSION

The theory, design and implementation of a high-accuracy incremental data converter was described. The converter incorporates several novel algorithms and circuit techniques for signal scaling, offset correction and digital filter implementation. The measured performance confirmed a very low offset and noise, as well as an accurately controlled gain, combined with a low power drain. Hence, the converter is suitable for many high-precision instrumentation and measurement applications.

APPENDIX A
FRACTAL SEQUENCING FOR OFFSET CORRECTION

Consider a cascade of m sampled-data integrators, such as those used in the loop filter of a delta-sigma or incremental ADC. An offset voltage $V_{\rm off}$ at the input terminal of the first integrator will be accumulated in the circuit, and cause large errors. Correlated double sampling may be used to reduce this effect, but it usually requires the use of an additional clock phase, and it enhances thermal noise. Simple chopper stabilization is effective for a cascade of amplifiers, but will not work for cascaded integrators.

In the proposed correction technique [9], in clock period k the input offset is either inverted or not, according to a pre-programmed sequence $S_m(k)$, which we named a fractal sequence. The zero-order fractal sequence may be defined as $S_0(k) = 1, 1, \ldots$, which will be denoted by $S_0(k) = (+)$. The first-order fractal sequence is defined as $S_1(k) = 1, -1, 1, -1, \ldots$, and denoted by $S_1 = (+-)$. It causes $V_{\rm off}$ to be inverted in every second period. If the cascade contains a single unit-gain delay-free integrator $(m = 1)$, then using S_1 to control the inversion, and assuming $V_{\rm off} = 1$, the sequence of the integrator outputs $v_1(k)$ will be $1, 0, 1, 0, \ldots$. Hence, in every second clock period, when $k = 2^m$, the offset is cancelled.

However, if there are two cascaded integrators $(m = 2)$, and S_1 is again used to control the inversion process at the input of the first integrator I_1, then the output of I_2 will be $v_2(k) = 1, 1, 2, 2, 3, 3, \ldots$. The offset now accumulates, and the output offset will never be zero. The solution is to note that after the second clock period $(k = 2)$ the first integrator output will be $v_1(2) = 0$, and the second integrator output $v_2(2) = 1$, the sum of $v_1(1)$ and $v_1(2)$. Hence, if the first integrator is fed during the next two clock periods with the inverted input samples -1, 0, then its outputs will be $v_1(3) = -1$ and $v_1(4) = 0$. Hence, the integrator output sequences will be

$$\begin{aligned} v_1(k) &= 1, 0, -1, 0, \ldots \\ v_2(k) &= 1, 1, 0, 0, \ldots \end{aligned} \tag{6}$$

Thus, after $k = 2^m = 4$ periods, $V_{\rm off}$ is cancelled in $v_2(k)$. Note that the inversion pattern which allows

this can be described by the second-order sequence $S_2(k) = 1,-1,-1,1,1,-1,-1,1,\ldots$ which can be abbreviated as $S_2(k) = ((+-)(-+)) = ((S_1)(\overline{S_1}))$. Here, $\overline{S_1}$ denotes the complement of S_1, i.e., $\overline{S_1} = -1,1,-1,1,\ldots$. Thus, the operation generating S_2 from S_1 involves the concatenation of S_1 and $\overline{S_1}$.

The argument presented for $m = 1$ and $m = 2$ can readily be generalized for the general case of m cascaded integrators as follows. If the inversion pattern of the input offset follows the mth-order sequence $S_m(k)$, then in the output $v_m(k)$ occuring during clock period $k = 2^m$ the offset will be cancelled. The cancellation will also occur after clock periods $k = 2 \cdot 2^m$, $3 \cdot 2^m$, etc. Hence, after any clock period which is an integer multiple of 2^m, the integrated offset will be zero.

The appropriate inversion sequence S_m may be obtained iteratively from

$$\begin{aligned} S_0 &= (+) \\ S_1 &= (+-) = \left((S_0)(\overline{S_0})\right) \\ S_2 &= ((+-)(-+)) = \left((S_1)(\overline{S_1})\right) \\ S_3 &= ((+--+)(-++-)) = \left((S_2)(\overline{S_2})\right) \\ &\cdots \\ S_m &= \left((S_{m-1})(\overline{S_{m-1}})\right). \end{aligned} \tag{7}$$

The name fractal sequence reflects this construction of the more complex sequences from simpler ones.

Note that fractal sequencing can be considered as a generalization of the chopper stabilization process, which uses S_1 only. Also, as in chopper stabilization, fractal sequencing reduces $1/f$ noise as well, by high-pass filtering it.

The periods of sequence S_0 generating the higher order ones S_m need not be restricted to a single number (1 or -1), as illustrated above. If S_0 has a period of duration L_0, it can be proven that the offsets at the outputs of all integrators is cancelled after $2^m \cdot L_0$ clock periods. As an example, for $m = 3$ and $L_0 = 4$, one can use

$$\begin{aligned} S_0 &= (++-+) \\ S_1 &= ((++-+)(--+-)) = \left((S_0)(\overline{S_0})\right) \\ S_2 &= ((++-+--+-)(--+-++-+)) \\ &= \left((S_1)(\overline{S_1})\right) \\ S_3 &= ((++-+--+---+-++-+) \\ &\quad \times(--+-+++-+++-+--+-)) \\ &= \left((S_2)(\overline{S_2})\right). \end{aligned} \tag{8}$$

In practice, maintaining a constant polarity during S_0 (e.g., $++++$) simplifies the design.

In our design, $L_0 = 64$ was used, and m was 3. Hence, the period of S_3 was $L_3 = 8 \cdot 64 = 512$. This pattern was repeated four times, to fill the 2048 clock periods of operation.

Appendix B
Efficient Digital Notch Filter Structure

The goal was to realize a high-rejection decimation filter with wider notches than those of the sinc filter, while keeping the advantages of modularity, low power and low complexity. These constraints were satisfied with slight modifications to the overall transfer function, by employing staggered zeros, resulting in wider but also less deep notches. The following transfer function is derived from the sinc filter equation:

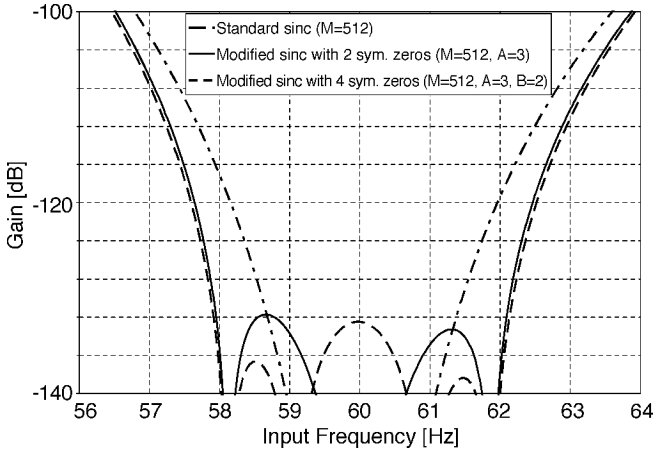

Fig. 15. Filter rejection for three different implementations around the main notch at 60 Hz.

$$H(z) = \prod_{k=1}^{L} \left(\frac{1 - z^{-M_k}}{M_k(1 - z^{-1})} \right). \tag{9}$$

This transfer function can be considered as a product of sinc filter transfer functions with different oversampling ratios (defined by the different M_k factors). The different M_k factors in the transfer function create side-notches in the frequency response which widen the main notch. If the M_k factors are sufficiently close, the rejection level is maintained and the notches are wider (see Fig. 15). The flexibility on the M_k factors can also be used for other purposes such as having simultaneous rejection at 50 Hz and 60 Hz (Fig. 7).

The integrator block is unchanged from the classical sinc filter, but the differentiator is different and it includes scaling that occurs at the end of each conversion so that the number of operations per conversion is minimal. The transfer function of the new Lth order differentiator is

$$H_d(z) = \prod_{k=1}^{L} (1 - z^{-M_k}). \tag{10}$$

In a simple sinc filter, the downsampling operation preceding the differentiator is done by a sample-and-hold circuit. Here, this is replaced by a programmable counter with different triggers. We can rewrite the differentiator transfer function in a more convenient form by developing the product into a sum of negative powers of z:

$$H_d(z) = 1 - \sum_{k=1}^{L} z^{-M_k} + \ldots + (-1)^L \cdot z^{-\left(\sum_{k=1}^{L} M_k\right)}. \tag{11}$$

In this sum, each term is a power of z^{-1} (delay) between 1 and the sum of the M_k factors. The programmable counter gives a way to realize these different delays and is followed by an ac-

cumulator doing the summation. Additional logic is needed to realize the sign and coefficients in the summation, and to calculate the delays given by the sum of M_k factors. The values of the delays are stored in a register which triggers the counter, and is loaded with a new value when the counter is triggered (see Fig. 6). For a low-order filter, the logic introduced is minimal, and the area saving is substantial, because there is only one adder regardless of the filter order.

The scaling is done after the differentiator, as shown in Fig. 6. Its function is to multiply the transfer function by a factor

$$H_s(z) = \frac{1}{\prod_{k=1}^{L} M_k} \tag{12}$$

insuring that DC signals have 0-dB gain. In this form, the scaling operation would require a full divider, with unacceptably high area and power consumption. This problem can be avoided by rewriting the M_k factors in terms of their differences from the oversampling ratio M, i.e., $M_k = M - x_k$. Hence, (12) can be rewritten as

$$H_s(z) = \frac{1}{\prod_{k=1}^{L} (M - x_k)} = \frac{1}{M^L \prod_{k=1}^{L} \left(1 - \frac{x_k}{M}\right)}. \tag{13}$$

In order to have high rejection, we need to have the M_k factors near each other (so $x_k \ll M$). The transfer function can then be expanded as a Taylor series, limited to the Lth order term for the desired accuracy. However, this expansion includes many terms and products which makes its realization impractical. The complexity can be reduced by applying restrictions on the x_k terms. Making them pair-wise symmetrical (for example $x_1 = -x_2$) reduces the number of terms by half. If the filter order is odd, one of the x_k terms is set to zero to satisfy this symmetry rule. Another practical restriction on the x_k terms is to allow them to be powers of 2 only. The x_k terms could then be $0, 1, -1, 2, -2, 4, -4, \ldots$. All products of x_k terms then become shift operations in a register, which are simple to implement. With these considerations, the scaling block is implemented simply with an adder and a shift register. Since the scaling only occurs once per conversion, this block consumes very little power.

In the present circuit, a fourth-order modified sinc filter was implemented with the transfer function

$$H(z) = \frac{(1 - z^{-M_1})(1 - z^{-M_2})(1 - z^{-M_3})(1 - z^{-M_4})}{M_1 M_2 M_3 M_4 (1 - z^{-1})^4}. \tag{14}$$

We had to find the factors M_1 to M_4 to determine our transfer function. Applying the above restrictions on x_1 to x_4 provides different possibilities such as: $M = 512$; $x_1 = 2^A$; $x_2 = -2^A$; $x_3 = 2^B$; $x_4 = -2^B$, where A and B are arbitrary integer numbers, or $M = 512$; $x_1 = 2^A$; $x_2 = -x_1 = -2^A$; $x_3 = 0$; $x_4 = 0$, where A is an arbitrary integer number. Fig. 15 compares the filter rejection using three different implementations. The operations done by the scaling block are much simplified when using the two symmetrical zeros. The series expansion of the scaling product becomes $1 + 2^{2(A-9)} + 2^{4(A-9)}$, which needs only two additions and two shifting operations. With four symmetrical zeros, the scaling function becomes $1+2^{2(-9+A)}+2^{4(-9+A)}+2^{4(-9+B)}+2^{2(-18+A+B)}$, which requires five additions with shifts. An implementation with wide notch rejecting both 50 Hz and 60 Hz is shown in Fig. 7, with two symmetrical zeros ($M = 512$, $A = 6$).

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