A low-power accelerometer IC with high sensitivity

Wang, Yan Mei

2015

A LOW-POWER ACCELEROMETER IC WITH

HIGH SENSITIVITY

WANG YAN MEI

SCHOOL OF ELECTRICAL AND ELECTRONIC

ENGINEERING

2015

A LOW-POWER ACCELEROMETER IC WITH HIGH SENSITIVITY

WANG YAN MEI

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2015

ACKNOWLEDGMENTS

strongest support and have always been the most encouraging motivation on my

study all these years.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Abstract

The objective of this project is to design a low-power, low-noise, highly-sensitive accelerometer ASIC interface using standard CMOS technology. The capacitive acceleration sensor is based on Micro-Electro-Mechanical Systems (MEMS) technology. For the targeted security applications, the bulk-micromachined accelerometer which has been developed by Temasek Laboratory@NTU, is employed as the sensing element to couple with the abovementioned ASIC readout circuit.

The auto-zero time-multiplexed differential technique is able to tolerate a number of circuit non-idealities. These include operational amplifier (op-amp) offset, offset thermal drift and switch errors of switched-capacitor (SC) circuits. The unique single-ended circuit architecture avoids the stringent requirement for component matching and eliminates the common-mode problem in conventional fully differential interface circuitry. Ultimately, it improves S/N ratio and cancels the common-mode errors in the sensing system with low power consumption.

For the implementation of the ASIC design to the intended accelerometer application, it involves several circuit building blocks. They are readout circuit, oscillator, differential-to-single-ended SC gain amplifier stage, passive RC filter and low-offset low-noise op-amp buffer.

A novel Auto-Zero Time-multiplexed Capacitance-to-Voltage Converter (AZTMD-CVC) is proposed for the readout circuit in this project. The circuit architecture achieves differential output performance whilst using only single-ended CVC topology. This approach eliminates the use of bulky full Wheatstone bridge sensing element in the MEMS sensor as required in

conventional fully differential sensor interface architecture, with additional benefit in reducing the fabrication cost of the MEMS sensor and readout circuit, as well as the power consumption. Besides, a low-power design strategy, pertaining to power versus noise in the readout circuit, is proposed. It permits the design to attain low noise without using excessive power consumption. This offers the optimal power-noise product in a form of figure-of-merit (FOM) on the AZTMD-CVC.

Two new oscillator circuits have been presented in this work. Both the oscillator designs offer clock signals with good temperature and supply variation immunity. The first oscillator design is a compact low-power CMOS ring oscillator with temperature and supply compensation whereas the second oscillator design deals with the relaxation oscillator using the tracking current comparator. The second design is adopted in this AZTMD-CVC circuit together with the silicon implementation for prototype testing. The key feature of the second oscillator is that of the temperature compensation without resorting to any external resistor component. The tracking current comparator based oscillator provides a 172 kHz clock for the interface circuit. This clock signal displays a 0.17% variation within the supply range from ±1.6V to ±2V whereas the mean temperature compensated coefficient for 5 samples of this oscillator frequency is around 0.018%/°C with a temperature range of -40 to 90°C. The power consumption of this oscillator circuit is only 4.2uA (21uW), demonstrating low-power consumption feature.

The accelerometer ASIC has been designed and implemented using the AMS 0.35μm CMOS 3.3/5V process technology. This accelerometer interface IC features both the offset and gain trimming which enable the IC to operate correctly even under the process variation of the fabricated MEMS capacitance

sensor. The prototype testing results have shown that the accelerometer readout system achieves a sensitivity of 1.95V/g. The system achieves a low noise level of -100 dBm/Hz, which corresponds to an equivalent acceleration noise of 1.16 $\mu g/\sqrt{Hz}$. The total power consumption including the clock generator is only 1.2 mW with ± 2.5V dual supplies. The measured in-run bias stability under 0g acceleration is 7.5 μg over around 3 hours' time. This is comparable with other reported highly-sensitive accelerometers. This measurement results have validated that the proposed design can meet low-power low-noise objectives with very high sensitivity. It outperforms the reported state-of-art works in performance comparison.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivations

Micro-Electro Mechanical System (MEMS) is an enabling technology that can integrate both mechanical components and small electrical/electronic devices onto the same silicon substrate using semiconductor wafer fabrication technology. After several decades' research and development effort, more and more miniaturized MEMS devices nowadays permits the realization at a lower cost, lower power consumption, much smaller package size and better stability. Micro-sensors and Micro-actuators, which are well-known in the transducers, are the most notable and well-developed elements among such a variety of MEMS functional products. In miniaturized micro-sensor system, the micromechanical device fabricated using micromachining process can sense physical signals like temperature, pressure, inertial forces, chemical species, magnetic fields, radiation and so forth. At the same time, the electronic circuits fabricated using CMOS process technologies provide the readout function for interface circuit designs and the control function for mechanical components. These micro-system devices have demonstrated in a wide range of commercial markets at a rapid rate due to their exceptional performance at low cost.

MEMS accelerometer is a kind of micro-sensor system that can sense the system acceleration onto which the sensing element is attached and convert the physical parameter to an electrical signal. Accelerometers can be integrated together with gyroscopes for angular rotation measurement. This is called the

inertial measurement unit (IMU) for the measurement of linear and angular acceleration, velocity and displacement. Accelerometers can also be used for vibration and shock measurement as well as the tilt and inclination measurements. They have been widely used in consumer electronics, automobile, industrial electronics as well as navigation and portable devices. An exemplary application is the area of automobiles in which accelerometers are used for crash detection to activate the deployment of airbags, active suspension and adaptive brake and anti-skiing application. Turning to industrial applications, accelerometers are employed in machine condition monitoring, such as the vibration monitoring for the prediction of operation condition of moving machine that helps to improve the machine stability and safety. Besides, the tilt and inclination measurements can be applied in robotics and instrumentation area. With the fast development of the micromachining process technologies, the cost of accelerometer goes down rapidly in view of the push from the market demand.

Through the research and development efforts over the past decades, a lot of sensing mechanisms have been developed and realized in MEMS based accelerometer devices. These mechanisms include the piezoresistive, capacitive, piezoelectric, electromagnetic, tunneling and so on. Among the choices of these various sensing techniques, the capacitive micro-accelerometers have the advantages of high sensitivity, low drift, low temperature dependence, low power consumption and good compatibility with IC process technology. These strengths ensure a big market for capacitive accelerometers. For precision applications like inertial grade navigation system, platform stabilization, low cost inertial measurement units (IMUs) as well as microgravity measurement systems [1], they push for the demand of μg level based micro-accelerometers. Some of these MEMS accelerometers are powered up by a battery or

incorporated with a large number of sensing interfaces, hence the power-aware concern becomes one of the design priorities.

Of the two main micromachining processes for MEMS accelerometers, the bulk micro-machined accelerometers [2]-[4] have higher sensitivity as well as lower mechanical thermal noise performance than that of the surface micro-machined counterpart [5]-[8] due to the inherent large seismic or proof mass in bulk micro-machined devices. The sensor device developed in this work is a bulk micro-machined capacitive sensing element which is based on a cantilever suspension structure. The out-of-plane sensing scheme results in a much higher capacitive sensitivity. However, higher parasitic capacitances of bulk micro-machined sensing devices will be unavoidable. They contribute to the noise issue in a form of high noise gain factor associated with the interface electronics. To circumvent the drawbacks, low-power low-noise circuit architecture, low-noise amplifier design and noise-power optimization become the design agenda.

Continuous-time chopper stabilization (CHS) [9], discrete-time switched-capacitor auto-zero (SC-AZ) and switched-capacitor correlated double sampling (SC-CDS) [10], [11] are well-known circuit design techniques suitable for capacitive sensing applications. CHS, SC-AZ and SC-CDS techniques can all effectively reduce the dc offset as well as the low frequency 1/f noise associated with the MOS devices in CMOS circuits. CHS has the advantage of a lower baseband noise level since it is not affected by the thermal noise folding effect which is always associated with SC sampling based circuits. Despite of the merit, the technique suffers from the residual offset [12] usually caused by the clock feed-through and charge injection in a form of spikes. For the application in MEMS sensors with large sensing and parasitic capacitances in form of large time constant formed together with the MOS switches, it tends

to have a larger mismatch effect. This gives rise to unavoidable big AC spikes to the sensitive input of chopper amplifier whilst displaying potential large dc offset as well as chopper ripple in the demodulation process that may deteriorate the CHS technical merit. Therefore, it is common to see that the CHS sensing interfaces [13]-[16], are mainly applied in small sensing elements using surface micro-machined mechanical sensors.

For an electronic interface dedicated to couple with a bulk micro-machined MEMS device involving large capacitances as well as large charging/discharging time constants, the SC sensing method is preferred because of its nature supporting fast charging/discharging on capacitances without significantly jeopardizing the front-end interface performance.

1.2 Objectives

The objectives of this work are to research, design and realization a highly-sensitive accelerometer ASIC dedicated to the security sensing system which is able to tolerate large parasitic capacitances from the sensing element whist addressing low noise performance metric in along with power-aware implementation. The scope of the research project is listed as follows:

1. To review and investigate of two main capacitive interface circuit techniques applicable for highly-sensitive accelerometers which are based on continuous-time chopper stabilization and discrete-time switched-capacitor approach.

2. To study the representative switched-capacitor interface circuits and identify the imperfections associated with the circuits together with their detailed analyses.

3. To investigate, design and analyze a new switched-capacitor front-end readout circuit that can be interfaced with a large parasitic based capacitive sensor whilst sustaining good performance metrics.

4. To design and realize the back-end electronic circuits that form the accelerometer ASIC with the proposed readout circuit.

5. To conduct the prototype testing of the accelerometer ASIC interfaced with the sensing element developed by Temasek Laboratory@NTU

1.3 Major Contributions of the Thesis

The major contributions of the research work are summarized as follows:

1. A novel Auto-Zero Time-multiplexed Capacitance-to-Voltage Converter (AZTMD-CVC) is proposed for the readout circuit in this project. The circuit architecture achieves differential output performance whilst using only single-ended CVC topology. This approach eliminates the use of bulky full Wheatstone bridge sensing element in the MEMS sensor as required in conventional fully differential sensor interface architecture, with additional benefit in reducing the fabrication cost of the MEMS sensor and readout circuit, as well as the power consumption.

2. A low-power design strategy, pertaining to power versus noise in the readout circuit, is proposed. It permits the design to attain low noise without using excessive power consumption. This offers the optimal power-noise product in a form of figure-of-merit (FOM) on the AZTMD-CVC.

3. Two new oscillator circuits have been presented in this work. Both the oscillator designs offer clock signals with good temperature and supply variation immunity. The first oscillator design is a compact low-power CMOS ring oscillator with temperature and supply compensation whereas the second oscillator design deals with the relaxation oscillator using the tracking current comparator. The second design, which offers significantly low power consumption, is adopted in this AZTMD-CVC circuit together with the silicon implementation for prototype testing.

4. The signal processing block is designed and integrated together with the proposed AZTMD-CVC to form the accelerometer ASIC.

1.4 Organization of the Thesis

This thesis comprises nine chapters. Following the introduction, Chapter 2 describes the micro-machining fabrication technology for capacitive MEMS accelerometer devices and the structure of bulk micro-machined sensor device developed in this research project. Behavioral model based on Verilog-A language is developed for the capacitive sensor in order to permit system-level simulation and verification whilst incorporating the transistor-level circuits.

Chapter 3 reviews two representative capacitive sensing methods: continuous-time chopper stabilization (CHS) scheme and discrete-time switched-capacitor (SC) sensing scheme with an in-depth study of the strength and weakness encountered in each scheme. This gives the rationale to the design of accelerometer ASIC using SC design approach. The fundamental switch error mechanism in SC circuit design is discussed. Three representative SC interface circuits are analyzed and discussed in details. These include additional

imperfect circuit effects such as 1/f noise, dc offset and finite gain of operational amplifier (op-amp).

Chapter 4 presents overall system architecture in conjunction with its core building blocks. They are the new AZTMD-CVC, the low-noise operational transconductance amplifier (OTA), the differential-to-single-ended amplifier and the on-chip low-noise buffer dedicated to form a signal-conditioning circuit with an external passive filter. Apart from the basic operation principle, the cancellation of the 1/f noise, dc offset, charge injection and clock feed-through effect are discussed in detail. The thermal noise effect, with particular emphasis in the presence of strong sensor parasitic capacitances, is analyzed to serve as the design basis for the low-noise low-power interface circuit. The noise-power optimization is given on how to obtain the optimal figure-of-merit (FOM) in terms of noise-power product on the AZTMD-CVC. Finally, the simulation study for comparison with the three interface circuits, as discussed in Chapter 3, is presented.

Chapter 5 presents the peripheral house-keeping circuitries that include the design and analysis of two integrated clock oscillators with emphasis on both temperature and supply variation compensation for sensor applications. The comparison with other reported counterparts are also given. Besides, another digital control logic module for multi-phase clock generator is also discussed.

Chapter 6 deals with the low-noise layout issues for mixed-signal sensor system. Several layout techniques for low noise consideration are discussed. These include cross-talk reduction between integration capacitors, guard rings for analog switches, sandwich shielding structure for critical analog input paths and power supply decoupling.

Chapter 7 presents the measurement results of the accelerometer ASIC, the integrated oscillator and the low-noise low-offset buffer. The performance of the AZTMD-CVC based accelerometer ASIC system is compared with other prior-art reported works.

Chapter 8 summarizes the concluding remarks of research work and discusses the future work of this project.

CHAPTER 2

CAPACITIVE MICROMECHANICAL ACCELEROMETER SENSOR

2.1 Silicon Based MEMS Micromachining Technologies

Micromachining is the process technology used to create micromechanical structures with the aid of etching techniques to remove part of the substrate or a thin film. Silicon, one of the nature's cheapest and most abundant elements, has long been exploited as the most commonly used material for semiconductor and IC manufacturing [17]. It is also the ideal substrate material for micro-machining of micro-mechanical devices due to its excellent mechanical properties in being ideally elastic, having small thermal expansion coefficient and good functioning stability over a wide temperature range. Hence, most of today's MEMS technology is based on silicon even though not restricted to.

The similar process technologies and compatible equipment used for IC manufacturing and micro-mechanical device development make it possible the monolithic integration of the micro-mechanical devices and electronic functional blocks on to the same silicon wafer or a single chip [18]. Processes like photolithography, growth, deposition and doping are the most basic micro-fabrication technologies commonly used in both micromachining and microelectronics fabrication. Photolithography is always combined with etching to pattern parts of a thin film or the bulk of a flat substrate to create specific shapes. Growth and deposition are methods to make structures in or on silicon with additional materials to achieve certain material properties or to shield the underlying parts under some specific fabrication process. Doping some certain

dopant ions into silicon can change the electrical properties of silicon. It can also change the mechanical properties such as etching rate and can achieve a well-defined stopping position during etching process. Wafer bonding and chemical mechanical polishing are also commonly used techniques in MEMS device fabrication as well as IC packaging and assembly. However, despite these fundamental process technologies in common, specific micro-fabrication processes must be developed for the mechanical device and microelectronics in order to ensure a successful design and development of a monolithic MEMS system, which may need multi-disciplinary efforts and approaches.

Bulk-micromachining and surface-micromachining are the two main well-explored micro-fabrication process techniques in the development of the silicon based micromachining technologies [19]. In bulk-micromachining, the structures are made in the silicon substrate by selectively removing material while surface-machining is to make small features above the silicon substrate through etching away layers deposited on top of it. The most important aspect for both of these two technologies is the etching of silicon. Among various etching methods, the most widely used techniques are wet-chemical etching and dry etching. Wet etching uses aqueous chemicals to etch away the wafer surface and can be classified into two categories based on the etching etchant's properties: isotropic wet-chemical etching and anisotropic wet-chemical etching. The isotropic silicon etchants have the same etching rates at all directions in the silicon crystal such that the silicon can be etched equally in all directions. Unlikely, the etching rates of anisotropic etchants depend on the crystal orientation and hence anisotropic etching is direction sensitive. The etchants for wet-etching are chosen on the basis of the desired etching rate and the level of anisotropy as well as selectivity required for specific task. An etch stop is adopted to define the required structure. Dry etching employs accelerated ions

or atoms for etching and the process is usually performed in a vacuum chamber under low pressure environment. It includes two techniques: vapor-phase and plasma-phase etching (RIE etching). Although both wet etching and dry etching or the combination of these two etching techniques are available for both bulk and surface micromachining, wet etching is predominantly used in bulk micromachining while dry etching is the primary choice for surface micromachining.

Both bulk micro-machining and surface-micromachining techniques have been widely used in the MEMS device fabrication, but there exists big differences in the two techniques' processing technologies. Hence, it results in considerable differences in the microstructures created. The most significant difference of the devices fabricated in the two technologies lies in the structure dimensions. The vertical dimensions of the bulk micro-machined device are determined by the thickness of the wafer used (typically 500-700 μm), while that of surface micro-machined counterpart is the thicknesses of the film deposited onto the substrate (around 1 μm). Similar difference is observed in the lateral dimensions. Bulk micromachining is usually used to create microstructures like trenches and holes. The bulk wet etching technique can quickly and uniformly etch a large wafer surface area which makes it less time-consuming and relatively low cost process. However, bulk micromachining using wet etching techniques has difficulties in monolithic integration with IC process technology: isotropic wet etching limits the line width resolution while anisotropic etchants is not compatible with the clean room service. Surface micromachining is widely applied in free-moving microstructures fabrications such as basic rotating structures that cannot be realized using bulk micromachining and shows better compatibility with microelectronics process. Unfortunately, surface micro-machined devices may encounter bigger process variations in

both mechanical and electrical properties since the device is using deposited structural and sacrificial layers. Therefore, both of these two micromachining technologies have their own advantages in different aspects. With their own unique process properties, each of these two technologies may dominate the other when involved in various application directions.

2.2 Micromechanical Accelerometer Sensors

A variety of MEMS functioning products have been developed and widely applied in various areas since the emergence of silicon based MEMS micromachining technology. Among them, the micro-sensor-system is the most successfully developed for a vast sales volume and it still embraces great growth potential in commercial markets in the coming years. Micromechanical accelerometer can sense the system acceleration and convert the external force to a physical signal being read by the electronic interface. Fig. 2.1 shows the simplified lumped element model of an accelerometer.
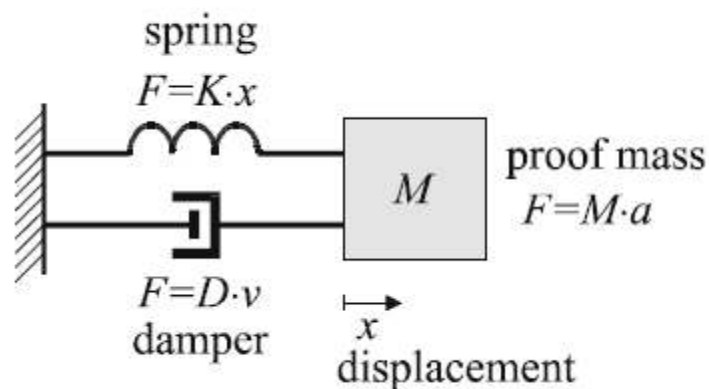
Fig. 2.1 Lumped element model of accelerometer

The accelerometer is a mass-spring-damper system which is composed of a proof mass, a frame and a suspension structure modeled as a spring and a

damper. When an external acceleration is exerted, the proof mass will exert an inertial force on the suspension structure and cause the deformation of the frame as well as the displacement of the mass relative to the fixed electrode. The resulting displacement of the proof mass can be expressed using differential equations as follows:

$$F_x = m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = ma \tag{2.1}$$

(2.1) can be transformed to s-domain as

$$\frac{X(s)}{F_x(s)} = \frac{1}{ms^2 + bs + k} \tag{2.2}$$

$$\frac{X(s)}{a(s)} = \frac{1}{s^2 + \dfrac{b}{m}s + \dfrac{k}{m}} \tag{2.3}$$

where m is the mass of the proof mass, b is the damping factor and k is the spring constant. The damper will also affect the motion of the proof mass. The squeeze film damping will occur when two plates are moving towards each other in parallel structures. When the plate is moving slow, the gas is squeezed out causing dissipation loss. When the plate moves fast, the gas will be compressed, leading to spring force. In order to reduce the damping caused viscous loss, the mechanical device is packaged under low pressure or vacuum condition. Brownian noise caused by the gas molecular motions around the proof mass limits the performance of the accelerometer device. By the laws of thermodynamics, the Brownian noise equivalent acceleration is calculated as [20]

$$BNEA = \sqrt{\frac{\overline{a_n^2}}{\Delta f}} = \frac{\sqrt{4k_B bT}}{m} = \sqrt{\frac{4k_B T\omega_r}{Qm}} \tag{2.4}$$

where Q is the quality factor, ω_r is the resonance-frequency of mass-spring-damper system. Hence, it is clearly from (2.4) that in order to achieve a low Brownian noise level, a large proof mass with high quality factor is required.

Accelerometers have been widely used in consumer electronics, automobile, industrial electronics as well as navigation and portable devices. For an exemplary application such as automobile, accelerometers can be utilized for crash detection to activate the deployment of airbags, active suspension and adaptive brake and anti-skiing application. Turning to industrial applications, accelerometers have found in machine condition monitoring, such as the vibration monitoring for the prediction of operation condition of moving machine that aims to improve the machine stability and safety. The tilt and inclination measurement can be used in robotics and instrumentation area. Basing on these applications, MEMS accelerometers are made to have a large range of performance specifications. Table 2.1 shows different performance specifications of accelerometers required for various application categories ranging from the low-cost automobile application to high accuracy navigation application.

Table 2.1 Specifications of accelerometers for different applications

Parameter	Automotive	Stability	Navigation
Range (g)	50-100	±1	1
Frequency range (Hz)	0-400	0-400	0-200
Resolution (mg)	<100	<10	<0.004
Maximum shock in 1 ms (g)	>2000	>2000	>20
Off axis sensitivity	<5%	<5%	<0.1%
Temperature range (°C)	-40-85	-40-85	-40-80
Temp. Co. of sensitivity (ppm/°C)	<900	<900	<50

2.3 Capacitive Micromechanical Accelerometer

Through the research and development efforts, a lot of sensing mechanisms have been developed and realized in MEMS based accelerometer devices. These mechanisms include the piezoresistive, capacitive, piezoelectric, electromagnetic, tunneling and so forth. Among various sensing techniques, capacitive micro-accelerometers have the key advantages of simple structure, high sensitivity, low drift, low temperature dependence, low power consumption and good compatibility with IC process technology. Capacitive accelerometers can offer more sensitivity levels and more resolution choices than similar piezoresistive counterparts. These strengths ensure an ever growing commercial market. The capacitive accelerometer products can cover the low-end application requirement of less than 1g sensing resolution up to the high-end accuracy application requirement of micro-g resolution. In recent years, high accuracy accelerometers with micro-g resolution have found many applications in high precision systems like inertial grade navigation system, platform stabilization, low cost inertial measurement units (IMUs) as well as microgravity measurement systems. As a result, they are in big demand.

2.3.1 Surface-Micromachined Capacitive Accelerometer

Both bulk micromachining and surface micromachining techniques have been successfully applied to capacitive micromechanical accelerometer sensor design and fabrication. Surface micro-machined accelerometer is formed by selectively etching the sacrificial layer deposited on the silicon substrate, which is typically around 1μm thick. Fig. 2.2 shows the basic surface micromachining process [21]. First, a sacrificial layer is deposited on the silicon substrate. This layer is then patterned using photolithographic and etching techniques. Subsequently, a

structural layer is deposited over the sacrificial layer. This layer will be shaped again using photolithographic and etching techniques. Finally, the sacrificial layer is removed from under the mechanical structures either through the side of the structure or the etch holes.
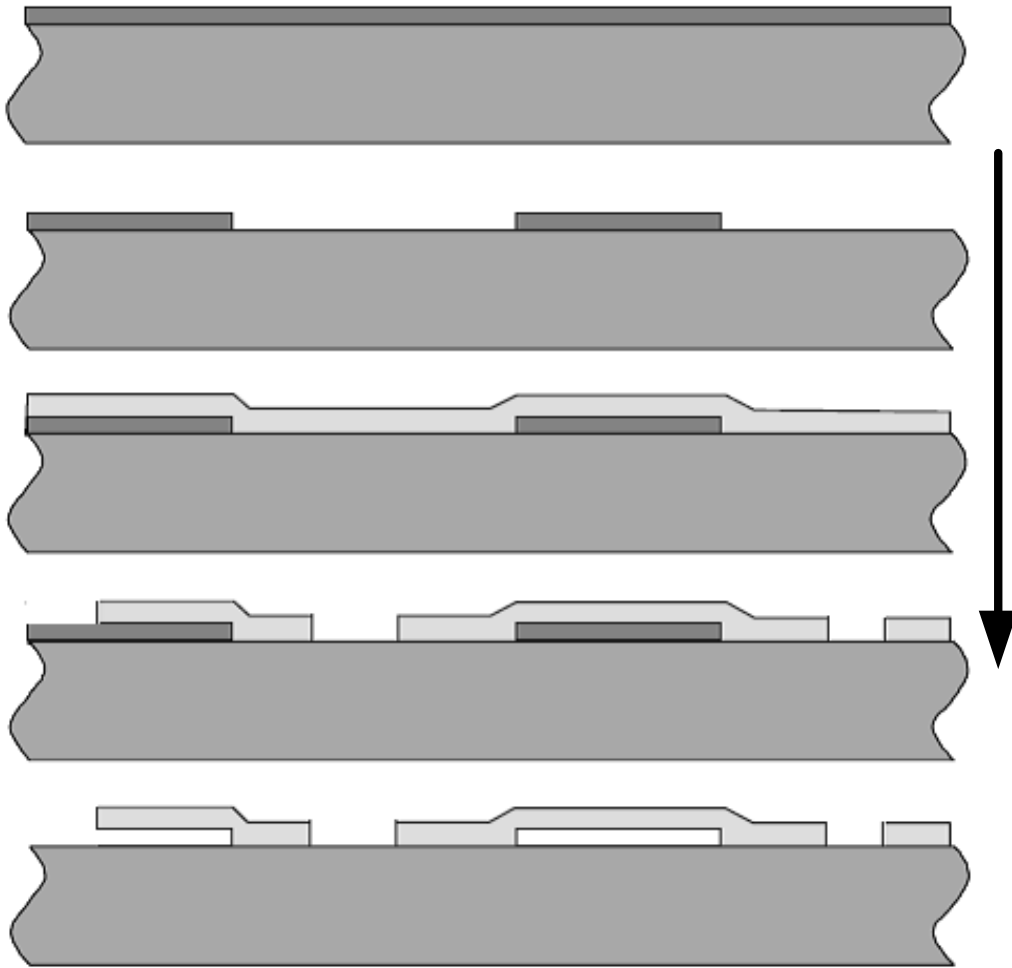
Fig. 2.2 Basic steps of surface micromachining processes

Surface micromachining lends itself well to lateral accelerometer structure fabrication. Fig. 2.3 shows the planar view of a lateral surface micromachined accelerometer and its membrane [19]. A number of moving fingers attached to

the proof mass and the fixed beams attached to the substrate form the comb structures.
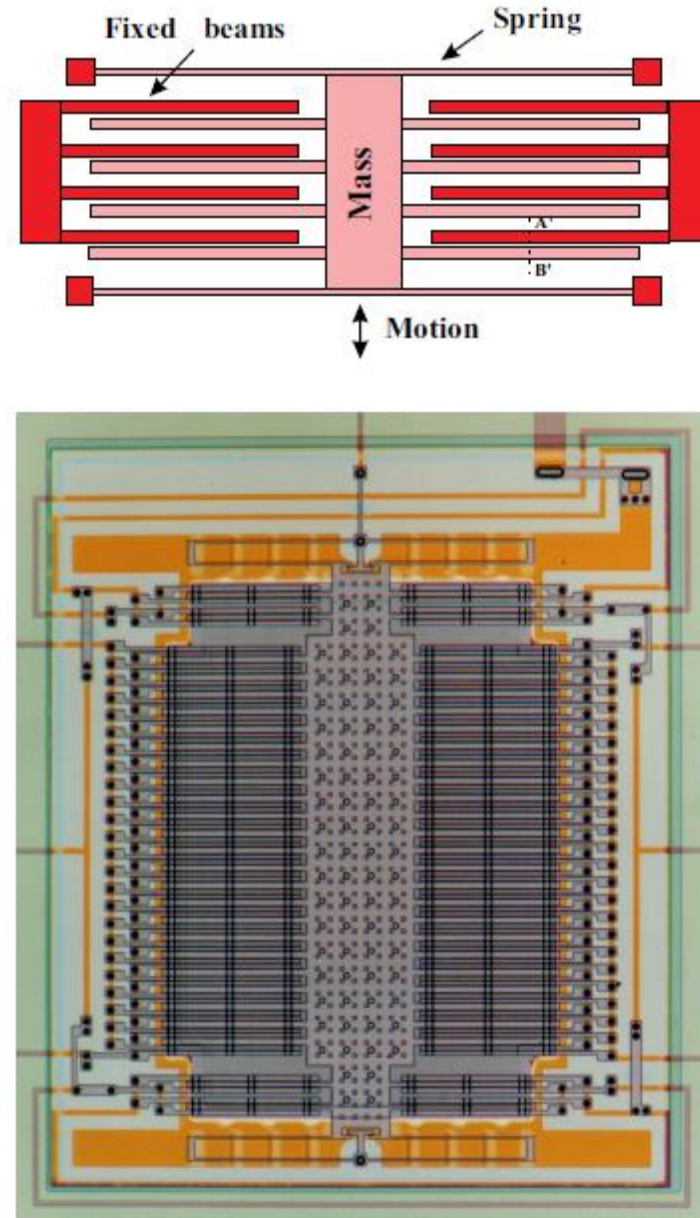
Fig. 2.3 Planar view of a lateral accelerometer device and its membrane layout

Since the mass of surface micromachined accelerometer is formed by the deposited sacrificial layer, the thickness of comb structures is only on the order of 1 to 2 μm. Except for the small sensing mass, under most cases, the motion of the proof mass in surface micromachined device is in the wafer plane. Hence,

the resulting nominal sensing capacitance as well as capacitive sensitivity are both small. Besides, the small mass weighing in a range of from 0.03 to 0.3 mg leads to a much higher mechanical noise as well as lower stability when compared to bulk micromachined devices. In order to increase the nominal capacitance as well as the capacitive sensing sensitivity, hundred finger pairs may be implemented in a lateral accelerometer device. Surface micromachining have also been applied to vertical accelerometer fabrication using double mechanical layer structures by Motorola [22]. Those vertical accelerometers typically have bigger sensing capacitance as well as capacitive signal than lateral structures. Typical surface micromachined accelerometers have noise floors varying from hundreds of $\mu g/\sqrt{Hz}$ to $mg/\sqrt{Hz}$ level [23].

2.3.2 Bulk-Micromachined Capacitive Accelerometer

Bulk micromachining techniques usually etch through the wafer from the back side to form the desired structures. Therefore, the whole wafer thickness can be utilized for seismic mass in bulk micromachined device. As such, the bulk micromachined accelerometers have much bigger device sizes than that of surface micromachined counterparts. The thick proof mass typically weighs in the range of from several mg to more than 10 mg. The large proof mass provides much larger capacitances and ensures significantly lower Brownian noise and higher stability for bulk micromachined accelerometer devices. Bulk micromachining process is well suited for vertical accelerometer fabrication. A typical bulk micromachined vertical accelerometer is illustrated in Fig. 2.4. This device is based on a 3-wafer structure assembled by low pressure silicon fusion bonding. In this structure, the top and bottom wafers create the damping needed to prevent excessive moving when an external acceleration approaching the resonant frequency is exerted. Besides, these two wafers also act as counter

electrodes while they provide shock protection for the sensor device at the same time. The proof mass of bulk micromachined accelerometers moves perpendicularly to the wafer plane, resulting in a much higher sensing sensitivity.
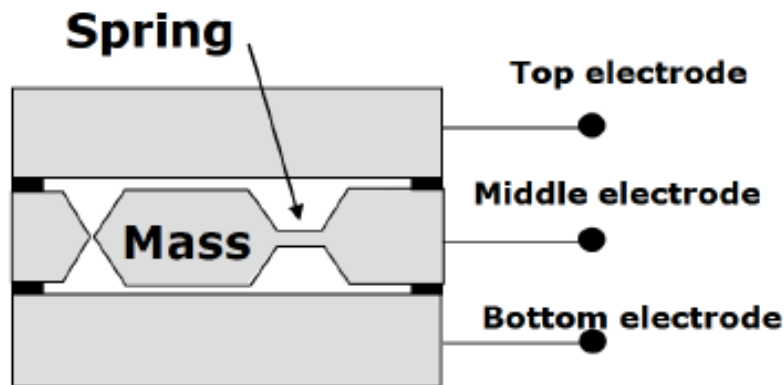
Fig. 2.4 Planar view of a typical bulk micromachined vertical accelerometer

2.4 Single-Beam Cantilever Suspension Structure

2.4.1 Sensor Structure and Fabrication Process

The micro-mechanical accelerometer device adopted in this research project is shown in Fig. 2.5. It is based on a single beam cantilever suspension structure which is fabricated using bulk micromachining process. The middle part of this sensor is a movable proof mass suspended by one cantilever beam at one end, while the top and bottom plates are fixed elements.
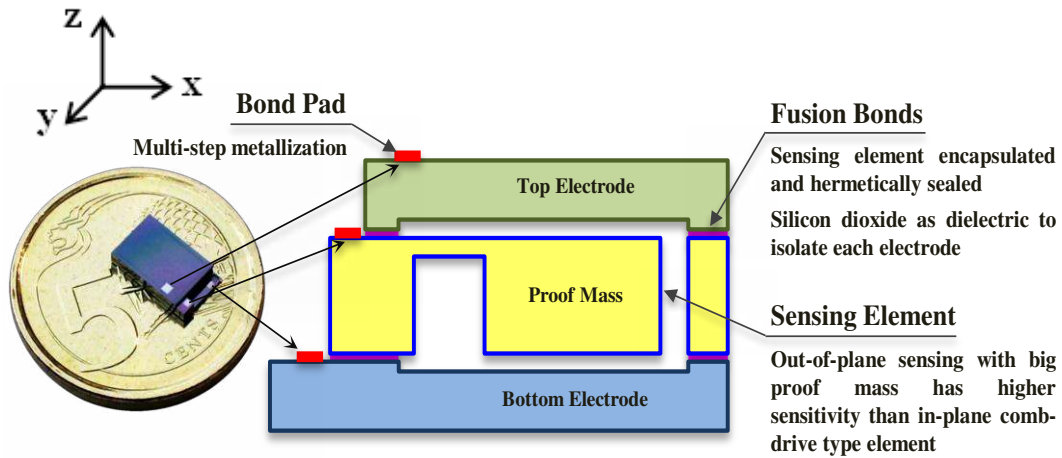
Fig. 2.5 Cross-sectional diagram of the bulk micro-machined accelerometer sensor

In this structure, the external acceleration perpendicular to the plane of the proof mass causes the proof mass to move in the z-direction, resulting in capacitance changes between the proof mass and two fixed conductive electrodes as illustrated in Fig. 2.6. Variable capacitors C_{1S} and C_{2S} represent the differential sensing capacitances while C_{1P} and C_{2P} are the parasitic capacitances consisting of bonding capacitances as well as stray capacitances contributed from the oxide insulator between two conducting electrodes.
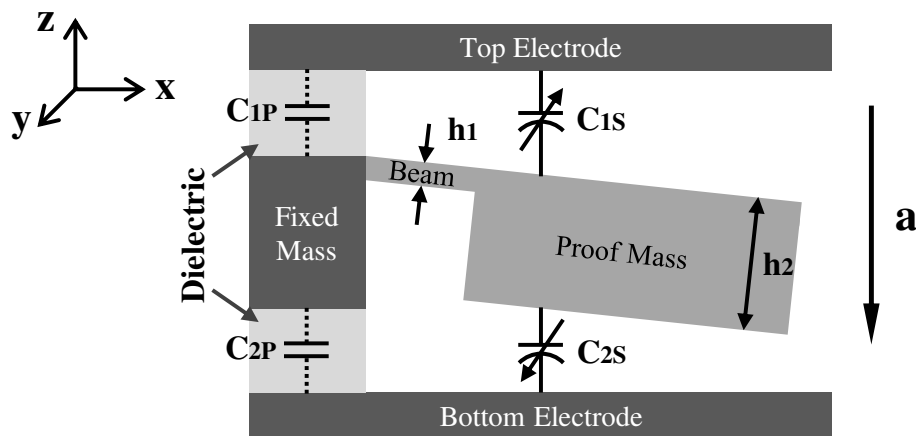
(a)
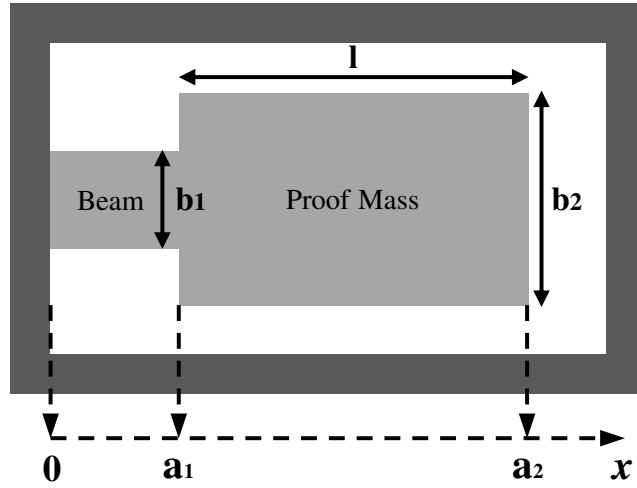
(b)

Fig. 2.6 Cross-sectional view (a) and top view (b) of the single beam cantilever structure

Under small deflections condition, the deflection of the proof mass end can be expressed as

$$w(a_2) = \frac{2ma}{Eb_1h_1^3}\left(15La_1 - 5a_1^2 - 12L^2\right)a_1 \tag{2.5}$$

where E is the modulus of elasticity for silicon ($1.7\times e^{11}$ Pa), a is the external acceleration, h_1 is the thickness of beam, b_1 is the width of the beam, a_1 is the length of beam, a_2 is the distance of the proof mass end from the frame and L is the distance of the proof mass center from the support. The sensing capacitance C_{1S} and C_{2S} can be estimated by integrating along the length of proof mass [24] as follows:

$$C_{1S} = \int_{a_1}^{a_2} \frac{\varepsilon\varepsilon_0 b_2}{d_0 + w(x)}dx \tag{2.6}$$

$$C_{2S} = \int_{a_1}^{a_2} \frac{\varepsilon\varepsilon_0 b_2}{d_0 - w(x)}dx \tag{2.7}$$

where d_0 is the nominal distance between the proof mass and the fixed

electrodes and b_2 is the width of the proof mass. Hence, the external acceleration is converted to the sensing capacitance changes which can be measured by the electronic front-end interface circuit. The out-of-plane sensing scheme significantly increases the capacitance sensitivity for bulk micro-machined device than any in-plane sensing scheme. High sensor sensing sensitivity is desired for low-noise sensor system [25]. Mechanical thermal noise caused by the Brownian motion of proof mass is another important factor that will limit the system noise performance. This can be reduced by increasing the mass of the movable electrode. Since the bulk micromachining process creates micro-mechanical structures through selectively etching a whole silicon wafer, the vertical dimensions of the created structures can be made of the typical wafer thickness of 500-700 μm. This makes the fabrication of large proof mass possible, which is critical to ensure a lower Brownian noise floor.

Referring to Fig. 2.5, the fabrication of the mechanical sensor device is based on three silicon wafers. The center wafer is made as the middle moving electrode whilst the upper and lower wafers are dry-released as the external fixed electrodes. These three wafers are fusion bonded together with an optimal gas damping and bandwidth control whilst at the same time allowing the sensing element to be encapsulated and hermetically sealed. Silicon dioxide is buried as the dielectric to isolate these three electrodes. Sensor bonding pad are made through multi-step metallization. The sensor device is wire bonded to a standard DIP package to mount together with the readout integrated circuit (IC) on the PC board for system integration. The specifications of the accelerometer IC targeted for security application are summarized in Table 2.2.

Table 2. 2 Specifications of Accelerometer IC

Parameter	Security (gravity tilting sense)
Range (g)	+/-1g
Frequency range (Hz)	0-300
Resolution (ug/√Hz)	<5μg/√Hz
Maximum shock in 1 ms (g)	10 g
Temperature range (ºC)	-40 to 90
Temp. Coeff. of sensitivity (ppm/ºC)	<50

2.4.2 Sensor Modeling in Verilog-AHDL

In order to perform circuit simulation for proper analysis and design of the sensor system composed of the accelerometer device and electronic interface block, a sensor model must be established. Sensor sensitivity, nominal sensing capacitances and parasitic capacitances are essential model parameters for a sensor model. Compared with those mixed-signal simulators with built-in mechanical-type models, the electrical sensor model is much easier to be implemented since the algorithm is efficient and compatible with electrical simulators [26]. This Section introduces the Verilog-AHDL based behavioral modeling for the single beam cantilever based accelerometer sensor device.

Under 0 g acceleration condition, the nominal capacitance value is characterized as follows:

$$C_{1S} = C_{2S} = \frac{\varepsilon_0 A_M}{d_0} \tag{2.8}$$

where A_M is the proof mass area. Figure 2.7 illustrates the movement of the proof mass under external force with the change of the gap distances between middle to top electrode and middle to bottom electrode respectively.
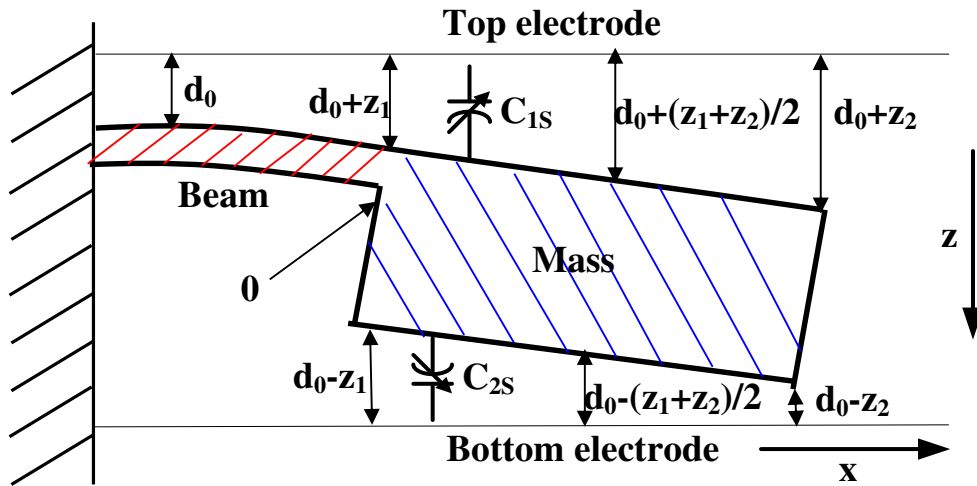
Fig. 2.7 Gap distance changes with proof mass movement under external acceleration

In a cantilever structure, the accelerated proof mass is tilting instead of moving parallel to the fixed electrodes. Hence, as depicted in Fig. 2.7, the displacement varies from z_1 to z_2 along the length of the proof mass. Under real conditions, both the movable proof mass and the beam will bend due to the exerted force. However, the displacement of the proof mass is thousand times of that of the cantilever beam [27]. Thus, the change of the beam capacitance can be deemed as negligible which means $z_1 \approx 0$. Hence, in the sensor modeling equation, only the deflection of the proof mass is considered. As discussed in the single beam cantilever structure, the exact equations (2.6) and (2.7) characterizing sensing capacitance under acceleration should be obtained through integrating methodology. However, the equations embedded with integration are too

complex to be described using Verilog-A language. Since the displacement along z axis is much smaller than the length of the proof mass along x axis. Hence, the variation of the gap distance along the proof mass can be deemed as linear, thus one can simply assume a constant displacement along the proof mass and use the displacement value z at the mid-point of the proof mass to represent the total capacitance change. Hence, the equations of sensing capacitance under external acceleration can be simplified as follows:

$$C_{1S} = \frac{\varepsilon_0 A_M}{d_0 + z} \tag{2.9}$$

$$C_{2S} = \frac{\varepsilon_0 A_M}{d_0 - z} \tag{2.10}$$

Based on the simulation results of the given bulk micromachined MEMS accelerometer, the maximum displacement at the tip of the proof mass under 1 g acceleration is around 0.483 µm or $z_2 = 0.483\ \mu m$. Thus, the displacement at the mid-point of the proof mass is $z_2/2$=0.2416 µm ($z_1 = 0$ µm) under 1g acceleration. Since the displacement is proportional to external acceleration, the average displacement z under an external acceleration α can be expressed as

$$z = 0.2416\alpha \tag{2.11}$$

Substitute (2.11) to (2.9) and (2.10) to characterize the relationship between the sensing capacitance and the external acceleration α (in g), we obtain

$$C_{1S} = \frac{\varepsilon_0 A_M}{d_0 + 0.2416\alpha} \tag{2.12}$$

$$C_{2S} = \frac{\varepsilon_0 A_M}{d_0 - 0.2416\alpha} \tag{2.13}$$

(2.12) and (2.13) can be described using Verilog-A language. Following is the introduction of the Verilog-A language.

Verilog-A language characterizes the behavior model of differential sensing capacitance structure and generates a sensor model symbol for the simulation [28]. The model description is summarized as follows:

- The Verilog-A module is a text file with code statements written in Verilog-A syntax.

- The text file describes the function of the Verilog-A module.

- The text file is saved as a Verilog-A view of the cell.

- A corresponding symbol view for the module will be generated and used as an instance in a schematic for simulation.

The major types of Verilog-A modules include:

- Behavioral models — The model is defined by mathematical descriptions relating output signal behavior to the input signals.

- Structural models — The model is defined by instantiation of components.

- Mixed structural and behavioral models— The model is defined by instantiation of the primitives and by mathematical descriptions relating output signal behavior to input signals.

The behavioral description is a mathematical mapping which relates the output signals of the module to input signals in terms of a large-signal or time-domain behavioral description. The mapping uses the Verilog-A language contribution operator "<+" which assigns an expression to a signal. The assigned expression can be linear, non-linear, algebraic and/or differential functions of the input

signals. These large-signal behavioral descriptions define the constitutive relationship of the module, and take the form of following:

output_signal <+ f (input_signal);

In signal contribution, the right-hand side expression, or f (input_signal), is evaluated, and its value is assigned to the output signal. The connection points of the module are defined by the port signal interface declarations.

For illustration of the large signal behavioral model, a simple charge-based model for capacitive component is introduced. As shown in Fig. 2.8, for a capacitive component with two connection nodes n_1 and n_2, the proper approach to build a large-signal behavior is to reconstruct q as a function of the capacitance C as well as the voltage $V(n_1, n_2)$ across it. It is also to make charge q as the right-hand signal to be evaluated while the current $I(n_1, n_2)$ is the output signal.
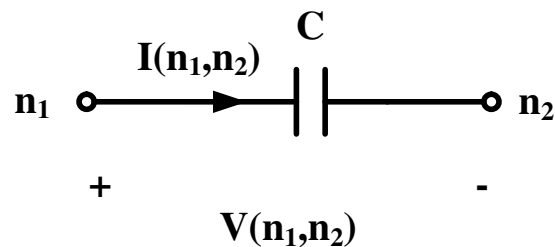
Fig. 2.8 Behavioral model of a two node capacitor

The current through a capacitor is the time derivative of the capacitance charge which is expressed as [29]

$$i(t) = \frac{dq(v(t))}{dt}$$
(2.14)

Hence, for the two node capacitor component shown in Fig. 2.8, one can write:

$$i_c = \frac{d}{dt}(C \cdot V(n_1, n_2)) \qquad (2.15)$$

Converting (2.15) to signal contribution form used in large-signal behavioral descriptions, it yields

$$I(n_1, n_2) < + ddt(C \cdot V(n_1, n_2)) \qquad (2.16)$$

where ddt() performs time-differentiation of its argument. The simplified electrical circuit model [30] for the bulk micro-machined sensor developed in this research project is shown in Fig. 2.9, which is consisted of the two differential sensing capacitors C_{1S} and C_{2S} as well as the parasitic capacitances C_{1P} and C_{2P} connected between node N_{o1}, N_{o2} and node N_{o3}, N_{o2} respectively. Node Na and Gnd belong to the input signal port. In this electrical sensor model, a variable voltage source is used to simulate the external acceleration signal. 1 V input voltage is treated equal to 1g acceleration in the model.
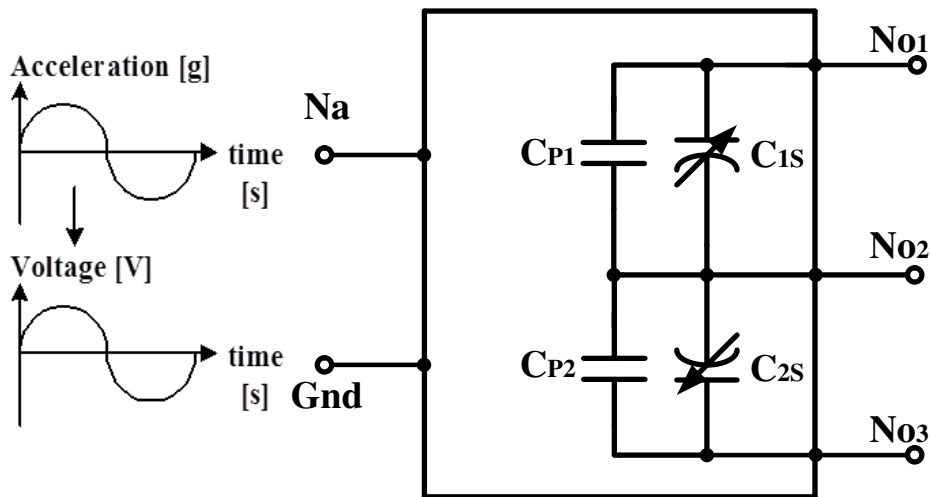
Fig. 2.9 Equivalent electrical circuit symbol for the accelerometer sensor device

Following is the Verilog-A text file of the large signal description of the electrical circuit model shown in Fig. 2.9.

VerilogA for sensormodeling, sensor model, veriloga

'include "constants.vams"

'include "disciplines.vams"

Module sensormodel(Na, No1, No2, No3, Gnd):   (Module interface declaration)

Inout Na, No1, No2, No3, Gnd; ──────────────►   (Port directions)

electrical Na, No1, No2, No3, Gnd; ──────────────►   (Port disciplines)

parameter real cp1=50p;

parameter real cp2=50p;

parameter real rnv=10T;

real V1, V2, q1, q2, Vin;

analog begin;

```
        V1=V(No1, No2);

        V2=V(No3, No2);

        Vin=V(Na, Gnd);

        q1=43.874e-12*v1/(4.5+0.2416*vin);

        I(No1, No2)<+ddt(q1);

        I(No1, No2)<+cp1*ddt(V(No1, No2));

        q2=43.874e-12*v2/(1.4-0.2416*vin);

         I(No3, No2)<+ddt(q2);

         I(No3, No2)<+cp2*ddt(V(No3, No2));

         I(Na, Gnd)<+V(Na, Gnd)/rnv;

    end

endmodule
```

Behavioral description of the sensing and the parasitic

2.4.3 Verification of the Sensor Model

The two expressions of q1 and q2 of the Verilog-A syntax are the equations describing the variable capacitance and capacitance sensitivity, respectively. Vin is used to model the physical acceleration and 1V represents 1g acceleration on the sensor device. Hence, it is easy to calculate the capacitance sensitivity using these two expressions. Under 1g acceleration, the capacitance change is calculated in the following:

$$\Delta C(N_{o2}, N_{o3}) = \frac{43.874}{4.5 + 0.2416} - \frac{43.874}{4.5} = -0.495\,pF \qquad (2.17)$$

$$\Delta C(N_{o1}, N_{o2}) = \frac{43.874}{1.4 - 0.2416} - \frac{43.874}{1.4} = 6.54\,pF \qquad (2.18)$$

In order to verify the correctness of the capacitance behavioral description based equation, a simple circuit setup shown in Fig. 2.10 is implemented incorporating the generated sensor symbol for the verification.
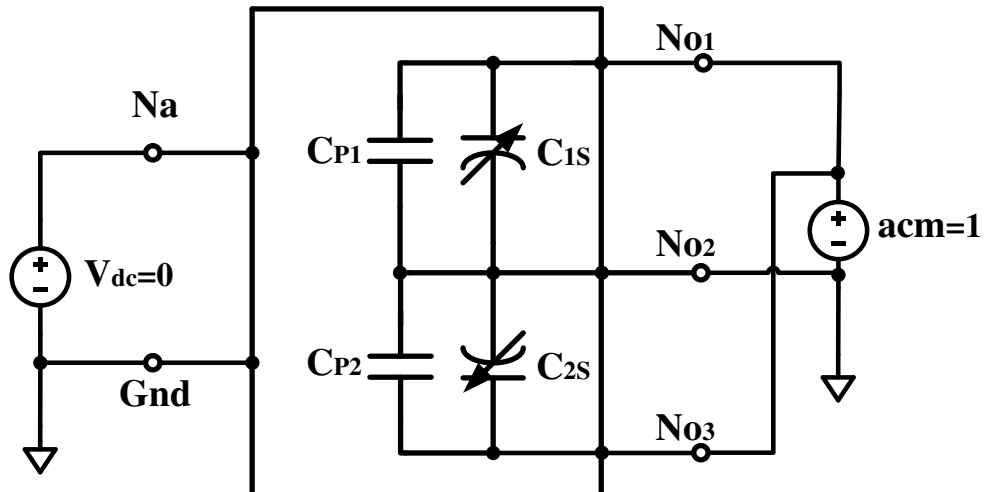
Fig. 2.10 Sensor model test circuit

- Driving the sensing capacitor with a voltage source with unity AC magnitude.

- Perform an AC analysis at $1000/2\pi$ Hz while sweeping the DC source voltage from -1V to 1V.

- Plot the current through the capacitor and change the units from Amperes to Farads.

The relationship between current, capacitance and the voltage across the capacitor is

$$I=\omega*C*V=2\pi f*C*V \tag{2.19}$$

According to (2.19), for $f=1000/2\pi$ Hz, V=1V, we will obtain C=I/1000, yielding $\Delta C=\Delta I/1000$. This means that one can get the capacitance sensitivity through measuring the current change between 0 and 1V voltage input (1V input represents 1 g acceleration). Fig. 2.11 shows the simulation result. Under 1V voltage change, the current change is 6.5nA and -0.5nA for the node N_{o1} and N_{o2} respectively. As a result, the capacitance change between N_{o1} and N_{o2} is 6.5/1000nF=6.5pF. On the other hand, the capacitance change between N_{o2} and N_{o3} is -0.5/1000nF=-0.5pF. This simulation result is close to the calculations according to (2.17) and (2.18). Therefore, it has verified the modeling equations.
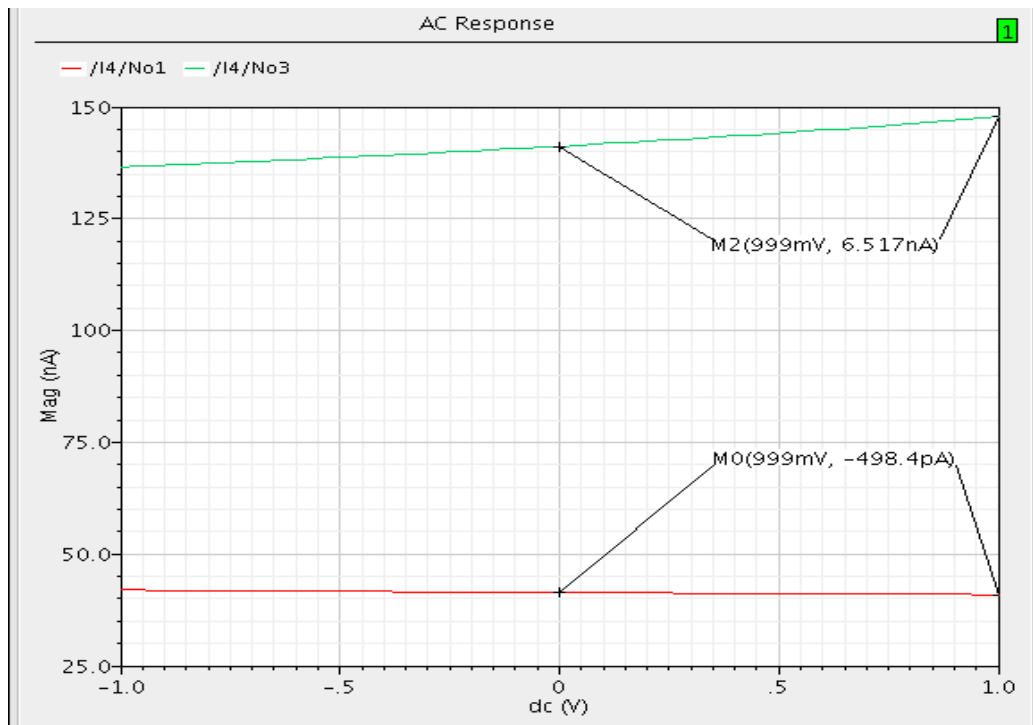
Fig. 2.11 The output ac currents of the two sensing nodes

The equation is a simplified first-order approximation of the cantilever sensor structure. In practice, the structure will suffer from higher-order nonlinear dependence between the acceleration and gap distance deflection. As such, there exists a certain error in the simplified model result. The percentage errors between the model capacitance sensitivity value and the ideal value at different levels of acceleration are listed in Table 2.3. The average percentage error for C_{1S} is 4.48% with a standard deviation of 0.04 whereas the average percentage error for C_{2S} is 3.58% with a standard deviation of 0.02. Since the percentage errors are reasonably small, the simplified model is adequate to predict the capacitance values for obtaining reasonable good accuracy.

Table 2.3 Percentage errors of the capacitance between the first-order model

and the ideal case at different acceleration levels

Acceleration (g)	Percentage error (%)	
	C_{1S}	C_{2S}
0	4.3961	3.5456
0.05	4.4084	3.5490
0.1	4.4201	3.5527
0.15	4.4312	3.5568
0.2	4.4416	3.5610
0.25	4.4515	3.5654
0.3	4.4606	3.5698
0.35	4.4692	3.5742
0.4	4.4771	3.5785
0.45	4.4844	3.5826
0.5	4.4910	3.5866
0.55	4.4970	3.5902
0.6	4.5023	3.5937
0.65	4.5070	3.5967
0.7	4.5111	3.5995
0.75	4.5146	3.6018
0.8	4.5174	3.6038
0.85	4.5196	3.6053
0.9	4.5211	3.6065
0.95	4.5221	3.6071
1	4.5224	3.6074

CHAPTER 3

CIRCUIT TECHNIQUES FOR CAPACITIVE ACCELEROMETER INTERFACE

3.1 Introduction

As discussed in the preceding Chapter, a capacitive micro-accelerometer system is composed of a mechanical sensor device and an electrical capacitance-to-voltage converter (CVC). The capacitance-to-voltage converter interfaced with the sensor device will convert the capacitance changes, caused by external forces exerted onto the micro-sensor system, to an electrical output for further signal processing. The electronic interface plays the most important role in determining the overall system performance such as the power consumption, sensing resolution, system noise level as well as linearity and distortion. For a high resolution microsystem, design considerations of the interface circuit are necessary to ensure a high quality system performance.

The electronic interface circuit techniques suitable for capacitive sensing can be roughly divided into the continuous time (CT) chopper stabilization (CHS) [31] sensing scheme and the discrete time (DT) auto zero (AZ) sensing scheme (or the switched-capacitor (SC) scheme) [32],[33]. Both schemes can be implemented in either open-loop architecture or closed-loop architecture in a system. A variety of highly-sensitive interface circuits had been reported in the literatures. In this Chapter, the CHS scheme and switched-capacitor correlated double sampling (SC-CDS) scheme as a special case of AZ technique will be firstly reviewed. Besides, the strength and weakness of each circuit technique

34

are discussed and compared. It is then followed by the detailed analysis and discussion on several recently published works on SC-CDS sensing scheme.

3.2 Review of Capacitive Sensing Interface Circuit Schemes

Sensor interface circuitry in CMOS technology always encounters the problems such as DC offset and the low frequency noise (flicker noise) introduced by the high gain amplification stage (op-amp). These will significantly hinder the final system sensing resolution. Both CHS and SC AZ sensing schemes can successfully resolve these issues. CHS is based on continuous time modulation technique while SC AZ technique is basically a discrete time sampling technique. In AZ technique, the unwanted low frequency errors will be sampled at one clock phase and automatically subtracted from the contaminated signal at the next working phase. Due to different cancellation approaches, AZ technique can be clarified into three categories: the open-loop offset cancellation (offset cancellation at the output), closed-loop offset cancellation (offset cancellation at input) and closed-loop auxiliary offset cancellation. CDS is an AZ technique which is quite suitable to be employed in the sample-and-hold process based SC circuitries. While both being able to suppress the DC offset and low frequency errors arising from the CMOS amplifier, each scheme has its own advantages as well as problems or pitfalls embedded within their implementations for different specific application cases. The following Sections will give a general introduction of both schemes' working principles. Moreover, the limitations and drawbacks associated with each technique are discussed to provide a better guide for a quality interface circuit design with different mechanical accelerometer sensor specifications.

3.2.1 Continuous-Time Chopper Stabilization Sensing Scheme

Chopper stabilization is a continuous time modulation and demodulation technique. It is widely adopted in sensor interface applications as well as low-offset low-drift instrumentation amplifier designs. The first vacuum tube chopper-stabilized op-amp was introduced by Edwin A. Goldberg in 1949. This technique significantly reduces the DC offset and offset drift. As such, a much higher amplifier gain is allowed. Since the development of the IC technology in 1960s, this technique continues to grow widely for low-offset low-drift instrumentation based designs as well as other analog signal processing circuits and systems for on-chip applications.

Fig. 3.1 shows the basic operation principle of the CHS scheme [31]. There are two ac signals denoted as $m_1(t)$ and $m_2(t)$ acting as modulating and demodulating carrier signals. In this process, the signal is modulated twice while the noise and offset are modulated only once. The input signal V_{in} will firstly be modulated to the odd harmonic frequencies of $m_1(t)$. After an amplification stage, the modulated signal as well as the error voltages, $V_{OS} + V_n$, in the amplification stage will be modulated by the second carrier signal $m_2(t)$. After this stage, the error voltage is modulated to the odd harmonic frequencies of $m_2(t)$ while the signal is demodulated back to the baseband. The combined modulated signal is then passed through a low-pass filter having the bandwidth slightly larger than the input signal bandwidth so that the noise and offset errors will be filtered out to give the quality and amplified sensor signal.
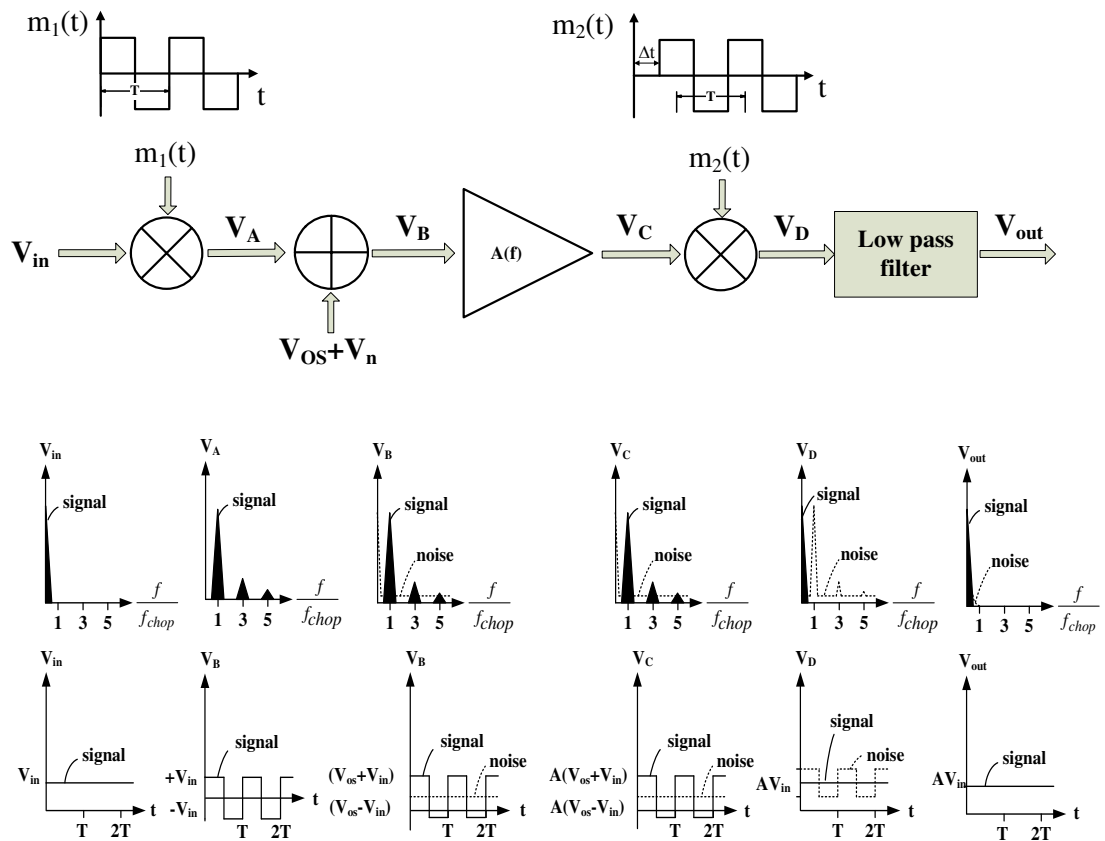
Fig. 3.1 Chopper-stabilization amplifier for reduction of noise and offset

A typical implementation of CHS based capacitive sensing scheme [13] is illustrated in Fig. 3.2. Capacitor C_{1S} and C_{2S} are the two differential sensing capacitors which will change under external acceleration forces at a relatively slow frequency. V_{m+} and V_{m-} are two out-of-phase high frequency square wave signals applied to the two sensing capacitors. The amplifier OA is the charge sensing amplifier and C_f is the feedback or charge integration capacitor. A large bias resistor R_{bias} (typically in the range of Mega ohms) is connected between the output and the negative input of the op-amp to define the dc voltage level at the input high impedance node. During the first modulation step of the chopper stabilization scheme, the low frequency changes in C_{1S} and C_{2S} are modulated by the carrier signals V_{m+} and V_{m-}. This is represented in the form of the sidebands and odd harmonics of the high frequency carrier signals at the input

37

of the sensing amplifier OA. The charge difference between the two sensing capacitors at the differential driving voltage of ($V_{m+} - V_{m-}$) will be integrated by the sensing amplifier OA, resulting in an amplitude modulated signal at the op-amp output. The modulated signal in conjunction with the dc offset as well as the 1/f noise of sensing amplifier OA will then be amplified by a gain stage. Subsequently, in the second step of the CHS scheme, the modulated signal will be demodulated back to the base band by a high frequency demodulating signal, while the dc offset and low-frequency 1/f noise will be modulated to high frequency bands. They will finally be attenuated through the low-pass filter to obtain the clean sensing signals.
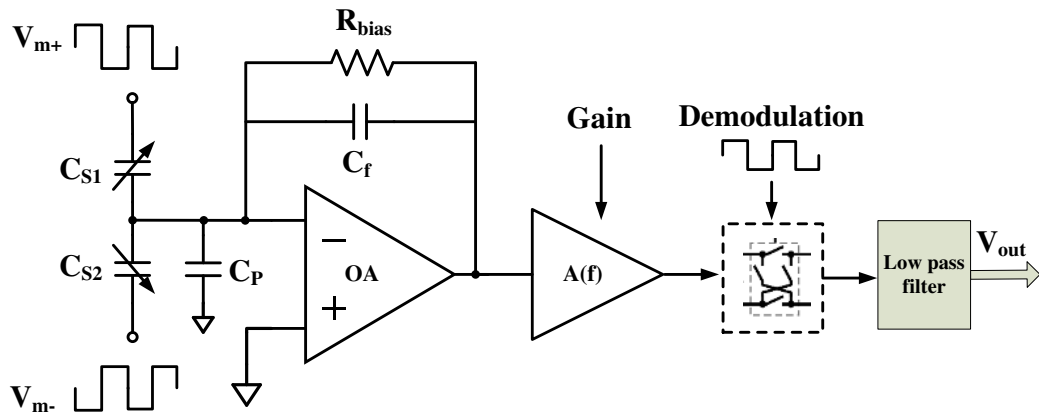
Fig. 3.2 Typical implementation of CHS capacitive sensing scheme [13]

Fig. 3.3 shows a fully differential trans-capacitance interface utilizing CT CHS technique [34]. The fully differential structure can effectively reject common-mode errors and provide better performance of linearity and power supply rejection ratio. This system is made up of a front-end CHS CVC followed by a variable gain amplifier (VGA) stage to provide additional gain for better system flexibility. To reduce the die area, three MOS transistors configured as back-to-back connected diodes are implemented in series as the large DC bias resistor. A driving voltage V_{drive} is applied to the sensing capacitors. When the sensing

capacitance starts to deviate from the nominal values due to external accelerations, an amount of charge proportional to the total capacitance changes and the amplitude of the driving voltage V_{drive} will be integrated by the CVC, thus resulting in an output voltage which is a function of the sensing capacitors. The transfer function of the first CVC stage is given in (3.1)

$$V_{out} = 2\Delta C_s \left(V_{drive} - V_{cm} \right) / C_{int} \tag{3.1}$$

After the second variable gain stage, the signal is demodulated to the baseband while the 1/f noise and DC offset are modulated to the harmonics of the chopper frequency which will be filtered out by the subsequent low pass filter.
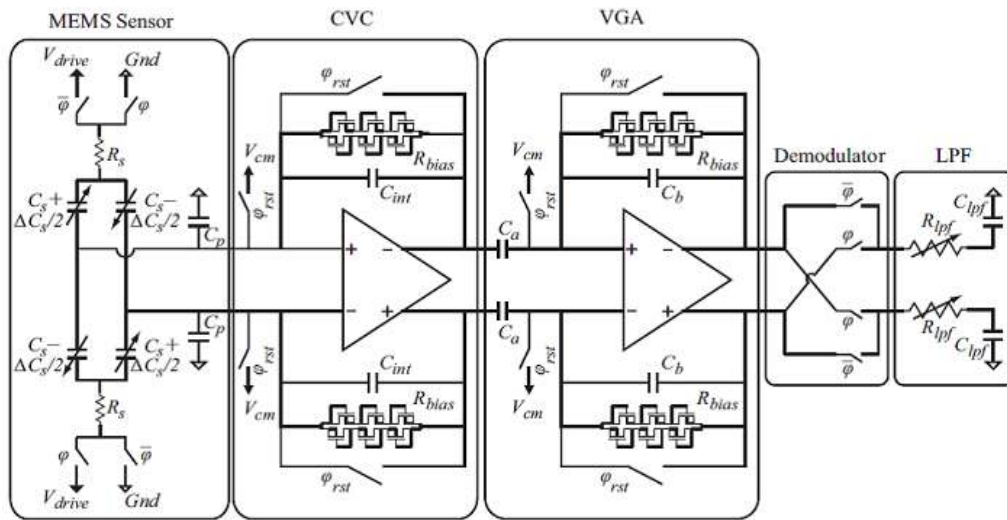
Fig. 3.3 A fully differential implementation of CHS sensing scheme

3.2.2 Discrete-Time Switched-Capacitor Correlated Double Sampling Scheme

CDS scheme as a special case of SC AZ technique is first introduced in charge couple device applications [35]. In CDS technique, the op-amp DC offset as well as the low frequency noise will be sampled twice during the two working phases of a whole clock cycle. Fig. 3.4 shows a simple single stage

implementation of the CDS technique. The op-amp offset error and the flicker noise are represented by two dc voltage sources connected to the positive input of the op-amp and are denoted as V_{OS} and V_n respectively.
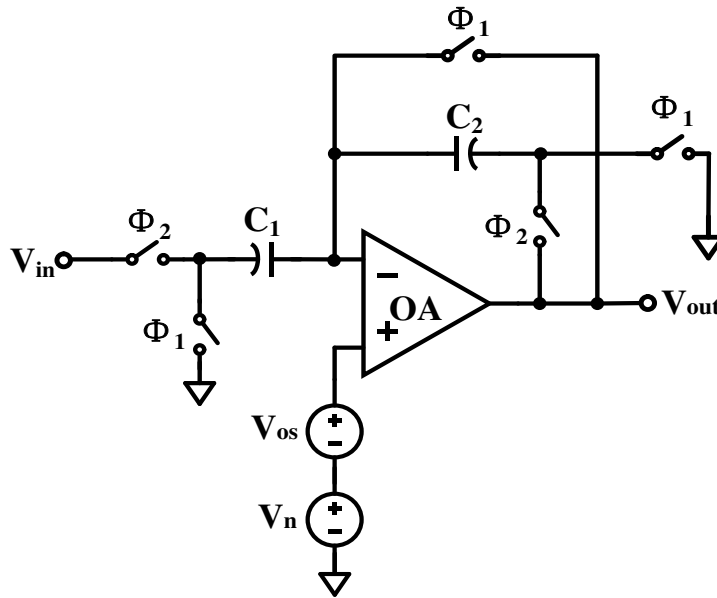
Fig. 3.4 SC circuit using CDS technique

The two working phases in this CDS circuit are: the reset phase (Φ_1) and the charge transfer phase (Φ_2). When Φ_1 phase is on, the op-amp as well as the capacitors C_1 and C_2 will be reset. The circuit during the reset phase is configured as shown in Fig. 3.5, capacitor C_1 and C_2 are both charged up to the error voltage of $V_{OS} + V_n$. This means that the error voltage is sampled by the capacitors once.
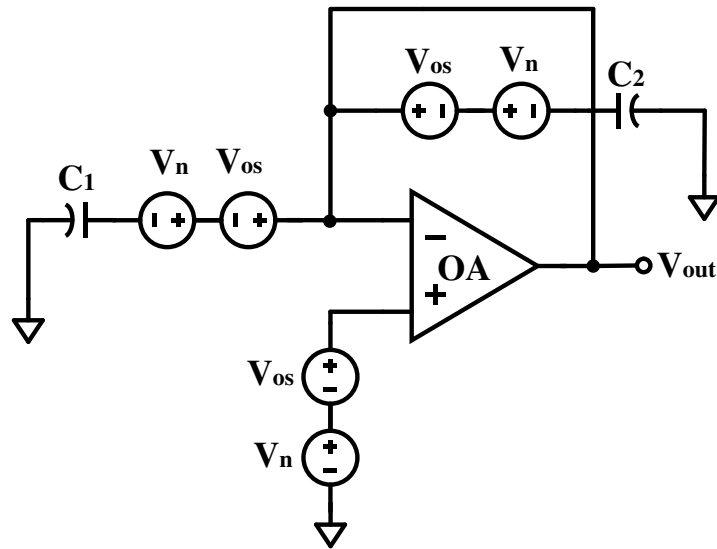
Fig. 3.5 Configuration of SC-CDS Circuit in Reset mode

When Φ_2 phase is on, the circuit is configured in the charge transfer mode as depicted in Fig. 3.6. The input voltage Vin will charge up capacitor C_1 and the charging currents running through capacitor C_2 and C_1 would be of the same magnitude, these two capacitors will accumulate the same amount of charge after the charge transfer process is completed(Φ_2 phase is off). At the same time, the same error voltage is sampled by these two capacitors again. This means that the voltage at the common electrodes of the two capacitors (inverting terminal of the op-amp) remains unchanged during the charge transfer phase clock period. Then, the accumulated charge in C_2 during the charge transfer period will be fully reflected on the voltage change at its other electrode (Vout). The charge accumulated by C_2 during the charge transfer phase is equal to Vin*C_1 which is independent of the error voltage. The output voltage, equal to -Vin*C_1/ C_2, is not affected by the error voltage. Thus, by sampling the error voltage twice during the whole working clock cycle (reset phase and charge transfer phase), the amplified output voltage is independent of the error voltage.
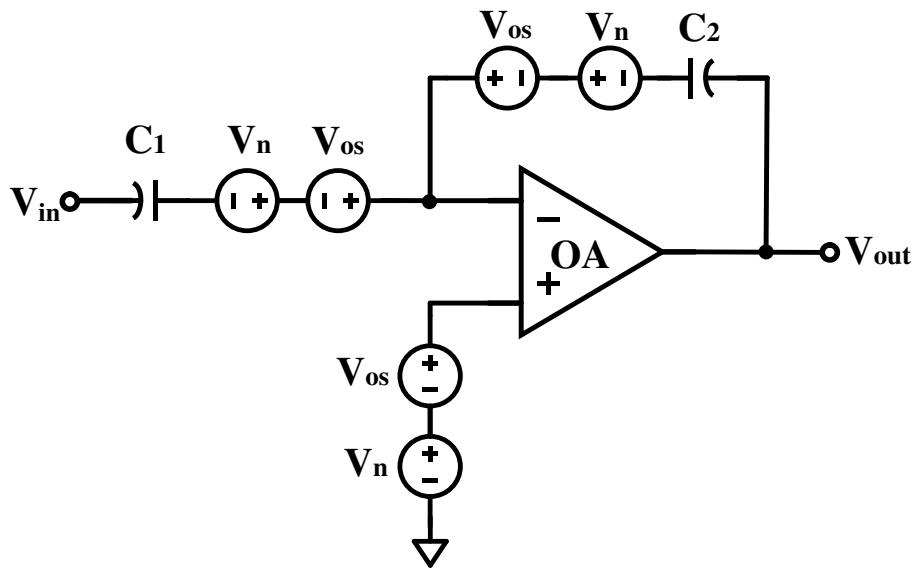
Fig. 3.6 Configuration of SC-CDS Circuit in Charge transfer mode

SC-CDS technique usually would result in relatively smaller power consumption and is easy to be implemented in CMOS technology. However, the problems of thermal noise folding effect and switch errors arising from charge injection and clock feed-through effects in SC-CDS circuits need to be solved. The concept of charge injection and clock feed-through will be briefly introduced here. Detailed analysis and comment on this issue can be found in literatures [36]-[38]. Several of the recently reported works [39]-[41] on SC capacitance-to-voltage converter (CVC) sensing scheme will be investigated in details.

3.2.3 Switch Errors in SC Design

In CMOS SC circuit, switches are usually realized with MOS transistors or CMOS transmission gate. There exists an inversion layer in the channel under the gate oxide between the source and drain regions of the MOS device. It is filled with charges when the MOS transistor is turned on. When the MOS transistor is switched off, these channel charges will flow out through the

source junction and the drain junction. If this charge is sampled by a capacitor (either the stray capacitance or the input capacitance of the next stage connected to the switch), it will cause a dc offset voltage at the switch output that would lead to charge injection error. On the other hand, when the clock signal applied to the gate terminal of the SC switch goes from high to low, the transition of the clock wave will cause the charge in the inversion channel to be injected (charge injection) or coupled (clock feed-through) to the sampling capacitor due to the overlapping capacitance between gate and source/drain junction. Fig. 3.7 shows the charge injection mechanism in a NMOS switch.
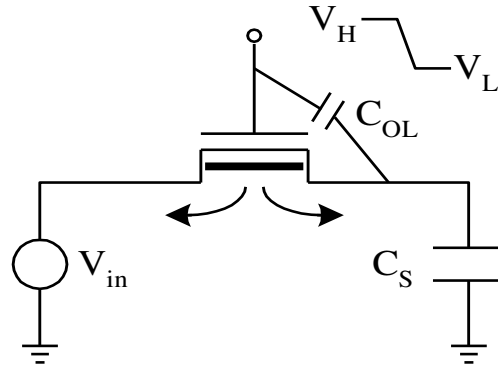
Fig. 3.7 Charge injection mechanism when the NMOS switch is turned off

The inversion channel charge of the NMOS transistor switch can be estimated as

$$Q_{ch} = -WLC_{ox}(V_{GS} - V_{th}) \tag{3.2}$$

where W and L are the channel width and length respectively, C_{ox} is the oxide capacitance per unit area, V_{GS} is the gate-to-source voltage and V_{th} is the threshold voltage of the MOS transistor used to implement the switch. If the control clock turns off fast enough, one can assume that half of the channel charge $Q_{ch}/2$ will flow into the drain junction and the other half will enter into the source junction. The charge injected into the source terminal of the switch

will be absorbed by the input voltage source while the latter half will be sampled by capacitor C_S and results in a dc offset voltage of the amplifier stage. The offset voltage is equal to

$$\Delta V_S^{'} = \frac{Q_{ch}}{2C_S} = -\frac{WLC_{ox}(V_{GS} - V_{th})}{2C_S} \tag{3.3}$$

When the gate voltage changes from V_H to V_L, the overlapping capacitance C_{OL} and the sampling capacitor C_S form a capacitance voltage divider. The voltage change at the top electrode of C_S can be calculated as

$$\Delta V_S^{"} = -\frac{C_{OL}}{C_{OL} + C_S}\left(V_H - V_L\right) \tag{3.4}$$

The overall error voltage caused by channel charge injection and clock feed-through is given as

$$\Delta V_S = -\{\frac{WLC_{ox}\left(V_{GS} - V_{th}\right)}{2C_S} + \frac{C_{OL}}{C_{OL} + C_S}\left(V_H - V_L\right)\} \tag{3.5}$$

The overlap capacitance C_{OL} is usually much smaller than C_S, and the second clock feed-through term in (3.5) is usually very small and can be ignored. The charge injection error dominates the overall error voltage. Since both the threshold voltage and the oxide capacitance are temperature dependent, the error voltage will drift with the temperature change, hence hindering the thermal stability of the circuit system. As can be seen from (3.5), in order to reduce charge injection error voltage, the MOS transistor size (*W* and *L*) should be kept small while the sampling capacitor C_S should be large. However, the requirement for using smaller charging time constant and hence the faster sampling rate would determine the limitation of the minimum MOS transistor size. Several circuit techniques [42]-[45] have been proposed to reduce these non-ideal effects. Although using the dummy switch compensation can help

reduce some of the channel charge injection, it is still not fully cancelled out. Differential circuit structure provides a good solution but at the expense of a more complex circuit and imposes more stringent requirement on matching for some critical component pairs, resulting in higher cost as well as higher power consumption. Some SC-CVC architectures dedicated to relax the stated dc offset problems are reported in the literature [39]-[40]. These will be discussed in detail in the following sections.

3.2.4 Comparison of CHS and SC-CDS Schemes

Comparing these two capacitive sensing schemes, both CHS and CDS techniques can effectively reduce the dc offset and the low frequency noise associated with the CMOS devices used to build the op-amp or other analog circuits. The CDS technique is basically a sampling technique in which the limited sampling frequency will cause high frequency thermal noise to be folded back to the baseband, resulting in the increase of undesirable thermal noise level. Another issue needed to be considered for SC-CDS scheme is that of the charge injection and clock feedthrough errors during the turning off of the MOS switches. These injected charges will introduce additional dc offset at the output if not properly designed. CHS technique can effectively reduce DC offset and 1/f noise without causing thermal noise folding problem. However, the modulated DC offset and 1/f noise will appear as chopper ripple voltages in triangular wave forms at the amplifier output. Under some worst input offset cases, this ripple voltage may be intolerably big as the amplitude of the ripple voltage is proportional to the input offset voltage. Besides, CHS technique will also suffer from charge injection and clock feedthrough problems arising from MOS switch based modulators. The charge injection and clock feedthrough errors will cause spikes at the input of the main amplifier which will be

rectified by the chopping operation, leading to residual offset voltage. For MEMS sensors with large parasitic capacitance and hence large charging time constants, this may cause problem in the implementation of CHS technique. This is mainly because the charging and discharging actions take long time to settle down. Although the use of large switches with lower on-resistance in CHS implementation would partially relax the issue, the large magnitude of unsymmetrical spikes arising from the large time constants and switch errors of the chopping switches in practical sensing structure will still lead to a big dc output offset. This may not be tolerable for highly-sensitive sensor application. CHS readout interface circuits are commonly used in surface micro-machined MEMS capacitive sensing device rather than bulk micro-machined MEMS capacitive sensing device because the relatively small parasitic capacitances in surface-micromachined MEMS sensor can be easily handled from the circuit design point of view. On the basis of design consideration and the requirement for interfacing bulk-micromachined MEMS device with large stray capacitances, the SC-CDS sensing method is preferred and realized in this project.

3.3 Review of Switched-Capacitor Interface Circuits

3.3.1 Offset-Canceled Cascade Capacitance-to-Voltage Converter (OCC-CVC)

3.3.1.1 Operation Principle of the OCC-CVC

The basic SC-CVC circuit was further modified into the form as shown in Fig. 3.8. This is the well-known Offset-Canceled Cascade Capacitance-to-Voltage Converter (OCC-CVC) design [39] and was reported to have the ability to

suppress the dc offset or 1/f noise. This improvement was achieved by adding one more SC gain stage after the front-end interface circuit and modifying the control clock waveforms as depicted in Fig. 3.9.

Refer to Fig. 3.8, when the clock signal P_1 is turned on, the first op-amp is in reset mode, the differential sensing capacitors C_{s1} and C_{s2} are charged up by the bipolar reference voltages, V_{ref+} and V_{ref-}, and the middle common capacitor electrode samples the offset of the first op-amp. Charge transfer takes place after P_1, P_2 are turned off and the clock Φ_2 is turned on. When P_1 and P_2 are turned off, they will cause charge injection errors on the output of each op-amp. Since P_2 turns off later than P_1, the second stage is still in reset mode when SW_1 switches off, so that the input capacitor C_3 will sample the first stage output signal plus its dc offset, flicker noise as well as the error voltage caused by charge injection on one end and the second stage dc offset on the other end during P_2 is on. Therefore, the first stage dc offset, flicker noise and charge injection error caused by SW_1 will be canceled during charge transfer phase but not that of the second stage.
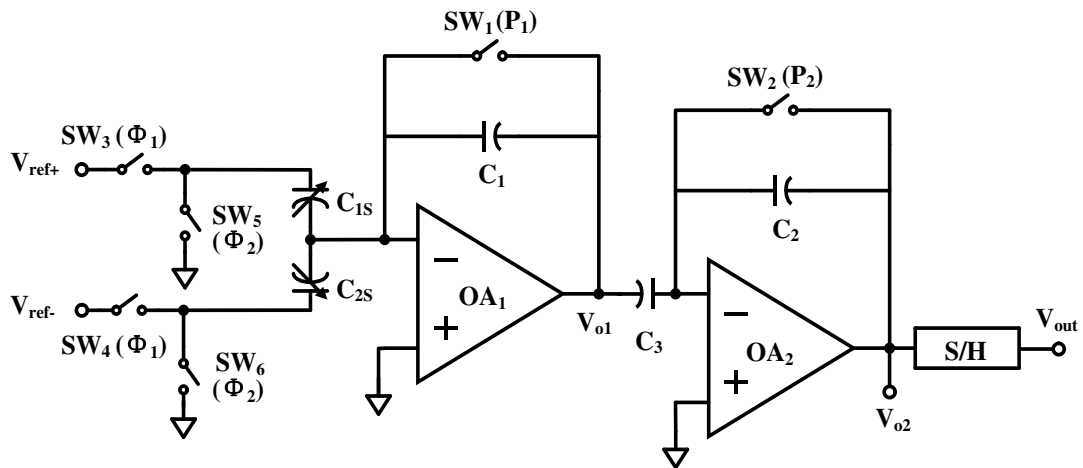
Fig. 3.8 Offset-canceled cascade capacitance-to-voltage converter (OCC-CVC) [39]
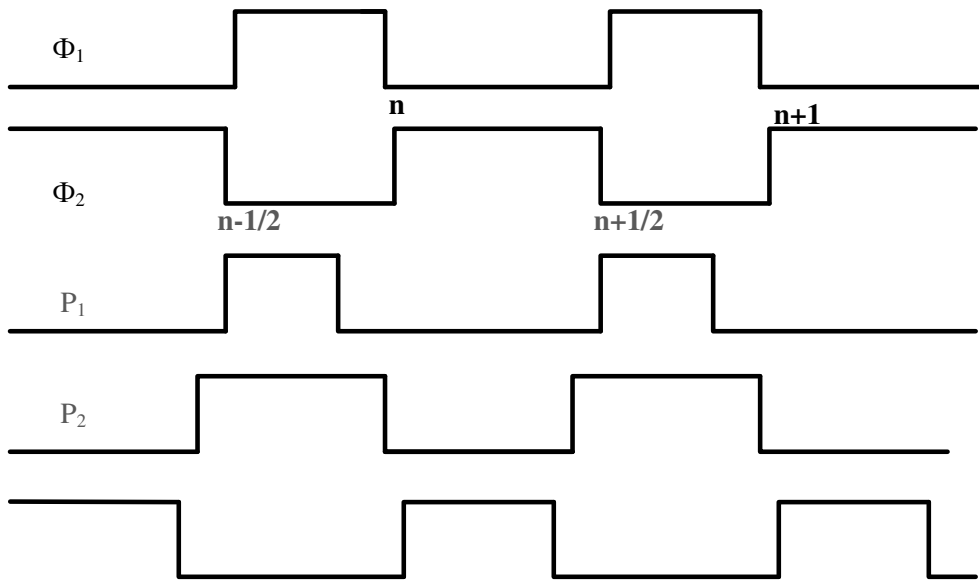
Fig. 3.9 Control clock waveforms for OCC-CVC [39]

Finally, the second stage output signal of the SC sensing interface will settle to its final value when Φ_2 is turned on, in which the first stage offset and 1/f noise are canceled whilst yet containing the errors of second stage. It is noted that a sample-and-hold block is added to model the sample-and-hold process arising from the subsequent SC interface stage such as SC integrator, SC Analog-to-Digital Converter (ADC) and so forth.

3.3.1.2 Offset and Flicker Noise Error Analysis of the OCC-CVC

Fig. 3.10 OCC-CVC with offset and flicker noise error sources [39]

The offset error and flicker noise can be represented by two voltage sources connected to the positive input of the op-amp. They are denoted as V_{os1} and V_{no1} for the first op-amp and V_{os2} and V_{no2} for the second op-amp respectively. Assume that the open-loop gain of the op-amp is high enough and the sensing capacitances can be charged up fully. When Φ_1, P_1, P_2 are on, the sensing capacitors C_{1S}, C_{2S} and the bottom plate of capacitor C_3 will be charged up to

$$Vc_{1S}(n) = V_{ref+} - \left[V_{os1}(n) + V_{no1}(n) \right] \tag{3.6}$$

$$Vc_{2S}(n) = V_{ref-} - \left[V_{os1}(n) + V_{no1}(n) \right] \tag{3.7}$$

$$V_{o1}(n) = V_{os1}(n) + V_{no1}(n) \tag{3.8}$$

The voltage across capacitor C_3 will be

$$V_{C_3}(n) = V_{os1}(n) + V_{no1}(n) - V_{os2}(n) - V_{no2}(n) \tag{3.9}$$

P_1 will be switched off first while Φ_1 and P_2 are still on. Assuming a fast clock waveform, when SW_1 turns off, half of the channel charge will be injected into the output node while the other half will flow to the negative input node of the first op-amp. The first part will only cause a temporary glitch at the output while the latter will result in a dc offset. Since P_2 is still on when P_1 is off, the second stage is still in reset mode while SW_1 turns off, so that the dc offset will be sampled by capacitor C_3. Thus, $V_{o1}(n)$ should be rewritten as

$$V_{o1}(n) = V_{os1}(n) + V_{no1}(n) - \frac{Q_{sw1}(n)}{2C_1} \tag{3.10}$$

where Q_{sw1} is the channel charge of switch SW_1 when it is on. Then P_2 is turned off and half of the channel charge of SW_2 flowing to the negative input of the second op-amp will cause a dc offset at the output node. When Φ_1 is turned off and Φ_2 is turned on, charge transfer will begin. After Φ_2 turns on, the voltages across capacitors C_{1S} and C_{2S} are changed to

$$Vc_{1S}\left(n+\frac{1}{2}\right) = -V_{os1}\left(n+\frac{1}{2}\right) - V_{no1}\left(n+\frac{1}{2}\right) \tag{3.11}$$

$$Vc_{2S}\left(n+\frac{1}{2}\right) = -V_{os1}\left(n+\frac{1}{2}\right) - V_{no1}\left(n+\frac{1}{2}\right) \tag{3.12}$$

The charge of capacitor C_{1S} and C_{2S} will be transferred to capacitor C_1. By conservation of charges at the node of virtual ground, we have

$$
\begin{aligned}
&C_{1S}[Vc_{1S}\left(n+\frac{1}{2}\right) - Vc_{1S}(n)] + C_{2S}[Vc_{2S}\left(n+\frac{1}{2}\right) - Vc_{2S}(n)] \\
&= C_1[V_{os1}\left(n+\frac{1}{2}\right) + V_{no1}\left(n+\frac{1}{2}\right) - V_{o1}\left(n+\frac{1}{2}\right)] - Q_{SW_1}\left(n+\frac{1}{2}\right)/2
\end{aligned}
\tag{3.13}
$$

Substituting (3.6)-(3.9) and (3.11)-(3.12) to (3.13), we can get

$$V_{o1}\left(n+\frac{1}{2}\right)=\frac{C_{1S}V_{ref+}+C_{2S}V_{ref-}}{C_1}+V_{os1}\left(n+\frac{1}{2}\right)+V_{no1}\left(n+\frac{1}{2}\right)-\frac{Q_{sw1}\left(n+\frac{1}{2}\right)}{2C_1} \quad (3.14)$$

Since the charging current going through capacitor C_3 and C_2 is the same, we have

$$C_3\{V_{o1}\left(n+\frac{1}{2}\right)-\left[V_{os2}\left(n+\frac{1}{2}\right)+V_{no2}\left(n+\frac{1}{2}\right)\right]-[V_{o1}(n)-(V_{os2}(n)+V_{no2}(n))]\}$$

$$=C_2[V_{os2}\left(n+\frac{1}{2}\right)+V_{no2}\left(n+\frac{1}{2}\right)-V_{o2}\left(n+\frac{1}{2}\right)]-Q_{SW_2}\left(n+\frac{1}{2}\right)/2$$

$$(3.15)$$

The low frequency flicker noise $V_{no}(n)$, dc offset $V_{os}(n)$ as well as the switch charge injection $Q_{sw1}(n)$ during the charge transfer phase n are equal to those values of the reset phase (n+1/2), hence they can cancel each other in the equation. Solving (3.15) for $V_{o2}\left(n+\frac{1}{2}\right)$, we obtain

$$V_{o2}\left(n+\frac{1}{2}\right)=-\frac{C_3[C_{1S}V_{ref+}+C_{2S}V_{ref-}]}{C_1C_2}+V_{os2}\left(n+\frac{1}{2}\right)+V_{no2}\left(n+\frac{1}{2}\right)-\frac{Q_{sw2}(n+\frac{1}{2})}{2C_2}$$

$$(3.16)$$

As can be seen from (3.16), the OCC-CVC can efficiently eliminate the op-amp dc offset, flicker noise as well as the charge injection error of the first stage but not those coming from the second stage.

3.3.1.3 Finite Gain Error Analysis of the OCC-CVC
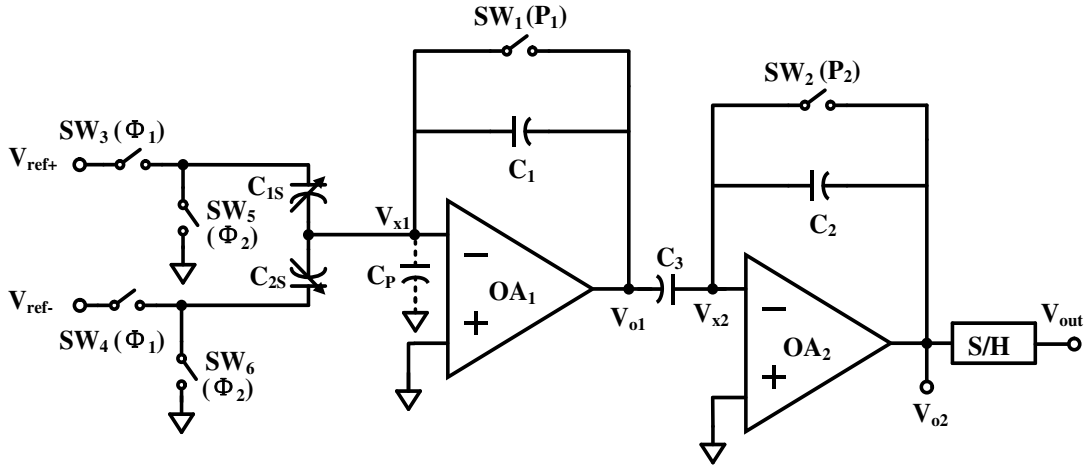
Fig. 3.11 OCC-CVC with parasitic capacitance at the middle sensing node

Assuming an infinite DC gain of the charge amplifier, the ideal output expression is derived as

$$V_o = -\frac{C_3(V_{ref+}C_{1S} + V_{ref-}C_{2S})}{C_1 C_2} \tag{3.17}$$

As observed, it is a function of the driving reference voltage, the sensing capacitor or and the feedback capacitor. However, the practical op-amp has finite gain effect, the inverting node becomes not exactly at virtual ground. In SC circuit, it will cause the finite gain error during charge transfer, hence degrading the accuracy. Since the finite gain is also subject to the process and temperature variations, this is translated to the output dependence on these variations as well.

For finite gain error analysis, the parasitic capacitance C_P between the middle sensing node and ground is added, the dc open-loop gain of these two op-amps are denoted as A_{v1} and A_{v2} respectively. V_{X1} and V_{X2} are the respective voltages

at the negative input node of these two op-amps. Thus, the nodal analysis for the first op-amp gives the following relationship:

$$C_{1S}[0-V_{X1}-V_{ref+}]+C_{2S}[0-V_{X1}-V_{ref-}]-C_PV_{X1}=C_1[V_{X1}-V_{o1}] \tag{3.18}$$

$$V_{o1}=-A_{v1}V_{X1} \tag{3.19}$$

Substituting (3.18) into (3.17), we get

$$V_{o1}=\frac{V_{ref+}C_{1S}A_{v1}+V_{ref-}C_{2S}A_{v1}}{C_P+C_{1S}+C_{2S}+(1+A_v)C_1} \tag{3.20}$$

Similarly, for the second op-amp analysis, we have the following relationship:

$$C_3[V_{o1}-V_{X2}]=C_2[V_{X2}-V_o] \tag{3.21}$$

$$V_o=-A_{v2}V_{X2} \tag{3.22}$$

Substituting (3.20) into (3.21), the output voltage with the finite gain taken into account is

$$
\begin{aligned}
V_o &= -\frac{C_3A_{v2}(V_{ref+}C_{1S}A_{v1}+V_{ref-}C_{2S}A_{v1})}{[(1+A_{v2})C_2+C_3][C_P+C_{1S}+C_{2S}+(1+A_{v1})C_1]} \\
&= -\frac{C_3(V_{ref+}C_{1S}+V_{ref-}C_{2S})}{C_1C_2(1+\dfrac{1}{A_{v1}}\cdot\dfrac{C_P+C_{1S}+C_{2S}+C_1}{C_1})(1+\dfrac{1}{A_{v2}}\cdot\dfrac{C_2+C_3}{C_2})}
\end{aligned}
\tag{3.23}
$$

Compared with the ideal output expression in (3.17), we can see that the output voltage in (3.23) consists of a finite gain factor related with the finite open-loop gains A_{v1} and A_{v2} of the op-amp. When A_{v1} and A_{v2} are infinite, (3.23) is equal to (3.17). The term

$$(\frac{1}{A_{v1}}\cdot\frac{C_P+C_{1S}+C_{2S}+C_1}{C_1}+\frac{1}{A_{v2}}\cdot\frac{C_2+C_3}{C_2}+\frac{1}{A_{v1}A_{v2}}\cdot\frac{C_P+C_{1S}+C_{2S}+C_1}{C_1}\cdot\frac{C_2+C_3}{C_2})$$

is the error factor indicated in (3.23). It characterizes the gain error of the SC

circuit induced by the finite gain of the op-amp. It is obvious from the gain error expression that each op-amp will contribute a certain fraction of the total gain error. Hence, in this OCC-CVC scheme, the added cascade stage will introduce additional gain error. A high enough DC open-loop gain is often required for both op-amps in order to limit this gain error to a tolerable range.

3.3.2 Zoom-In Capacitance-to-Voltage Converter (ZI-CVC)

3.3.2.1 Operation Principle of the ZI-CVC

The Zoom-In Capacitance-to-Voltage Converter (ZI-CVC) [40] is another high resolution circuit architecture that can sense small capacitance change. Fig. 3.12 shows the circuit schematic whereas Fig. 3.13 denotes the control clock waveforms. Refer to Fig. 3.12, the zoom-in capacitor, C_R, is made close the nominal value of the sensing capacitor, C_X. When the reset signal P_{rst} is turned off prior to the switching of the reference voltage source, V_{ref}, through control clocks, P_{EXE} and $\overline{P_{EXE}}$, the sample-and-hold capacitor C_{h1} will sample the reset noise arising from the sensing element C_X. After the event of switching the control clocks, P_{EXE} and $\overline{P_{EXE}}$, the sample-and-hold capacitor, C_{h2}, will sample both the signal and reset noise. If a differential operation is applied for the output signals, V_{o1} and V_{o2}, the reset noise is cancelled. As such, the 1/f noise and offset of the op-amp is suppressed. The offset drift will be significantly improved via the differential operation on the two output signals. Unfortunately, the signal swing will be reduced because of the sensing element is restricted to one capacitor only. Since the reset noise is cancelled out, the residual noise comes from the sampled op-amp's wideband thermal noise on the two sample-and-hold capacitors, C_{h1} and C_{h2}. Therefore, the bandwidth of the op-amp should be limited whenever possible.
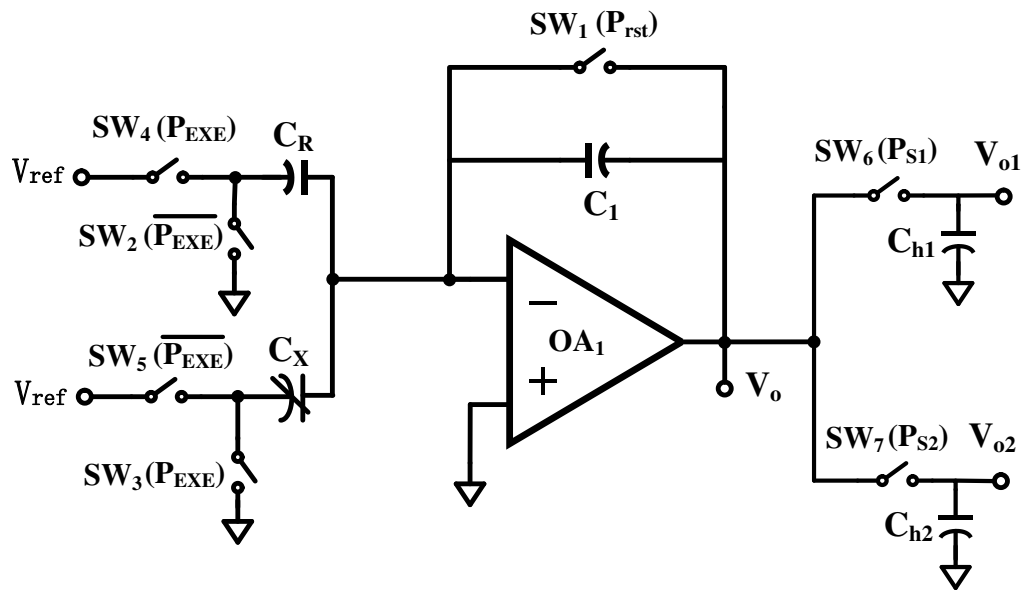
Fig. 3.12 Zoom-in capacitance-to-voltage converter (ZI-CVC) [40]
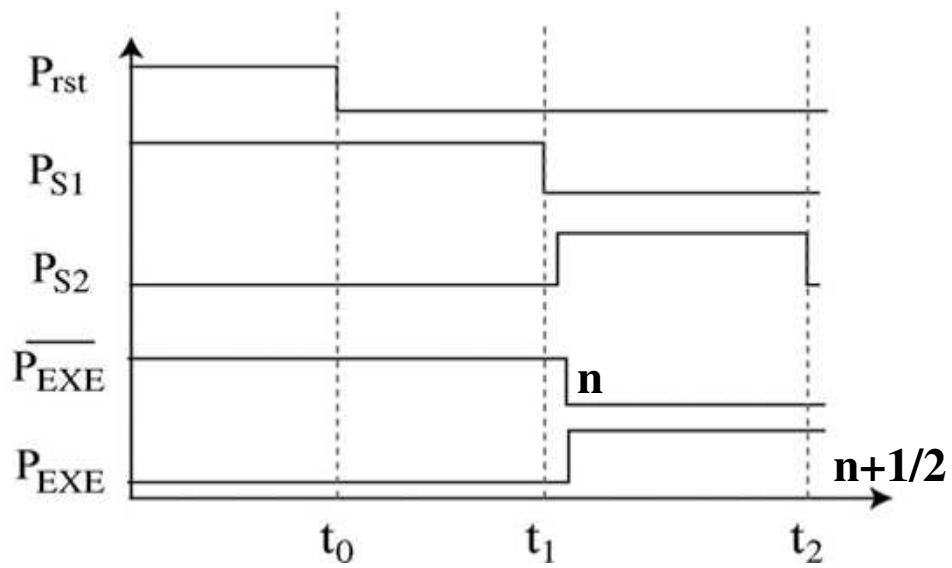
Fig. 3.13 Control clock waveforms for ZI-CVC

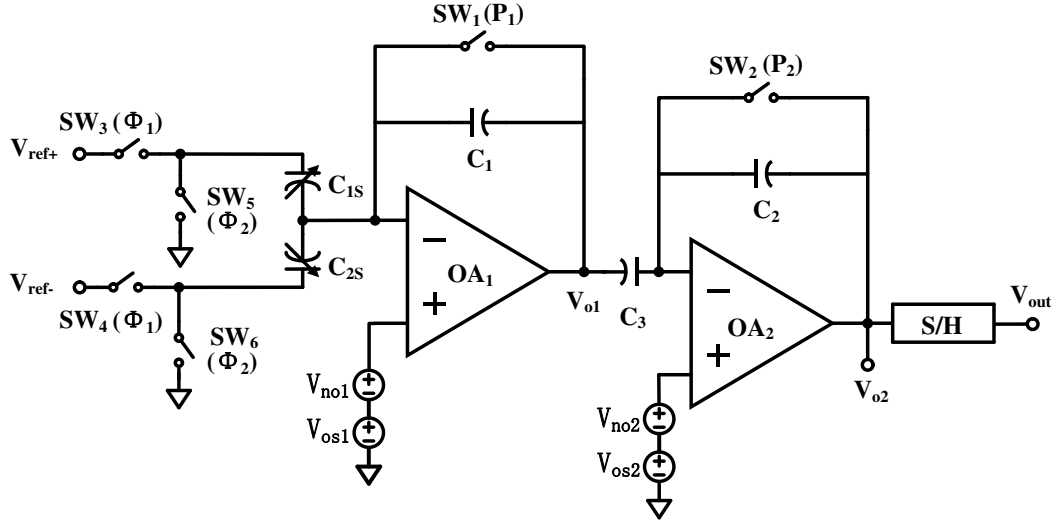### 3.3.2.2 Offset and Flicker Noise Error Analysis of the ZI-CVC
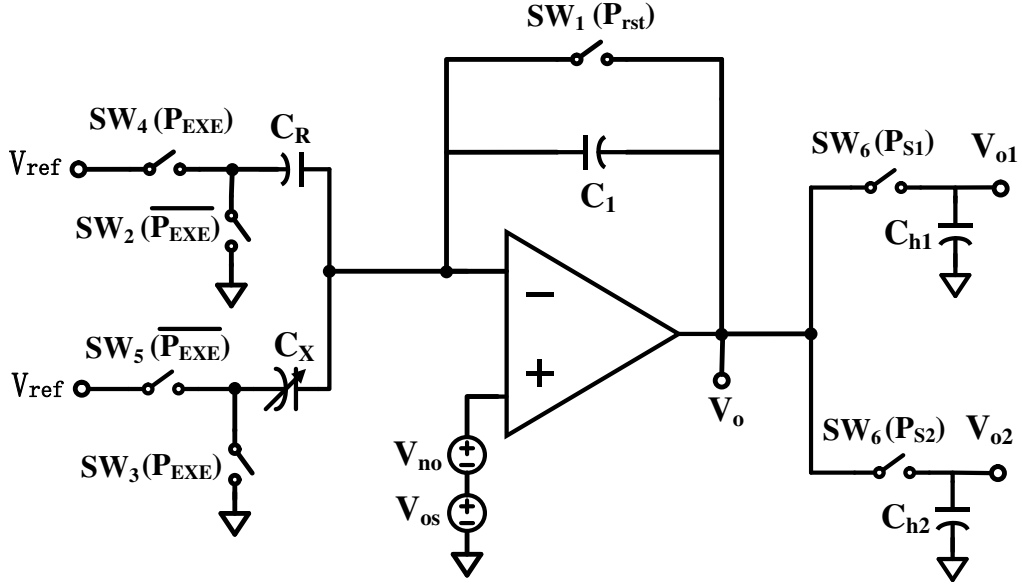
Fig. 3.14 ZI-CVC with offset and flicker noise error sources [40]

The offset error and flicker noise is represented by two voltage sources connected to the positive input of the op-amp denoted as V_{os} and V_{no}. Assume that the gain of the op-amp is high enough and the sensing capacitances can be fully charged up. When $P_{rst}, \overline{P_{EXE}}$ and P_{S1} are on, the reference capacitor and the sensing cap will be charged up to

$$Vc_R(n) = -V_{os}(n) - V_{no}(n) \tag{3.24}$$

$$Vc_X(n) = V_{ref} - V_{os}(n) - V_{no}(n) \tag{3.25}$$

After P_{rst} is turned off, half of the channel charge of switch SW1 will be injected into the output node while the other half will be injected to the negative input of the op-amp. The charge $Q_{SW_1}/2$ flowing into the input node will cause a dc offset at the output node and will be sampled by capacitor C_{h1}. Then P_{S1}

will be turned off and again half of the channel charge of switch SW_6 will flow into capacitor C_{h1}.

$$Vc_{h1}(n) = V_{os}(n) + V_{no}(n) - \frac{Q_{SW_1}(n)}{2C_1} + \frac{Q_{SW_6}(n)}{2C_{h1}}$$

(3.26)

After that, P_{S2} and P_{EXE} will be turned on, charge transfer will begin. The reference capacitor and the sensing capacitor will be charged up to the new voltage levels as follows:

$$Vc_R(n+\frac{1}{2}) = V_{ref} - V_{os}(n+\frac{1}{2}) - V_{no}(n+\frac{1}{2})$$

(3.27)

$$Vc_X(n+\frac{1}{2}) = -V_{os}(n+\frac{1}{2}) - V_{no}(n+\frac{1}{2})$$

(3.28)

By applying charge conservation theory at the node of virtual ground, we have

$$C_R[Vc_R\left(n+\frac{1}{2}\right) - Vc_R(n)] + C_X[Vc_X\left(n+\frac{1}{2}\right) - Vc_X(n)]$$
$$= C_1\left[V_{os}(n+\frac{1}{2}) + V_{no}(n+\frac{1}{2}) - V_o\left(n+\frac{1}{2}\right)\right] - Q_{SW_1}\left(n+\frac{1}{2}\right)/2$$

(3.29)

Solving (3.29) for $V_o\left(n+\frac{1}{2}\right)$, we can get

$$V_o\left(n+\frac{1}{2}\right) = \frac{V_{ref}(C_X - C_R)}{C_1} + V_{os}(n+\frac{1}{2}) + V_{no}(n+\frac{1}{2}) - \frac{Q_{SW_1}\left(n+\frac{1}{2}\right)}{2C_1}$$

(3.30)

As charge transfer phase completed, P_{S2} will be turned off first, and half of the channel charge of SW_7 will be stored by the holding capacitor C_{h2}. The sample-and-hold signal is as follows:

$$Vc_{h2}\left(n+\frac{1}{2}\right)=\frac{V_{ref}(C_X-C_R)}{C_1}+V_{os}(n+\frac{1}{2})+V_{no}(n+\frac{1}{2})-\frac{Q_{SW_1}\left(n+\frac{1}{2}\right)}{2C_1}+\frac{Q_{SW_7}\left(n+\frac{1}{2}\right)}{2C_{h2}}$$

<div align="right">(3.31)</div>

The low frequency flicker noise $V_{no}(n)$, dc offset $V_{os}(n)$ as well as the switch charge injection $Q_{sw1}(n)$ during the charge transfer phase n are equal to those values of the reset phase (n+1/2). The same goes for that of $Q_{sw6}(n)$ and $Q_{sw7}(n+1/2)$ since SW_6, SW_7, C_{h1} and C_{h2} are exactly the same. All these terms can be cancelled under differential operation, the subtraction result yields

$$Vc_{h2}\left(n+\frac{1}{2}\right)-Vc_{h1}(n)=\frac{V_{ref}(C_X-C_R)}{C_1}$$

<div align="right">(3.32)</div>

3.3.2.3 Finite Gain Error Analysis of the ZI-CVC
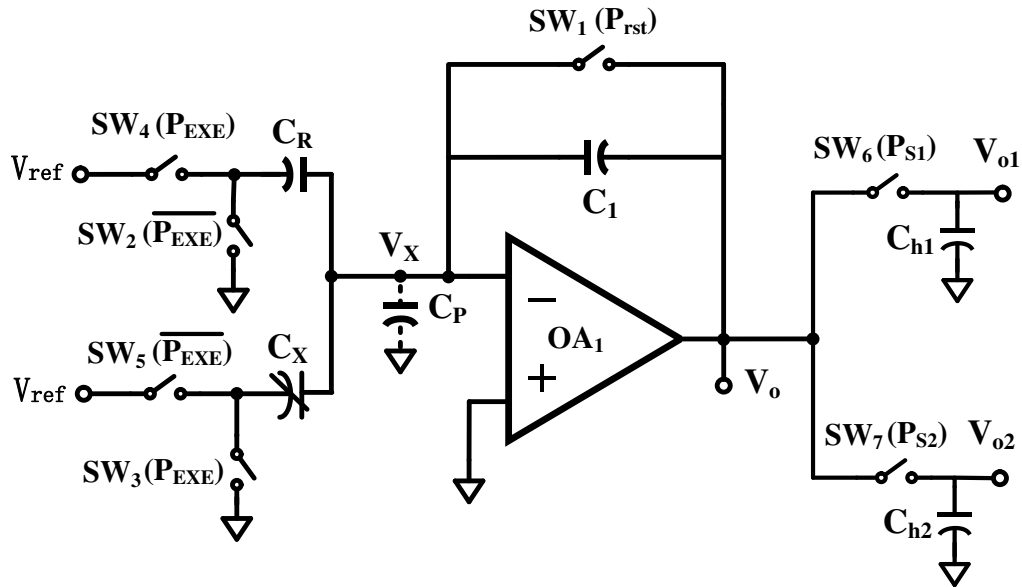
Fig. 3.15 ZI-CVC with parasitic capacitance at the middle sensing node

The finite op-amp dc open-loop gain is denoted as A_v and the voltage at the negative input node of the op-amp is defined as V_X, C_P is the parasitic capacitance. Using nodal analysis, we get

$$C_R[V_{ref} - V_X] + C_X[-V_X - V_{ref}] - C_P V_X = C_1 [V_X - V_o]$$ (3.33)

$$V_o = -A_v V_X$$ (3.34)

By substituting (3.34) into (3.33), we get

$$V_o = \frac{V_{ref}(C_X - C_R)}{C_1(1 + \dfrac{C_1 + C_X + C_R + C_P}{A_v C_1})}$$ (3.35)

The factor $\dfrac{C_1 + C_X + C_R + C_P}{A_v C_1}$ in (3.35) represents the magnitude error due to the finite open-loop gain A_v of the op-amp. It is inversely proportional to A_v and is approximately to be 0 when A_v tends to be infinity. Hence, in practical design case, A_v should be designed to be high enough to suppress the finite open-loop gain induced error.

3.3.3 Single-Ended-to-Fully-Differential Capacitance-to-Voltage Converter (SETFD-CVC)

Fig. 3.16 presents another capacitance-to-voltage conversion architecture which aims to achieve a differential output with a simple two terminal capacitive sensor [41]. This single-ended to fully differential capacitive-to-voltage converter (SETFD-CVC) senses the signal charge by using a capacitive divider structure formed by the sensing capacitor C_{sen}, a reference capacitor C_R and a sampling capacitor C_S. The sensor is interfaced with a fully differential amplifier to achieve a differential output voltage. The conversion mechanism is that it includes two different charge transfer states which can help cancel out

the leakage current problem caused by the ESD protection circuit. The circuit operation is described as follows: First, the capacitor divider will be reset to voltage V_M; next, the reference voltages V_{REFP} and V_{REFM} as well as the leakage current will charge up the capacitor divider node for the sampling capacitor C_S. This is then followed by the charge transfer mode. The charged sampling capacitor C_S will be connected to the differential input node of the op-amp and a differential output, V_{OUTP} and V_{OUTM}, will be generated, such that the capacitance change is converted to the output voltage for the first time. This voltage will be stored on the feedback capacitors C_F. For the successive second capacitance-to-voltage conversion cycle, the capacitor divider will be reset to V_M first, and the reference voltages V_{REFP} and V_{REFM} connection is switched this time, such that the sign of the signal charge on the sampling capacitor will be opposite to that of the first cycle. However, the charge caused by the leakage current will remain the same. Later during the charge transfer stage, the sampling capacitor C_S will be connected to the amplifier with an opposite polarity from the first charge transfer stage. Thus, during the second charge transfer stage, the signal charge is amplified with the same sign at the output while the error charge caused by the leakage current is opposite. Since the charge of the first charge transfer stage is preserved by the feedback capacitors, the error voltage will be canceled out while the output voltage is doubled during the second charge transfer process. The analysis of transfer function of the SETFD-CVC is given as follows.

During the first sample phase, the charge sampled by the sampling capacitor C_S is

$$Q_S' = C_S \cdot \frac{V_m \left(C_{sen} + C_R \right) - V_{refp} \cdot C_{sen} - V_{refm} \cdot C_R}{C_{sen} + C_R + C_S} - \Delta Q \qquad (3.36)$$

where $V_{ref} = -2V_{refm} = 2V_{refp}$, ΔQ is the error charge caused by the ESD leakage due to the single pin input for the sensing element. In the second sample phase, the polarity is changed so that the charge stored on C$_S$ becomes

$$Q_S^{"} = C_S \cdot \frac{V_m \left(C_{sen} + C_R \right) - V_{refp} \cdot C_R - V_{refm} \cdot C_{sen}}{C_{sen} + C_R + C_S} - \Delta Q \tag{3.37}$$

In the charge transfer phase, the charge stored on C$_S$ will be transferred to the charge amplifier output through the feedback capacitor C$_F$. The output voltage after the first charge transfer phase is obtained as follows:

$$V_{out} = 2 \cdot \frac{Q_S^{'}}{C_F} \tag{3.38}$$

From (3.38), the output voltage will be proportional to the sensing charge. Since the feedback capacitor C$_F$ will store the charge after the first charge transfer phase, the output voltage of the charge amplifier after the two successive charge transfer stages is the addition of these two output voltages. Therefore, we have

$$V_{out} = 2 \frac{Q_S^{'} - Q_S^{"}}{C_F} = \frac{2C_S}{C_F} \cdot V_{ref} \cdot \frac{C_R - C_{sen}}{C_R + C_{sen} + C_S} \tag{3.39}$$

From (3.39), the output voltage is independent of the leakage current induced error.

61
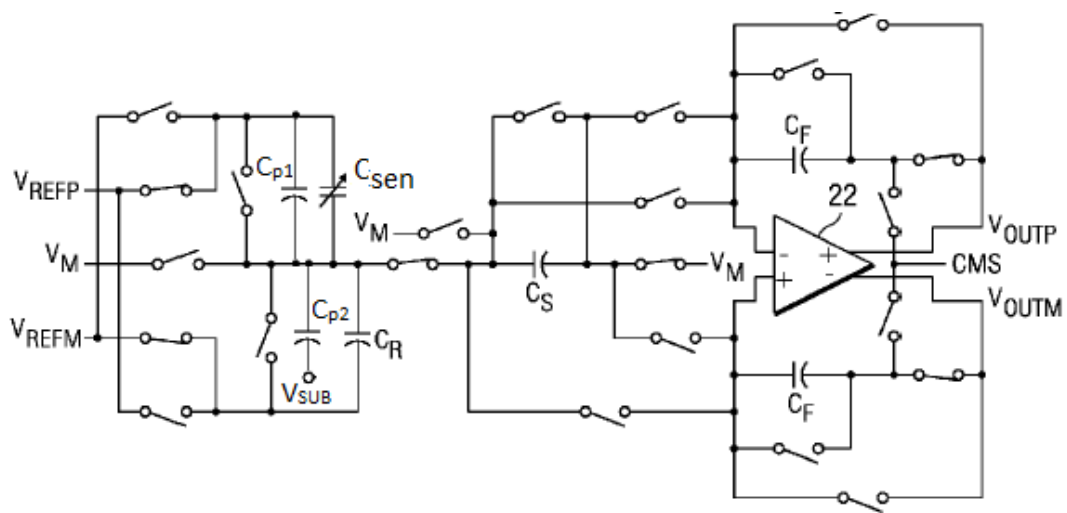
Fig. 3.16 Single-ended-to-fully-differential capacitance-to-voltage converter

Unfortunately, there are several problems embedded in this structure. First, this scheme is affected by the parasitic capacitances at the interconnection node between the sensor device and the interface circuit. As shown in Fig. 3.16, the parasitic capacitance C_{P1} and C_{P2} can be deemed as in parallel connection with the sampling capacitor C_S, which will produce charge sharing effect during the capacitor divider charging state, causing an error at the output voltage. Second, the capacitor divider sensing scheme is subjected to the charge injection and clock feed-through error contributed by switch SW_S. Since the signal is still not amplified at the input node, this charge injection will also cause a considerable error if not properly cancelled. Third, the 1/f noise as well as the dc offset error coming from the differential amplifier cannot be cancelled. Fourth, the capacitor divider sensing structure results in a non-linear transfer function between the capacitance change and the output voltage. Fifth, this scheme is not suitable for large rest capacitance sensor, since the capacitor charging and discharging process will cause big spikes or glitches, which subsequently contribute large dc offset at the output.

3.4 Summary

In this chapter, two most commonly-used capacitive sensing methods: continuous-time chopper stabilization (CHS) scheme and discrete-time switched-capacitor (SC) sensing scheme are reviewed with an in-depth study of the strength and weakness encountered in each scheme. This gives the rational to the design of accelerometer ASIC using SC design approach. The CMOS switch induced charge injection and clock feed-through error in SC circuit design are briefly discussed. Two improved single-stage SC-CVC circuit structures, Offset-Canceled Cascade Capacitance-to-Voltage Converter (OCC-CVC) and Zoom-In Capacitance-to-Voltage Converter (ZI-CVC), are discussed together with their detailed analysis. Finally, a Single-Ended-To Fully Differential Capacitance-to-Voltage Converter (SETFD-CVC), at the expense of complicated circuit architecture, dedicated to interface with a simple two terminal capacitive sensor is presented. All these three designs serve as the benchmarks to compare the performance of the proposed SC-CVC which is described in the following Chapter 4.

CHAPTER 4

SYSTEM ARCHITECTURE AND CORE BUILDING BLOCKS

4.1 System Architecture

Fig. 4.1 shows the simplified block diagram of the accelerometer ASIC together with the capacitive sensor device. The front-end interface is designed using the proposed auto-zero time-multiplexed differential capacitance-to-voltage converter (AZTMD-CVC), which is able to sense and convert sensor capacitance change to a differential output voltage without resorting to fully differential circuit architecture. The differential output is coupled to a differential-to-single-ended SC gain stage [46] with programmable gain. This is then followed by the signal-conditioning block which comprises an external passive first-order low-pass filter and an on-chip low-offset low-noise op-amp buffer. The external passive RC network provides smoothing function on the quasi-analog output from the SC gain stage and defines the bandwidth of the accelerometer IC. It can be a first-order or second-order networks. The op-amp buffer is realized using the instrumentation amplifier topology [47] except the use of folded-gain stage as the middle differential amplifier stage. This will be further described in sub-sequent section. Furthermore, a low-power supply-insensitive temperature-compensated relaxation oscillator incorporated with the control clock logic is designed to generate the control clocks for the SC system. This will be further described as a part of the housing keeping circuits in Chapter 5.
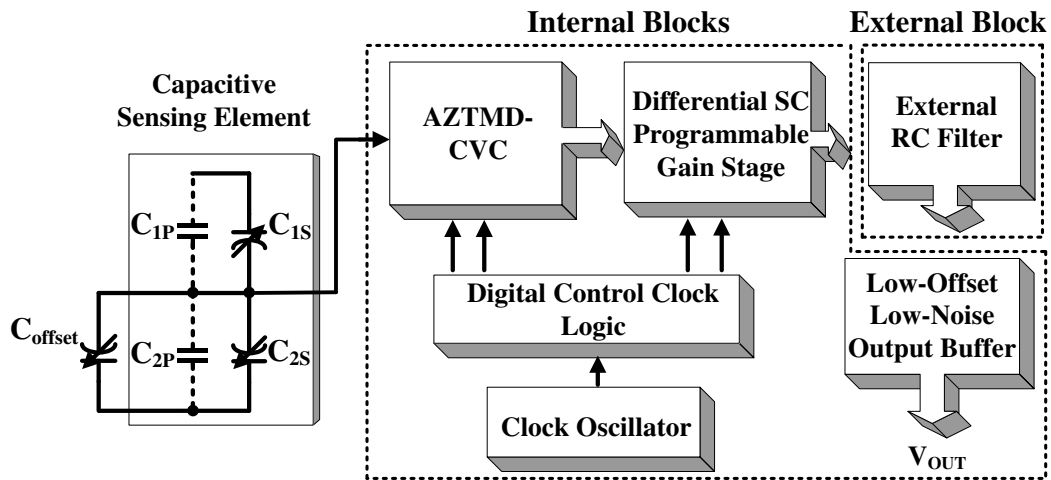
Fig. 4.1 Simplified block diagram of the capacitive accelerometer IC

4.2 Auto-Zero Time-Multiplexed Differential Capacitance-to-Voltage Converter

Based on the analytical study of the two main interface circuit techniques: CHS and SC-CDS, one can note that an electronic interface dedicated to couple with a bulk micro-machined MEMS device involves large capacitances as well as large charging/discharging time constants, the SC sensing method is preferred because of its nature supporting fast charging/discharging on capacitances without significantly jeopardizing the front-end interface performance. The focus of this work is to design a low-power, highly-sensitive SC accelerometer IC dedicated to the security sensing system.

In this SC front-end sensing interface, an Auto-Zero Time-Multiplexed Differential Capacitance-to-Voltage Converter (AZTMD-CVC) circuitry is proposed. This circuit architecture provides differential output using a simple single-ended CVC design structure. This approach eliminates the use of bulky full Wheatstone bridge sensing element in the MEMS sensor as required in

conventional fully differential sensor interface architecture [16], whilst offering an additional benefit in reducing the fabrication cost of the MEMS sensor and interface circuit, and the power consumption. The time-multiplexed differential output improves the S/N ratio and reduces the dc offset as well as the thermal drift without sacrificing the power consumption and increasing circuit complexity. Moreover, this scheme also avoids the stringent requirement for component matching and eliminates the common-mode problem in conventional fully differential interface circuitry. Finally, the low-noise design of front-end charge sensing amplifier in conjunction with the noise-power optimization in AZTMD-CVC is provided as another important part of the solutions.

4.2.1 Operation Principle of the Auto-Zero TMD-CVC

Fig. 4.2 depicts the schematic of proposed Auto-Zero Time-Multiplexed AZTMD-CVC together with its time-multiplexed control clock signals.
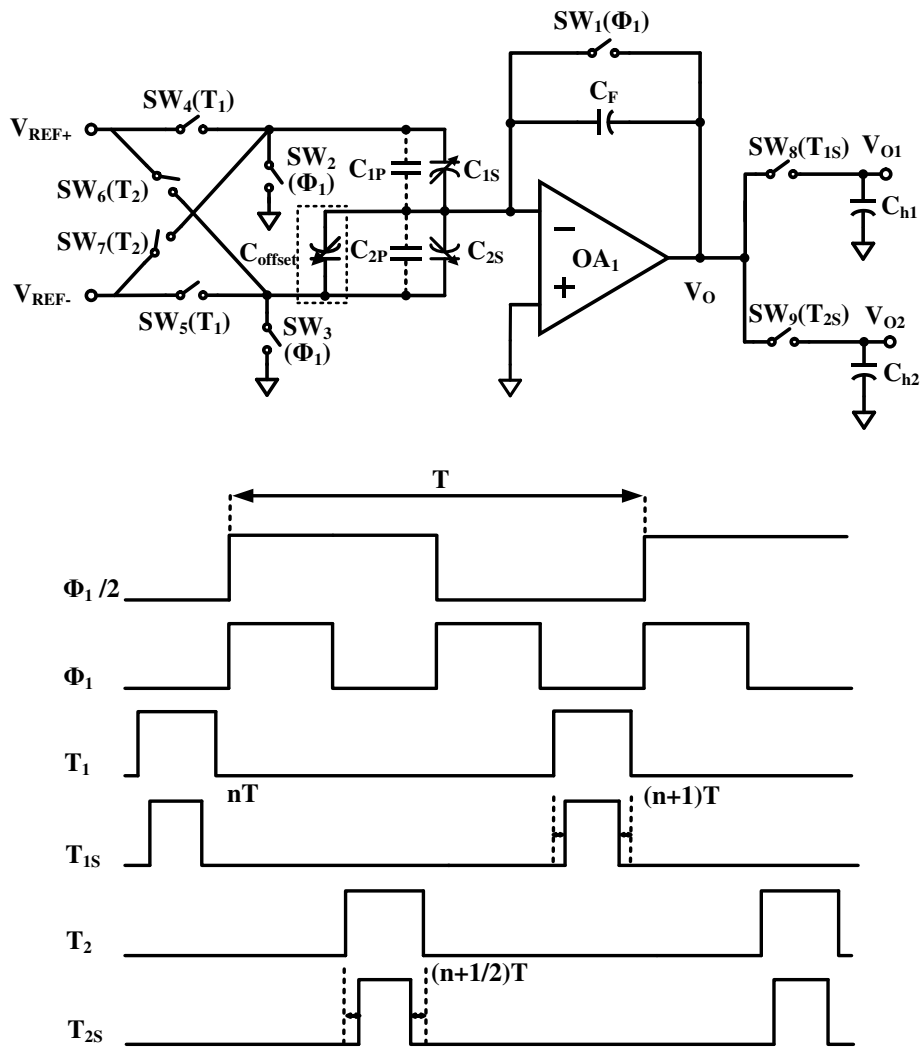
Fig. 4.2 Schematic diagram of the AZTMD-CVC with its control clocks

This structure deals with a multi-rate switched-capacitor design. This involves the storage of two time-multiplexed output results arising from two transfer phases of CVC. This arrangement permits conversion of capacitive senor signal from a single-end CVC output to the time-multiplexed output signals in differential format. The charge transfer phase consists of a sample-and-hold period. The frequencies of which are m times faster than that of the reset phase in the SC design. In this work, m is set equal to 2. As illustrated in the clock waveforms in Fig. 4.2, the reset clock Φ_1, which is equal to the master clock frequency, is designed to be twice the frequency of that of the multiplexed

clock $\Phi_1/2$ which comprises the charge transfer clocks T_1, T_2 and the respective reset period for time-multiplexed differential channel. Refer to Fig. 4.2, the differential capacitive sensor pair formed by C_{1S} and C_{2S} in conjunction with the parasitic capacitances C_{1P} and C_{2P} as well as the offset capacitor C_{offset} are controlled by seven switches, SW_1–SW_7 for time-multiplexing operation. The feedback capacitor, C_F and the op-amp OA_1 serve the charge-to-voltage conversion. The single-ended output of the op-amp OA_1 is sampled by two sample-and-hold (S/H) networks formed by the holding capacitors C_{h1} and C_{h2} and respective switches SW_8 and SW_9 under the control of the corresponding sub clock signals, T_{1S} and T_{2S} respectively. The functioning steps of the AZTMD-CVC are stated as follows: (a) When Φ_1 turns on, both the sensing capacitors and the op-amp are reset. (b) Φ_1 turns off and T_1 turns on. The reference voltage will charge up the sensing capacitors whereas the output of OA_1 will charge feedback capacitor in response to the charge transfer. (c) After a certain intentional delay, T_{1S} will turn on and the output voltage V_{o1} will be sampled and stored on C_{h1}. (d) This is then followed by the turn-on of Φ_1 again to reset the sensing elements and the op-amp prior to the second charge transfer phase. (e) Φ_1 turns off and T_2 turns on. The reference voltage will be interchanged to generate a time-multiplexed differential sensing charge signal across C_F. (f) T_{2S} will turn on and the output voltage V_{o2} will be sampled and stored on C_{h2}. (g) The process is repeated again.

In brief, the sequence of the clocks signals to control the operation of TMD-CVC is summarized as follows:

(1) reset phase Φ_1 prior to 1st charge transfer phase

(2) 1st charge transfer and sample-and-hold the sensor signal during T_1 and T_{1S} -> V_{o1},

(3) reset phase Φ_1 prior to 2nd charge transfer phase

(4) 2nd charge transfer and sample-and-hold the negated sensor signal during T_2 and T_{2S}, -> V_{o2},

(5) Repeat the process.

By charge conservation theory between the reset phase and charge transfer phases, the output voltage of V_{o1} and V_{o2} are obtained as

$$V_{o1}(n) = -\frac{(C_{1S} + C_{1P})V_{REF+} + (C_{2S} + C_{2P} + C_{offset})V_{REF-}}{C_F} \qquad (4.1)$$

$$V_{o2}(n+1/2) = -\frac{(C_{1S} + C_{1P})V_{REF-} + (C_{2S} + C_{2P} + C_{offset})V_{REF+}}{C_F} \qquad (4.2)$$

where $C_{1S} = C_{S0} + \Delta C_S$, $C_{2S} = C_{S0} - \Delta C_S$, C_{S0} is the nominal capacitance, ΔC_S is the ac incremental capacitance subject to acceleration. The offset compensation capacitor C_{offset} is programmed to a value that satisfies $C_{offset} + C_{2P} = C_{1P} = C_P$. Hence, (4.1) and (4.2) can be simplified as follows:

$$V_{o1}(n) = -\frac{\Delta C_S(V_{REF+} - V_{REF-})}{C_F} - \frac{(C_{S0} + C_P)(V_{REF+} + V_{REF-})}{C_F} \qquad (4.3)$$

$$V_{o2}(n+1/2) = -\frac{\Delta C_S(-V_{REF+} + V_{REF-})}{C_F} - \frac{(C_{S0} + C_P)(V_{REF+} + V_{REF-})}{C_F} \qquad (4.4)$$

Examining (4.3) and (4.4), it can be seen that the output signals V_{o1} and V_{o2} always have ac incremental signals with opposite magnitude. There may be a small common mode dc component under the condition that there is a mismatch between the magnitude of V_{REF+} and V_{REF-}. This residual common mode component can be cancelled by the subsequent differential-to-single-ended gain stage. With the assumption of $V_{REF+} = -V_{REF-}$, the dc component is cancelled and the above equations can be further simplified as follows:

$$V_{o1}(n) = -\frac{2V_{REF+}\Delta C_S}{C_F} \qquad (4.5)$$

$$V_{o2}(n+1/2) = \frac{2V_{REF+}\Delta C_S}{C_F} \tag{4.6}$$

Hence it can be concluded that due to the swapping action across the voltage references, V_{REF+} and V_{REF-}, during T_2 on-period, the as signal of the generated output V_{o2} is opposite in magnitude with respect to V_{o1}. As far as the time-multiplexing rate is much larger than the sensor signal frequency, the latency contributed by the switching duration of time-multiplex clock can be kept to minimum so as to reduce the sampled signal error due to latency. Therefore, the opposite cycle of converted electrical signal in the time-multiplexed based cross-coupling switching network will be very close to the magnitude of positive cycle generated by the single-ended CVC in the earlier time-multiplexing action. Hence, a time-multiplexed differential signal is established between V_{o1} and V_{o2}. This arrangement allows a simple single-ended CVC to perform the conversion of capacitive senor signal to a time-multiplexed output voltage signal in differential format.

This sensing scheme permits the low frequency error components such as 1/f noise, dc offset, switch errors contributed by charge injection and clock feed-through and thermal drift to be treated as common mode errors at the time-multiplexed differential output of the TMD-CVC. They will be simultaneously reduced by the following differential-to-single-ended gain stage. The detailed analysis of the low frequency error will be given in the following section 4.1.2. Unlike the classical fully differential structure [48], the matching requirement for the feedback capacitor, C_F, the reset switch, SW_1, and the symmetry requirement of op-amp implementation will be eliminated because the differential signal is generated by the same set of circuit components. This leads to smaller circuit error whilst without encountering the common-mode feedback circuit in the time-multiplexed differential circuit design. This offers

significant technical merits when compared to that of conventional differential CVC structures or prior-art single-ended CVCs (Fig. 3.7 and Fig. 3.11) as described earlier.

For capacitive sensor with large sensing and parasitic capacitances, the charging and discharging action in CVC will cause spikes because the voltages on the capacitors cannot change instantly. It needs time to charge or discharge to settle to the final values. The magnitude and duration of spikes depends upon the size of parasitic capacitances. It can be significant in bulk micro-machined capacitive sensors. On the contrary, it can be negligible in surface micro-machined capacitive sensors. The spikes will contribute dc offset of the sensing interface. It occurs when the reset signal Φ_1 is turned on or when T_1 or T_2 signals are turned on during the charge transfer phase. In order to minimize the impact of spikes, two special S/H sub clocks, T_{1s} and T_{2s}, are generated with the guard band, which rise up later and fall down earlier than the corresponding charge transfer clocks T_1 and T_2. The overall on-period is less than the respective period, T_1 and T_2. This arrangement ensures that the corresponding output signal being sampled to the associated holding capacitor is isolated first prior to the arrival of big spikes for the stated switching transitions. Ultimately, this gives the glitch free SC design with the dedicated S/H process which is one of the unique features in the proposed AZTMD-CVC design. Besides, the use of passive S/H circuits avoids the unnecessary increase of noise from the active counterparts. This helps the reduction of CVC circuit noise apart from the simplicity of the front-end interface.

4.2.2 Low Frequency Error and Finite Gain Error Analysis of AZTMD-CVC

4.2.2.1 Analysis of Op-Amp Offset, Flicker Noise and Charge Injection Error
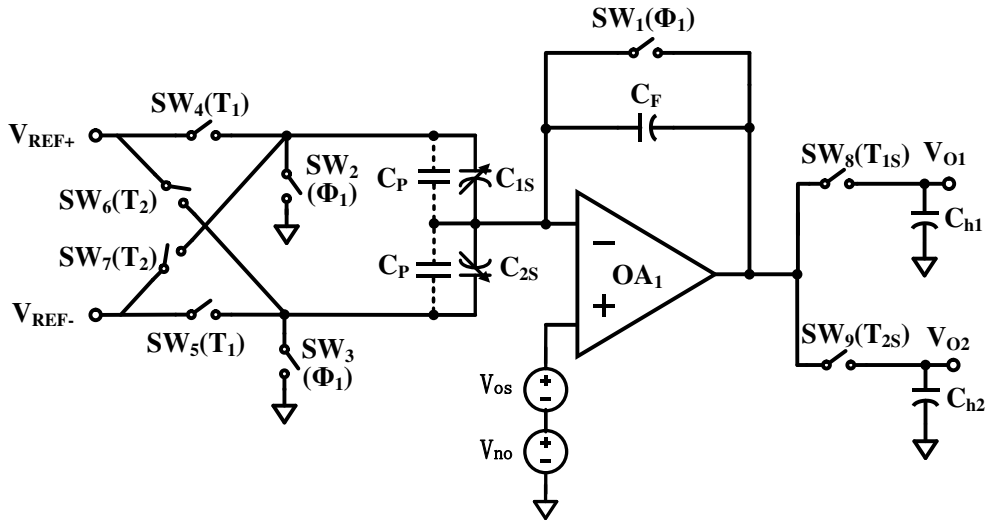
Fig. 4.3 AZTMD-CVC with offset and flicker noise error sources

When Φ_1 is on, the sensing cap C_{1S}, C_{2S} and the integration capacitor C_F as well as the op-amp will be reset. The offset voltage will charge up the sensing capacitors C_{1S} and C_{2S} as

$$Vc_{1S}(n) = Vc_{2S}(n) = -V_{os}(n) - V_{no}(n) \tag{4.7}$$

In next phase, Φ_1 is turned off, the channel charge of switch SW_1 will flow out to both the output node and the negative input node of the op-amp. The injected charge can be regarded as equal under fast clock waveforms. The half channel charge $Q_{SW_1}/2$ going to the negative input of the op-amp will cause a dc offset at the output while the other half will only cause a temporary glitch. When T_1 is

turned on, the reference voltage will start to charge up these two sensing capacitors. The charging current running through capacitor C_{1S} and C_{2S} is the same with the current through the feedback capacitor C_F. This yields

$$
\begin{aligned}
&[V_{REF+} - V_{os}(n) - V_{no}(n) - (-V_{os}(n) - V_{no}(n))](C_{1S} + C_P) + \\
&[V_{REF-} - V_{os}(n) - V_{no}(n) - (-V_{os}(n) - V_{no}(n))](C_{2S} + C_P) = \\
&[V_{os}(n) + V_{no}(n) - V_{o1}(n)]C_F - Q_{SW_1}(n)/2
\end{aligned}
\tag{4.8}
$$

$$
V_{o1}(n) = -\frac{\Delta C_S(V_{REF+} - V_{REF-})}{C_F} - \frac{(C_{S0} + C_P)(V_{REF+} + V_{REF-})}{C_F}
$$
$$
+ V_{os}(n) + V_{no}(n) - \frac{Q_{SW_1}(n)}{2C_F}
\tag{4.9}
$$

The first output voltage will be sampled by C_{h1}. The last four terms in (4.9), embedded with the box, are the reference mismatch induced dc component and the error offset voltages caused by respective op-amp offset, flicker noise and the switch charge injection error.

After T_1 is turned off, Φ_1 will be turned on, and the circuit will be in the reset mode again. The sensing capacitors will be charged up to

$$
Vc_{1S}(n + \frac{1}{2}) = Vc_{2S}(n + \frac{1}{2}) = -V_{os}(n + \frac{1}{2}) - V_{no}(n + \frac{1}{2})
\tag{4.10}
$$

In next phase, after Φ_1 is turned off, the same goes for the circuit, a fraction of the channel charge will cause a dc offset at the output. When T_2 is turned on, the swapped reference voltage will charge up the sensing capacitors. The same charging current flowing through C_{1S} and C_{2S} will charge up the feedback capacitor C_F. The nodal analysis shows that

$$[V_{ref-} - V_{os}(n+\frac{1}{2}) - V_{no}(n+\frac{1}{2}) - (-V_{os}(n+\frac{1}{2}) - V_{no}(n+\frac{1}{2}))](C_{1S} + C_P)$$

$$+[V_{ref+} - V_{os}(n+\frac{1}{2}) - V_{no}(n+\frac{1}{2}) - (-V_{os}(n+\frac{1}{2}) - V_{no}(n+\frac{1}{2}))](C_{2S} + C_P) \qquad (4.11)$$

$$= [V_{os}(n+\frac{1}{2}) + V_{no}(n+\frac{1}{2}) - V_{o2}(n+\frac{1}{2})]C_F - Q_{SW_1}(n+\frac{1}{2})/2$$

$$V_{o2}\left(n+\frac{1}{2}\right) = -\frac{\Delta C_S(-V_{REF+} + V_{REF-})}{C_F} - \frac{(C_{S0} + C_P)(V_{REF+} + V_{REF-})}{C_F}$$

$$+V_{os}(n+\frac{1}{2}) + V_{no}(n+\frac{1}{2}) - \frac{Q_{SW_1}(n+\frac{1}{2})}{2C_F} \qquad (4.12)$$

The second output voltage will be sampled by C_{h2}. The last four terms in the box are the reference mismatch induced dc component and the error voltages caused by respective op-amp offset, flicker noise and the switch charge injection error. Since these four terms independent of time, this error voltage can be regarded as a lumped common mode component which will be eliminated by the differential operation at the next stage.

Comparing equation (4.9) and (4.12), it has shown that there is a half clock period delay between these two output signals. Since the sampling clock frequency (10kHz) is much larger than the signal frequency (0~100Hz), the delay can be deemed as negligible, suggesting that the two output ac signals can be treated as a differential output.

4.2.2.2 Finite Gain Error Analysis
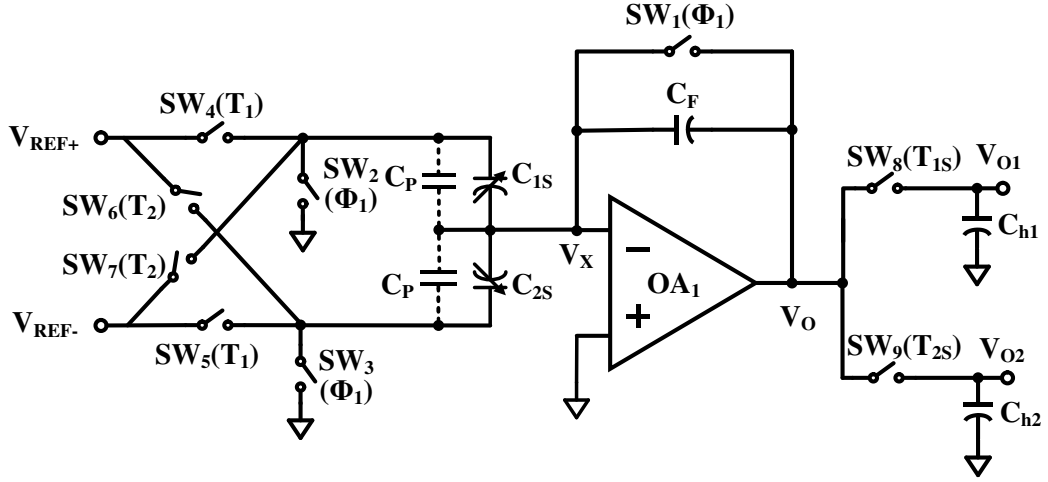
Fig. 4.4 AZTMD-CVC for finite gain error analysis

A_v is the finite open-loop gain of the charge amplifier. V_X is the voltage at the negative input node of the op-amp. By nodal analysis and taking into second order effects into account, we obtain $V_{o1}(n)$ with finite op-amp gain as follows,

$$\left[V_{o1}(n) - V_X\right]C_F = (V_X - V_{REF+})(C_{1S} + C_P) + (V_X - V_{REF-})(C_{2S} + C_P) \tag{4.13}$$

$$V_o(n) = -A_v V_X \tag{4.14}$$

Solving (4.14) and (4.13) with the assumption of $V_{REF+} = -V_{REF-}$, we can get

$$V_{o1}(n) = -\frac{2V_{REF+}\Delta C_S A_v}{C_F\left(1 + \dfrac{2C_P + C_{1S} + C_{2S} + C_F}{A_v C_F}\right)} \tag{4.15}$$

The same goes for $V_{o2}\left(n + \dfrac{1}{2}\right)$. Thus by nodal analysis, we have

$$\left[V_{o2}\left(n + \frac{1}{2}\right) - V_X\right]C_F = (V_X - V_{REF+})(C_{1S} + C_P) + (V_X - V_{REF-})(C_{2S} + C_P) \tag{4.16}$$

$$V_o\left(n + \frac{1}{2}\right) = -A_v V_X \tag{4.17}$$

75

Solving (4.16) and (4.17), we can obtain

$$V_{o2}\left(n+\frac{1}{2}\right)=\frac{2V_{REF+}\cdot\Delta C_S A_v}{C_F(1+\dfrac{2C_P+C_{1S}+C_{2S}+C_F}{A_v C_F})} \tag{4.18}$$

Similar to the ZI-CVC case, the factor $\dfrac{2C_P+C_{1S}+C_{2S}+C_F}{A_v C_F}$ in (4.15) and (4.18)

represent the magnitude error which is inversely proportional to A_v and is approximately to be 0 when A_v tends to infinity. In order to reduce this gain error, A_v should be designed to be high enough and the parasitic capacitance associated with the sensor device should be kept as small as possible.

4.2.3 Thermal Noise Analysis & Noise-Power Optimization of the AZTMD-CVC

The overall system noise performance metric is characterized by the total noise equivalent acceleration (*TNEA*) which is determined by the sensor Brownian noise equivalent acceleration (*BNEA*) and the circuit noise equivalent acceleration (*CNEA*). The relationship is defined as follows:

$$TNEA = \sqrt{BNEA^2 + CNEA^2} \tag{4.19}$$

In this design, the bulk micro-machined sensor device achieves a low Brownian noise level of less than 1 µg/√Hz, making *CNEA* the limiting factor of the total system noise level. For tradeoff design, there always exists a compromise between noise and power consumption in an electronic system. Lower circuit noise typically requires higher power consumption and vice versa. Therefore, it is imperative to examine the key parameters pertaining to the output noise PSD of the SC CVC with respect to the power consumption. Since both the accelerometer sensing capacitance and the integration capacitor used in the

interface circuit are large, the KT/C noise is negligible with respect to the amplifier noise comprising 1/f noise and wide band thermal noise. As interpreted in section A, the amplifier offset and 1/f flicker noise can be treated as common-mode errors. They can be cancelled at the time-multiplexed differential voltage output, leaving the wideband thermal noise as the dominant noise factor in the interface circuit. Hence, the thermal noise-power optimization becomes the major design strategy for low-noise front-end electronic interface. Lots of works [49]-[52] have been reported in addressing the noise issue in SC circuits using various methods and providing useful noise simulation methods for circuits working in DT domain. This section will present the noise analysis and noise-power optimization of the SC based AZTMD-CVC interface.

Fig. 4.5 depicts the push-pull current mirror based operational transconductance amplifier (OTA) topology [53] in this AZTMD-CVC. According to the current ratio setting in the current mirror transistors, the total current I_{tot} drawn by the core OTA is 5 times with respect to the respective drain current I_D biasing the transistors

Fig. 4.5 Schematic of the push-pull current mirror core OTA

MP$_7$ and MP$_8$ in the differential pair. For low-noise design consideration, the OTA is designed in a way that the aspect ratio of the differential input pair transistors MP$_7$ and MP$_8$ are significantly larger (600 µm/1 µm) than that of the current mirror transistors MN$_3$ (30 µm/50 µm) and MP$_1$ (10 µm/15 µm). The cascode transistors (MP$_3$-MP$_4$, MP$_6$, MN$_1$-MN$_2$, MN$_5$-MN$_6$) do not contribute significant output noise due to large source degeneration. The same goes for the tail current source transistor MP$_5$ which has very small transconductance value. Hence, the OTA input-referred noise PSD mainly comes from the input pair and the active current mirror loads. The derived result is obtained as follows:

$$S_{nop} = \frac{16KT}{3g_{mp7}}(1+\frac{7}{4}\cdot\frac{g_{mn3}}{g_{mp7}}+\frac{3}{4}\cdot\frac{g_{mp1}}{g_{mp7}}) \approx \frac{16KT}{3g_{mp7}} \tag{4.20}$$

where $g_{mp7} \gg g_{mp1}$, $g_{mp7} \gg g_{mp3}$, g_{mn3}, g_{mp1}, g_{mp7} are the respective transconductance of transistors, K is the Boltzman's constant, T is the temperature in Kelvin.

Fig. 4.6 Noise signal processing in the AZTMD-CVC interface

Fig. 4.6 illustrates the thermal noise model in the SC interface circuit. It is assumed that the parasitic capacitances associated with the sensor device are balanced such that $C_{1P} = C_{2P} + C_{offset} = C_P$. During the reset phase Φ_1 and charge sensing phase T_1 or T_2, the broadband thermal noise entering the system is directly amplified and low-pass filtered by the SC interface with respective continuous-time circuit transfer functions of $H(s)$. Between the transitions of these two working phases, the noise source is sampled at the end of the reset phase and later transferred to the output as a sampled-data signal during the charge transfer phase. Fig. 4.7(a) and (b) show the equivalent configuration of the AZTMD-CVC for noise calculation during the reset phase and the charge transfer phase on either T_1 or T_2, respectively.
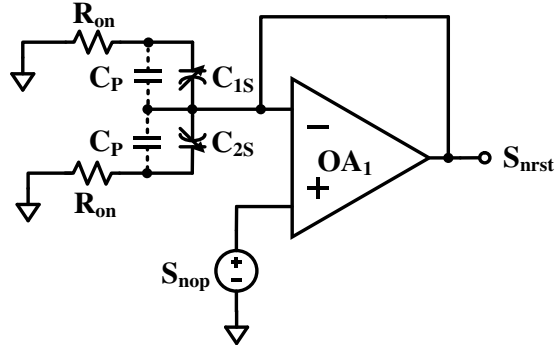
(a)
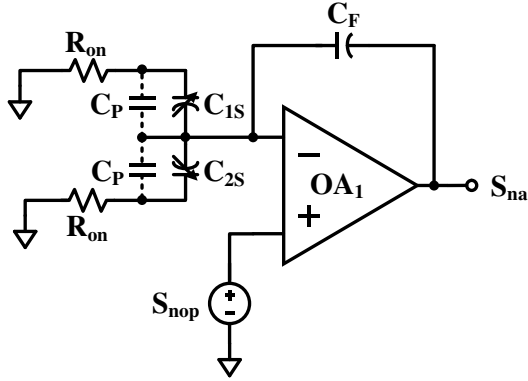
(b)

Fig. 4.7 Equivalent circuit configuration for noise calculation during (a) reset phase and (b) charge transfer phase

It is noted that R_{on} represents the switch-on resistance. Based on the SC thermal noise analysis in Fig. 4.6, the noise PSD S_{no} at the output of the charge sensing amplifier is summed as follows:

$$S_{no}(\omega) = S_{nrst}(\omega) + S_{na}(\omega) + S_{SH}(\omega T) \tag{4.21}$$

where $S_{nrst}(\omega)$ and $S_{na}(\omega)$ are the two broadband continuous-time components during the reset phase in Fig. 4.7(a) and the charge transfer phase in Fig. 4.7(b), respectively. They are derived as follows:

$$S_{nrst}(\omega) = \frac{S_{nop}}{2(1 + \frac{\omega^2}{\omega_u{}^2})} \tag{4.22}$$

$$S_{na}(\omega) = \frac{S_{nop} \cdot (1+\alpha)^2}{2[1+\omega^2 \left(\dfrac{1+\alpha}{\omega_u}\right)^2]} \tag{4.23}$$

where $(1+\alpha)$ is the noise gain factor, $\alpha = (C_{1S}+C_{2S}+2C_P)/C_F > 1$.

From (4.23), the interface noise gain factor $(1+\alpha)$ during the amplification phase will increase with the parasitic capacitances. High parasitic capacitances will significantly enhance the noise gain and they are unavoidable. $S_{SH}(\omega T)$ in (4.21) is the narrowband S/H component. It is obtained as

$$S_{SH}(\omega T) = \frac{\pi f_u}{(1+\alpha)f_s} \cdot S_{nop} \cdot \left| -\alpha \cdot \frac{z^{-\frac{1}{2}}}{j2\sin(\dfrac{\omega T}{2})} \right|^2 \cdot \sin c^2(\frac{\omega T}{2}) \tag{4.24}$$

It is the result of multiplying the op-amp equivalent input-referred noise PSD S_{nop} by the square of the unit cycle z-transform transfer function and the undersampling ratio, $(\pi f_u)/[(1+\alpha)f_s]$, weighted by $\sin^2 c(\omega T/2)$ [52].

Refer to Fig. 4.6, the output noise S_{no} of the charge sensing amplifier is then sampled by capacitor C_{h1} and C_{h2} during on-period of T_{1s} and T_{2s}. This process results in two sampled noise components S_{no1} and S_{no2} accordingly. During this sampling process, the two broadband continuous-time noise components, S_{nrst} (ω) in Fig. 4.7(a) and S_{na} (ω) in Fig. 4.7(b) being contained in S_{no} (ω) are undersampled because the noise cutoff frequency determined by the SC interface network is higher than the sampling frequency. The sampled results can be calculated using the same method as that of $S_{SH}(\omega T)$. The low frequency noise PSD S_{no1} is obtained as follows:

$$S_{no1} = S_{nop} \cdot \frac{\pi f_u}{2f_s} + S_{nop} \cdot (1+\alpha) \cdot \frac{\pi f_u}{2f_s} + S_{nop} \cdot \alpha \cdot \frac{\pi f_u}{f_s} = S_{nop} \cdot (1+\frac{3}{2}\alpha) \cdot \frac{\pi f_u}{f_s} \tag{4.25}$$

Since all the samples of the output noise signal are sampled from the same

noise source S_{no} by the capacitors C_{h1} and C_{h2} with the same sampling rate, the PSD of S_{no1} and S_{no2} are of the same value and they are uncorrelated with each other. As a result, the overall output noise $S_{nototal}$ arising from the time-multiplexed differential output ($V_{o1} - V_{o2}$) can be obtained as

$$S_{nototal} = S_{no1} + S_{no2} = 2S_{no1} = S_{nop} \cdot (2 + 3\alpha) \cdot \frac{\pi f_u}{f_s} \approx \frac{16KT}{3g_{mp7}} \cdot (2 + 3\alpha) \cdot \frac{\pi f_u}{f_s} \qquad (4.26)$$

From (4.26), it can be concluded that the overall output noise is a function of the transconductance g_{mp7}, the noise gain factor α and the undersampling ratio $(\pi f_\mu)/f_s$. Since both the sensing capacitance and parasitic capacitance value are quite large (at least several tens pF) for the bulk micro-machined sensor device in this design, the input capacitance of the charge sensing amplifier for the interface circuit has negligible effect on total noise gain factor. This is in contrast with that of the surface micro-machined sensor device [54] which features small sensing capacitance. The parasitic capacitances will be translated to the increase of power consumption for meeting a particular high sensitivity requirement. Therefore, apart from very low-noise OTA design and the SC thermal noise analysis for the front-end interface, the low-noise and low-power optimization strategy needs to be addressed for the front-end interface design. It is discussed in the following.
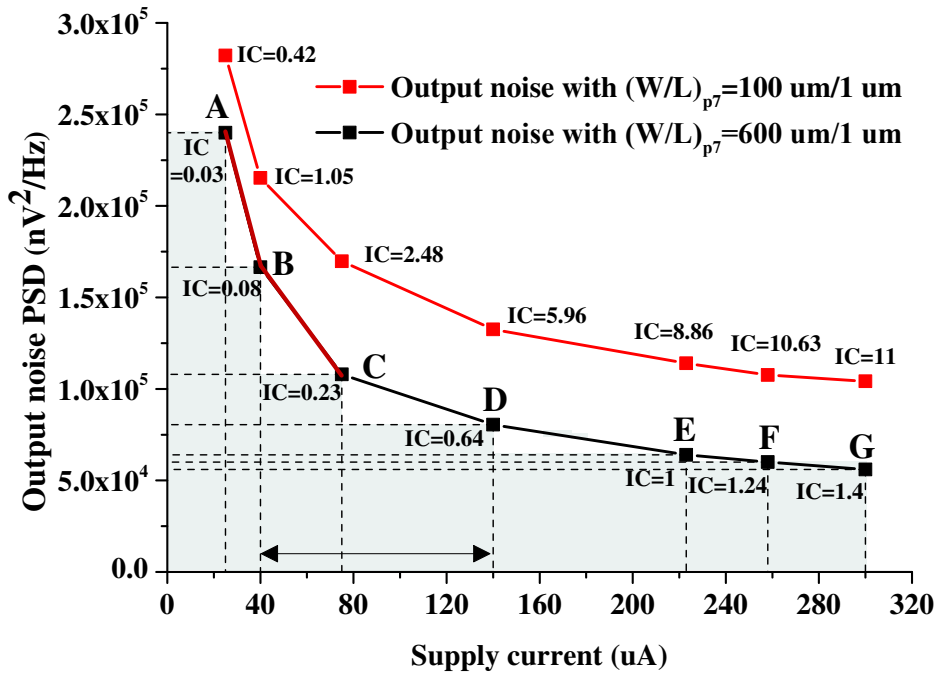
Fig. 4.8 AZTMD-CVC output noise PSD under different supply currents

Fig. 4.8 shows the simulation results of the output noise PSD $S_{nototal}$ of the AZTMD-CVC adopting different OTA input pair transistor aspect ratios at different I_D biasing currents, with the relationship that the supply current $I_{tot} = 5I_D$. It is noted that the unity gain frequency is maintained constant through keeping the constant ratio of g_{mp7} and C_{load}. From the two curves, when the core OTA's current consumption increases, $S_{nototal}$ keeps on decreasing but at a reduced rate, which indicates a reduction of the noise-power efficiency. Refer to the design using $W/L = 600\ \mu m/1\ \mu m$, each segmented area is formed by the multiplication of the output noise PSD and the supply current. The area represents the noise-power product (NPP) which shows the noise-power trade-off relationship. It can be seen that the noise-power area keeps on increasing nonlinearly with the increase of the current. Besides, by comparing these two output noise curves, the design with large aspect ratio indicates better NPP

which yields lower noise with effective input power. Based on the SC thermal noise analysis result of the interface circuit given in (4.26), the NPP can be expressed as

$$NPP = S_{nototal} \cdot I_{tot} \approx \frac{16KT}{3g_{mp7}} \cdot (2+3\alpha) \cdot \frac{\pi f_u}{f_s} \cdot I_{tot} = A \cdot \frac{I_D}{g_{mp7}} \tag{4.27}$$

where $I_{tot} = 5I_D$ is the total current drawn by the AZTMD-CVC OTA, A is a constant coefficient which is equal to $[80KT(2+3\alpha)\cdot\pi f_u]/3f_s$. According to [53] [55], the relative transconductance in all the transistor inversion regions is defined as

$$\frac{g_{mp7}}{I_D} \approx \frac{\kappa}{V_T} \cdot \frac{2}{1+\sqrt{1+4 \cdot IC}} \tag{4.28}$$

where κ is the subthreshold gate coupling coefficient, V_T is the thermal voltage, the inversion coefficient $IC = I_D/I_S$ as indicated in Fig. 4.7 is the ratio of the transistor drain current I_D over the moderate inversion characteristic current I_S. Substituting (4.28) into (4.27), we can get

$$NPP = A \cdot \frac{V_T}{\kappa} \cdot \frac{1+\sqrt{1+4 I_D/I_S}}{2} \tag{4.29}$$

From (4.29), the NPP is approximately linear with I_D when $4IC < 1$, else it becomes nonlinear function. The results of Fig. 4.7 have shown that the point C represents the optimal bias current when $I_D = 15$ µA or $I_{tot} = 75$ µA for this noise-power optimization design because it yields low noise while the power is not excessively increased.

4.2.4 Single Voltage Reference Based AZTMD-CVC and Multiple-Channel Implementation

The AZTMD-CVC can have different embodiments which are described in the following. This time-multiplexed differential output technique can also be implemented with a single voltage reference based time-multiplexed design as shown in Fig. 4.9. The multiplexing action is based on the two switching periods T_1 and T_2 that involve the connection of respective switches associated with the sensing capacitors C_{1s}, C_{2s} and the reset phase of amplifier. Contrasting to the differential voltage reference design, each switching period (T_1 or T_2) embodies two clock sequences. They are (i) a sub clock phase either T_{1s} or T_{2s} and (ii) a reset signal Φ_1. With respective sample-and-hold circuit located at the output of switched-capacitor amplifier, a time-multiplexed differential signal is equally generated.

Besides, these two schemes can be further extended to multi-channel time-multiplexed version as illustrated in Fig. 4.10 and Fig. 4.11. By properly choosing the charge transfer control clocks and enabling clocks, it is easy to achieve multichannel time-multiplexed differential output with a single-ended CVC. The channel enabling control clocks can provide the activation between respective sensor and readout circuit whilst isolating other unused sensing elements.
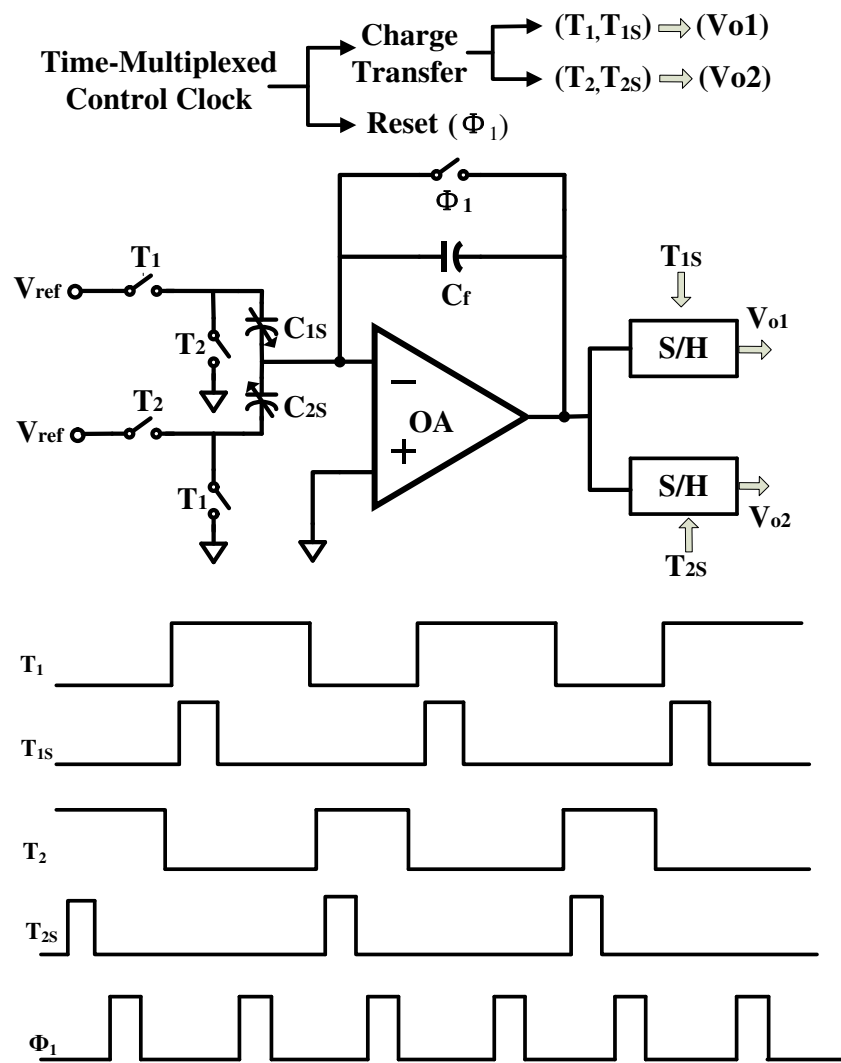
Fig. 4.9 Single voltage reference based AZTMD-CVC and its control clocks
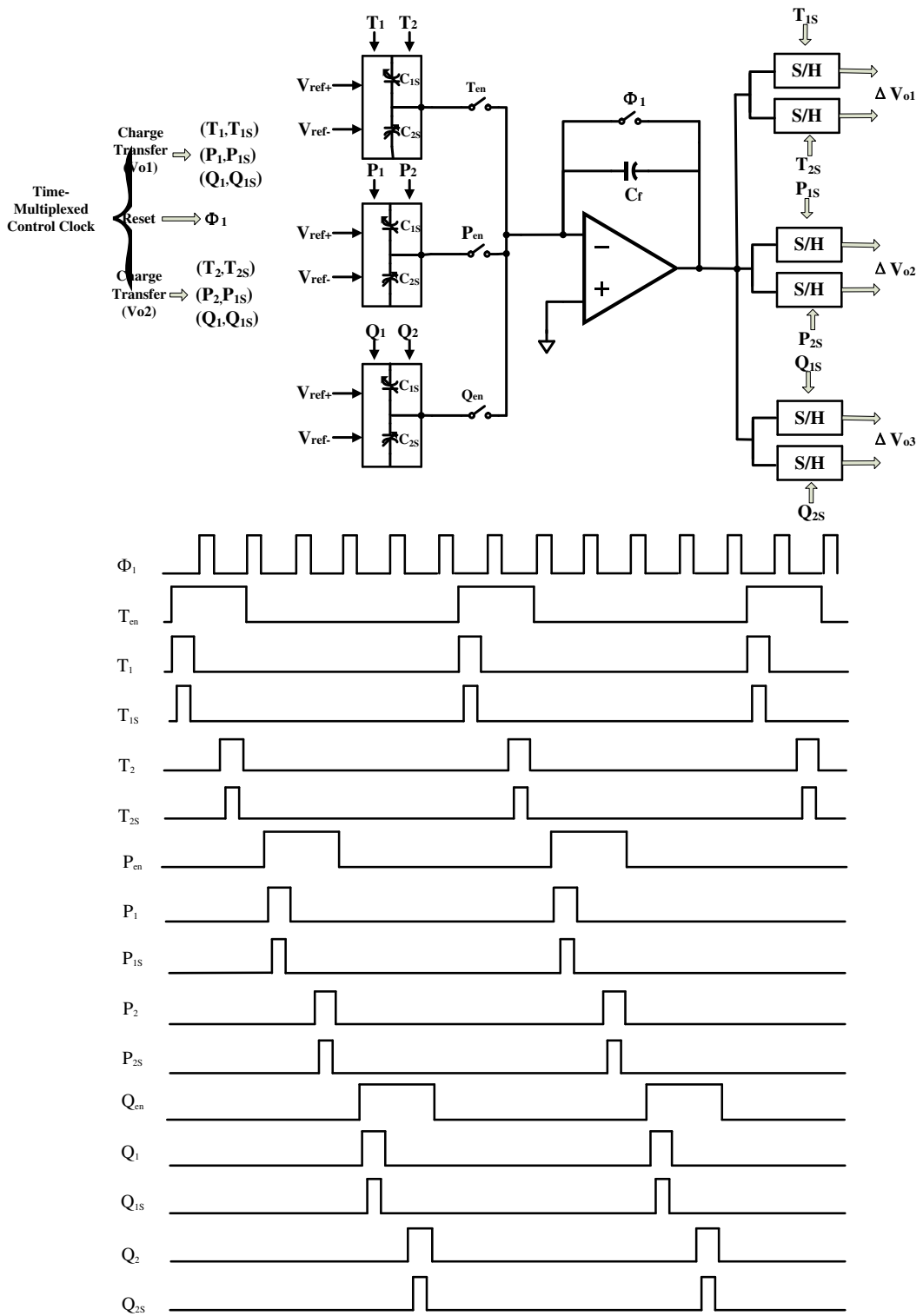
Fig. 4.10 Multi-channel AZTMD-CVC and its control clocks based on Fig. 2
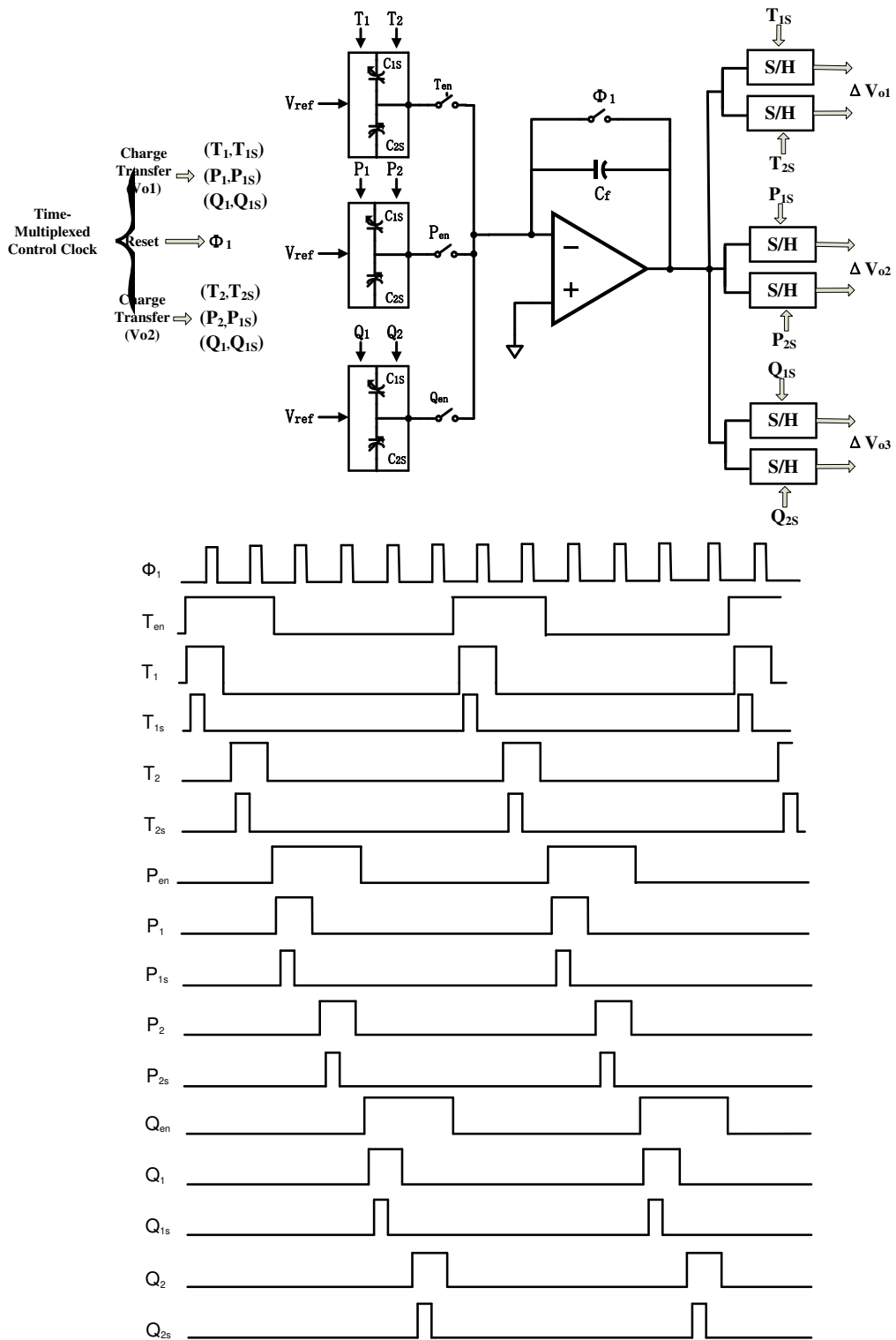
Fig. 4.11 Multi-channel single reference voltage based AZTMD-CVC and its control clocks

4.2.5 Comparison of the OCC-CVC, ZI-CVC, SETFD-CVC and AZTMD-CVC

The three CVC circuits and the proposed AZTMD-CVC circuit designs are implemented using AMS 0.35µm CMOS technology. The identical differential accelerometer capacitive sensor model in Verilog-A language is used for both OCC-CVC and TMD-CVC, while a simple two terminal capacitive sensor model is used for both ZI-CVC and the SETFD-CVC scheme. It is noted that a balanced symmetrical capacitance sensor model is assumed for both the analysis and simulations of these electronic readout circuits. The reference voltage is set as $\pm V_{REF} = \pm 1.5V$, while the input acceleration is represented by a sinusoidal voltage source. The voltage change to acceleration scale is 1 to 1 (voltage change of 1V represents 1g acceleration).The SC amplifier as well as the feedback capacitances of these three schemes are set to have the identical value in order to get the same output swing. Since the sensor in Zoom-in CVC scheme is a single capacitor sensing structure, the output swing is half of those in OCC-CVC, AZTMD-CVC and SETFD-CVC.

The dc offset for OCC-CVC, ZI-CVC, SETFD-CVC and AZTMD-CVC are simulated over the temperature range of -40° to 90°C so as to study their temperature dependence. The simulated results are shown in Fig. 4.12.

As can be seen from the thermal drift simulation results in Fig. 4.12, it shows the temperature dependence of the dc offset over the temperature range of -40° to 90°C, the thermal drift is much smaller in AZTMD-CVC circuit than those in the OCC-CVC, ZI-CVC and SETFD-CVC circuits. This simulation results have confirmed the advantages of improved dc offset and thermal drift performance with the time-multiplexed differential output using the single-end structure in

the AZTMD-CVC. Furthermore, the transient simulation results under 1g and 0.1mg acceleration are shown from Fig. 4.13 to Fig. 4.32. By examining the transient simulation results under 0.1mg acceleration, it can be observed that the dc offset of differential output of AZTMD-CVC circuit is considerably smaller than the other three readout circuits. The output waveforms, under various levels of ac acceleration, display relatively clean. Table 4.1 compares the simulated results for these three circuits.

Table 4.1 Comparison of simulated circuit performance for the four CVCs

Parameters	[39] OCC-CVC	[40] ZI-CVC	[41] SETFD-CVC	AZTMD-CVC
DC Offset	1.36mV	-0.55mV	4.3mV	1.1μV
Offset drift with temperature (-40 to +90°C) [μV/°C]	0.49	1.03	17.7	0.01
Output noise (0~200Hz) [μV]	6.14	4.14	11.5	8.53
Output Signal Swing [mV$_p$]	+/-254	+152.8/-101	+140.8/-107.5	+/-508
SNR (0~200Hz) [dB]	89.3	89.7	78	92.5
Power Consumption [mW]	0.8	0.4	1.5	0.4

In terms of DC offset and offset drift performance, the AZTMD-CVC structure significantly outperforms the three readout circuits due to its circuit simplicity and the elimination of the matching requirement of the charge transfer

components. The result of the integrated output noise over the frequency range of 0~200Hz shows that the ZI-CVC has the lowest output noise due to its reset phase noise cancellation technique. The second cascaded offset-cancellation stage induces excessive output noise in the OCC-CVC scheme. The proposed AZTMD-CVC has slightly bigger output noise than both of these two schemes because of the two uncorrelated noise sampling process between the two time-multiplexed differential output. However, under the same gain setting parameters, the output signal magnitude of the AZTMD-CVC is doubled with respect to that of the OCC-CVC and is four times of that of the ZI-CVC output. The SETFD-CVC displays worse noise performance which is arose from non-CDS technique as well as the hold operation after the first charge transfer phase. The AZTMD-CVC technique exhibits better SNR performance while achieving similar power consumption when compared with the other schemes. The simulation results have demonstrated that the AZTMD-CVC structure outperforms the three readout circuits. This is due to its simple circuit structure.

OCC-CVC Thermal Drift

ZI-CVC Thermal Drift

SETFD-CVC Thermal Drift

AZTMD-CVC Thermal Drift
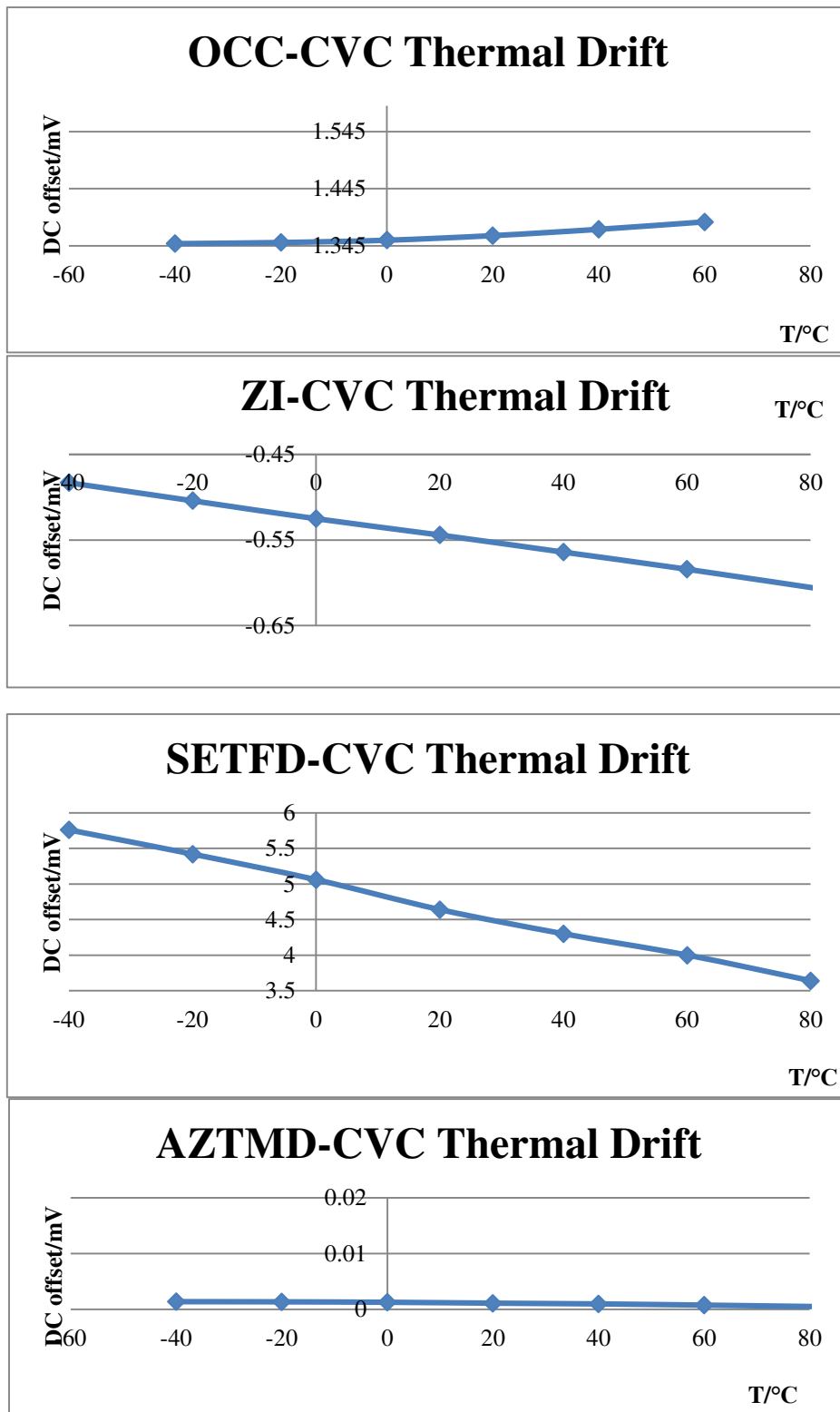
Fig. 4.12 Simulated thermal drift of the DC offset for the four CVC circuits

Simulated output waveforms under 1g sinusoidal acceleration
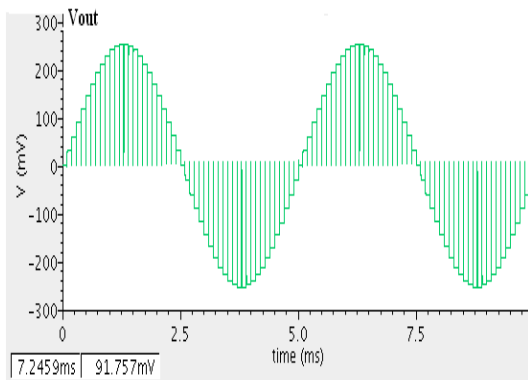
Fig.4.13 Output waveform V$_{out}$ of OCC-CVC after S&H
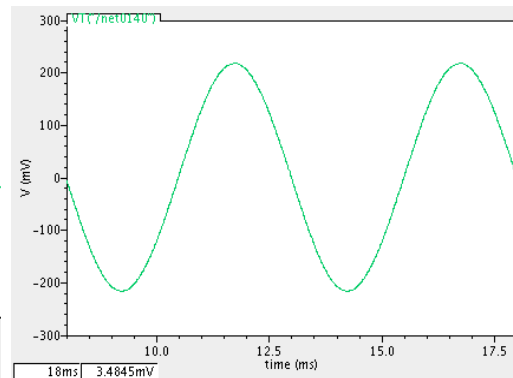
Fig. 4.14 Output response of OCC-CVC after an ideal 330Hz filter
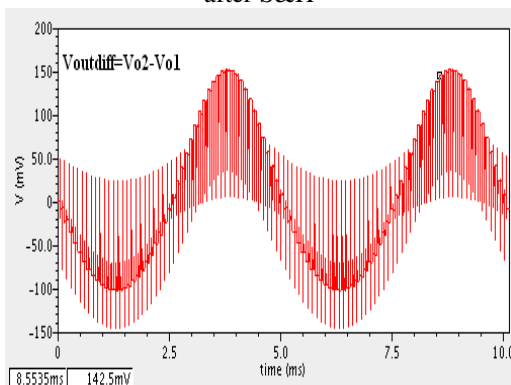
Fig. 4.15 Differential output waveform V$_{outdiff}$ of ZI-CVC after S&H
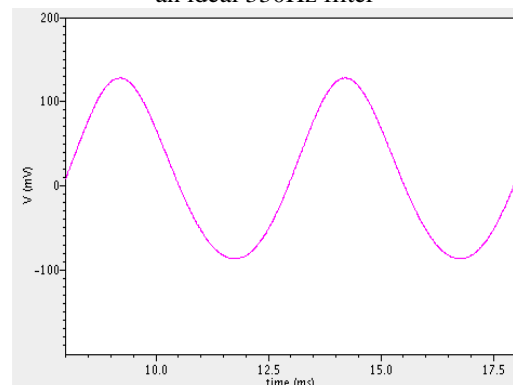
Fig. 4.16 Output response of ZI-CVC after an ideal 330Hz filter
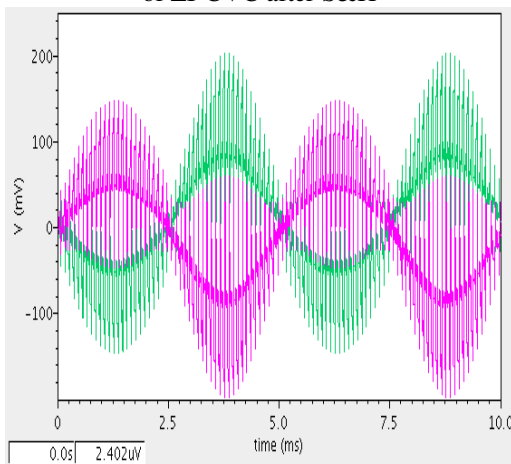
Fig. 4.17 Output waveform of the SETFD-CVC with a simple two terminal sensor device
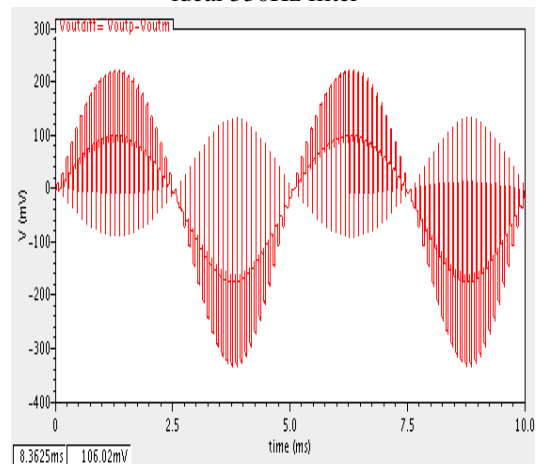
Fig. 4.18 Differential output waveform (without filtering) of the SETFD-CVC with a simple two terminal sensor device

93
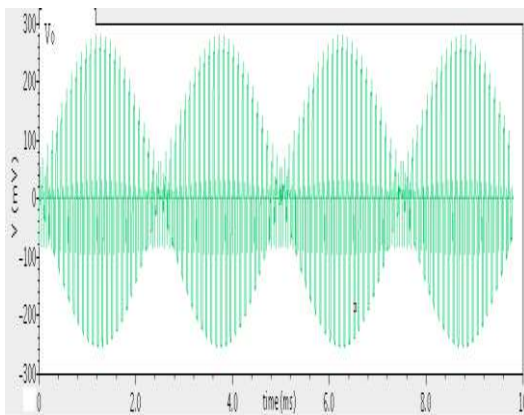
Fig. 4.19 Output waveform Vo of AZTMD-
CVC before S&H
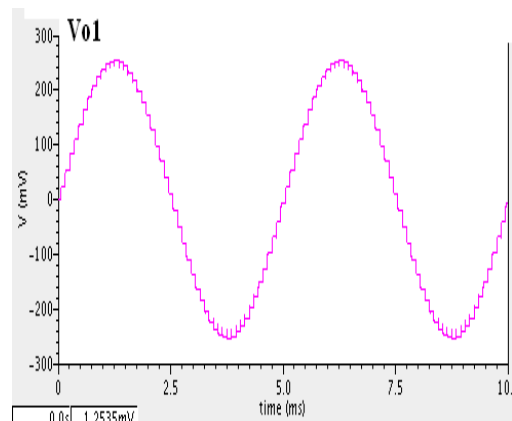
Fig. 4.20 Output waveform Vo_1 of AZTMD-
CVC after S&H
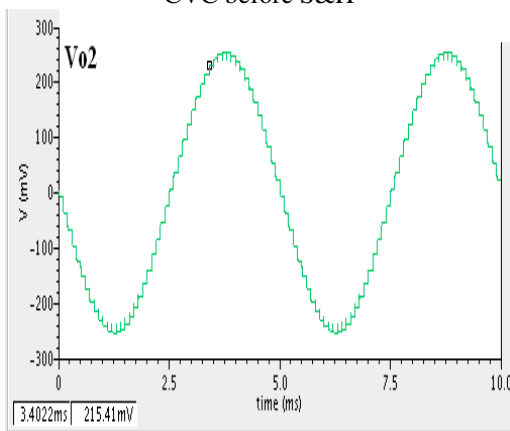
Fig. 4.21 Output waveform Vo_2 of AZTMD-
CVC after S&H
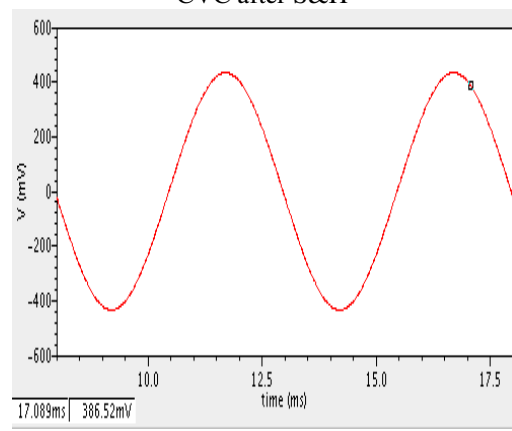
Fig. 4.22 Differential output waveform $V_{outdiff}$
of AZTMD-CVC after an ideal 330Hz filter

Simulated output waveforms under 0.1mg sinusoidal acceleration
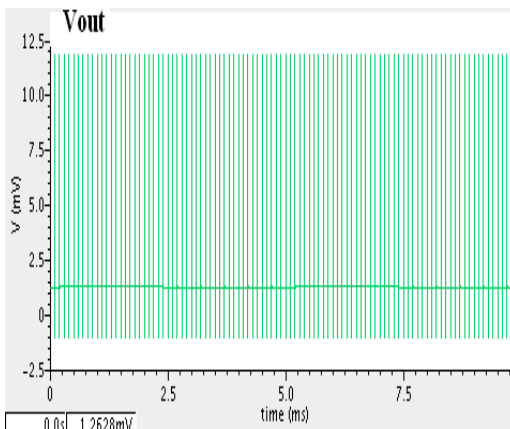
Fig. 4.23 Output waveform V_{out} of OCC-CVC
after S&H
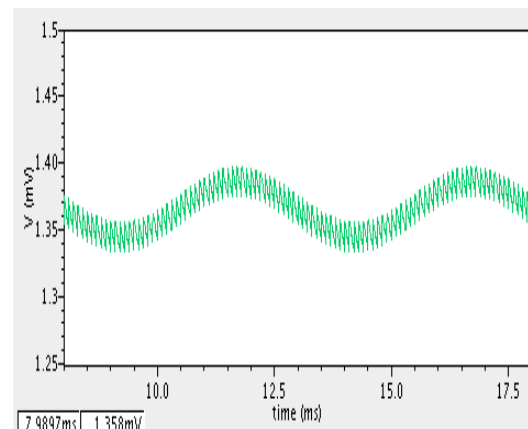
Fig. 4.24 Output response of OCC-CVC after
an ideal 330 Hz filter
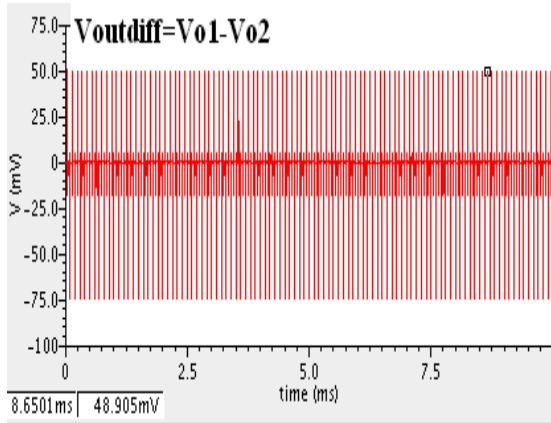
Fig. 4.25 Differential output waveform $V_{outdiff}$ of ZI-CVC after S&H
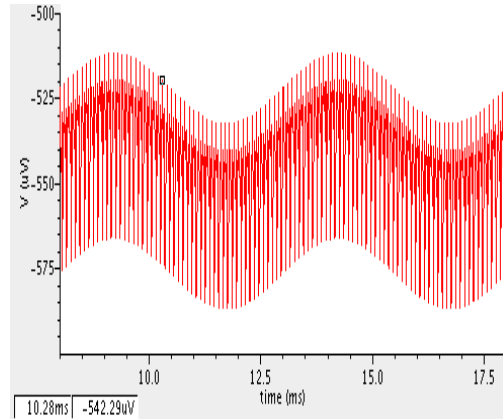
Fig. 4.26 Output response of ZI-CVC after an ideal 330Hz filter
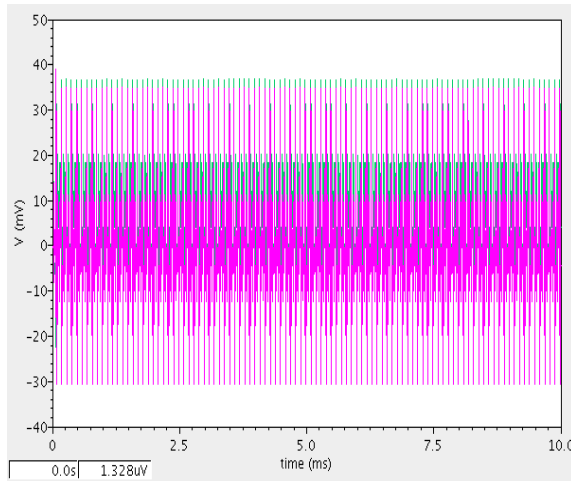
Fig. 4.27 Output waveform of the SETFD-CVC with a simple two terminal sensor device
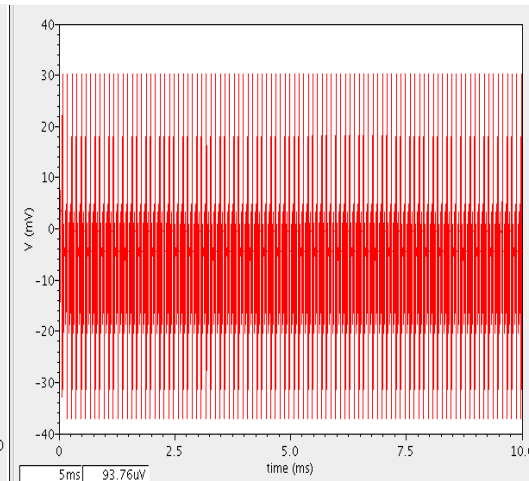
Fig. 4.28 Differential output waveform of the SETFD-CVC with a simple two terminal sensor device
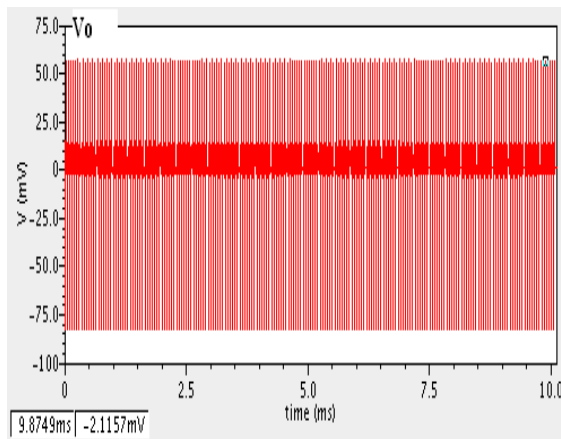
Fig. 4.29 Output waveform Vo of AZTMD-CVC before S&H
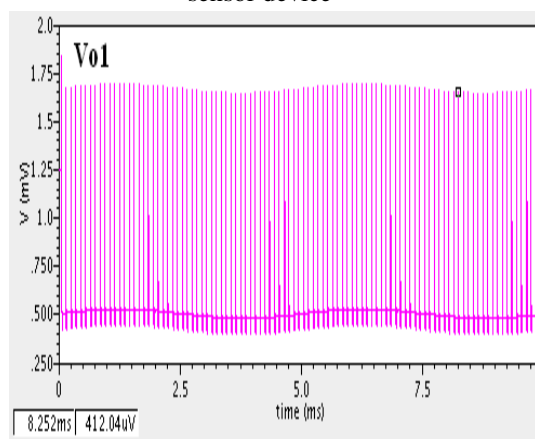
Fig. 4.30 Output waveform Vo_1 of AZTMD-CVC after S&H
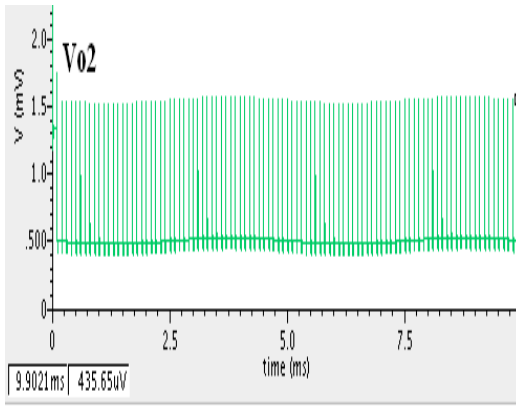
Fig. 4.31 Output waveform Vo$_2$ of AZTMD-CVC after S&H
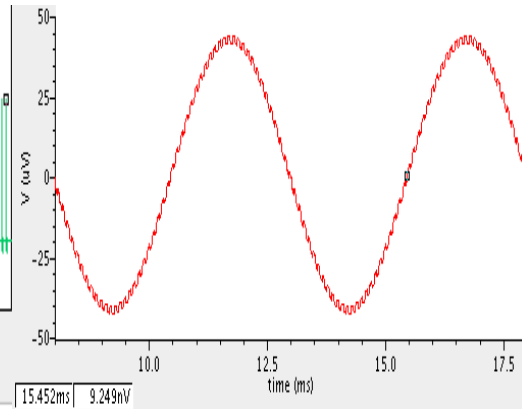
Fig. 4.32 Differential output waveform V$_{outdiff}$ of AZTMD-CVC after an ideal 330Hz filter

4.3 Differential-to-Single-Ended Programmable SC Gain Amplifier

The passive S/H outputs of AZTMD-CVC will be coupled to a SC amplifier for scaling the sensing signal. Fig. 4.33 depicts the schematic of the SC-CDS differential-to-single-ended programmable gain stage together with its control clocks. A 5-bit programmable capacitor array (PCA) is implemented in parallel with the feedback capacitors C_2 and C'_2. This permits the adjustment of second voltage gain stage so that it can compensate the gain variation from the sensor device. Since the signal coupling is based on passive capacitive components, charge sharing effect will occur between capacitor C_{h1} and C_1. The same goes for C_{h2} and C'_1. Taking into account of charge redistribution, the effective input voltages across capacitor C_1 and C'_1 become

$$V_{o1}^* = \frac{C_{h1}}{C_{h1} + C_1} V_{o1} \;,\; V_{o2}^* = \frac{C_{h2}}{C_{h2} + C'_1} V_{o2} \tag{4.30}$$

Therefore, the output signal after the programmable gain stage yields

96

$$V_{out} = \frac{C_1}{C_2 + C_{PCA}} \left(V_{o1}^* - V_{o2}^* \right) = - \frac{C_1}{C_2 + C_{PCA}} \cdot \frac{C_{h1}}{C_{h1} + C_1} \cdot \frac{2V_{REF+}\Delta C_S}{C_F} \qquad (4.31)$$

It is noted that capacitor C_1 is made 6 times smaller than the S/H capacitor C_{h1} to minimize the signal attenuation due to charge sharing effect between the capacitors.
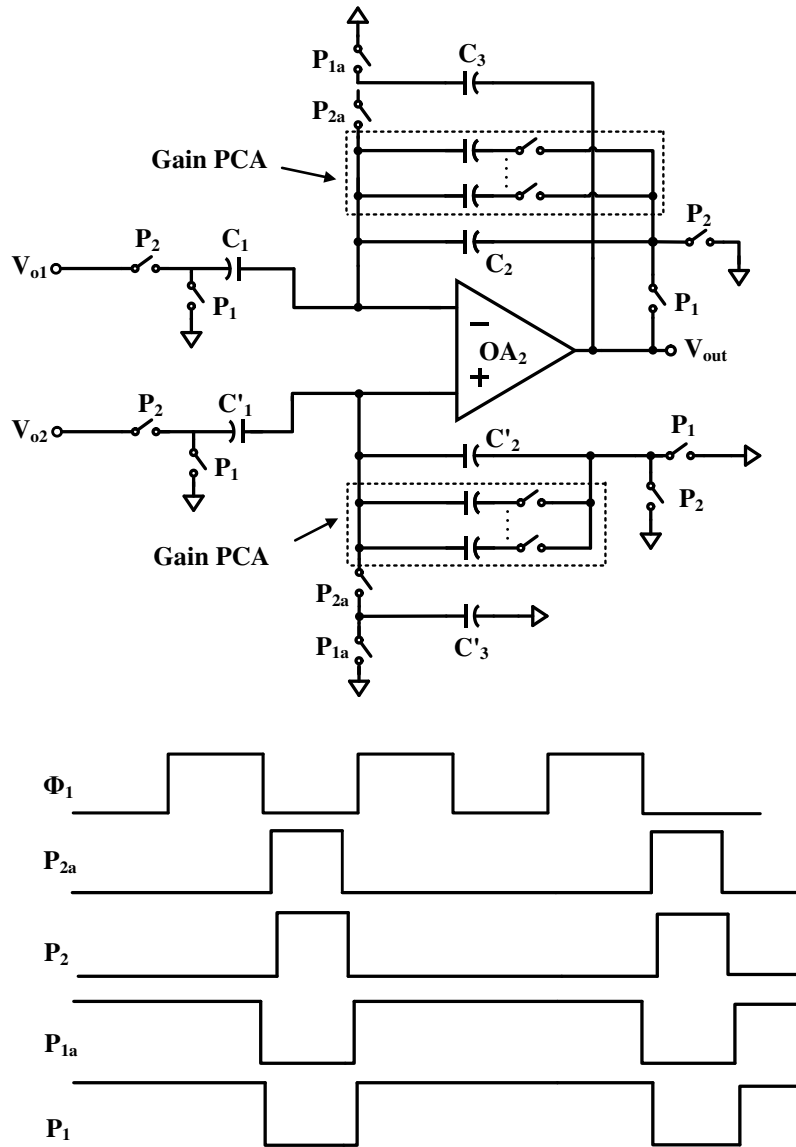
Fig. 4.33 Schematic of the differential-to-single-ended programmable SC-CDS gain stage with its control clocks with respect to reset clock Φ_1

4.4 Low-Offset Low-Noise Output Buffer

4.4.1 Low-Offset Design Considerations

It is well known that there are two kinds of offsets residing in a CMOS amplifier: systematic offset and random offset. Systematic offset typically results from improper circuit design. Basically, it is caused by the drain potential difference in a pair of load transistors, which can be avoidable when the current ratios are set properly. On the contrary, random offset is highly related to the fabrication process of IC devices, which is hard to be predicted at the design stage and will typically become the dominant offset source of a fabricated amplifier. The typical imperfect fabrication phenomenon includes non-uniform doping concentrations in the bulk and substrate, non-uniform implants in the gate oxide for threshold adjustment as well as implantation induced surface charge and edge effects. The non-uniform doping concentrations in the bulk and implantations in the gate oxide will cause threshold mismatch, while the oxide, edge effects, non-uniform substrate doping and surface charge effect will result in transconductance mismatch. Of these mismatches between the device pairs, they are supposed to be identical to avoid the offset voltage at the output. Under most op-amp design cases, the mismatch within differential input pair transistors, active load pair and current source pair contribute almost the output offset voltage. Hence, circuit techniques to reduce op-amp offset mainly are focused on tackling critical component pairs with careful layout techniques in association with the balanced circuit architecture.

4.4.2 Circuit Description

For better matching purpose, the input pair transistors and the load transistors are set with very large dimensions in most of low-offset op-amp design cases in continuous-time design approach. Various other circuit techniques have been reported to address low offset design issues. The low-offset amplifier topology in [47] utilizes a systematic offset minimizing circuit in which a replica-biasing network and a middle gain stage are adopted to equalize the drain potential of the input pair transistors. The low-offset output buffer used in this project is based on this technique through the use of a folded-gain stage as the middle differential amplifier stage to improve the voltage headroom incurred by the middle stage which aims at the balancing circuit design. Fig. 4.34 shows the schematic of the low-offset output buffer.
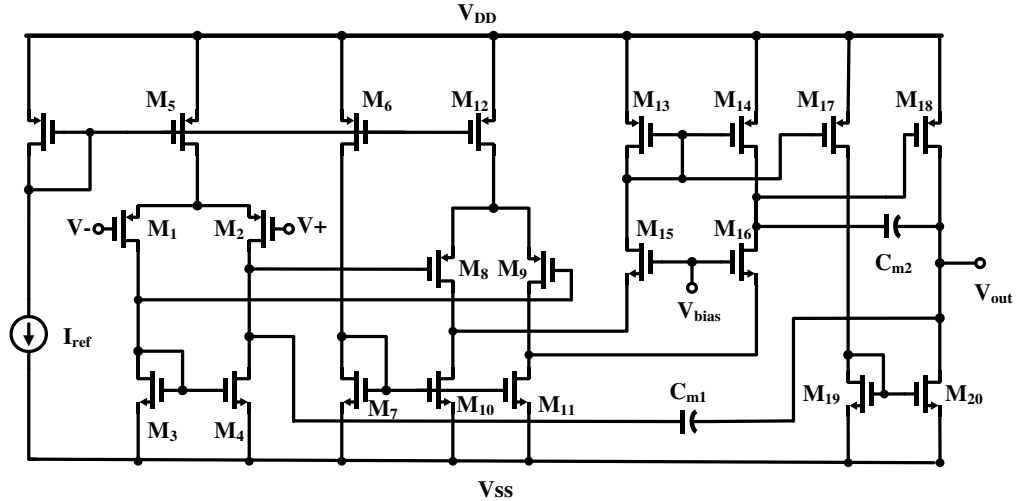
Fig. 4.34 Low-offset low-noise output buffer

As shown in Fig. 4.34, this low-offset amplifier is composed of a differential input stage, a folded-cascade middle differential amplifier stage, a class-AB output stage as well as the biasing networks. Nested Miller frequency compensation [56]-[57] is adopted for the amplifier's stability. The first

differential input stage consists of transistors M_1 to M_5. The drain potentials of the input pair transistors M_1 and M_2 are forced to equal to each other by the differential input of the second amplifier stage composed of transistors M_8 to M_{16}. The middle differential stage act as the interface between the input and output stage and cancels the design tradeoff by allowing the use of long channel length load transistors in the input stage and short channel length transistors in the output stage without sacrificing the bandwidth of the output driving transistors. It permits the noise optimization of the first input stage as well as the biasing control optimization at the output push-pull stage.

The push-pull stage comprising transistors M_{17} to M_{20} is driven by the output of the middle differential amplifier. The bias currents for the push-pull stage are controlled by transistor pair M_{13} and M_{14}. Push-pull operation scheme provides higher power efficiency, higher open-loop gain as well as good driving capability.

Layout is always one of the most important factors in ensuring a high quality design output. This is especially true in low-offset amplifier implementation since the IC fabrication process will highly affect the random offset value. In this low-offset buffer, the layout strategies for matching and symmetry considerations are critically planned and implemented. The common-centroid cross-coupling layout strategy is utilized to reduce process-related gradient effect. All the matched devices like differential input pair transistors, current mirror loads and the biasing current source transistors are selectively grouped and arranged tightly to minimize the spacing-dependent mismatch effect. Dummy transistors are always placed symmetrically at the end of the matched devices array to provide a similar boundary condition for the internal and external transistors.

4.5 Summary

The system architecture of the interface IC together with its core building blocks are presented in this Chapter. A novel Auto-Zero Time-multiplexed Differential CVC (AZTMD-CVC) readout circuit on the basis a foundation single-ended SC-CVC basic circuit structure is proposed. It is integrated with the signal-processing block containing a differential-to-single-ended programmable gain stage together with other house-keeping circuitries such as oscillator and clock generator in the ASIC design which has been fabricated using AMS 0.35-µm CMOS process. A bulk micro-machined accelerometer sensor device is interfaced with the ASIC.

This AZTMD-CVC is capable to deliver differential output performance without resorting to fully differential circuit architecture which requires the use of two parallel matched gain amplifier stages. The time-multiplexed single-ended CVC design offers low power consumption, simple circuit architecture and reduced stringent requirement for component pair matching in the amplifier circuits when compared to the conventional fully differential circuits. Special sample-and-hold operation procedure enables the time-multiplexed differential output to achieve reduced dc offset error arising from charging/discharging spikes, which is major originated from the large parasitics in the bulk micro-machined MEMS capacitive sensing elements. To the end, the summary of advantages and improvements over existing methods are given as follows:

(1) Eliminate the need of Wheatstone bridge sensing element whilst using a single differential sensor to support fully differential operation.

(2) Reduce the sensor and circuit cost due to the only use of single-ended structure for differential operation.

(3) Reduce the power consumption when compared with that of conventional differential structure.

(4) Give identical output as that of conventional differential circuit whilst double to the output with respect to single-ended sensor circuits.

(5) Display differential performance such as improved S/N ratio, dc offset and thermal drift with respect to that of single-ended structure whilst without increasing power consumption as well as circuit complexity.

(6) Reduce the component pair matching requirement in this AZTMD-CVC with respect to that of conventional differential counterpart.

(7) Eliminate common-mode circuit in the time-multiplexed differential design.

CHAPTER 5

PERIPHERAL HOUSE-KEEPING CIRCUITS

5.1 Introduction

Clock oscillator plays an important role in both the digital and mixed-signal systems. In sensor system application, clock oscillator should have the properties of low temperature coefficient, low power consumption and low sensitivity to supply and process variations. The integrated passive LC oscillator shows good frequency stability and high spectral purity due to the frequency-selective feedback network. However, the large passives needed for lower frequency applications makes the use of passive LC oscillator restricted. The crystal oscillators can provide clock signals with excellent stability with respect to supply voltage, temperature and process variations. Unfortunately, the incompatibility with IC technology makes it unsuitable for a low cost system. In this project, two clock generator schemes are proposed. They are the inverter-based ring oscillator and the current-comparator-based relaxation oscillator. The inverter-based ring oscillator output frequency is sensitive to the process variation and the temperature variation. To make it simpler in the design, overdesign is used to cope with the process variation whereas a simple PTAT control voltage source using Brokaw topology is proposed to compensate the temperature variation of charging and discharge currents in the inverter-based oscillator. This leads to a constant delay time and maintains a constant output frequency. The second approach using a current-comparator-based relaxation oscillator is investigated. A V_{dd}-tracking temperature-compensated current comparator based one-shot-timer is proposed in this

relaxation oscillator. The current-comparator-based relaxation oscillator utilizes the same structure as that of current-source-based relaxation oscillator while modifying the current source generator as well as the one shot timer circuit to achieve the temperature compensation property and fully integration.

5.2 Compact CMOS Ring Oscillator with Temperature and Supply Compensation

The inverter-based ring oscillator is simple, easy to be integrated and low cost when compared with other types of oscillators such as RC oscillator, crystal oscillator and relaxation oscillator. It is one of the oscillator topologies suitable for switched-capacitor applications in low-cost sensor systems [58]-[59] which do not demand highly precise sampling frequency. However, the output frequency of ring oscillator is a strong function of process, voltage and temperature variations. Various compensation approaches [60-63] have been reported to tackle these issues. These include external low dropout regulator or on-chip voltage regulator [60-61], [63] to drive the oscillator circuits with low noise and low sensitivity to supply variation. These configurations will lead to more complicated structures that potentially dissipate higher power consumption and produces larger active noise. In this work, a simple closed-loop controlled nonlinear PTAT source follower (SF) to bias a replica open-loop wideband SF driving stage is proposed to compensate the non-linear temperature dependence of the CMOS ring oscillator frequency as well as to effectively suppress the power supply noise and the intrinsic noise induced jitter error. The temperature compensated SF implementation is proved to be an economical and compact solution for the applications in sensor mixed-signal VLSI system.

Fig. 5.1 shows the conceptual diagram of proposed circuit. The Brokaw reference core together with the SF branch forms a closed loop to generate a PTAT voltage, which is replicated by an open-loop SF output driving stage. This open-loop PTAT voltage source serves as the power supply source of an inverter based ring oscillator core to compensate its negative frequency temperature dependence.
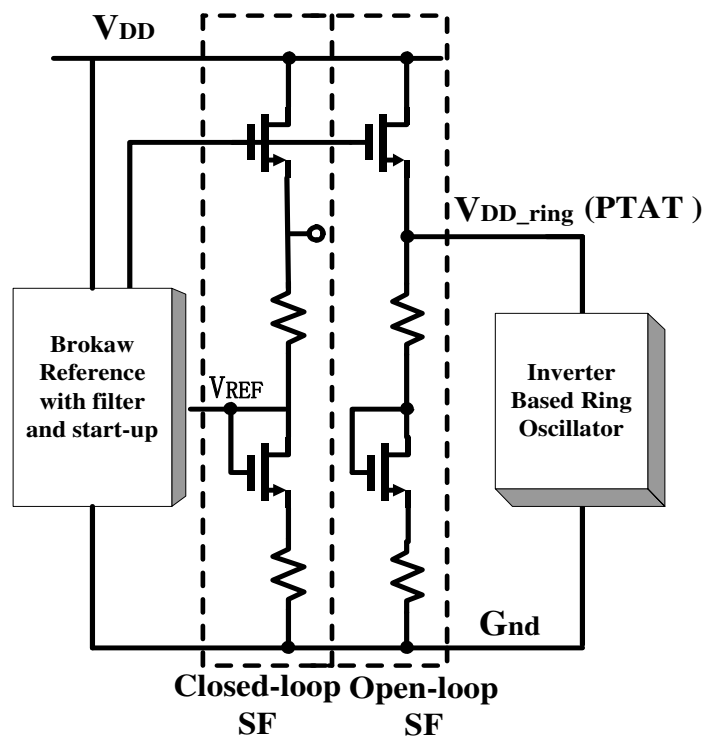
Fig. 5.1 Conceptual diagram of the proposed circuit

5.2.1 Temperature Variation Analysis of the Inverter Based Ring Oscillator

Fig. 5.2 shows the circuit schematic of the oscillator core. It consists of three-stage inverters and their respective Miller capacitors C_1, C_2 and C_3 in a ring

arrangement. Theses Miller capacitors are aimed to increase the effective load capacitance e of each stage through making use of the inverter gain factor during signal transition. The use of Miller capacitors help reduce the capacitor sizes needed to achieve large time delay in low frequency oscillation [57], hence saving the silicon area.
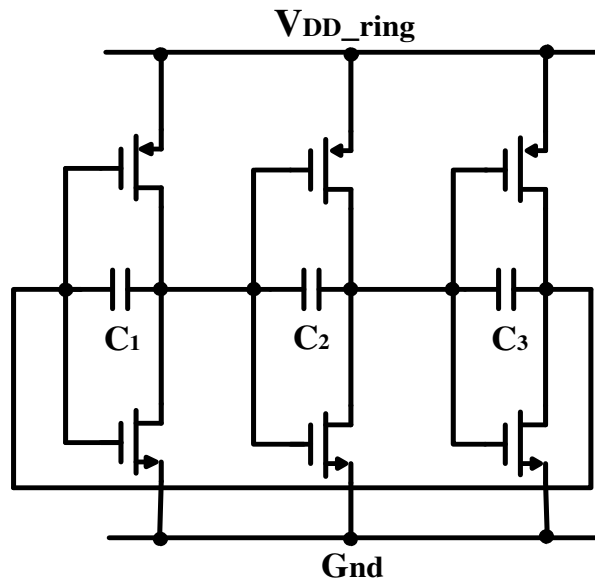
Fig. 5.2 Schematic of the three-stage inverter with Miller capacitors

The delay time τ_d of an inverter can be expressed as

$$\tau_d = \frac{C_{load}V_{DD}}{I_{average}} \tag{5.1}$$

where C_{load} is the load capacitance seen at the output of each stage, V_{DD} is supply voltage, and $I_{average}$ is the average charging/discharging current. $I_{average}$ is given by [64]

$$I_{average} = \mu C_{ox} \frac{W}{L} (V_{DD} - V_{th})^\alpha \tag{5.2}$$

106

where C_{ox} is the gate oxide capacitance, W/L is the aspect ratio of the transistor α is the carrier mobility degradation factor with a typical value between 1.5 to 2.0 [55]. Since the mobility μ and threshold voltage V_{th} are strongly dependent on temperature, the average charging and discharging current. As a result, the oscillation frequency shows a significant drift with temperature change. The temperature variation of mobility μ and threshold voltage V_{th} can be specified as follows [64]:

$$\mu = \mu_o (\frac{T_o}{T})^m \tag{5.3}$$

$$V_{th} = V_{th0} - K_o (T - T_o) \tag{5.4}$$

where m is the mobility temperature exponent, with typical values between 1.9 to 2.2 [55], K_o is the temperature coefficient of the threshold voltage, usually ranging from $1\ mV/°K$ to $4\ mV/°K$ [65]. In this derivation, it is assumed that $m = \alpha = 2$, therefore, the oscillation frequency can be written as

$$
\begin{aligned}
f = \frac{1}{N\tau_d} &= \frac{\mu_o C_{ox} \frac{W}{L} \left(V_{DD\_ring} - V_{th0} + K_o \cdot (T - T_o)\right)^2}{N C_{load} V_{DD\_ring}} \cdot \left(\frac{T_o}{T}\right)^2 \\
&= f_o \cdot \left[\left(\frac{K_o T_o}{V_{DD\_ring} - V_{th0}}\right) + (1 - \frac{K_o T_o}{V_{DD\_ring} - V_{th0}}) \frac{T_o}{T}\right]^2
\end{aligned}
\tag{5.5}
$$

where f_o is the central frequency at room temperature T_o. N is the number of inverter stages. Making $\Delta = \frac{K_o T_o}{V_{DD\_ring} - V_{th0}}$, (5.5) can be simplified as (5.6),

$$f = f_o \cdot \left[\Delta + (1 - \Delta)\frac{T_o}{T}\right]^2 \tag{5.6}$$

Examining (5.6), it can be seen that the supply voltage level of ring oscillator will affect its frequency temperature characteristic. Basically, the clock frequency will show a zero, negative and positive temperature dependence

under the conditions of $\Delta= 1, \Delta< 1, \Delta> 1$ respectively, which is in accordance with the simulation result reported in [62]. This design focuses on the negative temperature coefficient case to generate a temperature compensation voltage source V_p to power the ring oscillator.

Solving (5.5) for V_{DD_ring} and rejecting the unwanted root, the relationship between the oscillation frequency and the supply voltage V_{DD_ring} is obtained as follows [66]:

$$V_{DD\_ring} = A - K_0 T + BT^2 + \sqrt{B^2 T^4 - 2K_0 BT^3 + 2ABT^2} \qquad (5.7)$$

where $A = V_{TH}(T_0) + K_0 T_0$, $B = \dfrac{NC_{load}}{2T_0^2 \mu_0 C_{ox} W/L} f$ .Thus, term B becomes a constant value when the temperature dependent oscillation frequency is compensated. Under the design condition of f=1MHz, N=3 and C_{load}=1pF, the temperature coefficients of the third and fourth order term inside the square root item are thousand times smaller than that of the second-order term. (5.7) can be approximated as

$$V_{DD\_ring} \cong A + (\sqrt{2AB} - K_0)T + CT^2 \qquad (5.8)$$

in which the first-order temperature coefficient $\sqrt{2AB} - K_0$ is thousand times larger than that of the second-order term. Consider a practical temperature-dependent voltage source for powering the ring oscillator in a form of

$$V_{DD\_ring}^{\wedge} = M_0 + M_1 T + M_2 T^2 \qquad (5.9)$$

with the dominant dc term M_0=A and the dominant PTAT term $M_1 = \sqrt{2AB} - K_0$, the output frequency of the ring oscillator is temperature compensated.

Fig. 5.3 shows the exemplary simulation results of the frequency dependence on temperature with respect to various constant supply voltage levels. It can be shown that the compensated frequency, powered by a 3V supply, is compensated by a 4.8mV/°C temperature slope.
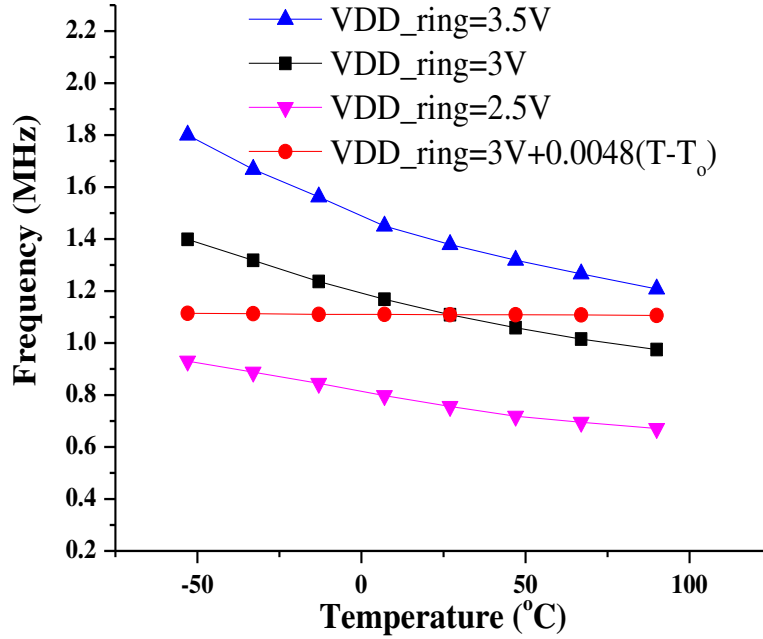
Fig. 5.3 Frequency dependence on temperature with different supply voltages

5.2.2 Proposed Voltage Source Follower with Temperature Compensation

The temperature compensation voltage circuit is shown in Fig. 5.4. It is composed of a Brokaw's voltage reference, a closed-loop SF branch dedicated to generate the temperature compensation bias for a replica counterpart in open-loop structure which serves as a supply voltage source to the ring oscillator. The voltage reference comprises a core reference circuit, a pseudo-resistive filter and a startup circuit. Within the core circuit, the transistors MN_1 and MN_2 are biased into weak-inversion region where the gate source voltage shows an almost linear dependence with temperature as is given by [67] as

$$V_{GS}(T) = V_{GS}(T_0)\frac{T}{T_0} + \left(V_{TH}(T_0) + K_0 T_0\right)\left(1 - \frac{T}{T_0}\right) + (1 - \beta)\frac{nkT}{q}\ln\frac{T}{T_0} \qquad (5.10)$$

where n is the inclination of the curve in weak inversion region, k is the Boltzmann constant, β is the temperature coefficient of the characteristic current and q is the charge of the electron. A PTAT voltage difference $\Delta V_{GS}(T) = n(kT/q)\ln\left[\frac{(W/L)_1}{(W/L)_2}\right]$ will be generated between the gate-to-source voltages of MN_1 and MN_2 due to different aspect ratios, leading to a PTAT current through the resistor R_2. It is given as

$$I_{PTAT} = n(\frac{kT}{q})\frac{1}{R_2}\ln\left[\frac{(W/L)_1}{(W/L)_2}\right] \qquad (5.11)$$

For proper choice of resistor values for R_2 and R_3, a constant voltage reference V_{REF} at the gate node of MN_1 and MN_2 can be obtained. The reference voltage can be expressed as

$$V_{REF} = 2I_{PTAT}R_3 + V_{GS2} = V_{TH}(T_0) + K_0 T_0 - (1 - \beta)nkT_0/q \qquad (5.12)$$
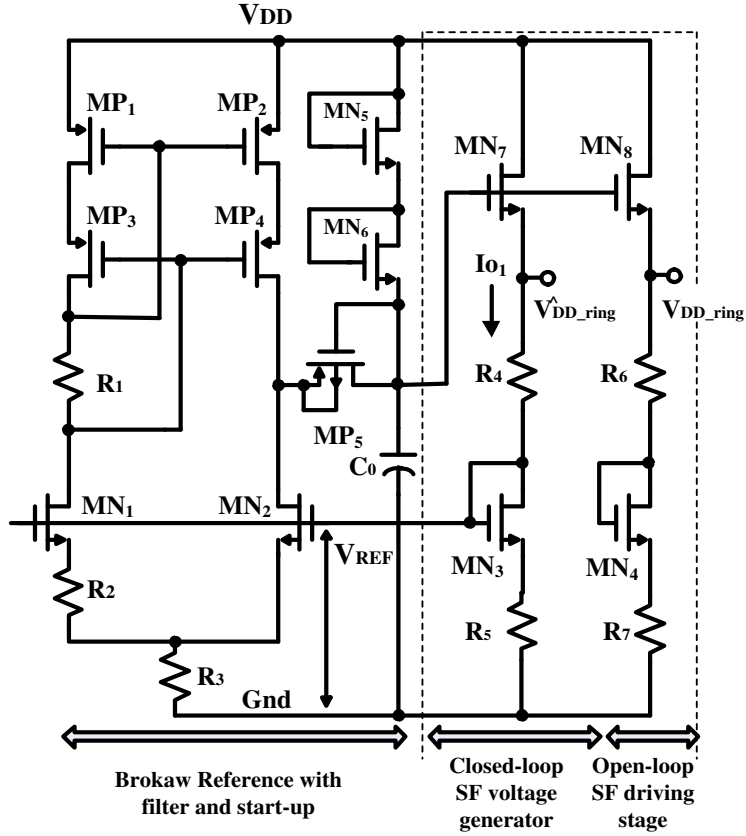
Fig. 5.4 The proposed temperature compensation voltage source circuit

The components MN_3, MN_7, R_4 and R_5 constitute the closed-loop SF branch which aims to generate the PTAT temperature compensation voltage $V^{\wedge}_{DD\_ring}$ as discussed in (5.9). By (5.10), the gate-to-source voltage $V_{GS3}(T)$ of the weak inversion region transistor MN_3 shows a negative temperature dependence, which can be expressed as

$$V_{GS3}\left(T\right)=V_{GS3}\left(T_0\right)\frac{T}{T_0}+(V_{TH}(T_0)+K_0T_0)(1-\frac{T}{T_0})+(1-\beta)\frac{nkT}{q}\ln\frac{T}{T_0} \qquad (5.13)$$

As a result, the loop established by V_{REF}, V_{GS3} and V_{R5} will yield a PTAT current I_{o1} due to the difference between a constant voltage V_{REF} and a complementary-to-absolute temperature (CTAT) voltage V_{GS3} of MN_3. The generated compensation voltage $V^{\wedge}_{DD\_ring}$ can be expressed as

$$V_{DD\_ring}^{\wedge} = I_{o1}R_4 + V_{REF} = \frac{R_4}{R_5}(V_{REF} - V_{GS3}) + V_{REF} \tag{5.14}$$

Substituting (5.12) and (5.13) into (5.14), it gives

$$V_{DD\_ring}^{\wedge} = (V_{TH}(T_0) + K_0 T_0 - \frac{(1-\beta)nkT_0}{q})$$
$$+ \left[\frac{R_4}{R_5} \left(\frac{V_{TH}(T_0) + K_0 T_0 - V_{GS3}(T_0)}{T_0} + \frac{(1-\beta)nk}{q} \right) \right] T \tag{5.15}$$

The first term in the bracket is a constant term of the generated supply source which is quite close to the constant value of V_{REF} which is the expected design parameter A denoted in (5.8). It is noted that β is smaller than 1 and n is approximately 1.5 [68]. The second term in (5.15) contributes the fundamental first-order PTAT term. Through proper choice of resistor values of R_4 and R_5, a supply voltage with the best fitted T.C. can be obtained through relating the respective coefficient in (5.9). Therefore, the design equation can be related as

$$\sqrt{2AB} - K_0 = \frac{R_4}{R_5} \left(\frac{V_{TH}(T_0) + K_0 T_0 - V_{GS3}(T_0)}{T_0} + \frac{(1-\beta)nk}{q} \right) \tag{5.16}$$

The components MN_4, MN_8, R_6 and R_7 compose the replica-biased open-loop SF driving stage. The devices in these two SF branches are set exactly the same. As such, V_{DD_ring} will be close to $V_{DD\_ring}^{\wedge}$ due to the identical bias at respective gate of MN_7 and MN_8 and the identical size of devices in the two source followers. The replica copy relationship is thus established and we get

$$V_{DD\_ring} \cong V_{DD\_ring}^{\wedge} \tag{5.17}$$

However, since the open-loop output branch has a larger bandwidth than that of the closed-loop one, V_{DD_ring} can respond faster than the closed-loop output $V_{DD\_ring}^{\wedge}$. Hence, it offers a faster voltage transient response to the oscillator

circuit and suppresses the spikes introduced by oscillation. This open-loop source follower driving structure helps improve the jitter performance of the ring oscillator.

The diode-connected transistors MN_5 and MN_6 form the startup circuit. Initially, the positive node voltage of C_0 is zero. When V_{DD} ramps up, the transistors MN_5, MN_6 will be turned on and a current will flow through the transistor MN_3. Consequently, it will pull up the gate voltage of MN_1 and MN_2 that turn on the subsequent self-biased voltage reference circuit. Then, the drain voltage of MN_2 will be pulled up, turning off the startup circuit. Fig. 5.5 shows the transient response during startup. The simulation result shows that the circuit can start up within 50µs.
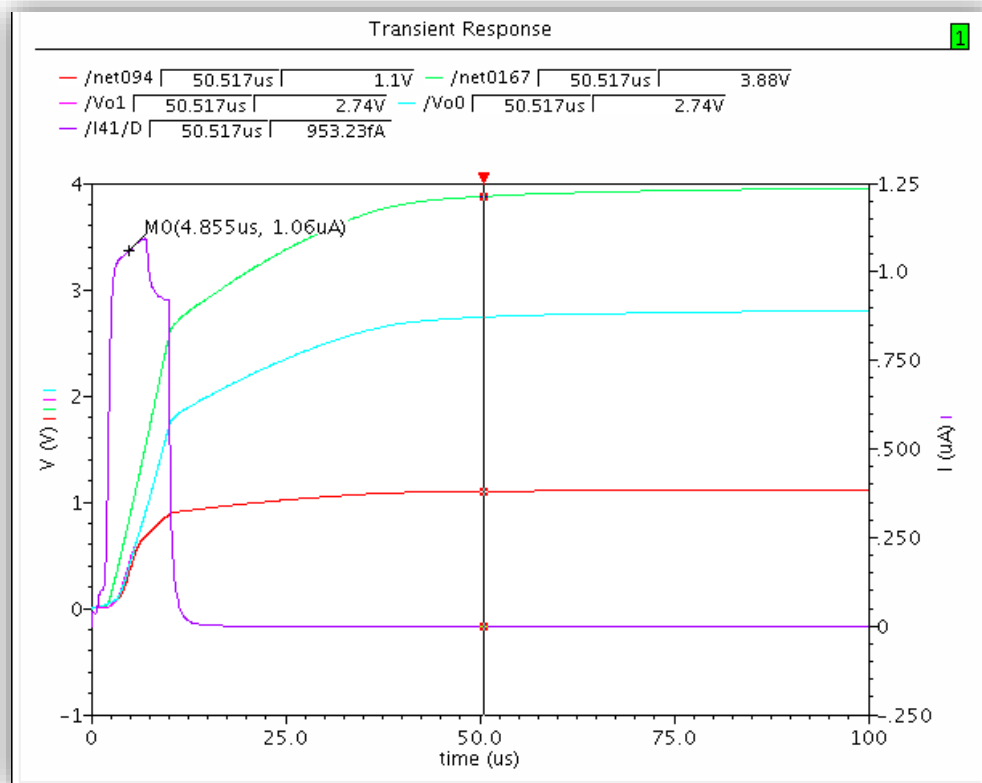
Fig. 5.5 Start-up response

5.2.3 Supply Noise Reduction

The phase noise of a voltage controlled ring oscillator circuit will be influenced by two noise factors: the device electronic noise or intrinsic noise of the ring oscillator core and the power supply noise [69]. Typically, the power supply noise will play a more significant effect than that of the oscillator core's intrinsic noise. This becomes the dominant factor that limits the ring oscillator's jitter performance if it were not tackled properly [70]-[75]. In this design, the generated temperature compensated control voltage will be used to power up the ring oscillator core. Therefore, the methods to reduce the noise of the generated temperature compensated control voltage must be addressed.

The generated temperature compensation voltage noise consists of device electronic noise including flicker noise and thermal noise as well as high frequency noise coupled from the cycle-to-cycle switching clock inside the power supply system. This demands a high PSRR inside the compensation voltage generator circuit to suppress the system power supply induced noise. In this work, a pseudo-resistive low-pass filter formed by the transistor MP_5 and the capacitor C_0 is included to help reduce the noise generated by the system power supply as well as the flicker noise coming from the compensation circuit. MP_5 is implemented as a minimum size diode-connected transistor with its source and substrate terminals self-connected. It is intended to exhibit a large resistance value. The simulated cutoff frequency of this low pass filter is 56 mHz. Since there is no dc current flowing through MP_5 under quiescent condition, the gate voltage of MN_7 is equal to the drain voltage of MP_4 [76]. Besides, the source follower structure inherently provides a better PSRR performance than that of the op-amp based structure. The open-loop source follower driving structure helps reduce the clock coupled ripple and provides a

fast-compensated solution due to a larger bandwidth. Both these methods contribute to reduce the phase noise and improve the ring oscillator jitter.

5.2.4 Trimming Circuit for Process Variation

Since the oscillation frequency is strongly dependent on threshold voltage, the process variation will cause a large fequency drift which should be taken into consideration. A simple method is to use a trimming circuit to tune the frequency to the typical mean condition value. The principle of the trimming circuit is to use digital data bits to trim the Miller capacitor values. These Miller capacitors are implemented in the form of arrays as illustrated in Fig. 5.6. Each array capacitor is switched either on or out of the input and output of each inverter stage through a data bits controlled analog switch. Thus, the frequency to the required value can be adjusted through trimming the Miller capacitor value by programming the data bits. For this circuit, it is designed to have a 4-bit trimming. The digital bits B_0 to B_3 that control the analog switch and the Miller capacitor array are with a step of 0.25pF.
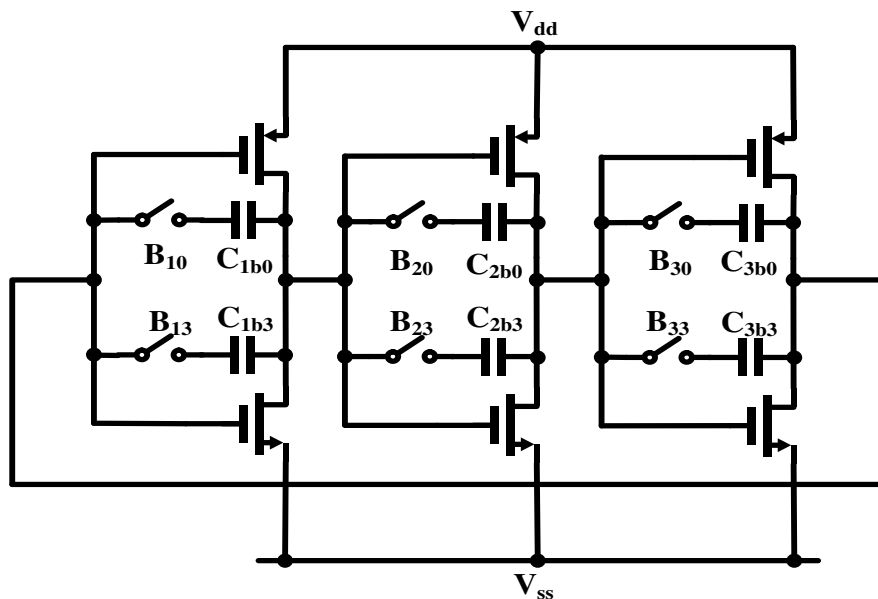
Fig. 5.6 Ring oscillator with data bits controlled Miller capacitor array

5.2.5 Simulation Results and Discussions

This temperature-compensated CMOS ring oscillator is realized using AMS 0.35µm CMOS process. The designed oscillation frequency is 1MHz at a 5V supply. Refer to Fig. 5.7, it compares the calculated and simulated results under typical process condition for uncompensated and compensated oscillation frequencies against temperature. Over the temperature range of −40°C to +90°C, the simulated frequency variation of the compensated oscillator is −0.1% to +0.19% (22.3 ppm/°C) with respect to the uncompensated frequency variation of −12.1% to +21.6% (2592 ppm/°C). These simulation results correlate well with the theory. Fig. 5.8 shows the temperature dependence of the uncompensated and compensated oscillator frequency under different process corners at a typical 5V supply voltage. The worst frequency variation occurs at FF corner which ranges from −1.5% to +1.9%. It has shown that the temperature compensation is insenstive to process variation.

Fig. 5.9 shows the process corner simulation results for ±10% supply variation. The worst case compensated oscillator frequency varies from −1.2% to +1.2% in comparison to the uncompensated one from −17.2% to +17.2%. The low supply sensitivity is due to self-biased voltage reference architecture in conjunction with the source follower driving topology.

Due to unavoidable mismatch in fabrication process, the replica voltage V_{DD_ring} will deviate from $V^{\wedge}_{DD\_ring}$. In order to assess the mismatch sensitivity of the two SFs, the parameters in replica SF are varied. The transistor width of MN_8, MN_4 and resistor value of R_6 and R_7 are intentionally mismatched with 1% with respect to their corresponding counterparts in the $V^{\wedge}_{DD\_ring}$ branch. As depicted in Fig. 5.10, the V_{DD_ring} displays only 50µV voltage difference from $V^{\wedge}_{DD\_ring}$

under each temperature point while having almost the same temperature coefficient. This result indicates that the proposed replica source follower structure can work well in the presence of component mismatches.
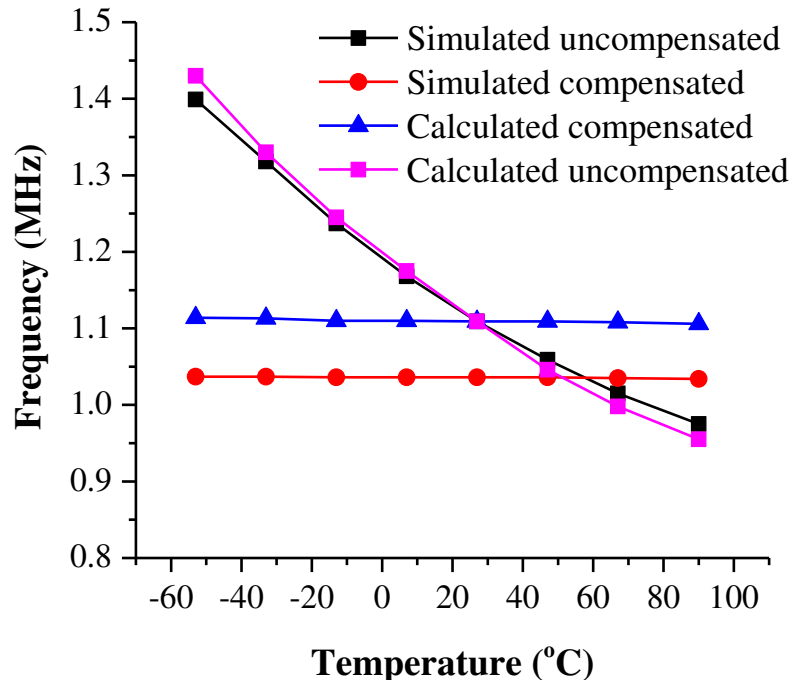
Fig. 5.7 Simulation and calculation results of the temperature characteristic of the oscillation frequency with and without compensation
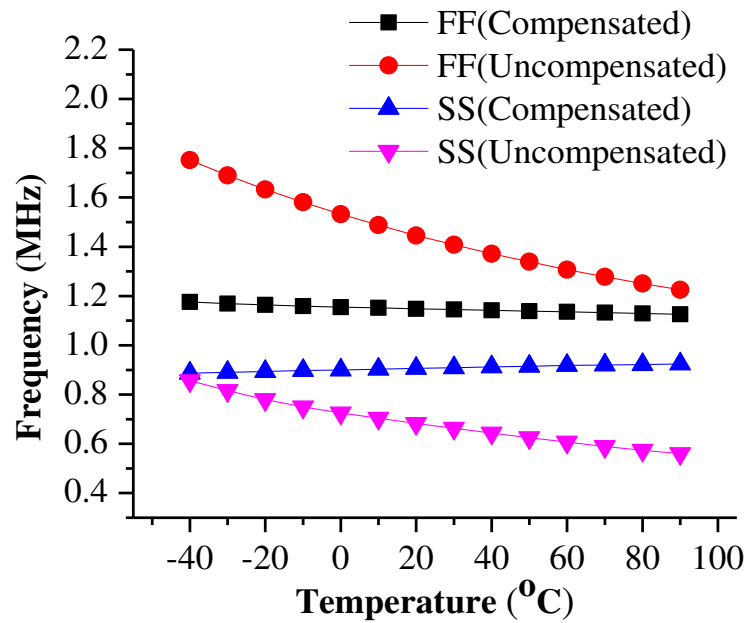
(a) Temperature characteristics of uncompensated and compensated oscillation frequency under FF and SS corners
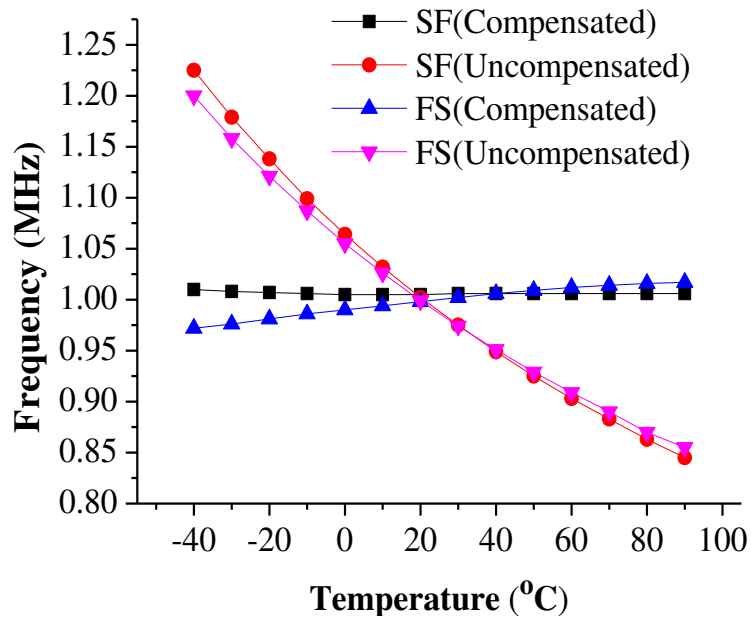
(b) Temperature characteristics of uncompensated and compensated oscillation frequency under SF and FS corners

Fig. 5.8 Simulation results for frequency versus temperature variation under (a) FF, SS corners and (b) SF, FS corners
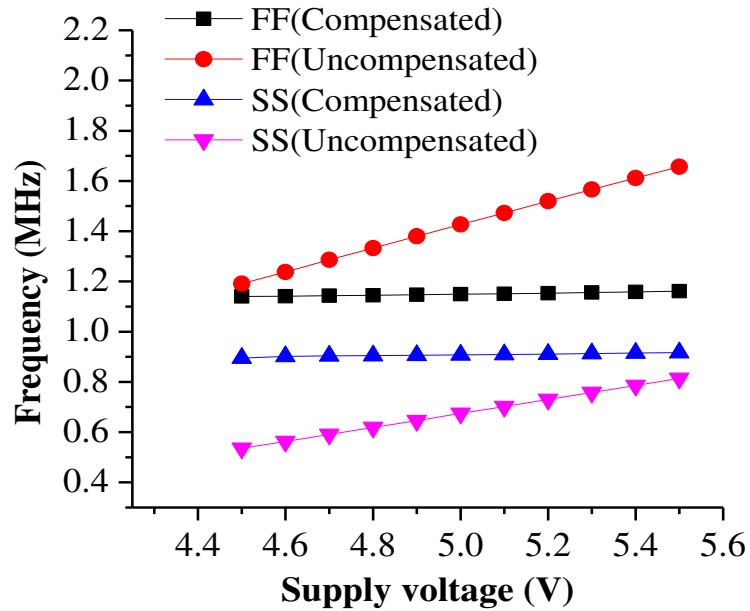
(a) Uncompensated and compensated oscillation frequency versus supply variation under FF and SS corner
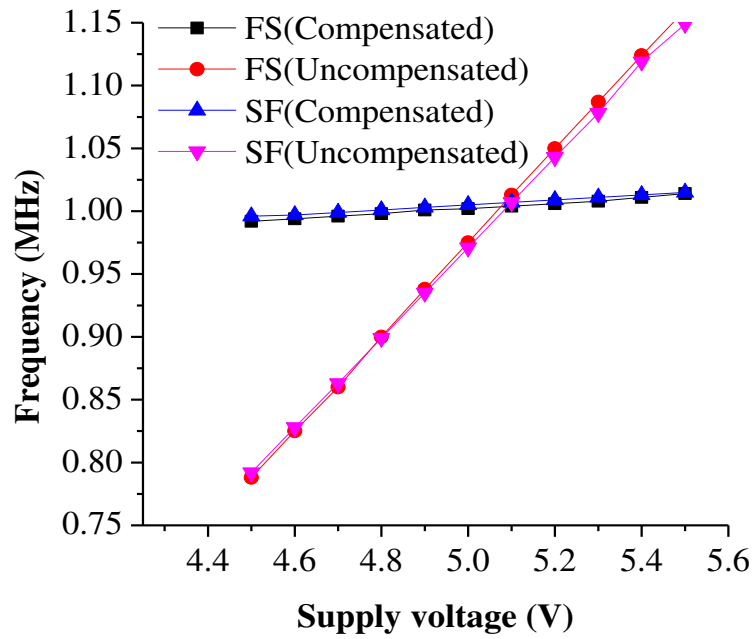
(b) Uncompensated and compensated oscillation frequency versus supply variation under SF and FS corners

Fig. 5.9 Simulation results for frequency versus ±10% supply variation under (a) FF and SS corners and (b) SF and FS corners
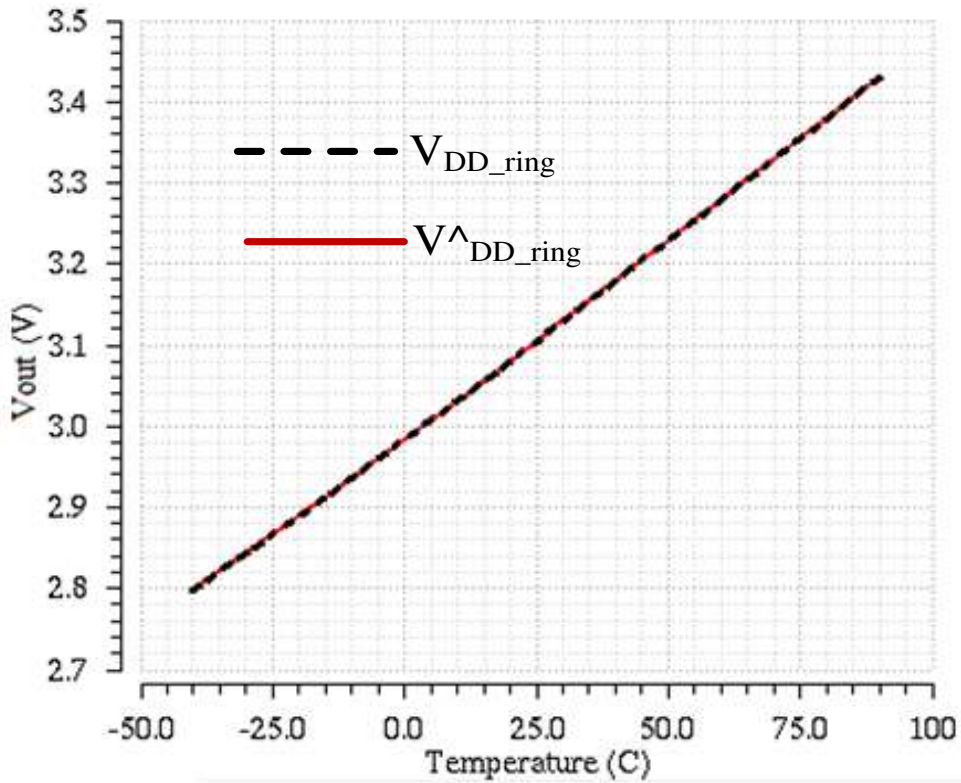
Fig. 5.10 Temperature sweep of the generated V_{DD_ring} and $V^{\wedge}_{DD\_ring}$ under 1% mismatch in the source follower pair

119

The simulation result of the intrinsic phase noise [77] with and without the RC filter in the compensation supply circuit are given in Fig. 5.11. The integrated cycle-to-cycle RMS jitter value with RC filter is 13ps with respect to 377ps without the RC filter. This suggests that the RC filter significantly reduces the circuit noise induced by the compensation supply circuit. Fig. 5.12 shows the simulated PSRR performance of the circuit. The simulation result shows that the proposed temperature compensated SF voltage generator has a minimum PSRR of 33dB from medium to high frequency bands.
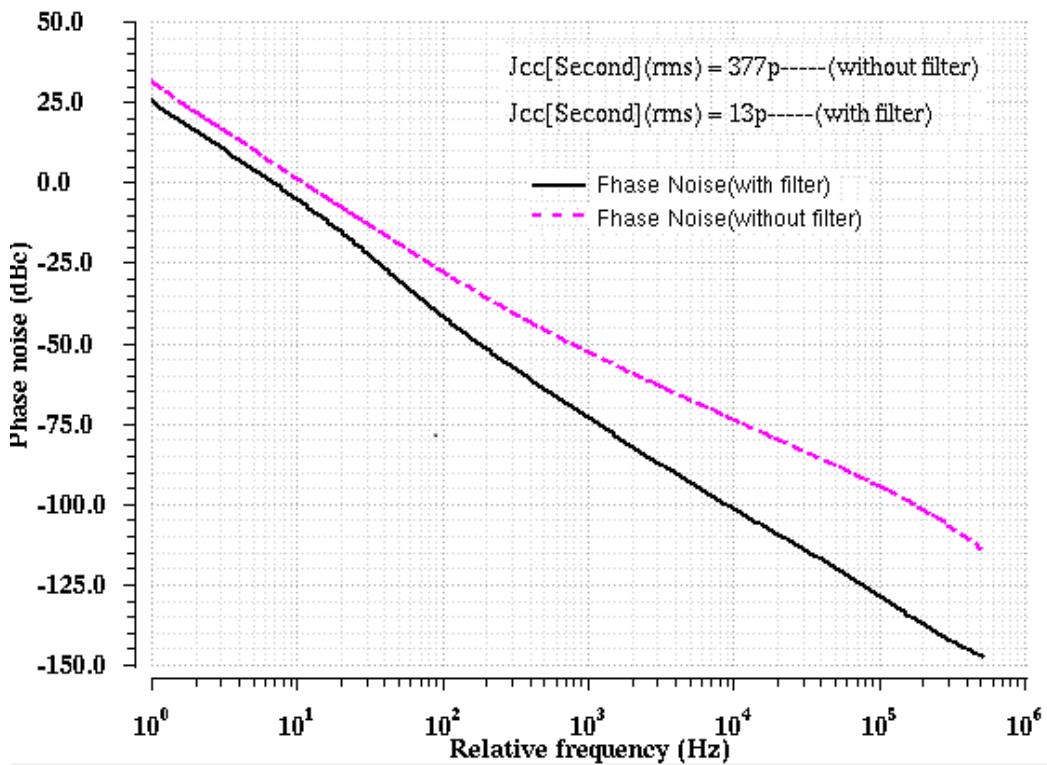
Fig. 5.11 Simulated phase noise due to intrinsic circuit noise with and without filter
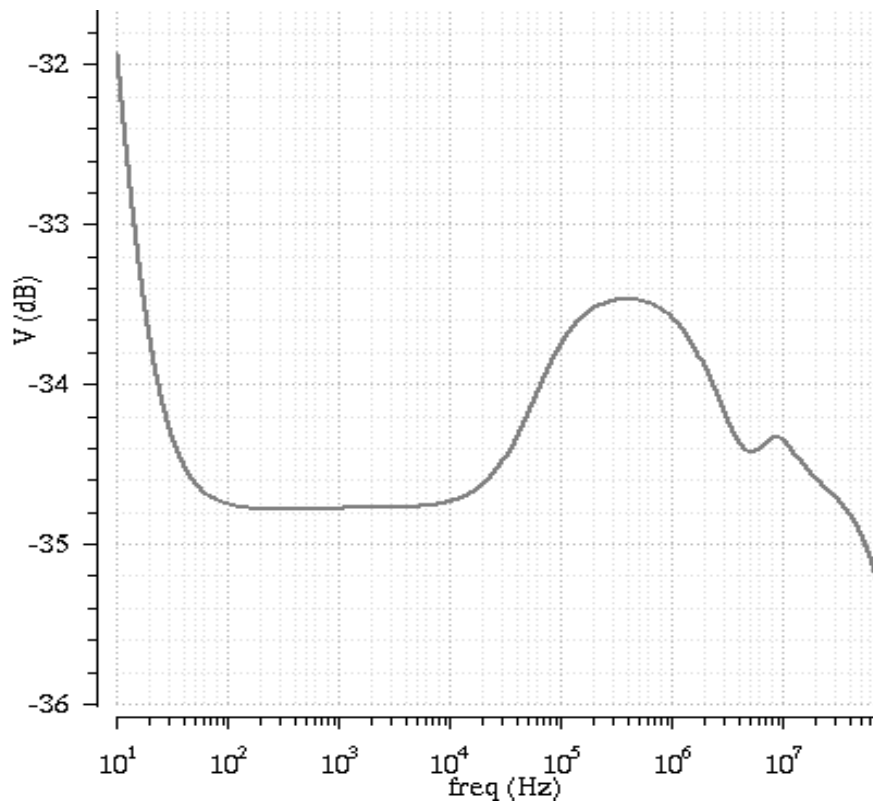
Fig. 5.12 Simulated PSRR response of the proposed temperature compensated
SF

The power supply noise induced jitter is characterized using SpectreRF phase noise simulator. The supply noise is modeled as band-limited thermal noise injected by a large resistor based on the simulation model and method [69]. Table 5.1 shows the jitter performance comparison between the proposed work and the standard inverter based ring oscillator [78] as well as the current-starved ring oscillator [70].

In order to have a fair comparison result, these three circuits are designed with the identical process technology, the same power supply together with its supply noise and the same oscillation frequency 1.04MHz. The simulation result of the proposed work demonstrates a significant reduction of respective jitter arsing from the power supply and the circuit with respect to the counterparts.

Table 5.2 compares the performance between the reported low-frequency oscillators and this work. As can be seen from the results, the proposed design provides the best temperature variation stability with 22.3ppm/°C over the temperature range of from -40 to 90°C and consumes much lower power consumption of 65 µA with 5V supply voltage. This is attributed to the circuit simplicity. The worst case oscillator frequency varies from −1.2% to +1.2% when the supply voltage varies from 4.5 to 5.5V. The low supply sensitivity demonstrates the effectiveness of the self-biased voltage reference architecture incorporating the source follower driving topology.

Table 5.1 Jitter performance comparison with benchmarks

Parameter	Inverter-Based Oscillator [78]	Current-Starved Oscillator [70]	**This work**
Frequency [MHz]	1.04	1.04	**1.04**
Intrinsic noise induced RMS jitter	12	14	**13**
Cycle-to-Cycle RMS jitter with $20mV_{pp}$ supply noise [ps]	297	288	**16**
Cycle-to-Cycle RMS jitter with $200mV_{pp}$ supply noise [ps]	3100	2870	**64**

Table 5.2 Performance comparison with prior-art works

Parameter	[58]	[60]	[62]	**This work**
Process	0.35µm	0.6µm	0.35µm	**0.35µm**
Freq. [MHz]	0.2	0.68	1	**1.04**
Power [µA]	810	100	NA	**65**
Supply [V]	1.25	4	3	**5**
Freq. variation with Vdd [%]	NA	NA	NA	**±1.2 @4.5 to 5.5V**
Freq. variation with Temperature [ppm/°C]	1000@ -25~80	105.7@ 35~115	333@ 0~100	**22.3@ -40~90**

5.3 Low-Power Vdd-Tracking Temperature-Compensated Relaxation Oscillator

The temperature-compensated inverter-based ring oscillator can provide clock signals with good immunity to temperature and supply variations. It is realized in a simple and compact circuit architecture. Unfortunately, the temperature-compensated source follower driving topology suffers from the voltage head room issue. Besides, the power consumption of the temperature compensation voltage source circuit tends to be too high for a readout IC system having the requirement of tight power consumption budget. To tackle these problems, the relaxation oscillator, based on charging and discharging of a capacitor by the precision current source [79]-[80], [81], proves to be another good alternative solution for SC sensor system applications. The reported works aim to design the oscillator with good temperature and supply stability. For most cases, the

relaxation oscillators rely on external precision passive components to generate an accurate clock. This in turn will increase the cost of the circuit and the pin count of the readout IC. In order to provide a fully-integrated solution while maintaining the property of low sensitivity with respect to the change of temperature and supply, a V_{dd}–tracking temperature-compensated current comparator based relaxation oscillator, which has the feature of low power consumption, is proposed and implemented for the readout house-keeping circuitry in this work.

5.3.1 Relaxation Oscillator Circuit Architecture

Fig. 5.13 shows the block diagram of the proposed current comparator based relaxation oscillator. It consists of the startup circuit, two one-shot timer circuits in the ring arrangement, a current source generator to produce currents I_1, I_2, I_3 and I_4 for biasing the respective one-shot timer [81] and two delay blocks to generate the non-overlapping clock period.

After the power is turned on, the start-up circuit will generate a single low-high-low pulse, causing the OR gate output to produce a high signal. After a delay period, this single pulse will reach S_1 at one-shot-timer 1 and reset its SR latch to generate the pulse CLK_1 and R_1. After another delay period, R_1, the output of timer 1 will trigger the SR latch of timer 2 to generate the pulse CLK_2 and R_2. R_2 will cause the OR gate to go high again and trigger timer 1 and timer 2 to initiate a new clock cycle. Hence, with the ring arrangement, the clock generator will continue to produce CLK_1 and CLK_2 after the single start-up pulse. The delay blocks are used to define the non-overlapping periods of the clock waveforms.

The oscillation frequency is mainly determined by the capacitor discharging time of timer 1 and timer 2 plus the non-overlapping period. Since the non-overlapping time is much less than the discharging time, the oscillator frequency can be approximated simply based on the discharging time as

$$f = \frac{1}{2T} = \frac{I}{2C_L(V_{dd} - V\_)} \tag{5.18}$$

where T is the discharging time of each timer (timer 1 and timer 2 take the same discharging time), C_L is the load capacitance, I is the constant discharging current provided by the current source generator, $I = I_1 = \frac{1}{2}I_2 = I_3 = \frac{1}{2}I_4 = \frac{1}{2}I_{ref}$, and $V\_$ is the voltage point of the load capacitor C_L during discharge process. From (5.18), the temperature property of the output frequency is determined by both the TC of the discharging current I and the trigger voltage V-. Hence, in order to find the appropriate compensation scheme to make the oscillation frequency temperature independent, the TC of both the discharging current and the trigger voltage needs to be defined first.
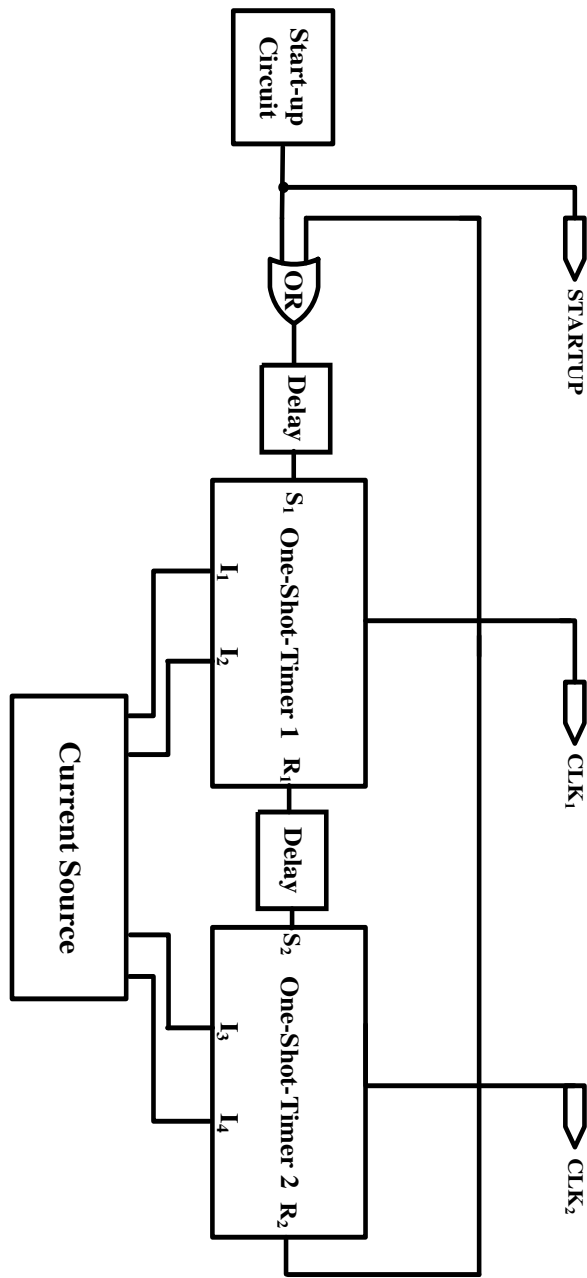
Fig. 5.13 Block diagram of the oscillator circuit

5.3.2 Current Source Generator

The current source generator is illustrated in Fig. 5.14. Transistors MP_6, MP_7, MN_5 to MN_8 and resistor R_3 form a supply independent bias current generator. MP_6 is biased in weak inversion region with large W/L ratio. This bias

condition will set the source-to-gate voltage of MP$_6$ close to its threshold voltage. This source-to-gate voltage over resistor R$_3$ defines the bias current for this circuit. Since both the threshold voltage and the high-resistive poly resistor have negative temperature coefficient (TC) characteristic, they partially compensate with each other. The TC of the threshold voltage usually varies from $1\,mV/°C$ to $4\,mV/°C$ [65] or 1000ppm/$°C$ to 4000ppm/$°C$ for a 1V threshold voltage, whereas the TC of the high resistive poly resistor is about 740ppm/$°C$. The result of the generated reference current I_{ref} still exhibits a negative dependence on temperature variation. This reference current is mirrored to the output branch by the cascode current mirror formed by transistors MN$_5$ to MN$_{16}$. I$_1$ and I$_3$ serve as the constant discharging currents for the two one-shot-timer circuits respectively while I$_2$ and I$_4$ are the reference currents to generate reference voltages for two current comparators of the one shot timer circuit. The reference current and I$_1$- I$_4$ are given by

$$I_1 = \frac{1}{2} I_2 = I_3 = \frac{1}{2} I_4 = \frac{1}{2} I_{ref} = \frac{V_{SG6}(T)}{2R_3(T)} \tag{5.19}$$

Usually, there are two stable operating points inside a self-biasing design structure. In order to ensure the correct state, a startup circuit is needed to force the circuit into the correct operating point. Transistors MP$_4$, MP$_5$ and capacitors C$_0$, C$_1$ form the capacitive coupled startup circuit. This circuit will not consume any static current, so it is suitable for low power design. Initially, capacitors C$_0$, C$_1$ are uncharged. Upon power on, the supply voltage V$_{dd}$ will surges high while V$_{ss}$ will go low from the ground level. As V$_{dd}$ surges high, V$_{ss}$ goes down, the uncharged capacitor C$_0$ and C$_1$ will cause the gate voltage of MP$_5$ to go low with V$_{ss}$ and the gate voltage of MP$_4$ to go high with V$_{dd}$ respectively. As a result, transistor MP$_5$ will be turned on and start to sink current through transistors MN$_6$, MN$_8$ and start up the circuit, while MP$_4$ will remain cutoff. As

current starts to flow, the gate voltage of MP_4 will drop and MP_4 will be turned on to charge up capacitor C_0. Eventually, transistors MP_4, MP_5 will be turned off and isolated from the current generator circuit.
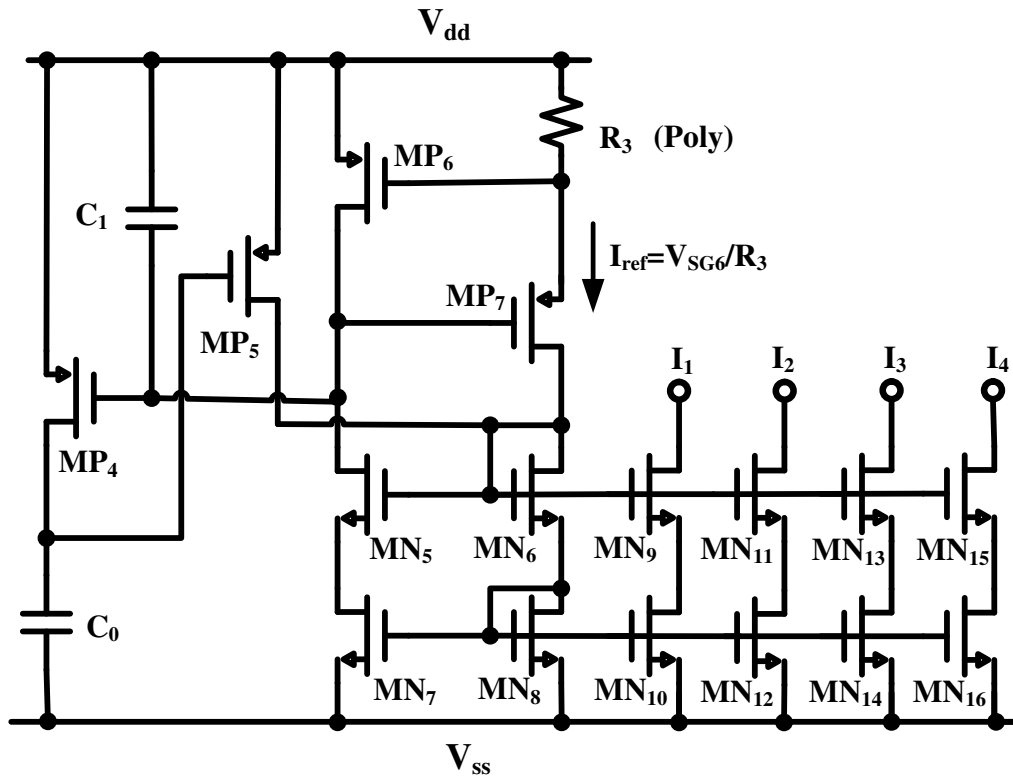
Fig. 5.14 Schematic of the current source generator (startup not shown)

5.3.3 V_{dd}-Tracking Temperature-Compensated Current Comparator Based One-Shot-Timer

As shown in Fig. 5.15, the one-shot timer circuit comprises a NOR based SR latch, a current source based comparator and a buffer inverter. Transistors MP_0 and MN_0 act as switches to control the charging and discharging of capacitor C_L.
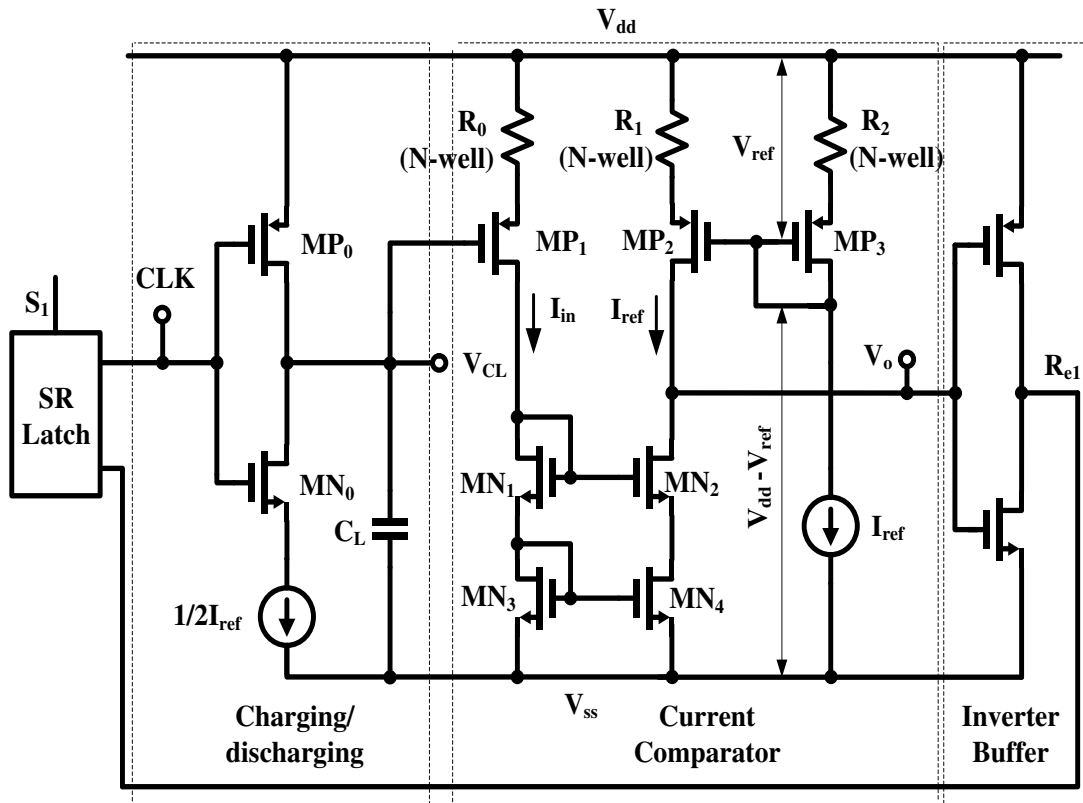
Fig. 5. 15 One-shot-timer circuit based on V_{dd}-tracking temperature-compensated current comparator

When CLK is low, transistor MP_0 is on. It will quickly charge up capacitor C_L. When CLK is high, transistor MN_0 will turn on and capacitor C_L will discharge almost linearly through the current source. Transistors MP_1-MP_3, MN_1-MN_4, resistors R_0-R_2 and current reference I_{ref} form the current comparator circuit. The diode connected PMOS transistor MP_3 is biased into weak inversion saturation region to convert the reference current I_{ref} to a source-to-gate voltage which is quite close to the threshold voltage of PMOS transistor. PMOS transistor pairs MP_1 MP_2, MP_3 and NMOS transistor pairs MN_1, MN_2 and MN_3, MN_4 are set with identical W/L ratios respectively. The current mirror structure mirrors the reference current I_{ref} to transistor MP_2 identically. The current comparator works as follows. When the node voltage Vc_L is equal to V_{dd}-V_{ref}, I_{in} is equal to I_{ref} and all the transistors of the current comparator will work in

saturation region. When Vc_L is charged up to some certain point that is bigger than $V_{dd}-V_{ref}$, I_{in} will be smaller than I_{ref} and eventually it will force transistor MN_2 and MN_4 to go off and exhibit a high resistance which will cause the output voltage V_o to go high. When Vc_L is discharged down to a potential which is smaller than $V_{dd}-V_{ref}$, I_{in} will be bigger than I_{ref} and will cause transistor MN_2 and MN_4 to go into triode region. This will result in a low potential level at the output node. The comparison result, V_o, which is sharpened by a buffer stage, generates the reset signal R_e for the SR latch.

The signal transition process of the whole circuit is as follows. Initially, all the node voltages are assumed to be low upon power on. As the single low-high-low startup pulse reaches S after the delay block, the SR latch will be set and the output signal, CLK_1, is forced to go high. The NMOS transistor MN_0 will then be turned on whereas capacitor C_L will start to discharge relatively slowly (as compared to the fast charge up time) through the current source until the voltage on C_L reaches the reference voltage $V_{dd}-V_{ref}$. This discharge process will cause V_o to go low as explained before. After a buffer inverter, the signal goes high at R_{e1}. This high potential voltage will reset the output of the SR latch and CLK_1 to go low. After a short delay period through another delay block, the voltage at node R_{e1} will be passed to S_2 of the SR latch inside the second one-shot timer. This immediately sets CLK_2 high. At the same time, after CLK_1 goes low, the PMOS transistor MP_0 will be turned on and quickly charge up the capacitor C_L and force R_{e1} to go low. The same transition goes between CLK_2 and R_{e2} in timer 2. CLK_1 will remain low since the SR latch of the first one-shot-timer circuit will be in hold state until the node voltage of R_{e2} finally goes high, triggering S_2 to go high again (note that the startup pulse is a single pulse with low-to-high and high-to-low transitions). After S_1 goes high, the oscillator

circuit will enter the next oscillation period. It continues to generate the non-overlapping clock CLK$_1$ and CLK$_2$.

After examining the signal transition process, it confirms that the output frequency is determined by the discharging time T_{dis} of capacitor C$_L$ and the non-overlapping period. Since the non-overlapping period is much smaller than the delay time, it can be ignored in calculation for simplicity. The output frequency is given by

$$f = \frac{1}{2T_{dis}} \tag{5.20}$$

The discharging time T_{dis} is expressed as

$$
\begin{aligned}
T_{dis} &= \frac{\Delta Q}{I} = \frac{2C_L\{V_{dd} - [V_{dd} - V_{SG1}(T) - I_{in}(T)R_0(T)]\}}{I_{ref}(T)} \\
&= \frac{2C_L[V_{SG1}(T) + I_{in}(T)R_0(T)]}{I_{ref}(T)} = \frac{2C_L V_{SG1}(T)}{I_{ref}(T)} + \frac{2C_L I_{in}R_0(T)}{I_{ref}(T)}
\end{aligned}
\tag{5.21}
$$

As can be observed from (5.21), the discharging time is independent of the supply voltage V$_{dd}$ since it will not affect the charge difference ΔQ. Substituting (5.19) into (5.21), we obtain

$$T_{dis} = \frac{2C_L R_3(T) V_{SG1}(T)}{V_{SG6}(T)} + \frac{2C_L I_{in}(T) R_0(T)}{I_{ref}(T)} \tag{5.22}$$

Examining (5.22), the temperature property of the discharging time and hence that of the oscillation frequency is mainly determined by the following terms: resistor $R_0(T)$ and $R_3(T)$, both the source-to-gate voltage of the PMOS transistor MP$_1$ and that of MP$_6$, current $I_{in}(T)$ as well as $I_{ref}(T)$. Of all these temperature dependent terms, the N-well resistor R_0 shows a linear positive dependence on temperature. This is defined as

$$R_0(T) = R_{00}(1 + \alpha_{r0}T) \tag{5.23}$$

where R_{00} is the n-well resistor value at room temperature and α_{r0} is the temperature coefficient of n-well resistor which is a positive value. R_3 is high poly resistor which shows small linear negative dependence on temperature which is given as

$$R_3(T) = R_{30}(1 - \alpha_{r3}T) \tag{5.24}$$

where R_{30} is the high-poly resistor value at room temperature. α_{r3} is the temperature coefficient with a positive value. The source-to-gate voltage of MP$_6$ is quite close to its threshold voltage and shows almost the same temperature properties. As such, it can also be estimated using a linear negative temperature dependence equation as follows:

$$V_{SG6}(T) = V_{SG60}(1 - \alpha_{V_{SG6}}T) \tag{5.25}$$

where V_{SG60} is the point for source-to-gate voltage of MP$_6$ at room temperature and $\alpha_{V_{SG6}}$ is the temperature coefficient with a positive value. For the source-to-gate voltage of MP$_1$ at the trigger point, it displays an almost linear negative temperature coefficient based on the simulation result. It is expressed as follows:

$$V_{SG1}(T) = V_{SG10}(1 - \alpha_{V_{SG1}}T) \tag{5.26}$$

where V_{SG10} is the trigger point voltage for source-to-gate voltage of MP$_1$ at room temperature and $\alpha_{V_{SG1}}$ is the temperature coefficient exhibiting a positive value. I_{in} is about two times of I_{ref}. Due to the current mirror structure, the source-to-gate voltage $V_{SG1}(T)$ and $V_{SG6}(T)$ of transistors MP$_1$ and MP$_6$ will track with each other and the same goes for that of $I_{in}(T)$ and $I_{ref}(T)$. Hence, of all these temperature-dependent terms in (15), the temperature coefficient (T.C.) of $V_{SG10}(T)$ and $V_{SG9}(T)$ can cancel each other and so is that of $I_{in}(T)$ and $I_{ref}(T)$.

Combining (5.22)-(5.26), we can get

$$
\begin{aligned}
T_{dis} &= \frac{2C_L R_{30} V_{SG10}\left(1-\alpha_{r3}\Delta T\right)}{V_{SG60}} + 2C_L \frac{I_{in}}{I_{ref}} R_{00}\left(1+\alpha_{r0}\Delta T\right) \\
&= \frac{2C_L R_{30} V_{SG10}}{V_{SG60}} + 2C_L \frac{I_{in}}{I_{ref}} R_{00} - \frac{2C_L R_{30} V_{SG10}\alpha_{r3}}{V_{SG60}}\Delta T + 2C_L \frac{I_{in}}{I_{ref}} R_{00}\alpha_{r0}\Delta T
\end{aligned}
\tag{5.27}
$$

As indicated in (5.27), there are two linear terms with opposite temperature dependence which can compensate with each other. Through adjusting the resistor value of R_{00}, the temperature coefficient of the output frequency can be optimized. Setting the coefficient of the temperature variation ΔT to be zero, we can get the required n-well resistor value R_{00} as follows,

$$
\frac{2C_L R_{30} V_{SG10}\alpha_{r3}}{V_{SG60}} = 2C_L \frac{I_{in}}{I_{ref}} R_{00}\alpha_{r0}
\tag{5.28}
$$

$$
R_{00} = \frac{R_{30} V_{SG10}\alpha_{r3}}{V_{SG60}\alpha_{r0}} \cdot \frac{I_{ref}}{I_{in}}
\tag{5.29}
$$

The temperature compensated output oscillation frequency can be expressed as,

$$
f = \frac{1}{2T_{dis}} = \frac{1}{\dfrac{4C_L R_{30} V_{SG10}}{V_{SG60}} + 4C_L R_{00}}
\tag{5.30}
$$

As can be seen from (5.30), the output frequency is unaffected by the supply variation. The frequency stability with respect to temperature is determined by the compensation result of the n-well and high poly resistors. It is given that the design parameters are $I_{ref}/I_{in} \approx 0.5$, $\alpha_{r0} \approx 8446 ppm/°C$, $\alpha_{r3} \approx 550 ppm/°C$, $R_{30} \approx 1M\Omega$, $V_{SG10} = 1.14V$, $V_{SG60} = 1.035V$. Substituting these results into (5.29) and solving for R_{00}, the obtained result is $R_{00} \approx 35.8k\Omega$. This is quite close to the simulation result of $34\ k\Omega$. This result verifies the derived temperature coefficient in (5.22) of the discharge time T_{dis}.

5.3.4 Results and Discussions

This current comparator based relaxation oscillator provides a low-frequency oscillation clock with a low-cost fully-integrated solution for the sensor readout circuit. It has the merit of good immunity to both temperature and supply variations whilst dissipating µW level power. The proposed circuit is realized in conjunction with the digital logic blocks using AMS 0.35µm CMOS technology. It generates the multi-phase control clocks for the operation control of the SC interface circuit. Table 5.3 summarizes the simulation results of the frequency variation with respect to the change of supply and temperature. The total frequency variation of the compensated oscillator over the temperature range of -40 to 90 °C is -1.8% (141ppm/°C). In terms of supply variation, the compensated oscillator frequency varies 0.16% for the supply varying from +/- 1.6V to +/-2.5V. The corner case simulation results have shown that the overall frequency variation under worst case condition (process, temperature and supply voltage) is –26% to +40% as the extreme range. Nevertheless, the SC system is insensitive to the clock frequency variation as far as the SC circuits can settle with the dedicated clock periods by the robust circuit design that takes into account of this lumped variation.

Table 5.3 Simulation results of frequency stability

Variation Parameter(s)	Value
Supply Voltage (+/-1.6V--+/-2.5V, Typical process, 27°C)	0.16%
Temperature (-40°C to 90°C, Typical process, +/-2.5V)	-1.8% (141ppm/°C)
Overall Worst Cases (Process, Temperature and Supply Voltage)	-26%--+40%

5.4 Digital Control Logic for Multi-Phase Clock Generator

The control clocks for first-stage AZTMD-CVC and second-stage SC programmable gain amplifier are shown in Fig. 5.16. These include the master reset clock Φ_1, which is twice the frequency of that of the multiplexed clock $\Phi_1/2$, two sets of non-overlapping control clocks: (1) the charge transfer clocks T_1, T_2 together with the respective sample and hold sub-clocks T_{1S}, T_{2S} and (2) charge transfer control clocks P_1, P_2 and their advanced counterparts P_{1a} and P_{2a} for SC gain stage.
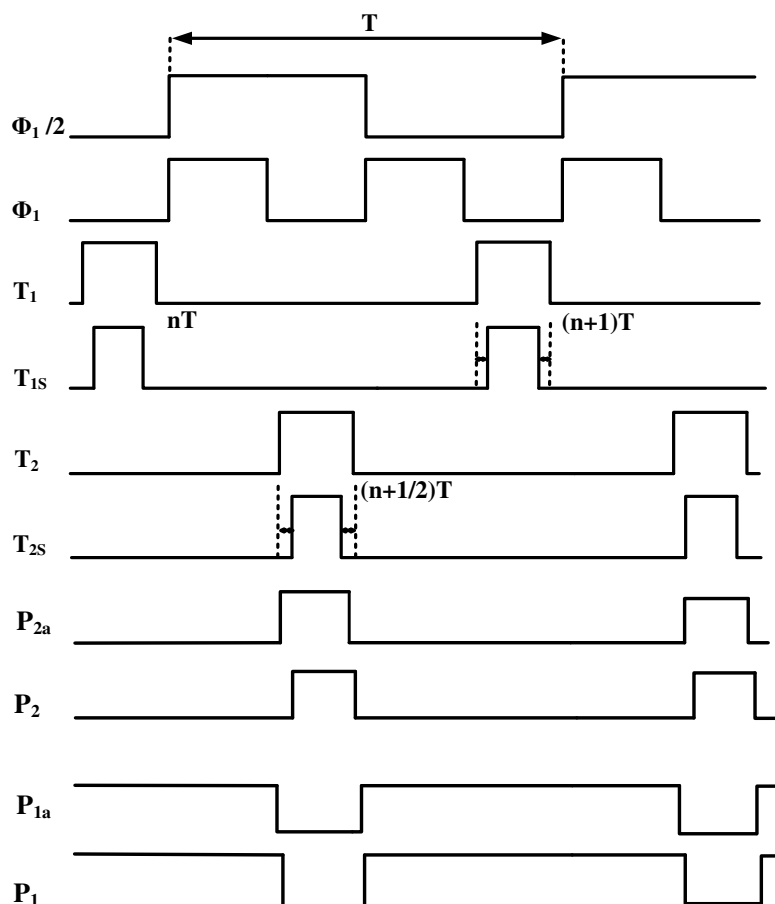
Fig. 5.16 Control clock signals for the SC readout out circuit

135

Fig. 5.17 shows the digital control logic blocks inside the multi-phase clock generator. Apart from the relaxation oscillator, it involves three sets of two-phase non-overlapping clock generator, one dynamic D Flip-Flop frequency divider as well as the basic AND gates, driving buffers and some delay blocks.
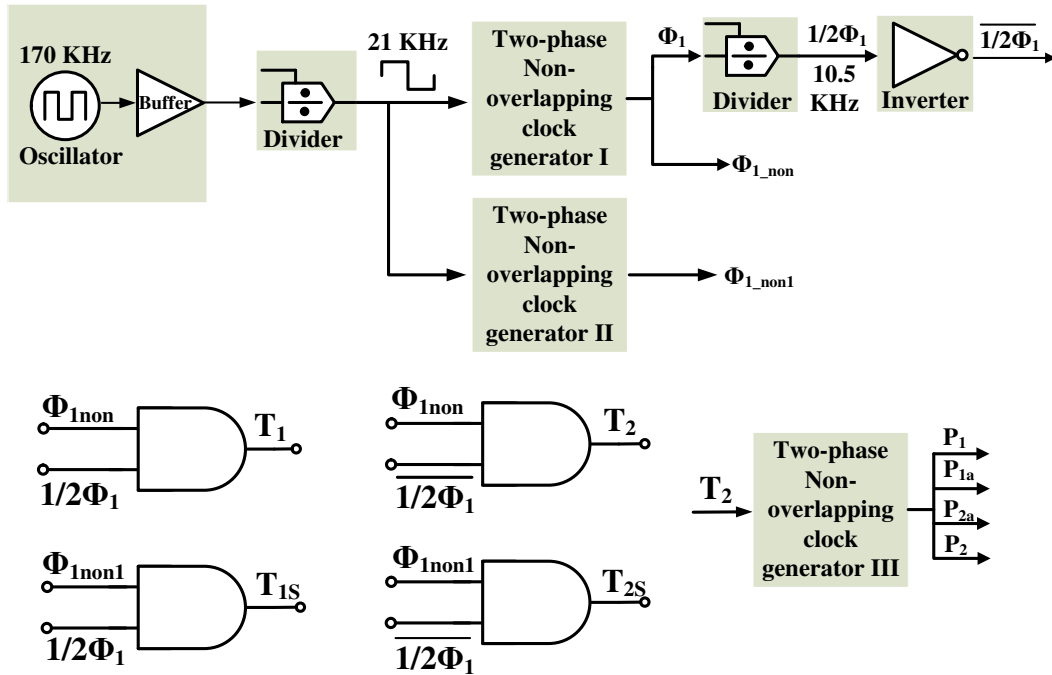
Fig. 5.17 The digital control logics for multi-phase clock generator.

The clock signal from the on-chip temperature compensated relaxation oscillator will first pass through a frequency divider, yielding the 21 kHz master clock. All the rest control signals are generated based on this master clock. The 21 kHz master clock will first pass through two non-overlapping clock generator blocks to generate the master reset phase clock Φ_1 with its two non-overlapping clocks Φ_{1_non} and Φ_{1_non1}. In order to get the charge transfer control clocks T_1 and T_2, the master clock Φ_1 is further divided to achieve a half frequency clock $1/2\Phi_1$ and its inverted version $\overline{1/2\Phi_1}$. Using a simple AND gate, the clock signals Φ_{1_non}, Φ_{1_non1}, $1/2\Phi_1$ and $\overline{1/2\Phi_1}$ are combined to

generate the non-overlapping charge transfer clocks T_1, T_2 as well as their sub sample-and-hold clocks T_{1S} and T_{2S}. With clock signal T_2 passing through a third two-phase non-overlapping clock generator, the control clocks P_1, P_2 for SC gain stage are generated.

5.4.1 Frequency Divider

5.4.1.1 Divide-by-2 Counter and Ripple Chain

Fig. 5.18 shows the configuration of a dynamic DFF used as a divide-by-2 counter for frequency division purpose. Configured as a binary divider, the output terminal Q_ of the DFF is fed back to the data input terminal D. Through feeding back the output from Q_ to the input terminal D, the output clock frequency at Q will be divided by a factor of 2 from that of the input clock frequency.
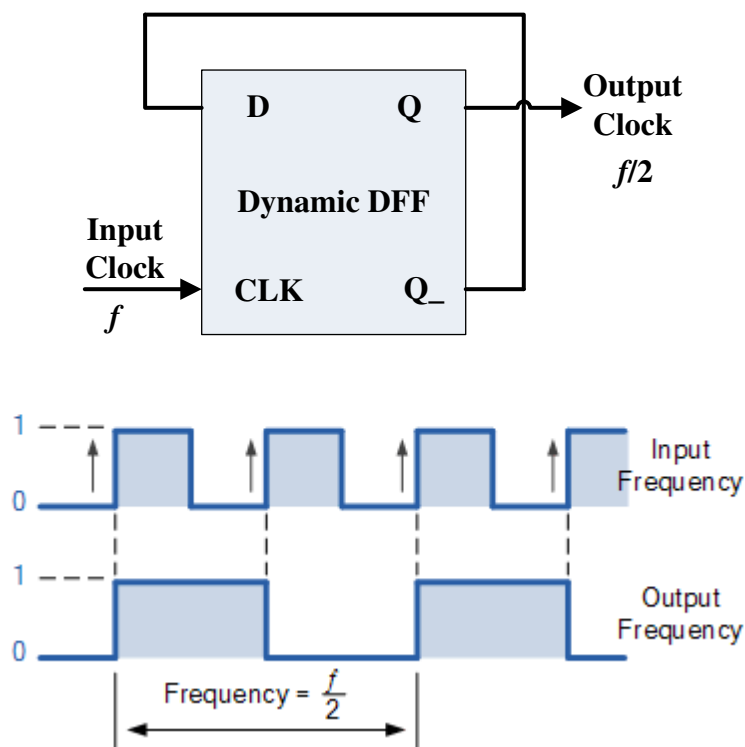
Fig. 5.18 Dynamic DFF configured as a divide-by-2 counter

This divide-by-2 counter can be cascaded in a ripple chain configuration by connecting the output of the first DFF to the input of the second DFF and so on. Hence, the input clock signal will trigger the first DFF and generate an output clock with half of the frequency of that of the input clock. The half frequency clock will in turn trigger the input of the second DFF and generate a quarter clock frequency of that of the original input clock, which will again be the input triggering signal for the following DFF stage. The chain formed by the cascaded divider-by-2 counter is named as ripple counter. As the signal passes though the ripple counter chain, ripple effect will be created and the final output clock frequency is equal to the input clock frequency divided by the factor of 2^N. N is the number of the divide-by-2 counter in the ripple chain. Fig. 5.19 shows the implementation of divider-by-8 counter.
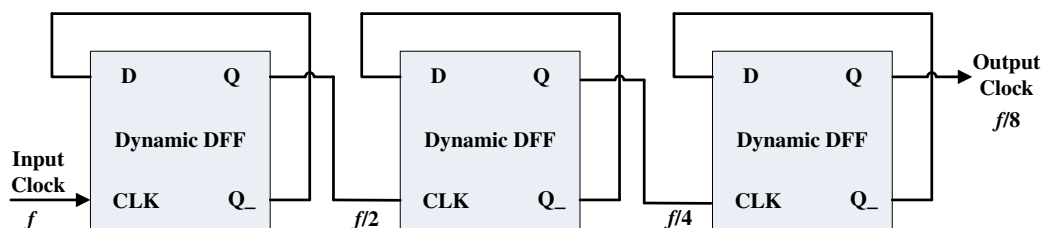
Fig. 5.19 Divide-by-8 counter

5.4.1.2 Dynamic D Flip-Flop

Fig. 5.20 shows the schematic of the dynamic DFF. This structure is a master-slave negative edge-triggered D Flip-Flop. The basic functioning blocks of the dynamic DFF are two clocked inverters controlled by two complementary clock signals CLK and CLK_. Hence it is typically called the clocked CMOS (C^2MOS) Flip-Flop. The function of the two clocked inverters formed by transistors M_1 to M_4 and transistors M_5 to M_9 respectively are similar to a tri-state inverter. Specifically, when CLK is high and CLK_ is low, the first

138

inverter is on while the second is off. The signal is clocked into the storage capacitor formed by the parasitic capacitance associated with the output of the first inverter and the gate capacitance at the input of the second inverter. In the negative cycle of CLK, the first inverter is off while the second is on. Finally, the signal is clocked out. The simple CMOS inverter formed by M9 and M10 is used to complete the feedback path needed for the toggle latch. The dynamic DFF uses much less transistors in the circuit and consumes less power consumption when compared with the static state version.

Fig. 5.20 Schematic of the dynamic DFF

5.4.2 Two-Phase Non-Overlapping Clock Generator

Fig. 5.21 shows the implementation of the non-overlapping clock generator. The delay blocks inside the non-overlapping generation network are necessary to define the non-overlapping time between the clock signals Φ_1 and Φ_1_non to ensure that at no time will both two signals be high. It is implemented through a cascade of even number of inverters with RC delay network as the load. Simple

buffers composed of inverters are added to ensure the drivability. Three non-overlapping clock generators with different delay time are used in the multi-phase clock generator to generate three sets of non-overlapping clocks.
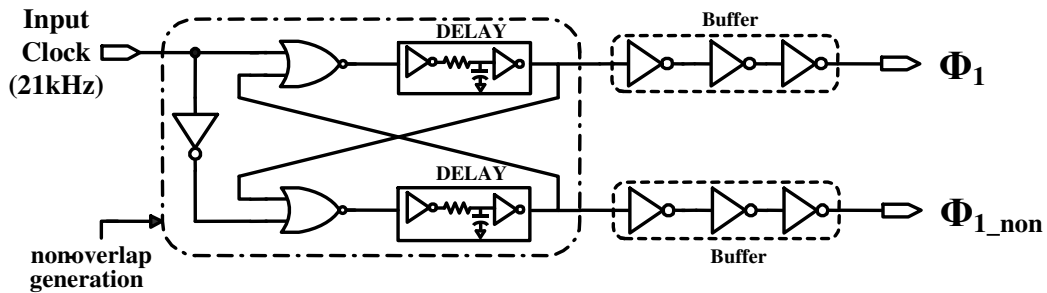
Fig. 5.21 Non-overlapping clock generator

5.5 Summary

In this part, two low-frequency temperature compensated oscillator schemes are examined and implemented for sensor applications. One is the low-frequency CMOS ring oscillator utilizing a simple temperature compensated source follower driving structure. The compensated oscillator shows the feature of low power, low phase noise, low jitter and wide temperature operation range with small temperature drift. Due to the self-biased and source follower topology, the oscillator displays good immunity against the supply variation. The embedded pseudo-resistive low-pass filter and the closed-loop temperature-compensated replica bias for the open-loop source-follower supply source significantly improve the jitter performance of the circuit. The second one is a V_{dd}-tracking temperature compensated current comparator based relaxation oscillator. This structure makes use of the temperature cancellation property between the negative temperature dependent poly-resistor and positive temperature

140

dependent Nwell-resistors. It achieves fully-integrated solution by saving pin counts and cost for the interface IC. It has the properties of high immunity to temperature and supply variations. Besides, this scheme proves to be a low power design with high robustness in the context of process variation.

The digital control logic blocks of the multi-phase clock generator are also presented. Together with the proposed oscillator circuit, it generates the required control clocks for the first stage AZTMD-CVC as well as the SC programmable gain stage for proper system operation.

CHAPTER 6

MIXED-SIGNAL ACCELEROMETER ASIC SYSTEM LAYOUT CONSIDERATIONS

In mixed-signal system which comprises both analog and digital functional blocks, special care must be given to the system layout design to prevent any noisy digital signals from coupling to the sensitive analog signal paths [82]. In order to achieve a high quality post-fabrication chip performance, a careful system floor plan at the system layout design together with special techniques aiming to reduce any unwanted noise sources must be conducted through the whole layout design process. This Chapter will give the techniques used in this micro-accelerometer interface system design with special attention on low noise layout.

6.1 Floor Plan of the Accelerometer ASIC Interface

In any kind of layout design, system floor planning is always the most important stage for a high performance system in which the circuit and system degradation from the practical fabrication will be kept as minimum as possible. In a system floor plan stage, the designer should decide where all circuit blocks are arranged and placed in conjunction with the routing of signal lines. The procedures are explained in the following. First, the width of the power supply lines must be carefully considered to reduce the supply line resistance, particularly for the ground and supply lines. Second, all the input and output signals must be listed and the functioning blocks should be roughly arranged according to the main signal flow direction. Third, after listing all the input and

output signals, the sensitive signal lines must be identified and the placement of the functioning blocks may need to be rearranged accordingly. Each signal port should be assigned to a proper location in order to permit the pad ring arrangement. Fourth, areas for internal routing and signal connections should be allocated and the routing layer in each interconnect area should be considered.

Taking into consideration of the floor plan, the routing of power supplies and ground lines, the routing of critical signal paths and the identification of possible noise coupling paths from digital blocks, the overall placement of the building blocks of the interface system is illustrated in Fig. 6.1.
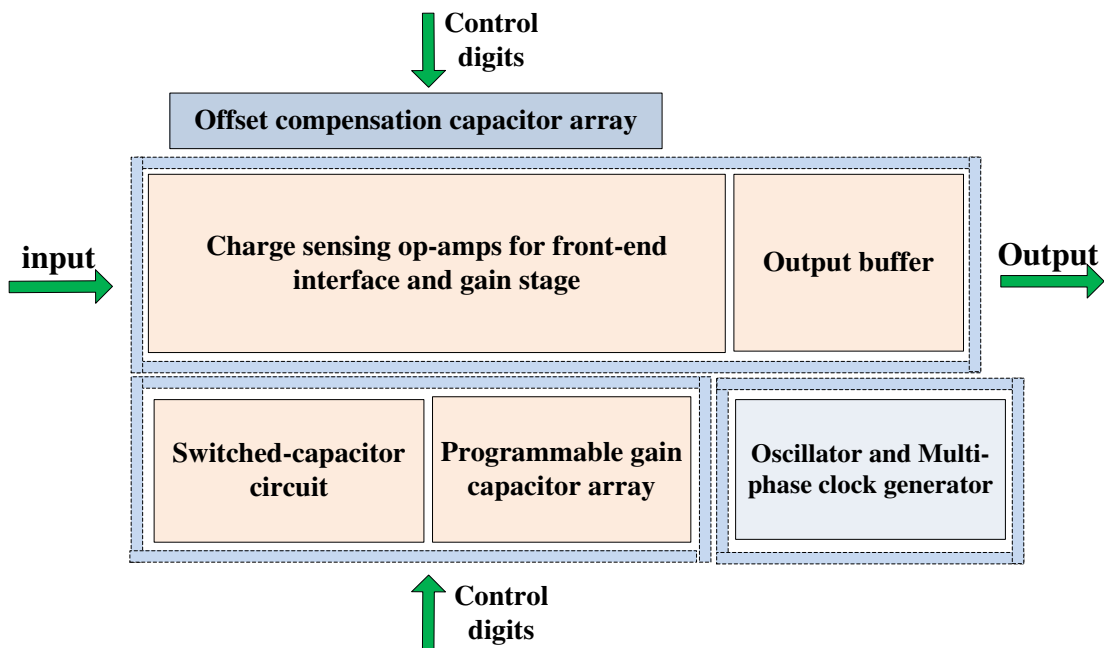
Fig. 6.1 Floor plan of sensing interface system layout

In this floor plan design, the main system signals start from the left hand side of interface and exits from the right hand side for connecting to either next stage electronics in a system-on-chip environment or the boundary of test chip in this design. The analog charge sensing op-amp and output buffer section are kept as

far as possible from the oscillator and clock generator block. The analog section is surrounded with double guard rings to prevent noise from coupling through the substrate and the same goes for the digital counterpart to minimize the digital noise injecting into the substrate. The PADs nodes are allocated according to the signal location with the goal of as short distance as possible. All the critical lines, which is subject to potential noise coupling effects from the environment, are identified. They will be shielded in the subsequent layout stage. The system layout configuration is shown in Fig. 6.2.
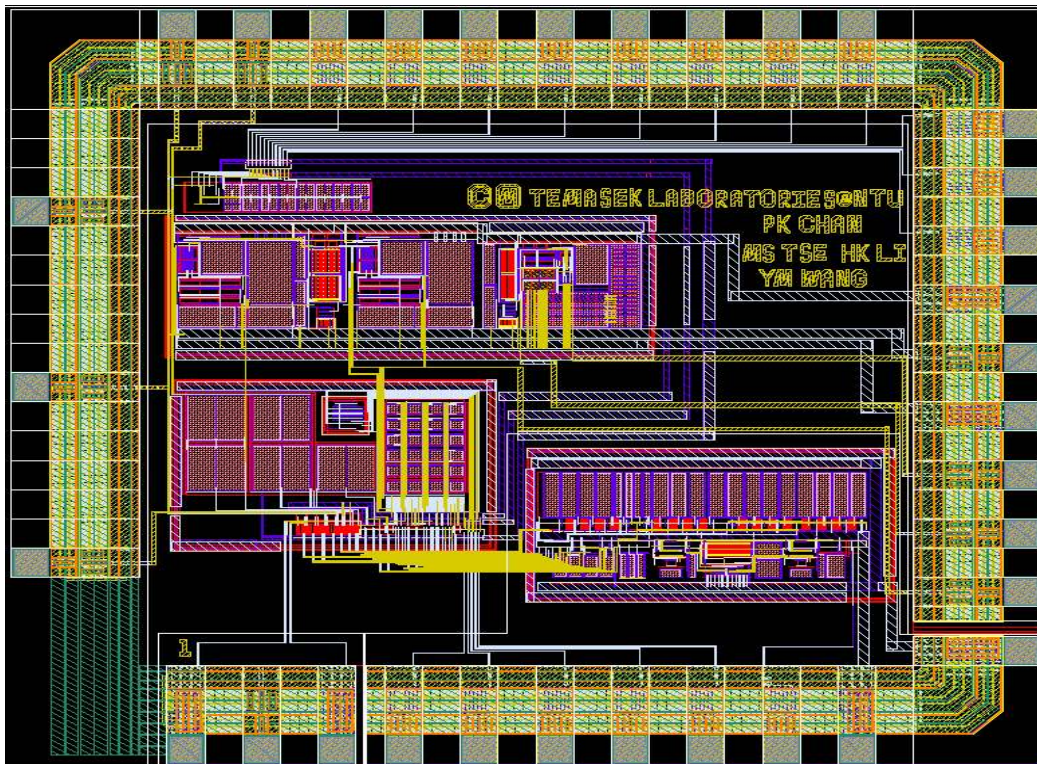
Fig. 6.2 System layout in AMS 0.35µm CMOS technology

6.2 Low-Noise CMOS IC Layout Techniques

Digital circuitries of the mixed-signal system always carries high frequency switching signals which will be easily injected into the substrate or coupled to the power supply lines. This is not an issue for the digital blocks themselves.

On the other hand, it is a concern for the analog circuitries which is sensitive to noise signals, particularly the low-noise front-end readout circuit. Besides, signal coupling always exists among signal lines themselves, signal lines to power supply lines and signal lines to substrate. Therefore, the important layout techniques pertaining to minimize various noise sources are described. They have been realized in this mixed-signal layout design. Finally, separate analog and digital power supply and supply decoupling are employed for mixed-signal system.

6.2.1 Reduction of Digital Signal Coupling Through Substrate

Fig. 6.3 illustrates the digital-to-analog signal coupling mechanism through on-chip substrate and its reduction technique. A typically used method is to lay out a N-well layer under the noisy digital circuitry area and add guard rings around both the digital and analog part to reduce the substrate coupling effect.
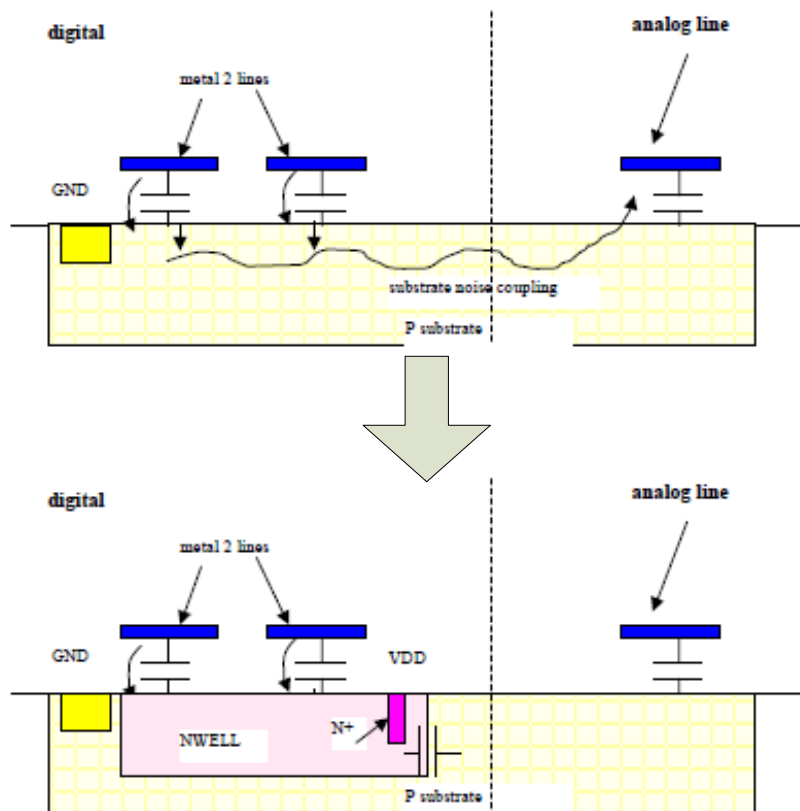
Fig. 6.3 Digital signal coupling mechanism through substrate and its reduction

6.2.2 Cross-Talk Reduction Between Integration Capacitors

In SC circuits, capacitive coupling is a most common phenomenon. Several techniques are implemented to help minimize these effects. Fig. 6.4 shows the typical integration capacitor layout which has two common cross-talking mechanisms existent in this layout. Refer to the figure, the first mechanism is through signal coupling between capacitors carrying different signals, like the cross-talking between two poly capacitors or poly capacitors to poly1-N-well parasitic capacitors. The second cross-talking mechanism comes from substrate resistive coupling.
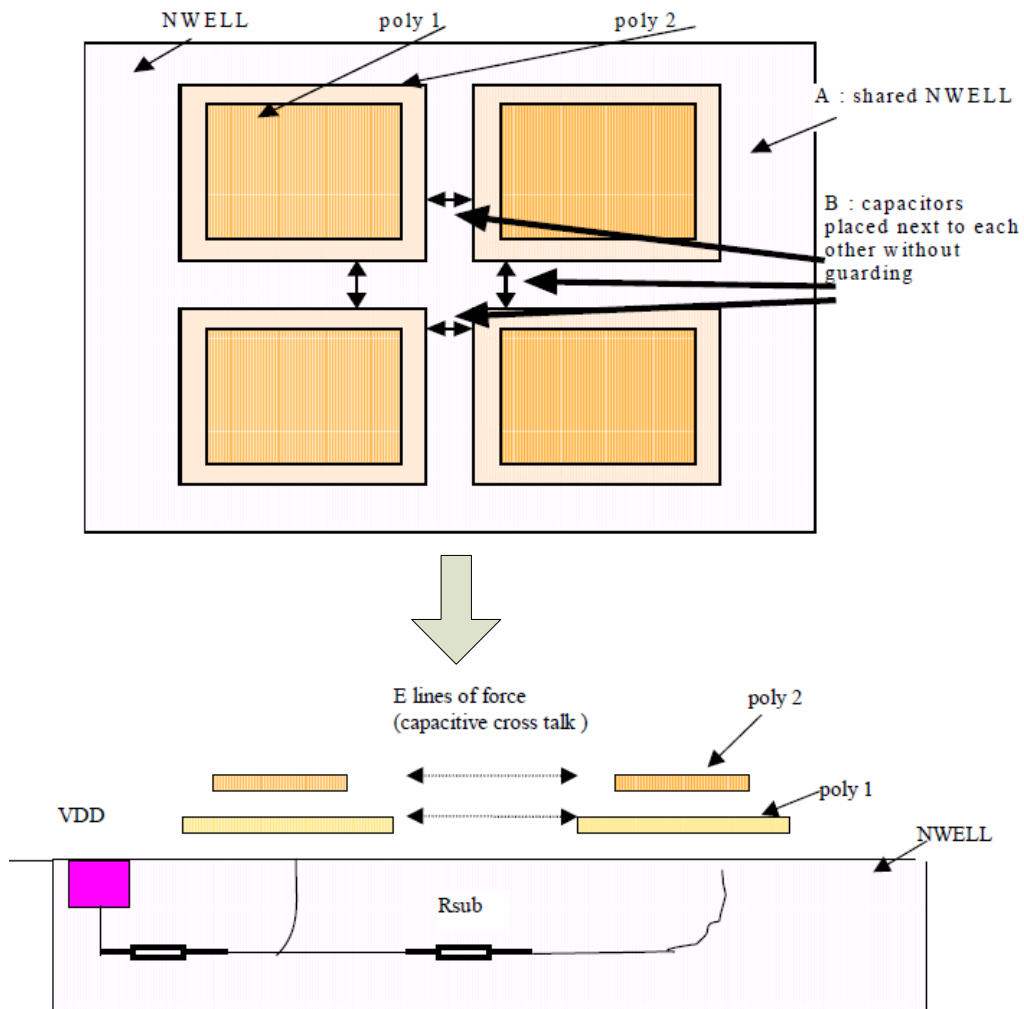
Fig. 6.4 Various cross-talk mechanisms in the layout of integration capacitors (a) between capacitors carrying different signals, (b) substrate resistive coupling

Fig. 6.5 shows the improved layout configuration. In this improved layout, the adjacent capacitors are shielded through placing grounded dummy capacitors in between individual signal capacitor. Besides, each capacitor has its own N-well area. The V_{DD} lines are connected to the power supply source in a star point configuration.
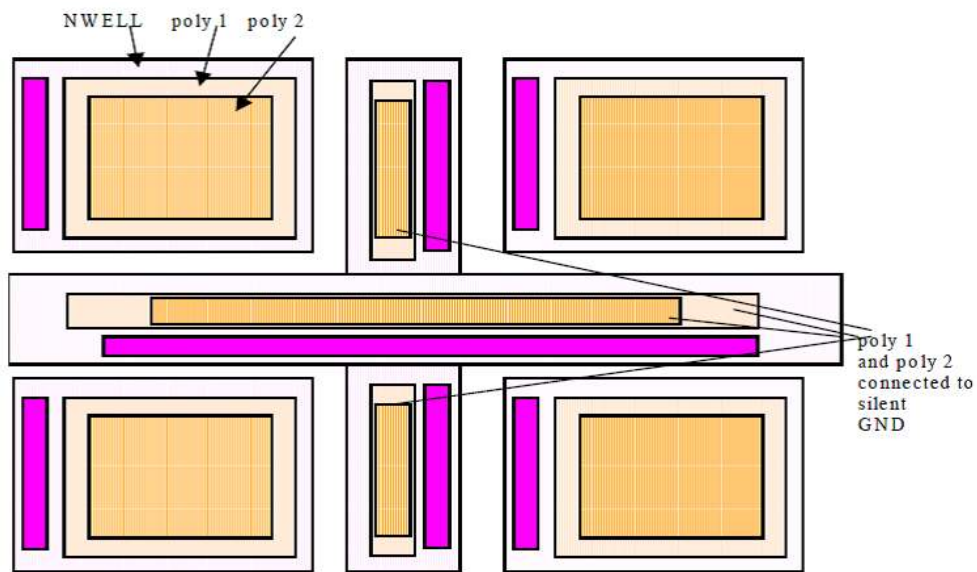
Fig. 6.5 Capacitors layout with shielding dummy capacitors

6.2.3 Guard Rings for Analog Switches

Cross-talk phenomenon will also happen between analog switches through substrate. P+ guard ring is laid out around each analog switch to absorb the substrate current, hence reducing the signal coupling. Although this method may increase the silicon layout area, the low-noise performance is of highest priority.
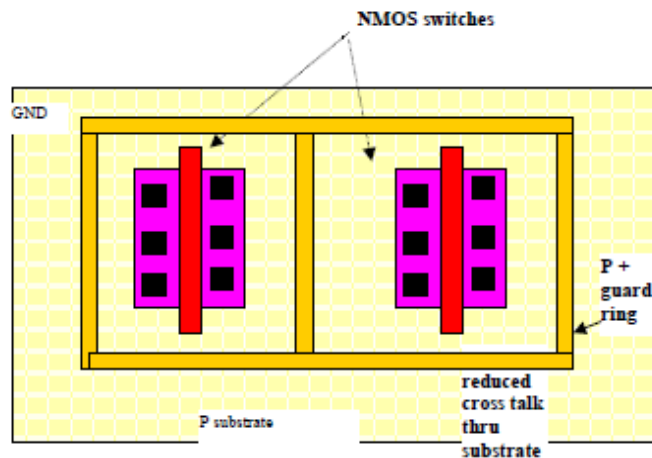
Fig. 6.6 Analog switches with individual guard rings

6.2.4 Shielding Structure for Critical Analog Paths

Noise signals exist at almost every part in the IC chip. Special attentions must be paid to those critical signal paths. They are the metal lines connected to capacitors, the analog input lines themselves and the connection between switches and op-amps. Apart from increasing the space between signals on the same layer to reduce the coupling capacitance between them, several shielding techniques are employed to reduce the signal coupling effect. As shown in Fig. 6.7, the concept of shielding signals is to insert a signal path at a static voltage level in between the critical signal routes. Fig. 6.8 shows a more complicated shielding structure where the signal lines in question are completely shielded by the surrounded layers.
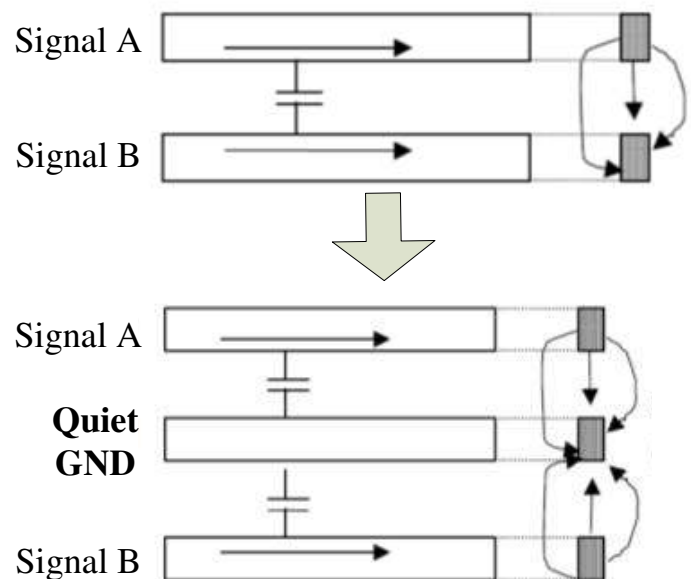
Fig. 6.7 Shielding the critical analog signal lines with a quiet signal line
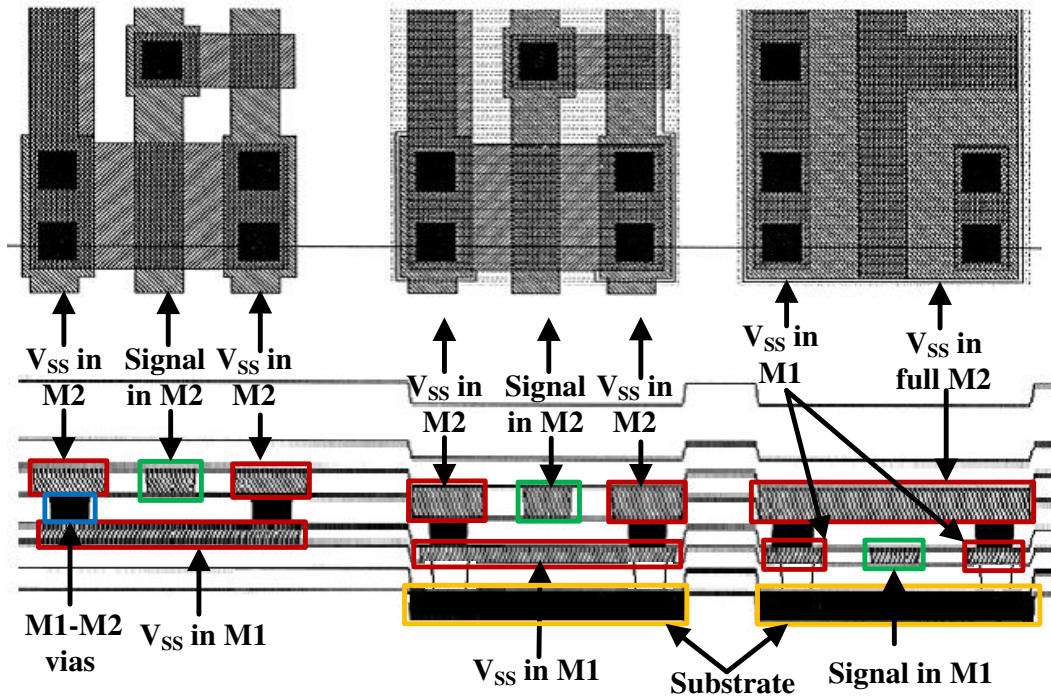
Fig. 6.8 Shielding examples in two metal process [83]

6.2.5 Post-Layout System Simulation Results With and Without the Cross-Talk Reduction Layout Technique

Fig. 6.9 and Fig. 6.10 illustrate the post-layout transient simulation results of the readout IC without and with integration capacitor cross-talk reduction and critical signal line shielding in the layout respectively. Each graph shows two transient voltage signals at the second differential-to-single-ended gain stage output and the low-pass filter output. The capacitive sensor is set under 0.1mg sinusoid acceleration. Under small acceleration excitations, it can be seen obviously from these two transient output voltages in purple curves (with the low-pass filter) that the layout, with the dedicated cross-talk reduction technique, efficiently helps the reduction of extra coupling signal, hence improving the readout signal quality when the minute sensing signals are encountered in the SC sensing system.
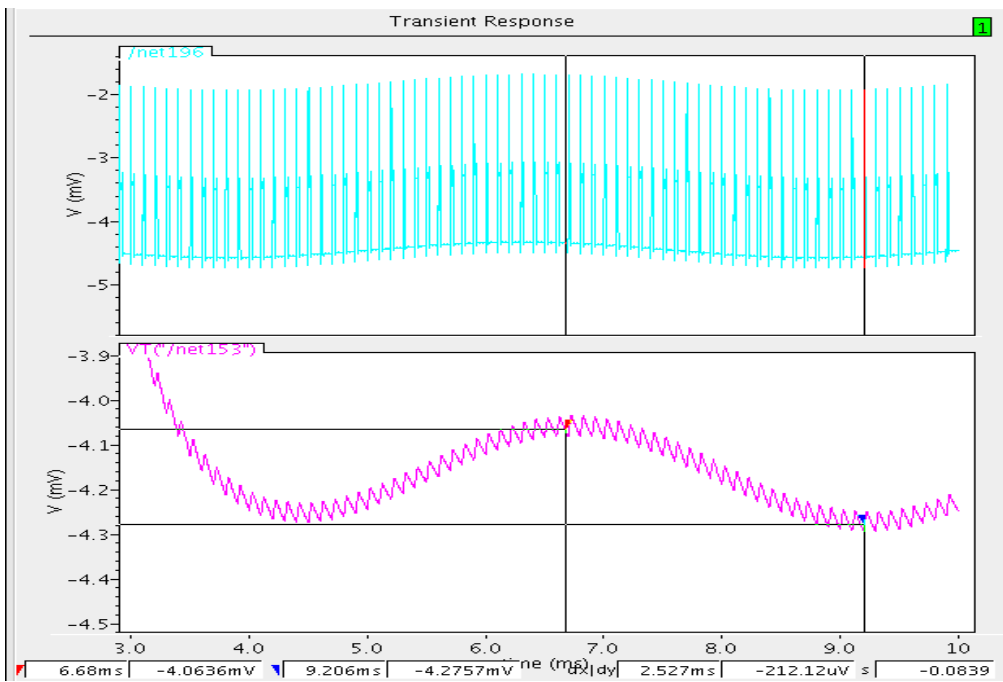
Fig. 6.9 Post-layout system simulation result under 0.1mg without cross-talk reduction technique
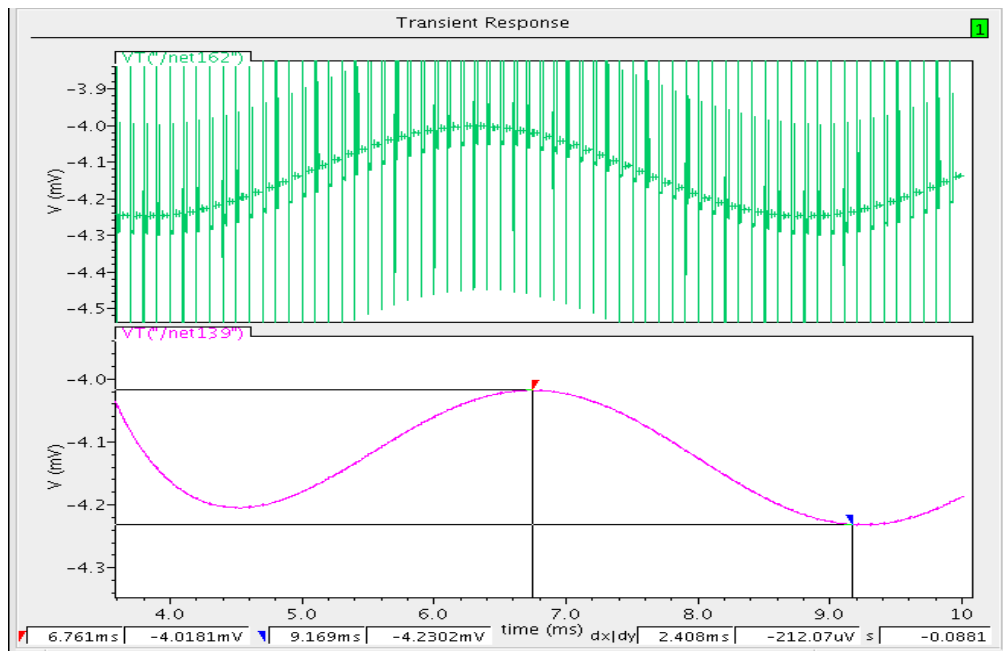
Fig. 6.10 Post-layout system simulation result under 0.1mg with cross-talk reduction technique

6.3 Low-Noise PCB Layout

Apart from a careful IC layout, PCB layout also plays an important role in ensuring a quality testing environment to prevent unwanted noise signal from going into the testing board whilst without jeopardizing the testing performance. Several commonly-used methods for low noise PCB layout design are presented.

First, the signal layers and power source layers should be determined. In this PCB design, it adopts a four-layer board with the signals lines routing on the top or bottom outer layers whereas the power and ground planes are located in the inner layers. It is easier to operate when placing the signal routing on the outer layers. On the other hand, the power and ground layers placed adjacent to each other at the center of the board will provide a larger decoupling capacitor as well as create the shield between different signal layers. Second, the star configuration for power and ground planes are used in order to minimize the noise cross talk in mixed-signal environment. Third, on the signal layers, the analog and digital circuitries should always be laid out apart from each other. It is often better with their separate ground planes. The overlaps between analog and digital areas are avoided. Fourth, power lines decoupling should be placed exactly at the shortest point where the power leads run into the board, thus preventing the return currents from passing through the ground planes. Fifth, decoupling capacitors must be added to all the analog IC chips' power leads to filter both high-frequency and low frequency noise. A general rule [84] is to place a small decoupling capacitor of 0.1 μF or 0.01 μF in parallel with a larger capacitor value of 10 to 47 μF and they are very close to the IC chip on the same layer.

CHAPTER 7

MEASUREMENT RESULTS & DISCUSSIONS

7.1 Accelerometer ASIC

Two interface ASICs have been designed and fabricated using AMS 0.35-µm CMOS 3.3/5V process in this project. Fig. 7.1 and Fig. 7.2 show the microphotographs of the two implementations of ASIC interface circuit with labeled dimensions. Each building block is highlighted in white box with its function name indicated. Refer to the second version in Fig. 7.2, it has the identical implementation with that in Fig. 7.1 but an interface block for Microprocessor Unit (MCU) is added for future system application. The electronic interface IC shown in Fig. 7.1 is wire-bonded using QFN 40-pin package whereas QFN 52-pin package is used in second version interface IC.

For testing purpose, PC boards with necessary peripheral circuits are designed and implemented. For the first PCB design, a series of jumpers and different values of discrete capacitances are used to model as the sensing element to test the sensitivity and verify the function of ASIC. These discrete capacitances range from 1 to 10pF. As there is relatively big variances in the absolute capacitance value of the discrete capacitor components together with the bonding parasitic capacitances, LCR meter with a minimum resolution of 0.01fF for capacitance measurement is used to verify each capacitor's value for more precise measurement. The measurement results have shown that the interface circuit exhibits a sensitivity of 145.45mV/pF. The testing result verifies the functionality of the interface circuit. For the second PCB design, the accelerometer sensor device is wire bonded to a standard DIP14 package (only

153

three pins are used) and is mounted onto the PC board together with the ASIC for system testing and verification. The testing results and discussions will be given in the following part.
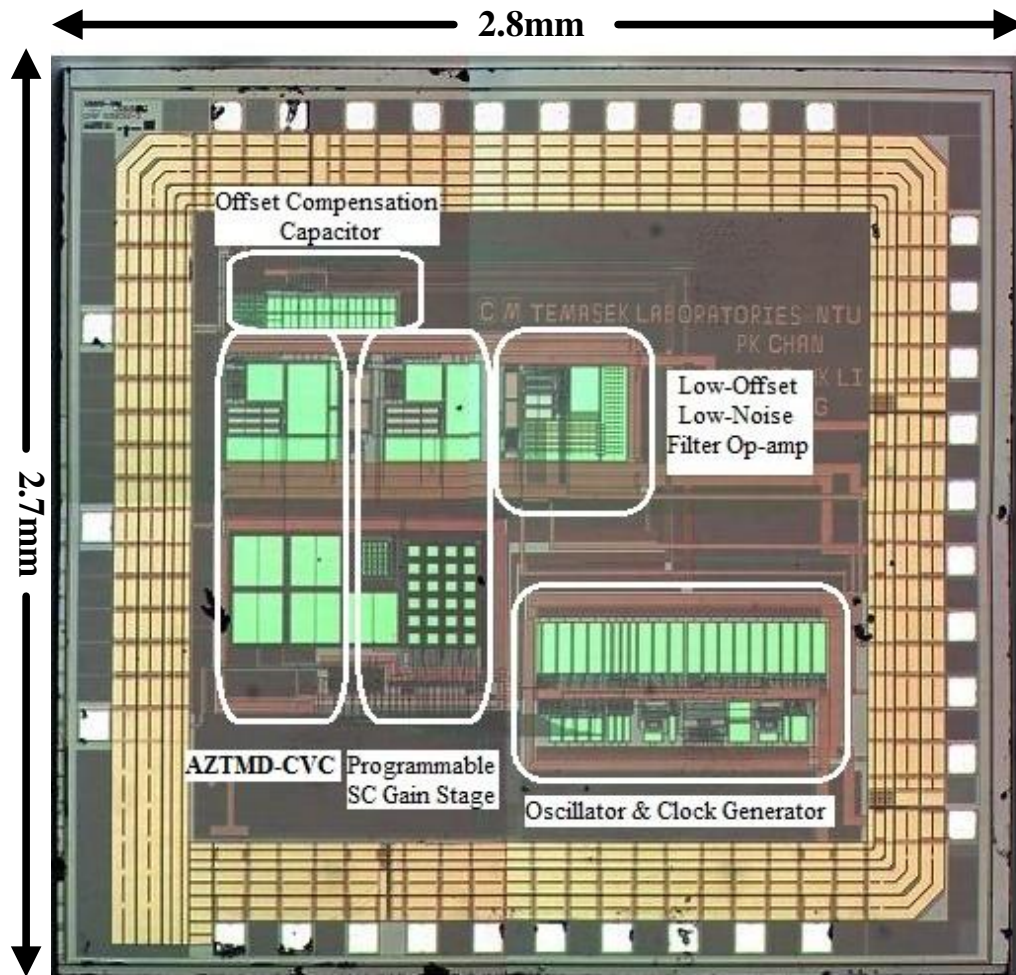
Fig. 7.1 Microphotograph of the first-version accelerometer ASIC
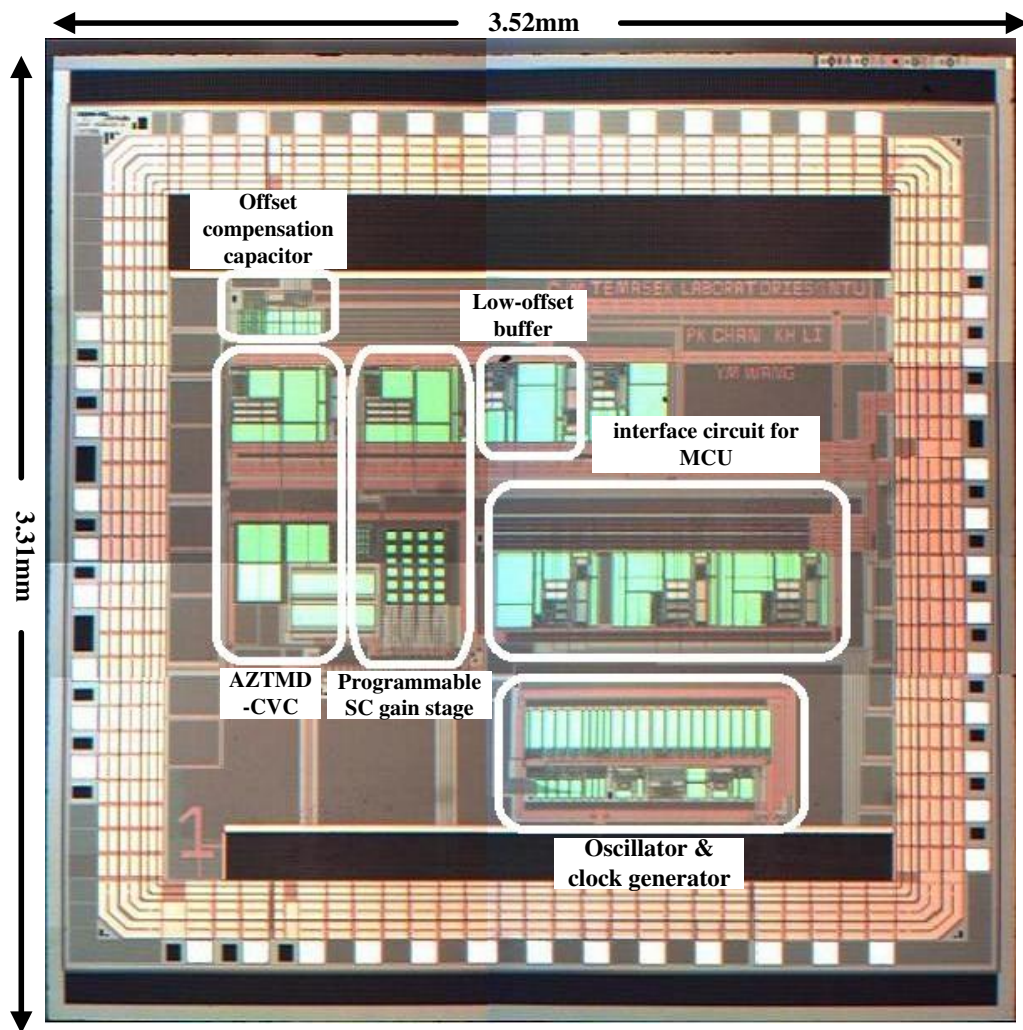
Fig. 7.2 Microphotograph of the second-version accelerometer ASIC with added interface for MCU

7.2 PCB Prototype and Test Setup

Fig. 7.3 shows the prototype of the PCB for the test and characterization of the accelerometer sensor system.
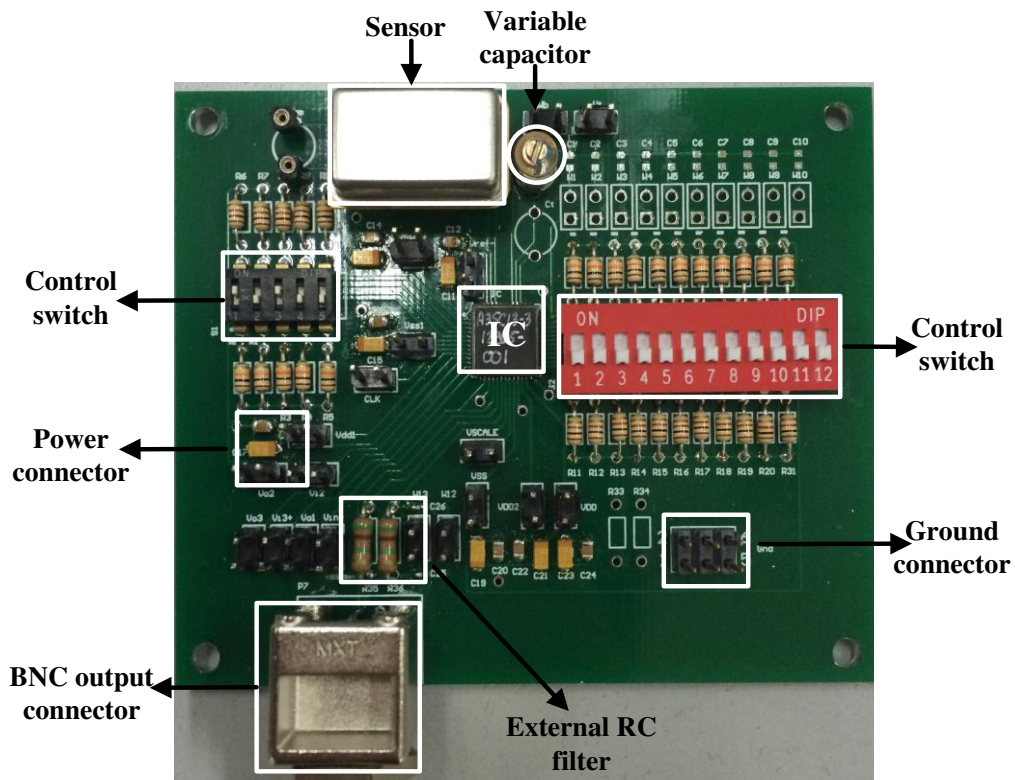
Fig. 7.3 PCB prototype for test

Due to non-perfect manufacturing, the capacitive micro-accelerometer sensor has unbalanced parasitic capacitances. Hence, in order to compensate the difference between parasitic capacitances, a fine trimming offset capacitor with programmability for balancing the differential capacitive sensor is realized inside the IC chip. At the same time, an off-chip coarse offset trimming capacitor is realized on the PCB having variable capacitors to emulate the differential capacitance. It is able to be configured to attach either on top-middle or middle-bottom position in the respective sensing capacitor. The switch on the left part of the PCB is the 5-bit digital control for the programmable gain stage, while that on the right part of the PCB is used to control the 11 digits fine offset trimming circuit formed by a programmable capacitor array inside the chip. There are three sets of DC supply source

connectors with corresponding decoupling capacitors implemented close to them on the board, they are for the analog power supply, digital power supply as well as reference voltage sources respectively. The analog output is connected to a low noise BNC connector for noise shielding purpose.

The equipment and instruments used for the testing include two DC source suppliers, an oscilloscope, a spectrum analyzer, a 4.5 digits multi-meter, a thermal stream unit, a precision LCR meter, a precision tilting table and some other supporting equipment. The specifications of the equipment are summarized in Table 7.1.

Table 7.1 Equipment and instruments used in the test

Name	Model	Key features
DC supply source	Hewlett Packard E3631A	0-6V,5A/0-±25V,1A triple output dc power supply
Oscilloscope	Agilent 54641A	Bandwidth:350MHz Sample Rate: 2 GS/s Two channels
Spectrum analyzer	Agilent 4395A	Bandwidth: 10~500MHz NA, SA and ZA functions
Precision LCR Meter	HP 4284A	Frequency: 20Hz~1MHz Measurement Range: $|Z|$, R, X :0.01 mΩ to 99.9999 MΩ $|Y|$, G,B :0.01 nS to 99.9999 S C :0.01 fF to 9.99999 F L :0.01 nH to 99.9999 kH D :0.000001 to 9.99999 Q :0.01 to 99999.9 Accuracy: ±0.01% Output Impedance: 100Ω, ±3%
Thermal Stream	TPS 4000A	Temperature Range: -50~200°C
Tilting Table	---	Tilting Range: 180° Resolution: 0.002°

7.2.1 System Sensitivity

The system sensitivity test is performed under a 1 g gravitational field with the PC board mounted onto a precise tilting table which can rotate 180º to change the acceleration on the sensor from -1 g to 1 g with a resolution of 0.002º. Fig. 7.4 shows the output response of the micro-accelerometer system under -1 g to 1 g external acceleration. The system shows a sensitivity of 1.95 V/g with a nonlinearity error of 0.4%.
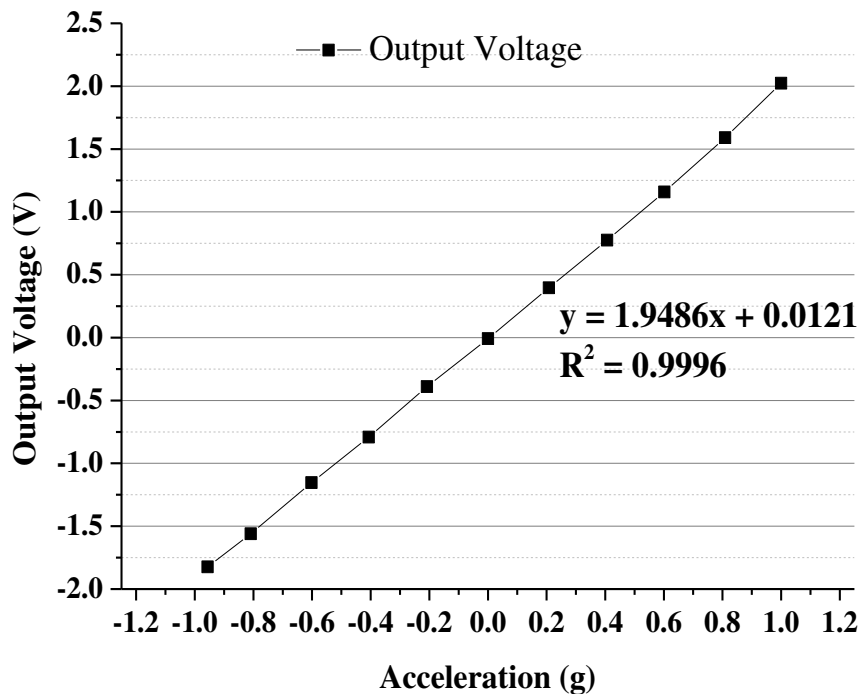
Fig. 7.4 Output voltage of the micro-accelerometer system against acceleration

7.2.2 Output Noise and In-Run Bias Instability

The measured output noise at 0g is shown in Fig. 7.5. The system achieves a low noise level of -100 dBm/Hz at 250Hz, which corresponds to an equivalent noise acceleration of 1.16 µg/√Hz. The total current consumption including the clock generator is 240 µA at a $\pm$2.5-V supply. The bias stability test is taken

under 0g acceleration over around 3 hours' time. The Allan variance analysis plotted in Fig. 7.6 indicates a best bias stability of 7.5 µg.
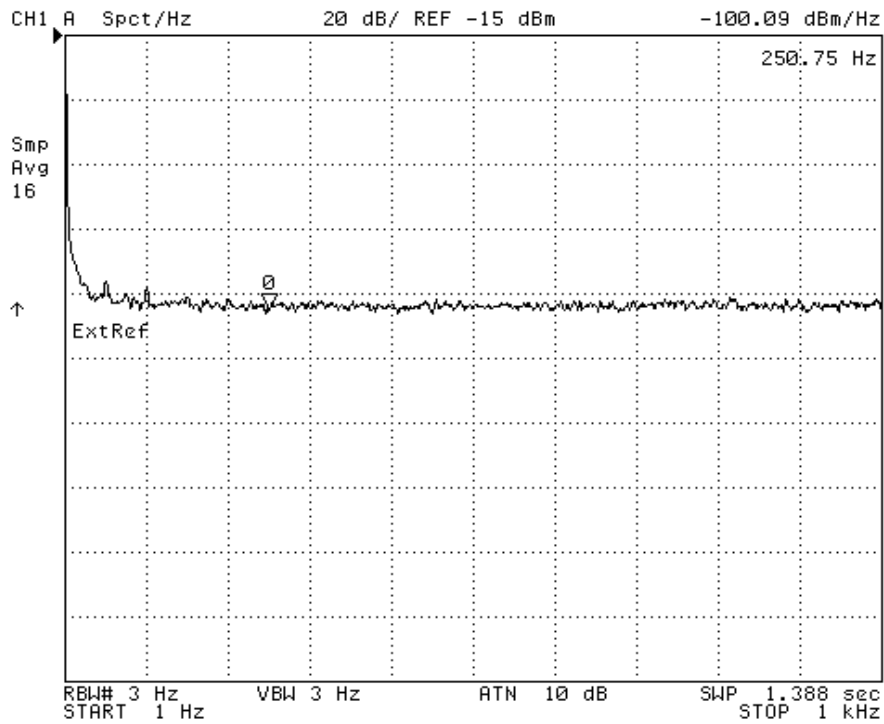
Fig. 7.5 Measured output noise at 0 g
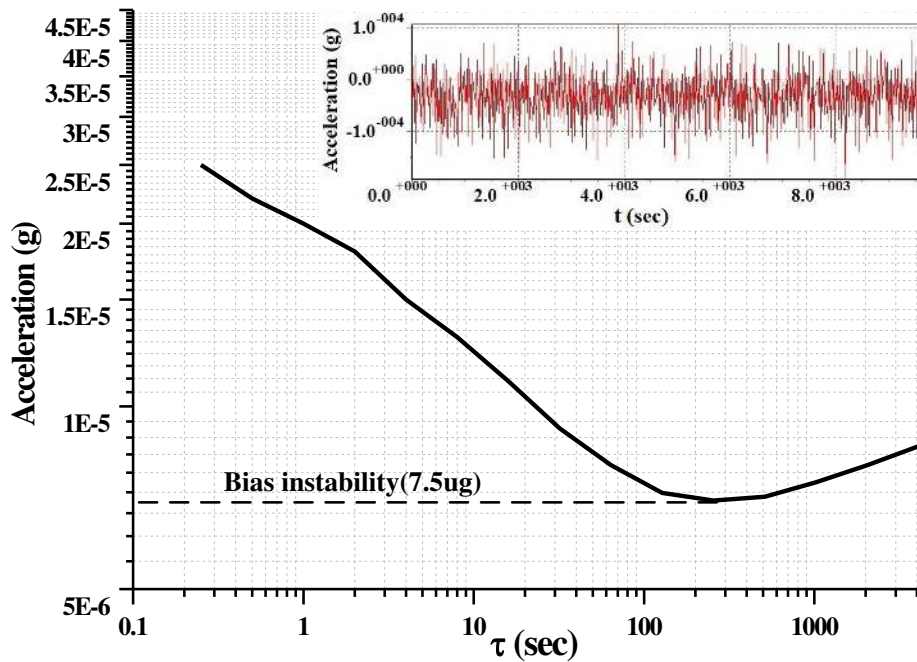
Fig. 7.6 Measured in-run bias instability

7.2.3 Performance Comparison with Prior-Art Works

Table 7.2 gives the measured performance as well as the comparison with other reported prior-art works. Fabricated using 0.35-µm CMOS technology, the ASIC chip is interfaced with a bulk micromachined capacitive accelerometer sensing device with µg resolution. With the measured accelerometer system sensitivity of 1.95 V/g, the system noise floor is only of 1.16 µg/√Hz at 250 Hz. The output noise-power product FOM is 0.28 (µg/√Hz)×mA with a total supply current of 240 µA at a ±2.5 V supply. It has shown that the proposed accelerometer IC achieves the best FOM in terms of output noise-power product. This has demonstrated the effectiveness of simple time-multiplexed single-ended CVC architecture, low-noise OTA design and noise-power optimization method.

Table 7.2 Performance comparison of the proposed accelerometer IC with reported works

Parameter	[85] JSSC 2006	[86] JSSC 2006	[87] ISSCC 2008	[88] ISSCC 2010	[89] JSSC 2013	This work
Process Technology [μm]	0.5	0.5	0.6	0.35	0.18	0.35
Power Supply [V]	3	5	3	3.6	3	±2.5
Brownian Noise Floor (BNEA) [μg/√Hz]	1	0.7	--	1	--	0.9
Total Output Noise Floor (TNEA) [μg/√Hz]	4	1.08	6.3	2	220	1.16
Total Sensitivity [V/g]	3	0.96	0.2	0.79	--	1.95
Power Dissipation [mW]	4.5	<7.2	3.75	8.64	3.1	1.2
Total Current [mA]	1.5	<1.44	1.25	2.446	1	0.24
FOM=Product of Output Noise and Current Consumption [(μg/√Hz)×mA]	6	<1.55	7.88	4.89	220	0.28
Chip Area [mm²]	2.25	3.42	--	9.5	9	7.28
Active Area [mm²]	--	--	0.33	2	1.35	3

7.3 Low-Offset Low-Noise Buffer

The low-offset low-noise output buffer is implemented using AMS 0.35μm CMOS process technology. The performance under typical condition is summarized in Table 7.3. This low-offset buffer provides a high DC gain as well as an excellent low-noise performance with a total supply current of only 80 μA.

Table 7.3 Measured results of the low-offset low-noise amplifier

Parameter (V_{DD}=5V @ 27°C)	Measured Results
DC Gain	103 dB
Unity Gain Bandwidth	650 kHz
Phase Margin	65º
Mean Offset	488 µV
Standard Deviation	418 µV
Noise @ 1kHz	20 nV/√Hz
Total supply current	80 µA
Effective Load	100kΩ//100pF

The offset performance is evaluated from the measurement results of 8 samples. Fig. 7.7 shows the offset distribution of the buffer stage. The average offset is 488 µV with a standard deviation of 418 µV. Despite of the small available sample numbers, it has demonstrated the trend of the offset distribution. As can be seen from the graph, 7 out of 8 samples have an offset less than 1mV. This low-offset low-noise output buffer is well suited for the signal-conditioning circuits for low-cost sensor applications.
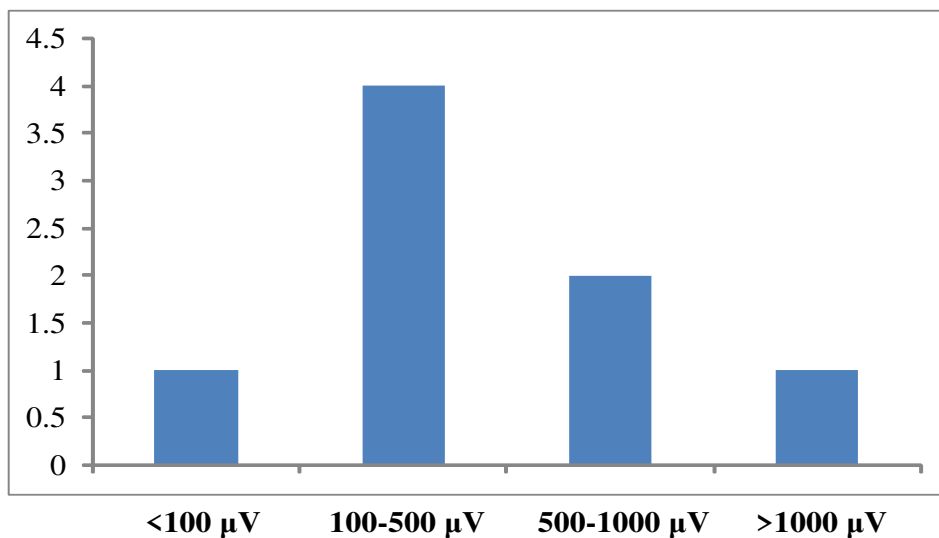
Fig. 7.7 Offset distribution of the low-offset buffer

7.4 On-Chip Relaxation Oscillator

Fig. 7.8 shows the setup for the temperature performance test of oscillator. Fig. 7.9 shows the clock signal from one sample. The V_{dd}-tracking current comparator based relaxation oscillator provides a 172 kHz fundamental clock for the interface circuit. The power consumption of this oscillator circuit is only 20 μW.
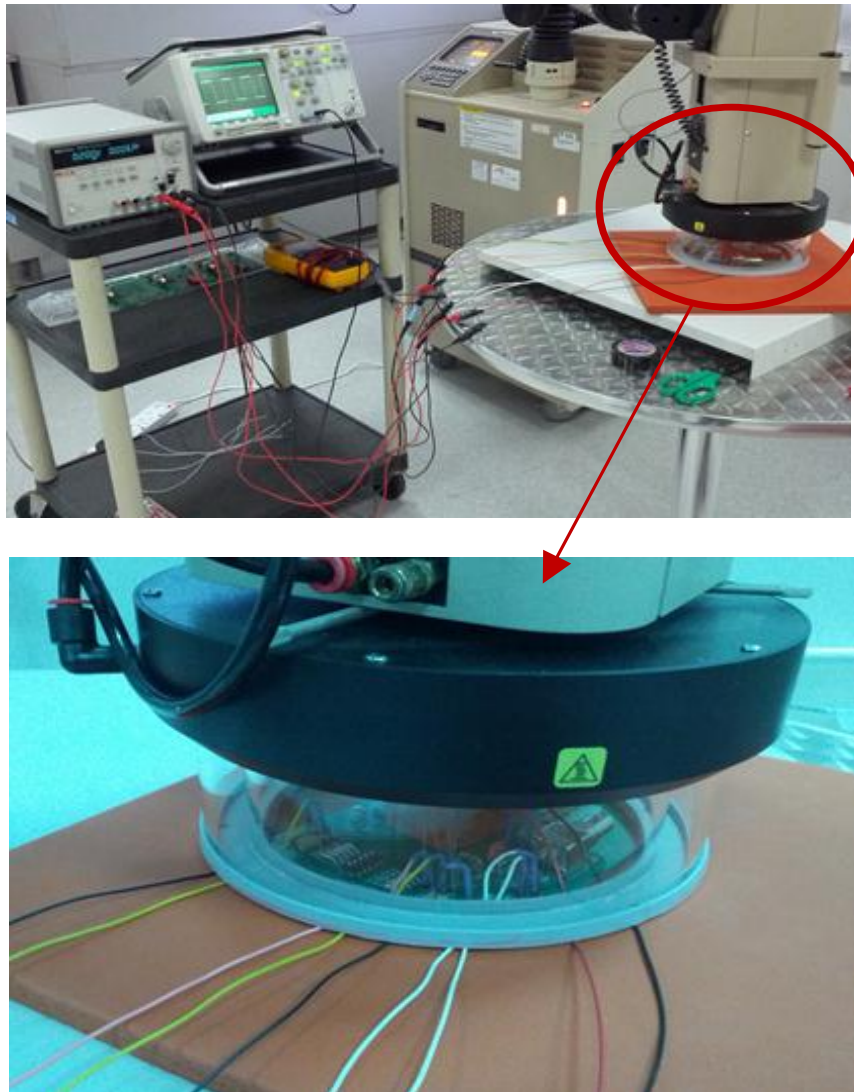
Fig. 7.8 Experimental setup for temperature performance testing of on-chip oscillator
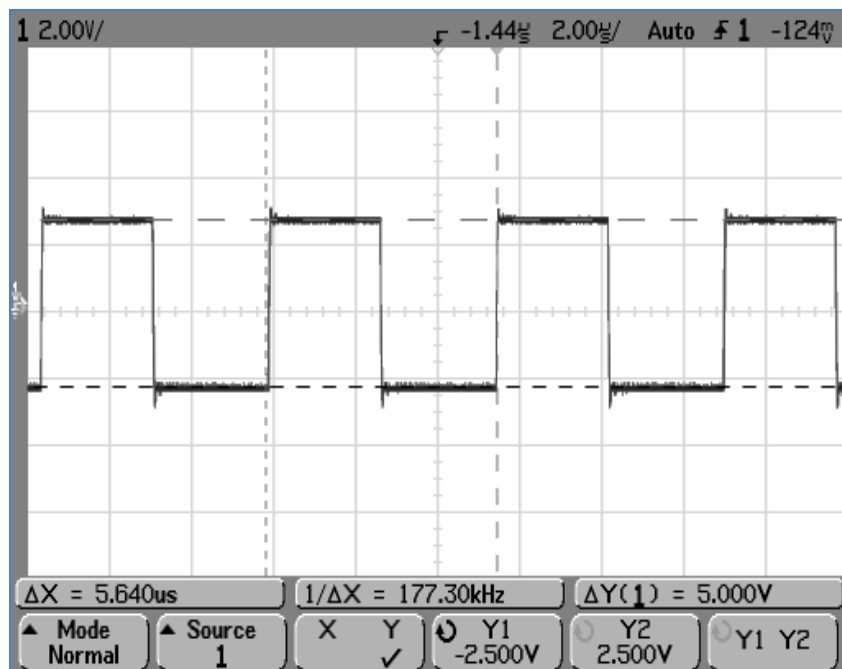
Fig. 7.9 Measured clock signal in one sample

Fig. 7.10(a) and (b) shows the measured clock frequency against temperature and supply variation, respectively. With 5 samples, the clock signal shows a mean variation of 0.23% for the supply ranging from ±1.6 V to ±2.5 V whereas a mean T.C. of around 0.018%/°C for the clock frequency ranging from -40 to 90 °C. The jitter performance of the oscillator circuit is also tested through employing the infinite persistence display mode of the oscilloscope. The test result shows the peak-to-peak jitter variation is around +/-5ns, which is around 1.34ns when converted to RMS jitter variation.
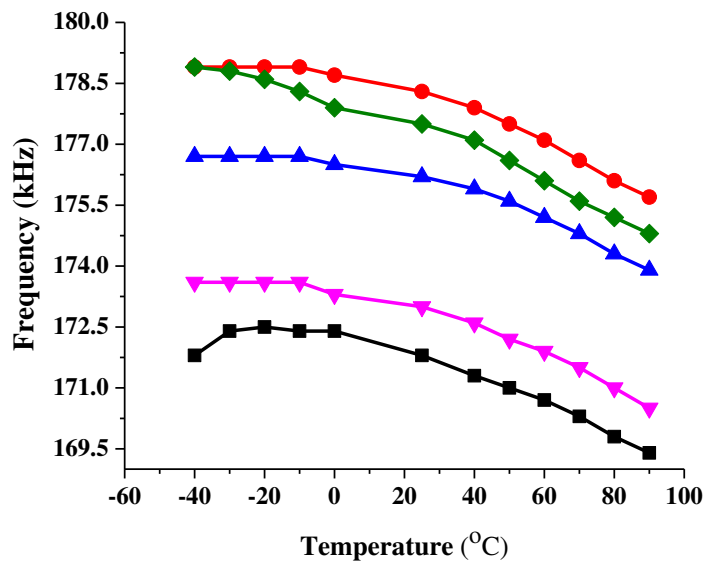
(a) Frequency variation with temperature
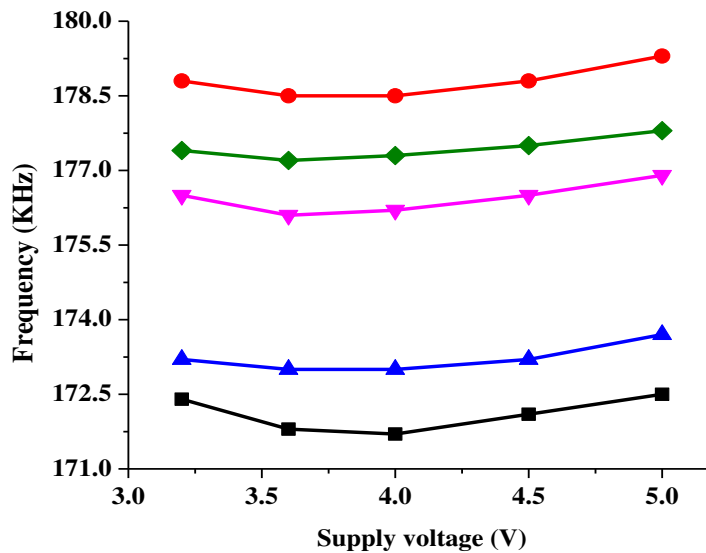
(b) Frequency variation with supply voltage

Fig. 7.10 Measured 5 samples' clock frequency against (a) temperature variation and (b) supply variation

Table 7.4 shows the performance summary and comparison with other reported works. As compared with the simulation results presented in 5.3.4, the testing result of the frequency stability is worse by 0.3~0.4 % due to the process variation during fabrication as well as the environment noise which is not

counted in the simulation result. In comparison to the works using internal RC components, the Vdd-tracking temperature compensated relaxation oscillator shows the best immunity to supply variation and a comparable temperature variation while consuming the least power consumption.

Table 7.4 Performance comparison of the proposed relaxation oscillator with reported works

Parameter	[90] 2002	[91] 2008	[92] 2004	[93] 2009	[94] 2009	[95] 2010	[96] 2012	[97] 2012	This work
Process [nm]	350	350	500	130	65	180	60	180	350
R, C Component	Ext.	Ext.	Int.	Ext.	Int.	Int.	Int.	Int.	Int.
Frequency [MHz]	5	4.87	11.6	3.2	0.1	14	0.032	6.7kHz	0.174
Total Current [μA]	20	70	133	25.6	34	25	2.8	0.63	4.2
Supply Voltage [V]	1	1.5	3	1.5	1.2	1.8	1.6	1.5	$\pm$2.5
Freq. Var. with Vdd [%/V]	6.33	0.16	0.64	4	1.53	1.6	0.2	0.98	0.21
Freq. Var. with Temp. [%]	$\pm$0.7 @ -20 to 60°C	$\pm$0.08 @ -20 to 60°C	$\pm$2.5 @ -40 to 125°C	$\pm$0.25 @ 20 to 60°C	$\pm$1.1 @ -20 to 80°C	$\pm$0.75 @ -40 to 125°C	$\pm$0.1 @ -20 to 100°C	-0.62 ~0.29 @ -40 to 100°C	$\pm$0.7 @ -40 to 60/°C $\pm$1.1 @ -40 to 90/°C

CHAPTER 8

CONCLUSIONS AND FUTURE WORKS

8.1 Conclusions

This thesis presents a low-noise low-power SC readout system interfacing with a bulk micromachined capacitive accelerometer sensing device with μg resolution. The MEMS process technology, the sensing principles and behavioral modeling for the capacitive micromechanical sensing device are described. A high capacitive sensitivity is achieved using the out-of-plane sensing scheme in conjunction with the large proof mass. Since this device offers sub-microgravity mechanical noise level, it turns out that the low-noise design of readout IC becomes one of the key objectives because it dictates the overall system noise performance.

A review of the strength and weakness in two common capacitive sensing methods, which are continuous-time chopper stabilization (CHS) scheme and discrete-time switched-capacitor (SC) sensing scheme, is presented. Three representative prior-art SC readout circuits are investigated in details. Their respective circuit operation principle and non-ideal circuit analysis are also presented for comparative study.

For interfacing with a bulk micro-machined MEMS sensing device with large sensing and parasitic capacitances, an open-loop switched-capacitor (SC) charge sensing architecture is preferred. The rational to the choice of SC technique is given, leading to the proposal of an Auto-Zero Time-multiplexed Capacitance-to-Voltage Converter (AZTMD-CVC). As such, the op-amp

circuit architecture/design can be made simple whilst the circuit imperfections such as offset and 1/f noise are effectively suppressed. The same goes for the reduction of switch errors. The comparative simulations are conducted to study the relative performance of each readout circuit. It has shown that the proposed circuit exhibits high thermal stability, low output glitches, low power consumption and good S/N dynamic range.

In order to circumvent the additional noise gain factor induced by the large parasitic capacitances, the low-noise OTA design, the SC thermal noise analysis and the low-noise low-power optimization strategy are addressed for the front-end interface. Optimal tradeoff for noise-power efficiency is thus achieved, meeting another objective for the design of low-power μg accelerometer system.

Integrated with the front-end readout circuit is that of the house-keeping circuits. They serve to provide all the control clocks for the SC charge sensing operation and the signal-conditioning function. Consequently, the quasi-analog output from the SC gain stage is smoothed whereas the bandwidth of the accelerometer IC is defined.

For house-keeping circuits, two new oscillators dedicated to sensor applications are proposed. The first oscillator is a low-frequency CMOS ring oscillator utilizing a simple temperature-compensated source follower driving structure. The second oscillator is a V_{DD}–tracking temperature-compensated current comparator based relaxation oscillator. Both the oscillator schemes offer stable clock signals with good immunity against temperature supply variations. Due to the relative headroom issue and process sensitivity, the second design is adopted in silicon realization. Digital control logic blocks are built for multi-phase clock generator. It generates the required control clocks for all the SC gain stages.

For mixed-signal system with particular emphasis on low-noise performance metric, IC layout becomes crucial in the realistic system performance. Several low-noise layout techniques are then described. Besides, particular attention is paid for plane grounding, IC and power supplies decoupling. The assignment of PCB layers are also addressed for PCB layout design.

The performance of accelerometer IC is compared with other reported state-of-art works. The measured results have shown that the proposed accelerometer IC achieves the best FOM in terms of output noise-power product. The outstanding figure has validated the effectiveness of time-multiplexed CVC architecture, low-noise OTA design and noise-power optimization method in this research work.

8.2 Future Works

Due to the time constraint, several important blocks are implemented in this project. It can be seen that the reference voltage used for charging/discharging the sensor capacitance has a significant influence on the overall system noise performance as well as the thermal stability. For further work, a low-noise low-power switched-capacitor voltage reference can be explored.

For the interface system, an external passive first-order low-pass filter is used to smooth the quasi-analog signal and define the system bandwidth. In future work, an on-chip solution for the low-pass function should be investigated, hence cutting two pins of the IC, leading to a compact integrated system.

In order to enable further digital signal processing after the analog readout, a data acquisition block can be integrated with the ASIC. It converts the analog

signal to digital data stream. The data acquisition block will involve the design of low-power high-resolution sigma-delta analog-to-digital converter

Furthermore, the system readout nonlinearity error is not of the major concern for the security application. However, both the small gap distances of the sensing capacitor as well as the single beam cantilever structure of the micro-accelerometer sensor device will considerably induce nonlinearity, especially under large external acceleration excitation condition. Besides, the non-perfect manufacturing of bulk micromachining sensor may also cause problems such as asymmetry, large and non-balance parasitic capacitances and nonlinearity effect. Circuit techniques must be deployed to tackle the stated problems. Although the non-balance parasitic capacitances can be easily compensated, the remaining parts of future works will be summarized as follows:

i.   To derive the equation between sensing capacitance and distance to get the nonlinearity part. This deals with the circuit theory for the compensation circuit design.

ii. To investigate the voltage gain controlled code used to control a pre-attenuation resistor network for linearization purpose.

iii. To design a MOS squaring circuit to generate the required compensation current. This compensation current is controlled by the gain-controlled resistor network.

iv. To research and design an improved low-offset summing amplifier to perform the summing function for the uncompensated signal and the compensation signal.

v.   To design on-chip output capacitor-less voltage regulator to provide the stable supply voltages and to generate low-noise reference voltages.

Fig. 8.1 depicts the possible building blocks for the linear sensor system that involves linearization technique in future. This involves physic-based study of accelerometer sensing device to derive the compensation theory. Extensive building blocks research and their circuit designs are explored.
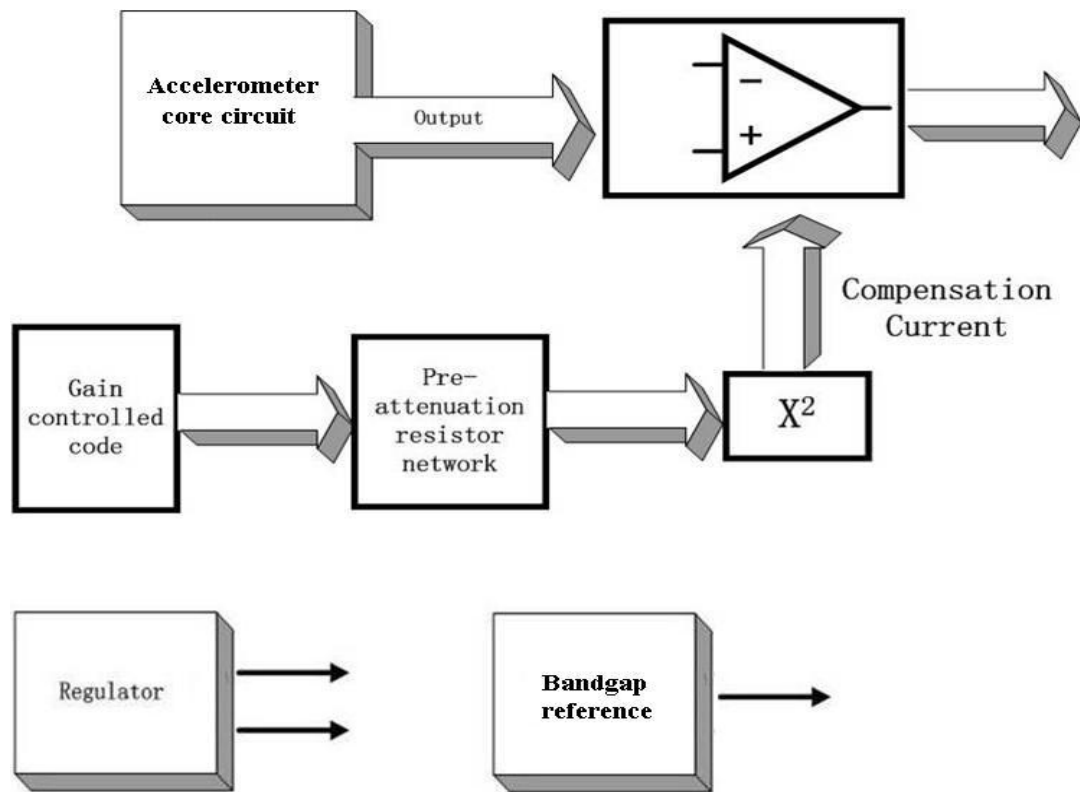
Fig. 8.1 Circuit blocks for future highly-linear accelerometer IC with wide g range

LIST OF PUBLICATIONS

1. P.K. Chan, Y.M. Wang and K.H. Li, "Circuit Arrangement And Method Of Operating The Same," PCT, Nanyang Technological University, NTUitive, Ref: PAT/225/12/14/PCT, 14 October, 2014.

2. Y. M. Wang, P. K. Chan and K. H. Li, "A compact CMOS ring oscillator with temperature and supply compensation for sensor applications," *IEEE, Computer Society Annual Symposium on VLSI*, Tampa, Florida, July, 2014.

3. Y. M. Wang, P. K. Chan, K. H. Li and Soon-Eng Ong, "A 240-µA 1.16-µg/ √Hz Capacitive Accelerometer IC using Auto-Zero Time-Multiplexed Differential Technique," submitted to IEEE Sensors Journal for review.

REFERENCES

[1] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," *Proc. IEEE*, vol.86, pp. 1640-1659, Aug. 1998.

[2] T. Smith, O. Nys, M. Chevroulet, Y. DeCoulon, M. Degrauwe, "A 15 b electromechanical sigma-delta converter for acceleration measurements," in *IEEE ISSCC, Digest of Technical Papers,* San Francisco, CA, pp. 160-161, Feb. 1994.

[3] H. Kulah, J. Chae, N. Yazdi, K. Najafi, "A multi-step electromechanical $\Delta\Sigma$ converter for micro-g capacitive accelerometers," in *IEEE ISSCC,* San Francisco, CA, Feb. 2003, pp. 202-203.

[4] J. Chae, H. Kulah, K. Najafi, "An in-plane high-sensitivity, low-noise micro-g silicon accelerometer with CMOS readout circuitry," *IEEE Journal of Microelectromechanical Systems*, vol. 13, no. 4, pp. 628-635, Aug. 2004.

[5] B. E. loser, R. T. Howe, "Surface micromachined accelerometers," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 366-375, Mar. 1996.

[6] X. Jiang, F. Wang, M. Kraft, and B. E. Boser, "An integrated surface micromachined capacitive lateral accelerometer with 2µg/√Hz resolution," in *Solid-State Sensor, Actuator and Microsystems Workshop*, Hilton Head Island, SC, 2002, pp. 202-205.

[7] A. A. Seshia, M. Palaniapan, T. A. Roessig, R. T. Howe, R. W. Gooch, T. R. Schimert, and S. Montague, "A vacuum packaged surface micromachined resonant accelerometer," *IEEE Journal of Microelectromechanical Systems*, vol. 11, no. 6, pp. 784-793, Dec. 2002.

[8] J. Bernstein, R. Miller, W. Kelley, and P. Ward, "Low-noise MEMS vibration sensor for geophysical applications," *IEEE Journal of Microelectromechanical Systems*, vol. 8, no. 4, pp. 433-438, Dec. 1999.

[9] M. Lemkin, B. E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 456-468, Apr. 1999.

[10] B. R. Schiffer, A. Burstein, and W. J. Kaiser, "An active charge cancellation system for switched-capacitor sensor interface circuits," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2134-2138, Dec. 1998.

[11] R. Wu, J. H. Huijsing, and Kofi A. A. Makinwa, "Precision instrumentation amplifiers and read-out integrated circuits," New York: Springer, 2012, pp. 28-37.

[12] A. Bakker, K. Thiele, J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp.1877-1883, Dec. 2000.

[13] Wolfgang Kuehnel and Steven Sherman, "A surface micromachined silicon accelerometer with on-chip detection circuitry", *Sensor and Actuators*, A45, pp.7-16, 1994.

[14] C. Menolfi, Q. T. Huang, "A fully integrated, untrimmed CMOS instrumentation amplifier with submicrovolt offset," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 415-420, Mar. 1999.

[15] A. Bilotti, G. Monreal, "Chopper-stabilized amplifiers with a track-and-hold signal demodulator," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 46, no. 4, pp. 490-495, Apr. 1999.

[16] H. Luo, G. Zhang, L. R. Carley, and G. K. Fedder, "A post-CMOS micromachined lateral accelerometer," *IEEE Journal of Microelectromechanical Systems*, vol. 11, no. 3, pp. 188-195, Jun. 2002.

[17] K. E. Petersen, "Silicon as a mechanical material," *Proceedings of the IEEE*, vol.70, no.5, pp.420-457, May 1982.

[18] P. J. French, "Development of surface micromachining techniques compatible with on-chip electronics," *J. Micromech. Microeng.* pp. 197–211, 1996.

[19] P. J. French and P. M. Sarroz, "Surface versus bulk micromachining: the contest for suitable applications," *J. Micromech. Microeng.* pp. 45–53, 1998.

[20] C. Wang, C. Ming, and G. E. Uhlenbeck, "On the theory of the Brownian Motion II," *Rev. Modern Phys.*, vol. 17, pp. 323–342, April–July 1945.

[21] B. Kloeck, S. D. Collins, N.-F. Rooij, R. L. Smith, "Study of electrochemical etch-stop for high-precision thickness control of silicon membranes," *IEEE Transactions on Electron Devices*, vol.36, no.4, pp.663-669, Apr. 1989.

[22] L. j. Ristic, R. Gutteridge, B. Dunn, D. Mietus, P. Bennett, "Surface micromachined polysilicon accelerometer," *IEEE Solid-State Sensor and Actuator Workshop*, *Jun. 22-25*, *1992*, *5th Technical Digest*, pp.118-121.

[23] M. Paavola, "Integrated reference circuits for low-power capacitive sensor interfaces," *PhD thesis*, Aalto University.

[24] V. Agarwal, T. K. Bhattacharayya and S. Banik, "Design steps for bulk micro machined single axis silicon capacitive accelerometer with optimized device dimensions," *Journal of Physics: Conference Series 34, International MEMS Conference,* 2006.

[25] B. V. Amini, S. Pourkamali, M. Zaman and F. Ayazi, "A new input switching scheme for a capacitive micro-g accelerometer," *IEEE Symposium On VLSI Circuits Digest of Technical Papers* 2004.

[26] W. F. Lee, P. K. Chan, L. Siek, "Electrical Modeling of MEMS Sensor for Integrated Accelerometer Applications," *Proceedings 1999 IEEE Hong Kong Electron Devices Meeting*, Jun.1999, pp.88-91.

[27] R. P. van Kampen, R. F. Wolffenbuttel, "Modeling the mechanical behavior of bulk-micromachined silicon accelerometers," *Sensor and Actuators,* A64, pp.137-150, 1998.

[28] D. F. Patrick and I. Miller, "Analog behavioral modeling with the Verilog-A language," Kluwer Academic Publishers, 2003.

[29] K. Kundert, "Modeling varactors," *The Designer's Guide Community.* Designer's Guide Consulting, Inc.

[30] T. Veijola (Helsinki UT, Finland), "Equivalent Circuit Models for Micromachined Inertial Sensors," *PhD Thesis*, 1999.

[31] C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier", *IEEE J. of Solid-state circuits*, vol. sc-22, no. 3, Jun. 1987.

[32] K. Kondo and K. Watanabe, "A Switched-Capacitor Interface for Capacitive Sensors with Wide Dynamic Range," *IEEE Transitions on Instrumentation and Measurement,* vol. 38, no. 3. Jun. 1989.

[33] C. C. Enz and G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE,* vol. 84. no. 11, Nov. 1996.

[34] T. C. C. Kevin, D. Han, P. S. Ravinder, D. P. Duy, Y. P. Chin, W. L. Jian, D. Nuttman, J. Minkyu, "118-dB dynamic range, continuous-time, opened-loop capactance to voltage converter readout for capacitive MEMS accelerometer," *IEEE Asian Solid State Circuits Conference* (*A-SSCC*) Nov. 8-10 2010, pp.1-4.

[35] M. H. White, et al. "Characterization of Surface Channel CCD Image Arrays at Low Light Levels," *IEEE J. Solid-State Circuits*, vol.9, no.1, pp.1-3, Feb. 1974.

[36] C. Eichenberger, W. Guggenbuhl, "On charge injection in analog MOS switches and dummy switch compensation techniques," *IEEE Transactions on Circuits and Systems*, vol.37, no.2, pp.256-264, Feb. 1990.

[37] J.-H. Shieh, M. Patil, B. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol.22, no.2, pp.277-281, Apr. 1987.

[38] A. Danchiv, M. Bodea, A-M. Luca, I-A, Tranca, "Charge injection induced sample and hold error analysis," *International Semiconductor Conference, CAS 2009*, vol.2, pp.491-494, Oct. 12-14 2009.

[39] L. Zimmermann, J. P. Ebersohl, F. Le Hung, J. P. Berry, F. Baillieu, P. Rey, B. Diem, S. Renard, and P. Caillat, "Airbag application: A microsystem including a silicon capacitive accelerometer, CMOS switched capacitor electronics and true self-test capability," *Sens. Actuators A, Phys.,* vol. 46/47, no. 1, pp. 190–195, Jan. 1995.

[40] S. Xia and S. Nihtianov, "Power-efficient high-speed and high-resolution capacitive-sensor interface for subnanometer displacement measurements," *IEEE Transactions on Instrumentation and Measurement*, vol. 61, no. 5, pp. 1315-1322, May 2012.

[41] Oliver Nehrig, Kirchdorf(DE); Rudiger Ganz, Freising(DE), U. S. Patent No. US 7, 663, 379 B2, Feb.16, 2010.

[42] M. A. Lemkin, B. E. Boser, D. Auslander and J. H. Smith, "A 3-axis Force Balanced Accelerometer Using a Single Proof-Mass", 1997 Int'l Conf. On Solid-State Sensors and Actuators, pp.1185-1188, Jun. 1997.

[43] B. R. Schiffer, A. Burstein, and W. J. Kaiser, "An Active Charge Cancellation System for Switched-Capacitor Sensor Interface Circuits," *IEEE J. Solid-State Circuits,* vol. 33, no. 12, Dec. 1998.

[44] M. A. Lemkin, and B. E. Boser, "A Third-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics", IEEE J. of Solid-State Circuits, vol.34, no.4, pp.456-468, 1999.

[45] W. F. Lee and P. K. Chan, "A capacitive-based accelerometer IC using injection-nulling switch technique," *IEEE Trans. on Circuits and Systems, Part I*, vol. 55, no. 4, pp. 980-989, May 2008.

[46] K. Martin, L. Ozcolak, Y. S. Lee, and G. C. Temes, "A Differential Switched-Capacitor Amplifier," *IEEE J. Solid-State Circuits,* vol. SC-22, no. 1, Feb. 1987.

[47] X. L. Zhang, P. K. Chan, "An untrimmed CMOS amplifier with high CMRR and low offset for sensor applications," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS),* 2008, pp. 802-805.

[48] B. V. Amini, S. Pourkamali, and F. Ayazi, "A high resolution, stictionless, CMOS compatible SOI accelerometer with a low noise, low power, 0.25um CMOS interface," *IEEE MEMS* 2004.

[49] L. Forbes, H. Gopalakrishnan, W. Wanalertlak, "Simulation and analysis of noise in switched capacitor amplifier circuits," *Microelectronics and Electron Devices, 2005. WMED '05. 2005 IEEE Workshop on* , vol., no., pp.55,58, 15-15 Apr. 2005

[50] Gobet, Cl.-A; Knob, A, "Noise generated in switched capacitor networks," *Electronics Letters* , vol.16, no.19, pp.734,735, Sep. 11 1980

[51] O. Oliaei, "Noise analysis of correlated double sampling SC-integrators," *IEEE International Symposium on Circuits and Systems, ISCAS 2002*, pp.IV-445,IV-448 vol.4

[52] C.-A. Gobet, A. Knob, , "Noise analysis of switched capacitor networks," *IEEE Transactions on Circuits and Systems,* vol. 30, no. 1, pp.37-43, Jan. 1983.

[53] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits,* vol. 38, no. 6, pp. 958-965, Jun. 2003.

[54] J. F. Wu, G. K. Fedder, and L. R. Carley, "A low-noise low-offset capacitive sensing amplifier for a 50-μg/$\sqrt{Hz}$ monolithic CMOS MEMS accelerometer," *IEEE J. Solid-State Circuits,* vol. 39, no. 5, pp. 722-730, May 2004.

[55] Y. P. Tsividis, Operation and modeling of the MOS transistor. New York: McGraw-Hill, 1999.

[56] P. R. Grey and R. G. Meyer "MOS operational Amplifier Design -- A Tutorial Overview," *IEEE J. Solid-State Circuits*, vol.17, no.6, pp.969-982, Dec.1982.

[57] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "Improved Reversed Nested Miller Frequency Compensation Technique with Voltage Buffer and Resistor," *IEEE Transactions on Circuits and Systems*-II: Express Briefs, vol. 54, no. 5, May 2007.

[58] J. Nebhen, S. Meillere, M. Masmoudi, J.Seguin, H. Barthelemy amd K. Aguir, "A temperature compensated CMOS ring oscillator for wireless sensing applications," *IEEE New Circuits and Systems Conference (*NEWCAS)*, Montreal, QC, pp. 37-40, Jun. 2012.

[59] J. L. Merino, S. A. Bota, R. Casanova, A. Diéguez, C. Cané, and J. Samitier, "A reusable smart interface for gas sensor resistance

measurement," *IEEE Transactions On Instrumentation and Measurement,* vol. 53, no. 4, pp. 1173-1178, Aug. 2004.

[60] Y. S. Shyu, J. C. Wu, "A process and temperature compensated ring oscillator," *The First IEEE Asia Pacific Conf. on ASICs, 1999. AP-ASIC '99,*, pp. 283-286, Aug.1999.

[61] W. F. Lee and P. K. Chan, "A low-cost programmable clock generator for switched-capacitor circuit applications," *Analog Integrated Circuit Signal Process,* vol. 47, pp. 247-257, Apr. 2006.

[62] K. N. Leung, C. H. Lo, P. K. T. Mok, Y. Y. Mai, W. Y. Leung and M. J. Chan, "Temperature-compensated CMOS ring oscillator for power-management circuits," *Electronics Letters,* vol. 43, no. 15, pp. 786–787, Jul. 2007.

[63] J. G. Tang, F. Tang, "Temperature and process independent ring-oscillator using compact compensation technic," *IEEE Conf. on Anti-Counterfeiting Security and Identification in Communication (ICASID),* pp. 49-52, Jul. 2010.

[64] Y. Tsugita, K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "An On-Chip PVT Compensation Technique with Current Monitoring Circuit for Low-Voltage CMOS Digital LSIs," *IEICE Trans. Electron.*, vol. E93-C, no. 6, Jun. 2010.

[65] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Trans. on Ciruits and System, Part I, Fundam. Theory Appl.*, vol. 48, no.7, pp. 876–884, Jul. 2001.

[66] K. Sandaresan, et al., "Process and Temperature Compensation in a 7 MHz CMOS Clock Oscillator", *IEEE J. Solid-State Circuits,* vol. 41, pp.433-441. Feb. 2006.

[67] L. H. C. Ferreira and T. C. Pimenta, "A CMOS voltage reference for ultra low-voltage applications," *IEEE Conf. on Electronics, Circuits and Systems (ICECS),* pp. 1-4, Dec. 2005.

[68] I. Nissene, J. Kostamovaara,   "A low voltage CMOS constant current-voltage reference circuit," *IEEE International Symposium on Circuits and Systems (ISCAS),* vol.1, pp. 381-384, May 2004.

[69] M. Brownlee, P. K. Hanumolu, Un-Ku Moon and K. Mayarain, "The effect of power supply noise on ring oscillator phase noise," *IEEE New Circuits and Systems Conf. (NEWCAS),* pp. 225-228, Jun. 2004.

[70] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuit,* vol. 34, no. 6, pp. 790-804, Jun. 1999.

[71] W. Steinhagen and W. L. Engl, "Design of integrated analog CMOS circuits-a multichannel telemetry transmitter," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 799-805, Dec. 1978.

[72] T. J. Yamaguchi and M. Ishida, "Timing Jitter Measurement of Intrinsic Random Jitter and Sinusoidal Jitter Using Frequency Division," *Journal of Electronic Testing*: Theory and Applications 19, pp. 183-193, 2003.

[73] A. Sai, T. Yamaji, and T. Itakura, "A Low-jitter Clock Generator based on Ring Oscillator with 1/f Noise Reduction Technique for Next-Generation Mobile Wireless Terminals," *IEEE Asian Solid-State Circuits Conference*, Nov., 2008.

[74] A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 8, Aug, 2006.

[75] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and Phase Noise in Ring Oscillators," *IEEE J. Solid-State Circuits,* vol. 34, no. 6, Jun. 1999.

[76] J. Ramirez-Angelo, R. G. Carvajal, J. A. Galan, A. Lopez-Martin, " A free but efficient low-voltage class-AB two-stage operational amplifier," *IEEE Trans. on Circuits and Systems., Part I*, vol. 53, no. 7, pp. 568-571, Jul. 2006.

[77] *Jitter Measurement Using SpectreRF.* Application Note. Cadence Design Systems, Inc.

[78] S. M. Kang and Y. Leblebigi, *CMOS Digital Integrated Circuits: Analysis and Design*, 2nd edition, McGraw-Hill, Singapore, 1999.

[79] J.Lee and S. Cho, "A 10MHz 80µW 67 ppm/°C CMOS Reference Clock Oscillator with a Temperature Compensated Feedback Loop in 0.18µm CMOS", *Symposium on VLSI Circuits Digest of Technical Papers*, 2009.

[80] K. Choe, O. D. Bernal, D. Nuttman, and M. Je, "A precision relaxation oscillator with a self-clocked offset-cancellation scheme for implantable biomedical SoCs," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 402–403.

[81] R. Woudsma and J. M. Noteboom, "The modular design of clock-generator circuits in a CMOS building-block system," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 770-774, Jun. 1985.

[82] D. A. Johns and K. Martin, "Analog integrated circuit design", *John Wiley & Sons,* 1997.

[83] R. J. Baker, *CMOS: circuit design, layout, and simulation*, 2nd ed.: Wiley-IEEE Press, 2005, pp. 829-834.

[84] "Analog layout and grounding techniques," Lattice Semiconductor Corporation.

[85] B. V. Amini, R. Abdolvand, and F. Ayazi, "A 4.5mW closed-loop ΔΣ micro-g CMOS SOI accelerometer," *IEEE, JSSC*, vol. 41, no.12, Dec. 2006.

[86] H. Kulah, J. Chae, N. Yazdi, K. Najafi, "Noise analysis and characterization of a sigma-delta capacitive microaccelerometer," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 352-361, Feb. 2006.

[87] D. N. Zhao, M. F. Zaman, and F. Ayazi, "A chopper-stabilized lateral-BJT-input Interface in 0.6um CMOS for capacitive accelerometers," in *IEEE ISSCC* 2008, session32, MEMS&Sensors 32.5.

[88] M. Yucetas, J. Salomaa, A. Kalanti, L. Aaltonen, and K. Halonen, "A Closed-Loop SC Interface for a ±1.4g Accelerometer with 0.33% Nonlinearity and 2μg/√Hz Input Noise Density," in *IEEE ISSCC 2010. Session 17. Sensors & MEMS. 17.7*. Feb. 2010.

[89] P. Lajevardi, V. P. Petkov, B. Murmann, "A ΔΣ interface for MEMS accelerometers using electrostatic spring constant modulation for cancellation of bondwire capacitance drift," *IEEE J. Solid-State Circuits*, vol.48, no.1, pp. 265-275, Jan. 2013.

[90] K. Lasanen, "A 1-V, Self-adjusting, 5MHz CMOS RC-oscillator," *Proc. ISCAS*, pp. 377-380, May 2002.

[91] K. Lasanen and J. Kostamovaara, "A 1.2-V CMOS RC oscillator for capacitive and resistive sensor applications," *IEEE Transactions on Instrumentation and Measurement,* vol. 57, no. 52, Dec. 2008.

[92] A. V. Boas and A. Olmos, "A temperature compensated digitally trimmable on-chip IC oscillator with low voltage inhibit capability," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, Sep. 2004, vol.1, pp. 501–504.

[93] K. Choe, O. D. Bernal, D. Nuttman, and M. Je, "A precision relaxation oscillator with a self-clocked offset-cancellation scheme for implantable

biomedical SoCs," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 402–403.

[94] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, and B. Nauta, "A low-voltage mobility-based frequency reference for crystal-less ULP radios," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 2002–2009, Jul. 2009.

[95] Y. Tokunaga et al., "An on-chip CMOS relaxation oscillator with voltage averaging feedback," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1150-1158, 2010.

[96] K.-J. Hsiao, "A 32.4 ppm/°C 3.2-1.6V self-chopped relaxation oscillator with adaptive supply generation," in *VLSI Circuits Symp. Dig. Tech.Papers*. Jun., 2012, pp. 14-15.

[97] K. Tsubaki, T. Hirose, Y. Osaki, S. Shiga, N. Kuroki, and M. Numa, "A 6.66-kHz, 940-nW, 56ppm/°C, Fully On-chip PVT Variation Tolerant CMOS Relaxation Oscillator," *IEEE International Conference on Electronics, Circuits and Systems,* pp.97-100, 2012.