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A low-power ASK demodulator for inductively coupled implantable electronics

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Abstract

An amplitude shift keying (ASK) demodulator is presented which is suitable for implantable electronic devices that are powered through an inductive link. The demodulator has been tested with carrier frequencies in the range 1–15 MHz, covering most commonly used frequencies. Data rates up to several 100kbit/s are supported, suitable for complex implants such as stimulating electrode arrays or visual implants. The circuit is compatible with modulation depths in the range 10–100%. The low end of the range permits data transmission without significant reduction in power transfer, or the use of transmitter designs with limited modulation capability. The power consumption is 60 μW from a 3 V supply. The circuit has been implemented in a standard CMOS process.

1. Introduction

Inductively coupled links are widely used nowadays in conjunction with high-performance implantable devices, to provide wireless power and data transmission to the implant. The link consists of two resonant RLC circuits, with the external primary circuit driven by a power amplifier, and the implanted secondary circuit acting as an antenna. Several different circuit topologies are possible [1] but it will be assumed here without loss of generality that the secondary circuit is parallel resonant. The power amplifier is usually a switching type such as a class D or E with an amplitude modulated output [2]. Efficient transmitter design and power transfer requirements can limit the AM modulation depth to 10–20%.

One of the special requirements of implantable systems is that maximum power transfer may be desired during periods when the data link is idle, as for example between stimulation commands in a stimulator system. Modulation of the carrier during idle periods is unwanted in such cases, and the idle periods can therefore not be used to establish the modulation levels in the detector.

The operating conditions for implantable electronics are in many respects similar to those experienced by contactless smart card ICs. The main difference is the available power in the transmitter. An ASK method based on sensing the current passed through an on-chip shunt regulator is presented in [3], but in a portable battery-operating system, the ideal situation is when little or no current is wasted in a shunt regulator. Ideally, the supply voltage of the implant is regulated by varying the transmitted power instead. This can be done by monitoring the supply voltage through a bidirectional data link, and regulating the transmitted power accordingly.

The weak coupling commonly found between the primary and secondary coils means that the power transfer is very inefficient. Any reduction in the power consumption of an implant can therefore significantly affect the power economy of the system as a whole, and in the case of battery-operated external transmitters, increase battery life.

One of the basic parts found in all digitally controlled implants is the demodulator, and this paper presents a versatile ASK demodulator, which features a low power consumption without limiting the bit rate or setting unreasonable constraints on the modulation form.

2. System overview

Figure 1 shows a block diagram of the demodulator. The input signal and power are received through an antenna consisting of a tuned parallel LC resonator. The power for the implant is extracted by a bridge rectifier and accumulated in a storage capacitor (not shown). Depending on the technology, the rectifier may be on-chip or external. The RF signal is taken from one side of the antenna and fed through a passive input network to a current-mode squarer. The squarer has a differential output which is connected to a differential low-pass filter, and an extracted carrier output which can be used as a system clock. The output of the LPF is connected to a level detector which extracts the digital modulation data from the envelope information.

2.1. Input network

The amplitude of the antenna signal can be far greater than that which can be handled by modern CMOS technologies. The signal can therefore not be connected directly to a transistor gate or diffusion, but must be conditioned in some way. Input protection diodes are not used since they would interfere with the operation of the bridge rectifier. In some cases it is desirable to maintain a supply voltage external to the chip which is higher than the on-chip supply. In that case, a voltage regulator is inserted into the supply path to the chip in figure 1, so the bridge rectifier does not provide sufficient input protection.

The passive input network consists of a capacitive divider and a resistor R_1 in series with the input resistance R_i of the squarer. This network has two purposes. One is

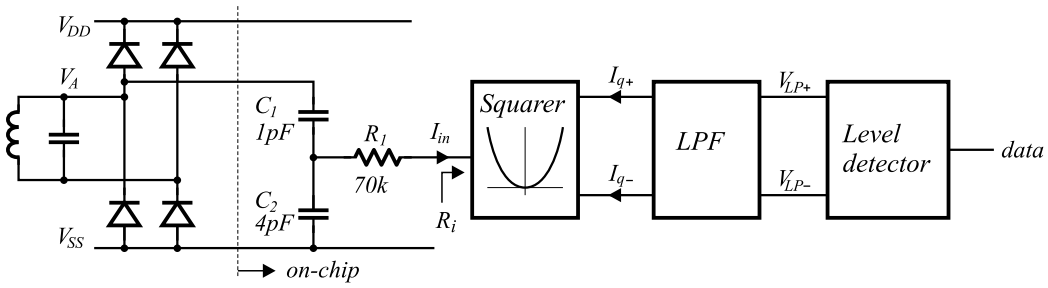

Figure 1. A block diagram of the demodulator circuit.

to convert the input voltage V_A to an input current of suitable amplitude for the squarer, and the other is to reduce the signal voltage seen by the active devices in the circuit. The capacitors are implemented using metal layers, so they can withstand quite high voltages. The capacitors are stacked on top of each other so that the chip substrate is shielded from input signal by the bottom plate of C_2.

Along with the source resistance R_S of the inductive link, the network has a second-order bandpass transfer function. Assuming that the corner frequencies are well separated (a decade or more), the transfer function in the middle of the band is approximately $I_{in}/V_A = C_1/((C_1 + C_2)(R_1 + R_i))$. The lower and upper corner frequencies are $1/\omega_l = (R_1 + R_i)(C_1 + C_2)$ and $1/\omega_u = R_S C_1$ respectively. These must be fitted to the used carrier frequency range.

2.2. Squarer

The current squarer is shown in figure 2. It is based on a four-quadrant class AB multiplier presented in [4], and uses the square-law characteristic of the MOS transistor in strong inversion. The output is given by $(I_{o+} - I_{o-}) = I_{in}^2/8I_b$ where I_b is the bias current of the input transistors.

One of the features which makes this circuit attractive for our purposes is that a relatively high small-signal bandwidth can be achieved with low power levels. Simulations show a bandwidth greater than 30 MHz with a total bias current of 5 µA. The supply current of the squarer is signal-dependent due to the class AB operation, and rises from 5 µA to 10 µA at the maximum specified signal amplitude.

One limitation of the circuit is that it relies on matching of P- and N-type devices to implement the quadratic transfer function. While this is impossible to achieve in practice, it does not matter in this application since the squarer is only used as an envelope detector. The mismatch of the current mirrors, which are implemented with high-swing cascodes, also affects the accuracy of the circuit, but to a much lesser extent.

The two current mirrors have secondary outputs which are connected together. The high-impedance node at these secondary outputs slews to the positive supply or to ground according to the sign of the input current, thus creating a clock signal corresponding to the carrier frequency. Many implantable electronic devices use the signal carrier as a timing reference and to clock sequential logic.

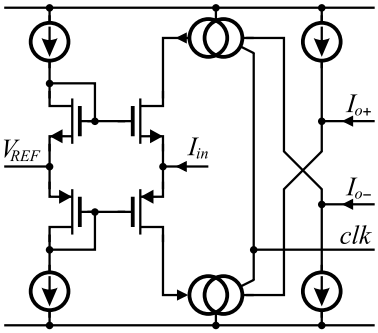

Figure 2. The current-mode squarer circuit. The bias current in each branch is 1 µA.

2.3. Low-pass filter

The low-pass filter is used to extract the envelope data from the squared input signal. It is a differential third-order filter, consisting of a passive first-order section and an active section which is implemented as a G_m–C filter. Figure 3 shows the filter.

The cutoff frequency of the filter is set with respect to the highest intended modulation frequency, taking process variations into account. In this case it was set to a nominal frequency of 350 kHz, to permit unencoded data rates of up to approximately 200kbit/s.

Figure 4 shows the transconductor used in the filter implementation, along with the common-mode feedback circuit which is necessary for each of the two internal differential nodes of the filter. The CMFB circuit is a current-

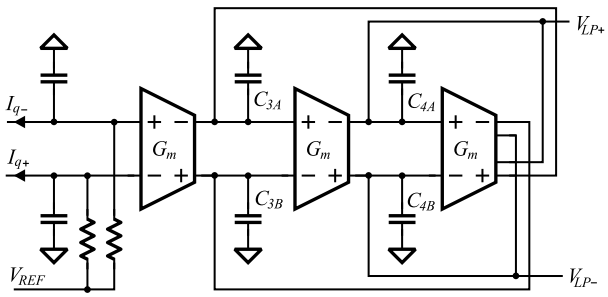

Figure 3. The differential LPF implementation.

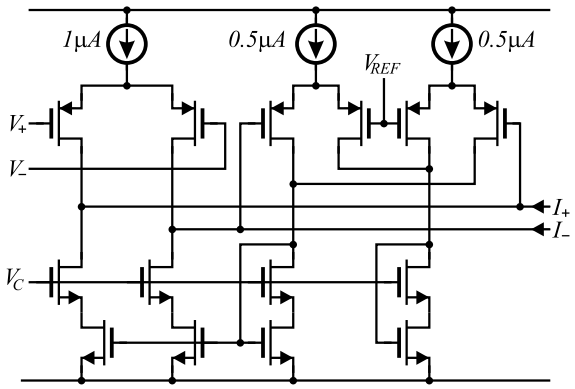

Figure 4. A single-output filter transconductor, with CMFB circuit.

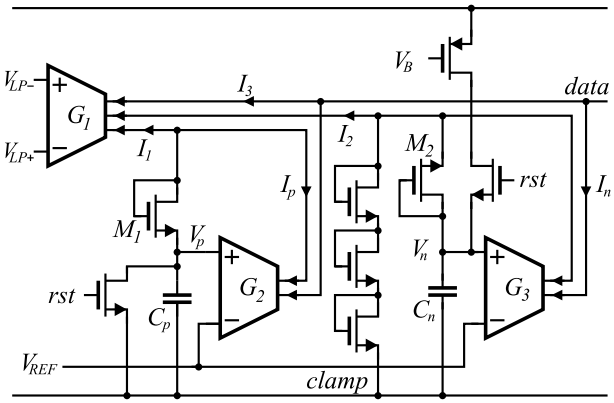

Figure 5. The peak detector and data signal extraction circuit.

steering type which causes relatively little distortion of the differential mode signal. The transconductor itself is based on a simple differential pair. The nonlinearity of the transconductor is of little importance at the applied signal level (up to 200 mV differential). The 3dB-frequency of the transconductors is approximately 10 MHz, which is sufficiently high not to affect the transfer function of the filter.

2.4. Level detector

The power requirements of the implant and considerations of the efficiency of the link generally require that the transmitter be operated at a constant level while the data link is idle. For much the same reason it is desirable to eliminate long synchronization/start sequences before each transmission. The ASK modulation levels are therefore not known by the demodulator *a priori*, and must be established quickly to detect the transmitted data. This eliminates the possibility of a LP filter with a long time constant to determine the average signal level. A method commonly used in sophisticated receivers, like the digital conversion and storage of the transmitted envelope with *a posteriori* processing, is not compatible with the power consumption criteria.

The level detector presented here uses only a pair of start bits for a simple baseband modulation scheme, or a single start bit in the case of biphase ("Manchester") encoding, to identify the two modulation levels and the threshold level.

A diagram of the detector is shown in figure 5. It uses three single-ended transconductors with multiple outputs. All three transconductors have the same transconductance G, except for the third output of G_1 which has twice the magnitude of the other outputs, $I_3 = 2I_2 = 2I_1$.

The positive peak voltage at the input is stored on C_p (referred to V_{REF}), while the negative peak is stored on C_n. In the following calculation of the transfer function from the input to the positive peak voltage V_p, the diode transistor M_1 can be ignored. The justification for this will be apparent from the results.

From the diagram, we have the small-signal currents $i_1 = G(v_{LP-} - v_{LP+}) := -Gv_d$ and $i_p = G(v_p - v_{REF}) = Gv_p$. The voltage on the capacitor is $v_p = -(i_1 + i_p)/sC_p$. Inserting the expression for the currents, and solving for the transfer function, we get

$$\frac{v_p}{v_d} = \frac{1}{1 + sC_p/G} \tag{1}$$

Two observations can be made at this point. In the first place, the DC value of this function is 1 (this result presumes perfect matching of the transconductances), so a true copy of the peak voltage is effectively stored on C_p. In the second place, this is a first-order LP function, so the voltage on the capacitor approaches the final value with no overshoot. This last fact is the justification for omitting the diode-connected transistor M_1 in the analysis. The result for the negative peak voltage is similar. The time constants C_p/G and C_n/G should be set in relation to the length of the start symbol, to allow the positive and negative peak voltages time to settle.

The digital *data* signal is extracted from the input signal by comparing it to the average of the two peak values. This is done by summing the currents $I_3 = -2GV_d$, $I_p = G(V_p - V_{REF})$ and $I_n = G(V_n - V_{REF})$ at the output node, and letting it slew to the positive supply or to ground according to the sign of the result.

The reset signal is used to initialize the values of the capacitors which store the positive and negative peak signal voltages. The positive peak voltage V_p is set to V_{SS} by the reset signal, while the negative peak voltage V_n is set to approximately four gate-source voltages. This last value is determined partly by a voltage clamp consisting of three diode-connected transistors. The purpose of the clamp is to limit the voltage swing on the summing node for the negative peak computation. This reduces the amplitude of the capacitive feed-through to C_n through the diode. No clamp is necessary for the positive peak since the available voltage range at the summing node is more limited. The negative peak reset transistor is not connected to V_{DD}, but to a current source, in order to limit the current through M_2 and the clamp during reset.

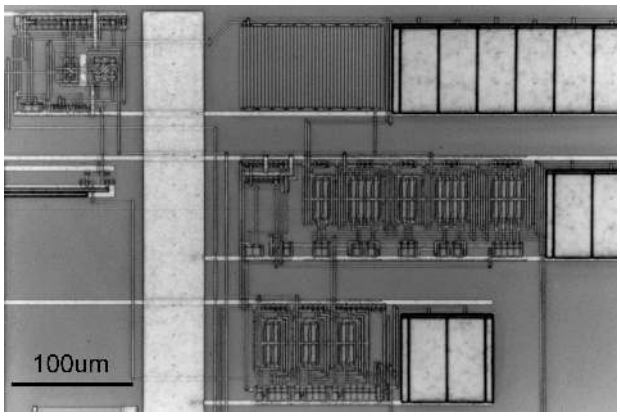

Figure 6. A photo of the demodulator core.

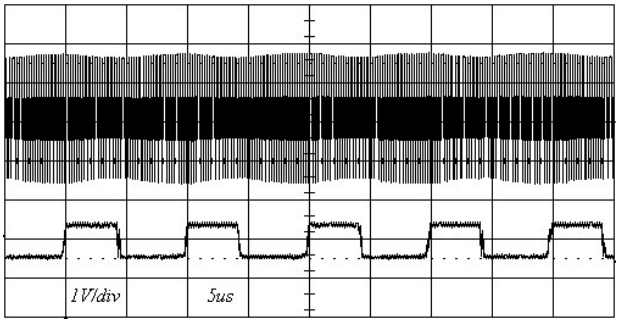

Figure 7. Measurement results for a 10 MHz carrier modulated 10% with a 0101... bit stream at 200kbit/s. The upper trace is the RF signal and the lower trace is the extracted data.

3. Experimental results

The demodulator was implemented in a standard digital 0.5 µm CMOS process, with one poly and three metal layers. The maximum supply voltage is 3.3 V.

All measurement results were obtained with a supply voltage of 3 V. In order to test the circuit with a wide range of carrier frequencies, modulation parameters and signal levels, a signal generator was used for most measurements. The functionality of the circuit was however verified with transmission through an inductive link with a carrier frequency of 5 MHz at 200kbit/s.

Due to the nature of the dual power/data link, the peak-to-peak amplitude of the unmodulated signal is almost constant, and equal to the supply voltage plus two diode voltage drops. In the following test results, the unmodulated signal level is fixed at $3.5\,V_{p\text{-}p}$.

3.1. Carrier extraction

The sensitivity of the carrier extraction mechanism is limited by the parasitic capacitance on the *clk* signal output node in the squarer (figure 2). The necessary signal level for detection rises as the frequency increases, since the current into the output node is proportional to the signal. An output buffer was connected to the *clk* signal, to drive the signal off-chip for testing purposes. Due to a layout error, the parasitic capacitance on this node is higher than necessary, and the sensitivity of the carrier extraction does therefore fall off faster with frequency than expected.

The measurements show that the detection threshold is approximately $0.4\,V_{p\text{-}p}$ up to 5 MHz, and rises to $3.6\,V_{p\text{-}p}$ at 12 MHz. Simulations of the circuit without the added parasitic capacitance show a threshold of $0.8\,V_{p\text{-}p}$ at 15 MHz.

3.2. Detection

The circuit works as expected for carrier frequencies between 1 and 15 MHz, with 10% AM modulation rates up to 200kbit/s. Figure 7 show the results for a 10 MHz carrier modulated at the maximum bit rate.

3.3. Power consumption

The supply current of the demodulator was measured for a wide range of operating conditions. At the nominal input signal level of $3.5\,V_{p\text{-}p}$ the supply current was constant at 20.0 ± 0.5 µA over the carrier frequency range of 1–15 MHz. A weak dependence on the signal amplitude was found, with the supply current decreasing by a few percent as the amplitude was reduced to zero. This dependence is due to the class AB operation of the squarer circuit.

4. Conclusion

A demodulator circuit has been presented, which in addition to a low power consumption of 60 µW, is versatile enough to be used in a wide range of implantable devices. Measurements show that the demodulator can handle up to 200kbit/s with a carrier frequency of up to 15 MHz. The sensitivity of the circuit makes it suitable for systems which must operate with low modulation indexes, either due to power transfer constraints or transmitter design.

The demodulator is designed for intermittent data transmissions and does not rely on constant modulation to determine the modulation levels. This allows maximum power transmission between data sequences.

The data rate and carrier frequency range can be extended by modifying the cutoff frequency of the LPF, and the passive component values in the input network.

[1] D. Galbraith, M. Soma and R. White, "Wide-band efficient inductive transdermal power and data link with coupling insensitive gain", *IEEE Trans. BME*, **34** (1987), pp. 265–275.

[2] A. Djemouai, M. Sawan and M. Slamani, "An efficient RF power transfer and bidirectional data transmission to implantable electronic devices", *Proc. ISCAS '99*, pp. II-259.

[3] G. Nebel *et al.*, "ASK 10% demodulator for contactless smart card IC", *Proc. ESSCIRC '99*, pp. 230–232.

[4] O. Oliaei and P. Loumeau "Four-quadrant class AB CMOS current multiplier", *Electronics Letters*, **32** (1996), pp. 2327–2329.