A Low-Power Capacitive Charge Pump Based Pipelined ADC

Imran Ahmed, *Member, IEEE*, Jan Mulder, and David A. Johns, *Fellow, IEEE*

***Abstract*—A low-power pipelined ADC topology is presented which uses capacitive charge pumps, source-followers, and digital calibration to eliminate the need for power-hungry opamps to achieve good linearity in a pipelined ADC. The differential charge pump technique achieves >10-bit linearity, and does not require an explicit common-mode-feedback circuit. The ADC was designed to operate at 50 MS/s in a 1.8 V, 0.18 μm CMOS process, where measured results show the peak SNDR and SFDR of the ADC to be 58.2 dB (9.4 ENOB), and 66 dB respectively. The ADC consumes 3.9 mW for all active circuitry and 6 mW for all clocking and digital circuits.**

***Index Terms*—ADC, charge pump, CMOS, common-mode-feedback, foreground calibration, linear sampling, low-power, opamp-less, pipelined.**

I. Introduction

THE proliferation of mobile applications and the cost sensitivity of IC packaging to heat dissipation have historically been the driving forces in the development of low-power circuits. ADCs being no exception to this trend have seen a flurry of development in recent years where several new and innovative architectures have been reported. For systems which require a medium to high resolution converter with a system clock at the Nyquist rate, the pipelined ADC is a popular choice. Within the scope of pipelined ADC research, the focus has been on techniques to reduce the power consumption of the Multiplying Digital to Analog Converter (MDAC), which is typically the largest consumer of power in the ADC. In the vast majority of pipelined ADCs, the MDAC is implemented with an opamp-based approach, where an example 1.5-bit pipeline stage is shown in Fig. 1. Research in reducing the power consumption of opamp-based pipelined ADCs have yielded innovations such as: opamp sharing [1], powering off the opamp when it is idle for half a clock cycle [2], [3], double sampling [4], and/or developing more power efficient opamp topologies (e.g., [5]–[8]) to name a few.

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I. Ahmed was with the Department of Electrical and Computer Engineering, University of Toronto, Ontario M5S 3G4, Canada. He is now with Kapik Integration, Toronto, Ontario M5T 2C2, Canada (e-mail: imran@kapik.com).

J. Mulder is with Broadcom Netherlands, Bunnik, The Netherlands (e-mail: jmulder@broadcom.com).

D. A. Johns is with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario M5S 3G4, Canada (e-mail: johns@eecg.toronto.edu).

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In the interest of prolonging battery life in mobile systems, recently there has been a shift to achieve even more power savings afforded from opamp-based techniques by substituting the opamp with alternative, more power efficient circuitry. For example, in [9] opamps with capacitive-feedback are replaced with open-loop resistively loaded differential-pairs, where a digital DSP calibrates the gain nonlinearity introduced by using an open-loop approach. Low-power is achieved as the open-loop gain stages do not require a large DC-gain, thus simplifying the MDAC circuit. Furthermore, the digital calibration circuits only add a relatively small amount of power. Examples of other subsequent works which also digitally calibrate nonlinear stage-gain are [10] and [11]. In [12] comparators and integrators are used in a topology which emulates the response of opamp-based switched capacitor circuits, but with far less power. The comparator-based topology of [12] has shown promising evolution where subsequent works have shown the architecture to be applicable in high-speed [13], differential [14], and high resolution [15] ADCs. In [16] a sampling scheme using parasitic capacitors and dynamic source-followers are used to approximately replicate the charge redistribution behavior of opamp based MDACs, but with much reduced power. By using digital calibration in [16], the non-idealities introduced by not having an opamp are corrected at approximately the 8-bit level.

In this work [17], a low-power pipelined ADC is presented which has a much lower power consumption than many previous 10-bit ADCs in the mid to high speed range. Low power is achieved as only a simple charge pump combined with a source-follower is required to achieve stage-gain in the pipeline stages. Thus, eliminating the need for a power-hungry opamp-based approach. This work achieves similar power savings as previous opamp-less ADCs, however this work has the advantages of: differential pipelined stages which do not require an explicit common-mode-feedback circuit, a sampling scheme which can achieve high linearity (SFDR of 66 dB and better than 9-bits ENOB), and a requisite of only linear stage-gain digital calibration.

The organization of this paper is as follows. Section II reviews classical capacitive charge pumps and outlines its advantages and disadvantages in the context of pipelined ADCs. Section III details the differential capacitive charge pump approach used in this work and presents a detailed discussion of the architecture. Section IV describes the circuit implementation of the design. Section V presents measurement results of a prototype fabricated in a 1.8 V, 0.18 μm CMOS process. Section VI summarizes and concludes the work.

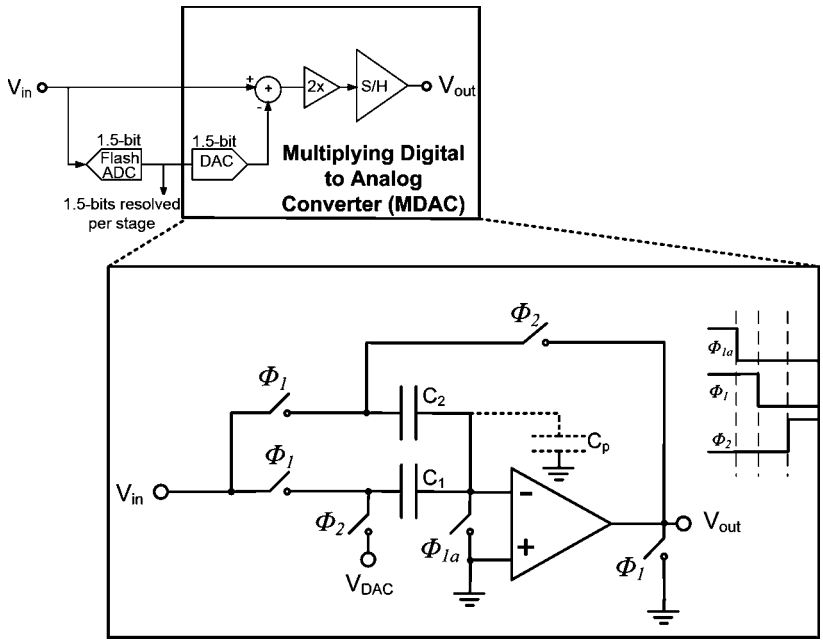

Fig. 1. Opamp based MDAC with stage-gain of two in a 1.5-bit pipelined ADC stage.

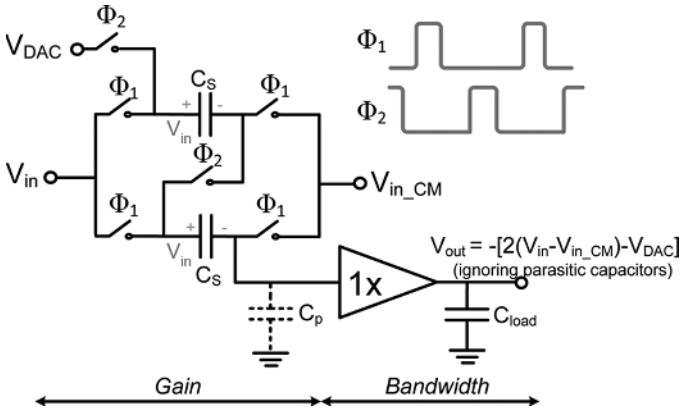

Fig. 2. Gain of approximately 2 using a capacitive charge pump approach.

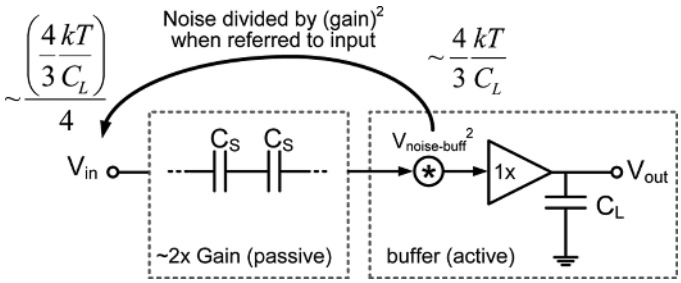

Fig. 3. Reduced noise from buffer with capacitive charge pump.

II. Gain With Capacitive Charge Pumps

A. Classical Capacitive Charge Pump

In a classical capacitive charge pump, voltage-gain is achieved by sampling an input voltage on multiple capacitors, and subsequently connecting each capacitor in series to yield a total voltage which is the sum of the individual voltages sampled on each capacitor. Charge pumps are commonly used in DC/DC boost converters (e.g., Dickson Charge pump [18]). Fig. 2 shows a classical capacitive charge pump used in a potential MDAC topology which implements a gain of approximately two, and is capable of driving a capacitive load. A unity-gain buffer is used in Fig. 2 to prevent charge sharing between the sampling and the load capacitors $C_{\rm s}$, and $C_{\rm load}$ respectively. In Fig. 2, $V_{\rm in\_CM}$ is a reference voltage which is set to the DC bias of the input.

Voltage gain using a charge pump based approach has a significant advantage in that the gain–bandwidth tradeoff which binds opamp-based MDACs is decoupled. With a capacitive charge pump, the gain is determined by the sampling capacitor arrangement, whereas the bandwidth of the output, $V_{\rm out}$, during Φ_2 is independently established by the unity-gain buffer and $C_{\rm load}$ (assuming the overall bandwidth is not limited by the 'on' resistance of the switches). Opamp-based approaches also suffer additional power penalties which do not affect the charge pump approach, such as parasitics which reduce the feedback factor β, and the necessity of multiple stages to achieve a large DC-gain.

An additional advantage of gain with capacitive charge pumps is that in each pipeline stage since the unity-gain buffer is preceded by the amplification of the input, the noise-power of the buffer when referred to the input of the pipeline stage is reduced by the square of the stage-gain, as shown in Fig. 3. Hence, the buffer adds only a small noise contribution, enabling the use of small sampling capacitors (thus reduced power consumption) to meet the desired thermal noise floor.

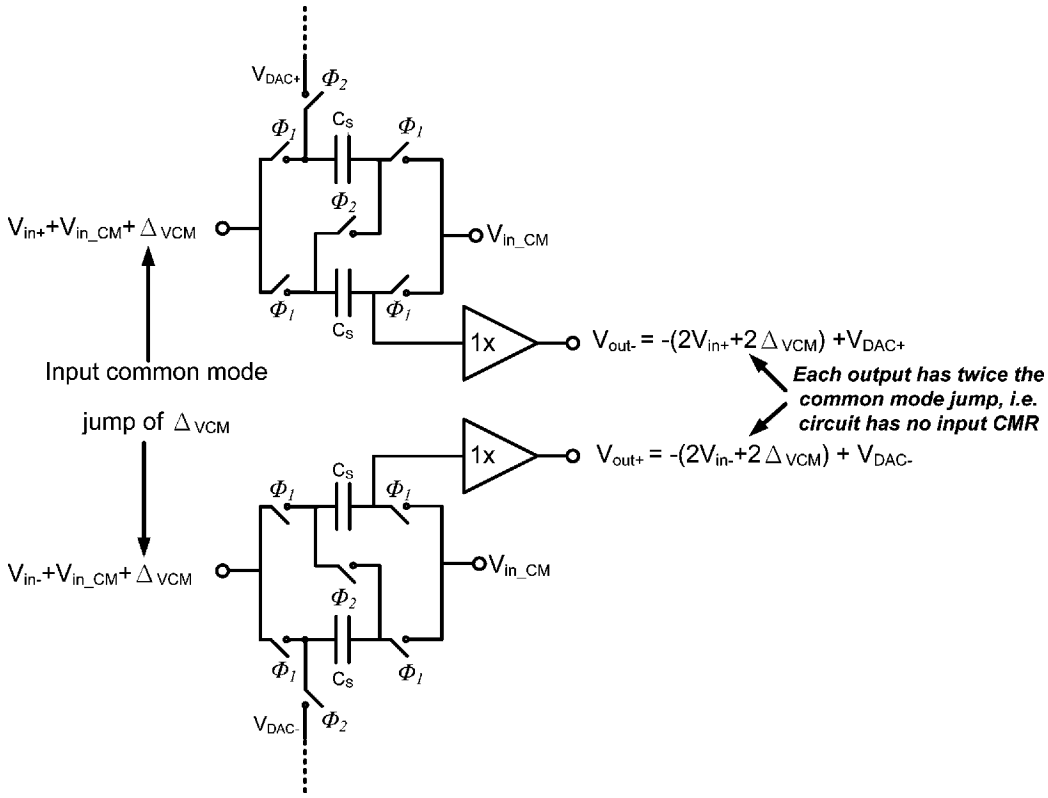

Fig. 4. Poor common-mode rejection in the classical capacitive charge pump.

B. Limitations of the Classical Capacitive Charge Pump for use in Pipelined ADCs

There are limitations of the classical capacitive charge pump topology of Fig. 2, however, which prevent it from being used "as is" in a pipelined ADC. The main limitations are imprecise gain, and poor common-mode rejection.

From Fig. 2, if the dominant parasitic capacitor $C_{\rm p}$ is included, the output of the classical charge pump based MDAC is given by

$$V_{\rm out} = -\left[\frac{2}{1+2(C_{\rm p}/C_{\rm s})}(V_{\rm in}-V_{\rm in\_CM})-\frac{1}{1+2(C_{\rm p}/C_{\rm s})}V_{\rm DAC}\right] \quad (1)$$

which is a direct function of parasitic capacitors. Parasitic capacitors vary from chip to chip and in general cannot be predicted to a sufficiently high accuracy prior to fabrication. In pipelined ADCs the maximum allowable stage-gain error in each pipeline stage must be lower than an LSB when the gain-error is referred to the ADC's input. Since a ratio of $C_{\rm p}/C_{\rm s}$ smaller than an LSB at the 10-bit level is highly unlikely, a design technique to cancel the impact of parasitic capacitors is required. For example, in [19] two opamps with large DC gain are used to negate the effect of parasitic capacitors in an algorithmic ADC which uses a charge pump inspired approach to achieve stage-gain. Rather than using an analog technique as used in [19] to account for stage-gain errors, in this work the gain errors in each pipeline stage are measured and corrected using a simple digital calibration scheme (the details of which are outlined in Section III-D). Thus, in this work analog complexity is traded with digital complexity—a favorable tradeoff as technology scaling favors digital circuits more than analog circuits.

Another limitation of the classical charge pump approach is that there is no common-mode rejection for a differential input signal. For example, consider the case where the classical charge pump is arranged to sample differential inputs $V_{\rm in+}$, $V_{\rm in-}$ as shown in Fig. 4, where the input common-mode has an offset from the desired input common-mode voltage by $\Delta_{\rm VCM}$. As shown in Fig. 4 this results in the common-mode of the output also being doubled in addition to the analog input, i.e., the topology of Fig. 4 is pseudo-differential, and thus very sensitive to common-mode noise. In a pipelined ADC consisting of many stages, if each stage has no common-mode rejection a small common-mode offset at the input of one of the pipeline stages could rapidly multiply along the pipeline. As a result the absolute voltage of the input to a latter pipeline stage could saturate at a supply-rail rendering subsequent pipeline stages unusable, thus significantly limiting the resolution of the ADC. To avoid the poor common-mode rejection problem of the classical charge pump, a modified differential charge pump suitable for pipelined ADCs is proposed and detailed in Section III.

III. Differential Capacitive Charge Pump Based Pipelined Stage

A. Differential Capacitive Charge Pump

To avoid amplifying common-mode offset voltages a differential capacitive charge pump based MDAC was developed for

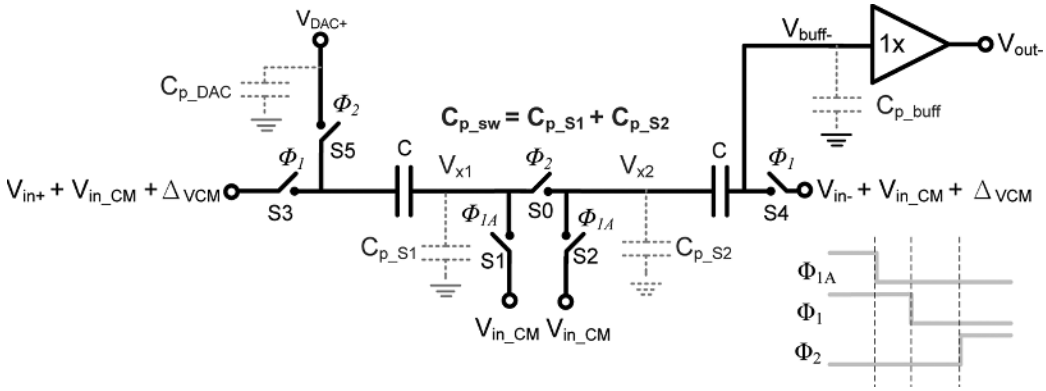

Fig. 5. 1.5-bit differential capacitive charge pump based MDAC with parasitic capacitors labeled (half circuit shown, negative half is identical with appropriate reversal of signs) .

this work as shown in Fig. 5 in a 1.5-bit pipeline stage. The sampling network was arranged such that the *differential input* was sampled in a fully bridged configuration across the sampling capacitors during Φ_1. Since the input common-mode voltage is sampled on *both sides* of the series combination of the sampling capacitors, common-mode variations in the differential input are hence rejected during Φ_2. From the analysis presented in the Appendix, the stage-gain of the topology in Fig. 5 is given by

$$V_{\text{out}-} = A_{\text{buff}}\left[V_i\left(\frac{2+X}{1+X}\right) - V_{\text{DAC}} + \left(\frac{1}{1+X}\right) - \left(V_{\text{in\_CM}} + \Delta_{\text{VCM}}\right)\left(\frac{X}{1+X}\right)\right] \quad (2)$$

where

$$X = \frac{C_{\text{p\_sw}}}{C} + 2\frac{C_{\text{p\_buff}}}{C} + \frac{C_{\text{p\_sw}}C_{\text{p\_buff}}}{C^2}, \quad (3)$$

$V_{\text{in}+} = -V_{\text{in}-} = V_i$, and A_{buff} is the gain of the unity-gain buffer which is approximately one. When the parasitic capacitors are zero, and $A_{\text{buff}} = 1$:

$$V_{\text{out}-} = -[2V_i - V_{\text{DAC}+}] \quad (4)$$

which is precisely the residue transfer characteristic of a 1.5-bit pipeline stage. If $C_{\text{p\_sw}}, C_{\text{p\_buff}} \ll C$ (which can be practically achieved with good design), from (3) X becomes very small. Hence, given a small X in (2) the input-common-mode $V_{\text{in\_CM}}$ and input-common-mode error of Δ_{VCM} are significantly attenuated in the MDAC's output. Thus, multiple pipelined stages can be cascaded using the topology of Fig. 5 without common-mode errors growing along the pipeline. Switch S0 is included in Fig. 5 to isolate nodes V_{X1} and V_{X2} during Φ_1, and thus ensure that switches S1 and S2 act as bottom-plate sampling switches [20] so as achieve a high linearity by minimizing charge-injection effects.

During Φ_2 a voltage divider is formed between the sampling capacitors and the parasitic capacitor $C_{\text{p\_buff}}$. Assuming $C_{\text{p\_sw}}$, $C_{\text{p\_buff}} \ll C$, the common-mode voltage of the buffer's input is approximately given by the common-mode voltage of the DAC. Thus, a significant advantage of the topology of this work is that an explicit common-mode feedback circuit is not required to establish a well known common-mode

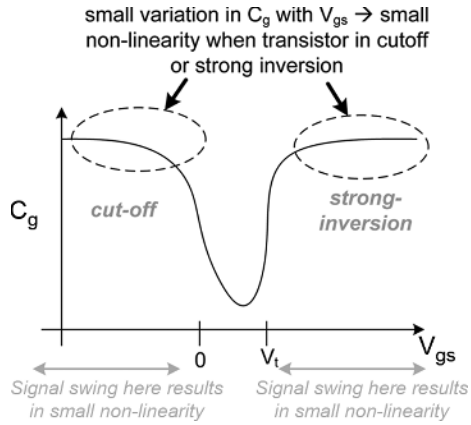

Fig. 6. Variation of gate capacitance with V_{gs} for a MOS device.

voltage at $V_{\text{buff}-}$. Even if the parasitic capacitors are large, no Common-Mode Feedback (CMFB) circuit is strictly required to define the common-mode level at node $V_{\text{buff}-}$ so long as the common-mode level is within the allowable input common-mode range of the unity-gain buffer. Since common-mode rejection is realized in the sampling network, it is possible for simple single-ended circuits such as source-followers to be used as a unity-gain buffer, yet achieve differential functionality between the input and output of the pipeline stage. In contrast, differential opamp based topologies typically use pseudo-differential sampling and a differential opamp. The large DC-gain of a differential opamp necessitates an explicit CMFB circuit to avoid saturating the opamp's output at a supply rail. As CMFB circuits add more power and complexity to a design, the elimination in this work of an explicit CMFB simplifies the ADC topology and also enables a further reduction of power.

B. Impact of Parasitic Capacitors: Maximizing Gain in the Pipeline Stage

The number of quantization levels in the digital output of a pipelined ADC is a function of the product of the gain of each stage in the ADC. Thus, to maximize the number of quantization levels in a pipelined ADC it is of interest minimize parasitic capacitors which reduce the stage-gain. $C_{\text{p\_buff}}$ is made relatively small in this work by using a source-follower based unity-gain

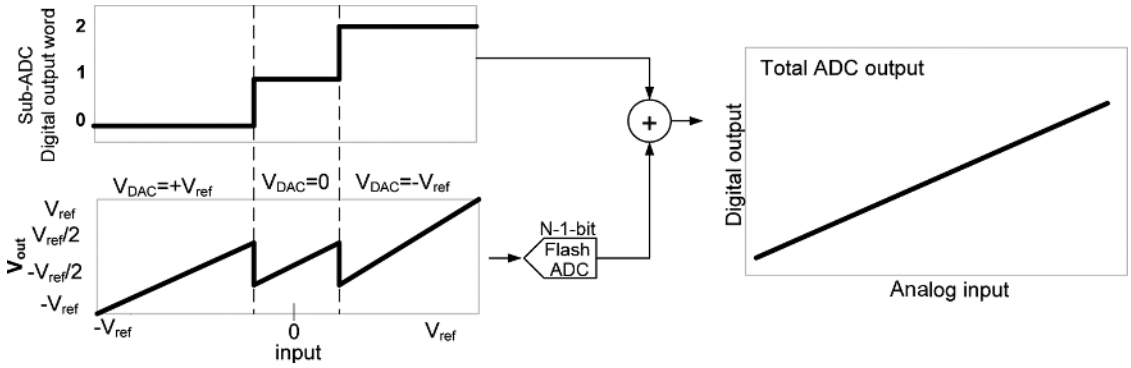

Fig. 7. Ideal 1.5-bit first pipeline stage.

buffer, which as will be seen in Section IV-B, has a small input capacitor. Switches S1 and S2 add only a small parasitic capacitor as they are used to pass DC voltages, hence can be sized relatively small. Switch S0 passes half of the output signal swing, thus must be large enough to allow $V_{\mathrm{buff}-}$ to settle to the desired accuracy within half a clock cycle. In general careful sizing of switch S0 is required to balance the conflicting requirements of small size to maximize stage gain and large size to minimize settling time. In this work S0 was implemented with a transmission gate, however in processes with small supply voltages a low V_t device or a technique such as bootstrapping can be used to implement switch S0. As $V_{\mathrm{DAC}+}$ is driven by a DC voltage source during Φ_2, parasitic capacitors at node $V_{\mathrm{DAC}+}$ have no impact on the stage gain, and thus the size of switch S5 can be made large without affecting stage-gain.

C. Impact of Parasitic Capacitors: Maximizing Linearity

From (2), since the gain of the pipeline stage is a function of parasitic capacitors, nonlinearities in the parasitic capacitors can limit the linearity of the gain. Fig. 6, however, (which shows a typical plot of gate capacitance for a MOS transistor versus gate-source voltage), illustrates that if a transistor is either cut-off or in strong inversion, the parasitic capacitor at the gate of a transistor is only a very weak function of variation in the gate-source voltage. Since all switches in the topology of Fig. 5 are designed to be strongly inverted/in cut-off while on/off, and the input transistor of the buffer also designed to be strong inversion, the impact of nonlinearities from parasitic capacitor variation with signal swing is relatively small at the 10-bit level. It is noted however that the effect of nonlinear parasitic capacitance could be a limiting factor in achieving linearity significantly higher than that targeted in this work (i.e., $\gg$10-bit linearity).

D. Digital Calibration Technique

Digital calibration was used to measure and correct the stage-gain errors of each pipeline stage. To minimize the design complexity of the prototype, a simple foreground calibration scheme [21] was used. In theory however, any prior pipelined ADC calibration scheme which calibrates multiple pipeline stages could be used with the topology of this work. Thus, for example it is also possible to use a background/continuous calibration [22] scheme if desired. The following paragraphs detail the calibration scheme [21] used in this work.

Consider the ADC topology of Fig. 7, which shows a 1.5-bit first pipeline stage followed by an ideal backend Flash ADC. If there is a stage-gain error in the first pipeline stage, the output of the ADC is as shown in Fig. 8. Thus, the objective of the calibration scheme is to estimate the number of missing codes, ε. Consider the residue transfer curve of a 1.5-bit stage as shown in Fig. 9. If the input to the pipeline stage is zero, the DAC voltage can be either 0, $+V_{\mathrm{ref}}$, or $-V_{\mathrm{ref}}$. Thus, in an ideal 1.5-bit pipeline stage with zero input, the output of the ADC will be constant regardless of the DAC voltage. However, if with zero input there is a stage-gain error, the ADC will output different values when the DAC voltage is connected to $+V_{\mathrm{ref}}$, 0, and $-V_{\mathrm{ref}}$, respectively. Thus, the missing codes produced by a non-ideal stage-gain can be corrected in the foreground by shorting the input of the pipeline stage under calibration to zero, and separately measuring the output of the ADC when the DAC voltage of the stage under calibration is connected to $+V_{\mathrm{ref}}$, 0, $-V_{\mathrm{ref}}$, respectively. By averaging out each value for a few clock cycles to suppress thermal noise an accurate estimate of the error ε can be found. The gain error is subsequently corrected by shifting the digital output by the negative amount of the missing codes during normal operation of the ADC as shown in Fig. 10.

Multiple pipeline stages were calibrated at startup by recursively using the described calibration initially on the last pipeline stage (while powering off all previous stages), then the second last, then the third last, etc., eventually calibrating the entire pipeline as shown in Fig. 11.

IV. Circuit Impelemntation

A. Top Level Topology

Fig. 12 illustrates the top-level topology of the ADC in this work. Simulation results showed each pipeline stage to have a stage gain of approximately 1.8. Thus, with 12 total stages followed by a 2-bit Flash ADC, the quantization accuracy of the ADC was $2 + 12\log_2(1.8) \simeq 12$ bits. As ADC power is dominated by thermal noise considerations, the thermal noise floor at the input of the ADC was designed to be approximately at the 10-bit level. To minimize power, the first three pipeline stages were scaled approximately by their respective stage-gains [23].

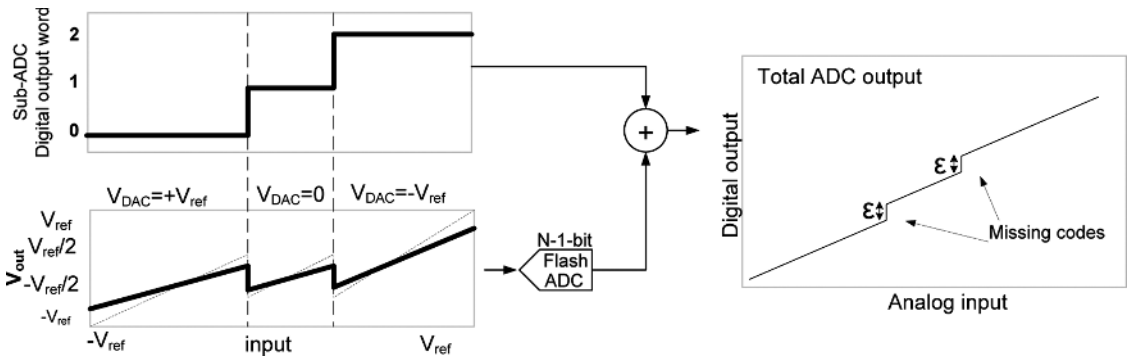

Fig. 8. 1.5-bit pipeline stage with gain error.

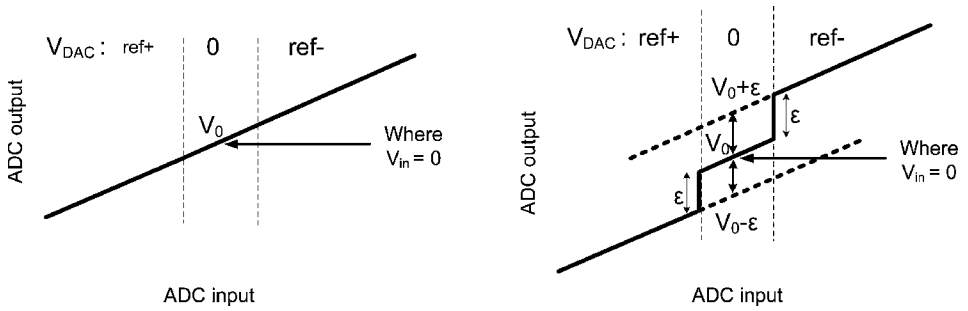

Fig. 9. Measure of missing codes when pipeline stage input ($V_{\rm in}$) is zero—left is ideal, right is with errors.

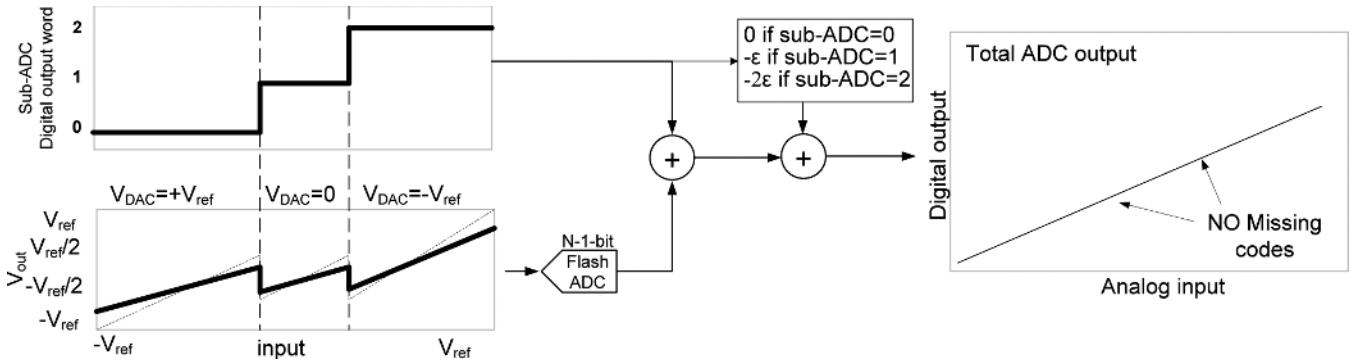

Fig. 10. Illustration of correction scheme.

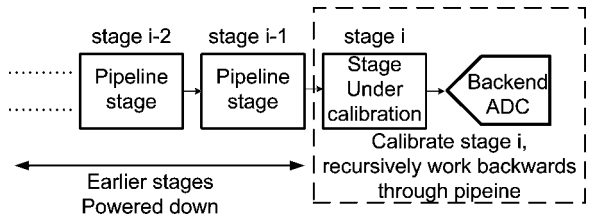

Fig. 11. Multistage foreground calibration.

B. Pipeline Stage With Source-Follower Unity-Gain Buffer

Although any sufficiently linear buffer topology can implement the unity-gain buffer of Fig. 5, source-followers were used in this work as they are simple to design, have a gain largely a function of device dimensions, and with proper design achieve good linearity. Fig. 13 shows the full topology of a single pipelined stage in this work (note that additional circuitry required for foreground calibration have been omitted to simplify the figure). A deep-N-well layer was used to eliminate the body effect for M1 in Fig. 13. nMOS devices were used as an nMOS source-follower achieves a larger g_m (thus larger bandwidth) than an identically sized and biased pMOS source-follower. Switch S6 was included to power off the buffer during the sampling phase Φ_1, thus enable a further reduction in power.

The signal swing of the buffer (which was 0.5 V peak-peak single-ended), was designed as large as possible to minimize the required sampling capacitance to achieve a noise floor of approximately 10 bits, while ensuring sufficient linearity from the source-follower. The length of the current-source transistor MB in Fig. 13, was made larger than minimum size to reduce the short-channel effects and hence nonlinearity induced from $I_{\rm bias}$ being modulated by the signal swing at $V_{\rm out\_}$. Since the source-follower is used in a discrete time system, nonlinearities in the parasitic capacitor loading the source-follower's output do not have a significant impact at the 10-bit level given a sufficient settling time. If a linearity higher than the 10-bits of this

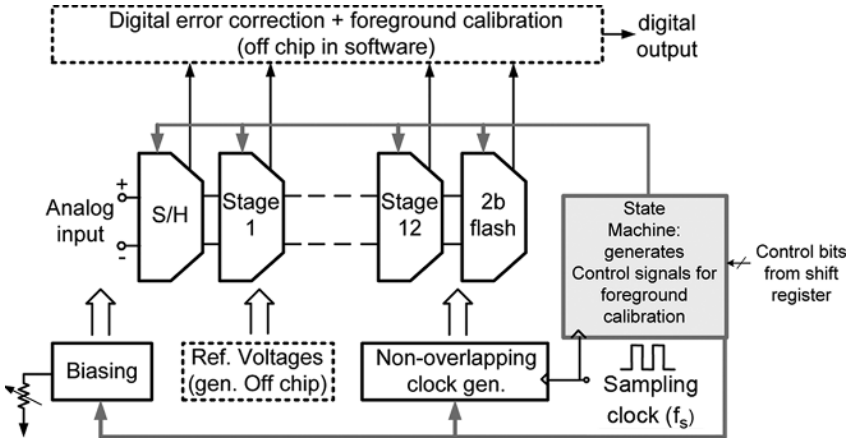

Fig. 12. Pipelined ADC top-level topology.

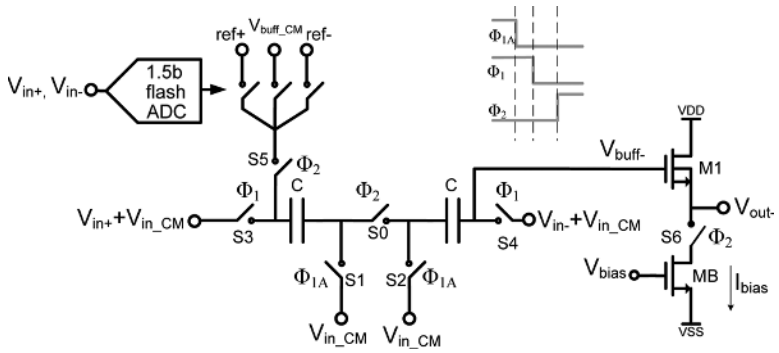

Fig. 13. Topology of each 1.5-bit pipeline stage in this work—the positive half is shown; the negative half is identical with a reversal of positive/negative signs.

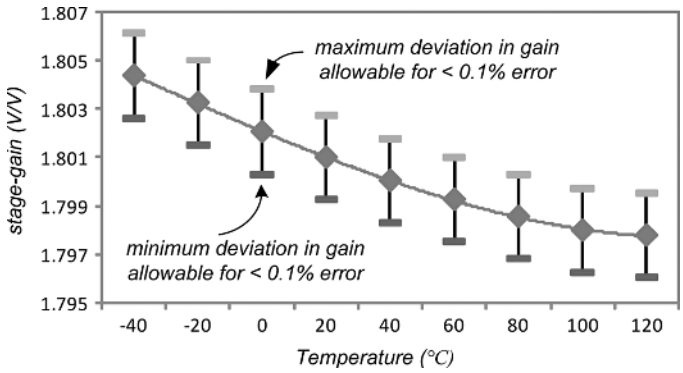

Fig. 14. Stage-gain variation with temperature (based on simulation).

work were targeted a source-follower linearization technique, for example such as that used in [24], could be used.

Since there is unity-gain between the gate and source of transistor M1, the gate and source move approximately together. Thus, the effect of the parasitic input capacitor $C_{\rm gs}$ is significantly reduced, leaving the parasitic input capacitor of the unity-gain buffer to be dominated by the relatively small $C_{\rm gd}$ [25]. The small parasitic input capacitance of the source-follower enables larger stage-gain in each pipeline stage and thus more quantization levels in the ADC.

Fig. 14 shows the variation of the stage-gain of Fig. 5 over temperature based on simulation results. From Fig. 14, it is clear that while the gain does vary $>0.1\%$ over the entire temperature range (from $-40\,^{\circ}$C to $120\,^{\circ}$C), the gain variation is $<0.1\%$ for a reasonably wide fraction of the entire temperature range. Thus, if the operation temperature does not change too widely, frequent recalibrations may not be required. To achieve a higher resolution than that targeted in this work and/or use the ADC used in a system which could have drastic temperature variations, a background calibration scheme [22] could alternatively be used to ensure temperature induced gain fluctuations were always accounted for.

C. 1.5-Bit Sub-ADC Comparators

The 1.5-bit Flash sub-ADC was designed using dynamic comparators as shown in Fig. 15. Dynamic comparators have the advantage of low power consumption, but at the cost of increased offset. However, increased comparator offset can be tolerated, since a 1.5-bit/stage pipeline topology affords a large amount of redundancy to trade with comparator offset [26].

The sub-ADC comparators required different reference voltages than those used in the MDACs of each pipeline stage, since the inputs of the sub-ADC connect to the outputs of nMOS source-followers which have a low output common-mode voltage. The redundancy of the pipeline stages allows the differential comparator reference voltages to be offset from the differential DAC reference voltages by as much as a quarter of the reference voltage without incurring any errors. Additionally, using separate reference voltages for the comparators reduces the amount of switching noise on the DAC reference voltages.

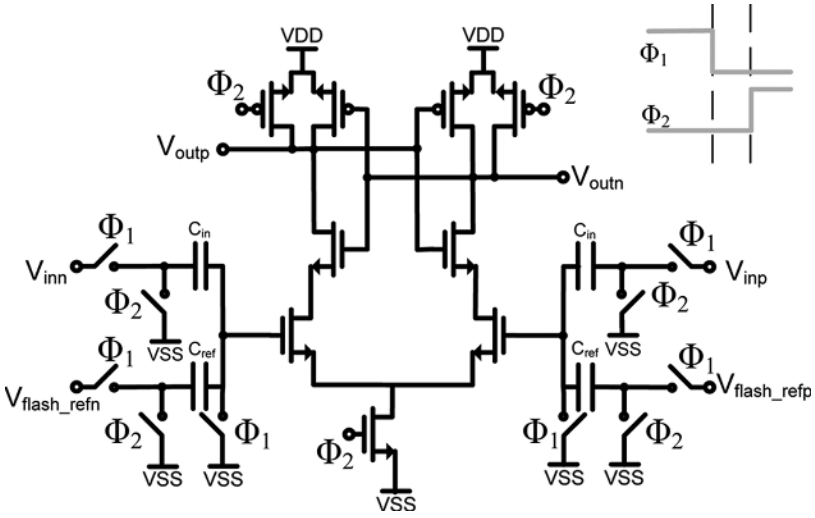

Fig. 15. Dynamic comparator used in 1.5-bit Flash sub-ADC.

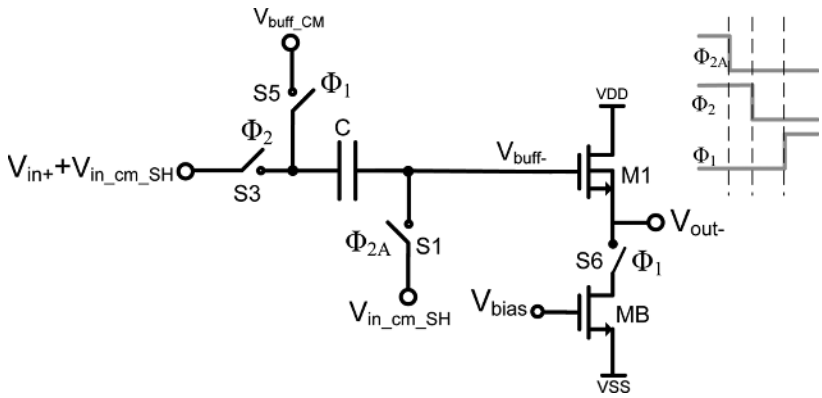

Fig. 16. Front-end sample-and-hold topology used in this work—positive half is shown; the negative half is identical with a reversal of positive/negative signs.

D. Front-End Sample-and-Hold

A front-end S/H was used to ensure the MDAC and 1.5-bit flash ADC of the first pipelined-stage operated on the same input for all input frequencies. The front-end S/H topology also was realized using a source-follower based approach [27] as shown in Fig. 16 so as to minimize power consumption. Switch S6 was included in Fig. 16 to power off the source-follower during Φ_1, and hence save additional power.

E. Off-Chip Foreground Digital Calibration

To enhance flexibility in the test setup, the foreground digital calibration engine was implemented off-chip, where the digital outputs of each pipeline stage were taken off-chip and imported into MATLAB via a logic analyzer. To correctly initialize each pipeline stage during calibration using the methodology described in Section III-D [21], an on-chip digital state machine was used to generate the control signals for each pipeline stage during foreground calibration. The state machine was only powered on during foreground calibration and powered completely off subsequently.

V. Measured Results

A prototype of the ADC of this work was fabricated in a 1.8 V, 0.18 μm CMOS process as shown in Fig. 17, where the

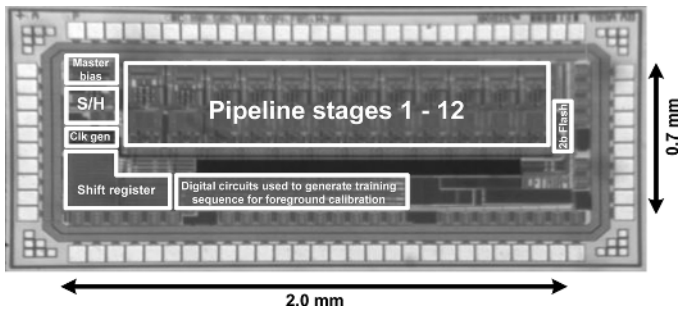

Fig. 17. Micrograph of ADC.

core area was 2.0 mm $\times$ 0.7 mm (1.4 mm^2). Approximately a quarter of the area was dedicated to test circuitry used to aid in testing the ADC (i.e., circuits which are not strictly required for functionality). Furthermore, from Fig. 17 it can be seen that the actual pipeline stages occupied an area of approximately 2 mm $\times$ 0.4 mm $=$ 0.8 mm^2.

The total power of the 50 MS/s ADC was 9.9 mW, including 3.9 mW from all active circuitry, and 6 mW from all clocking and clock distribution circuits. The fact that the majority of power consumed is dynamic suggests that a large reduction in power could be achieved by lowering the digital/clocking supply

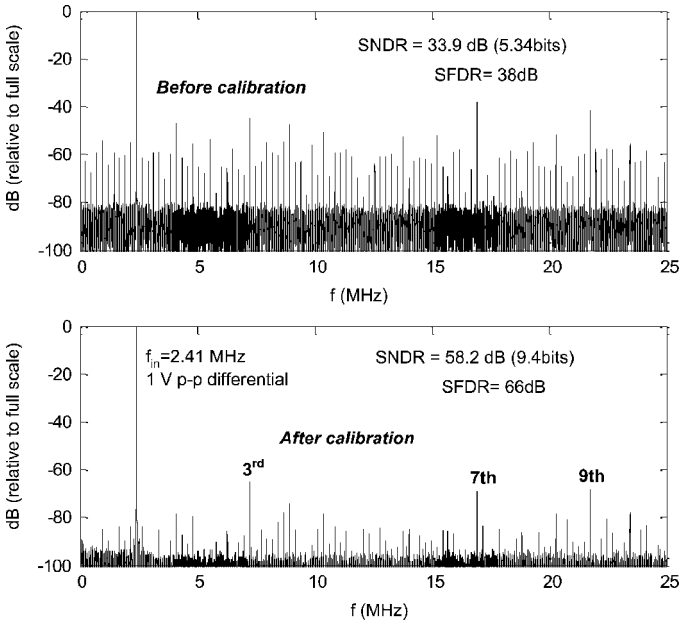

Fig. 18. FFT of ADC output before/after calibration with 2.41 MHz input tone, $f_s = 50$ MS/s.

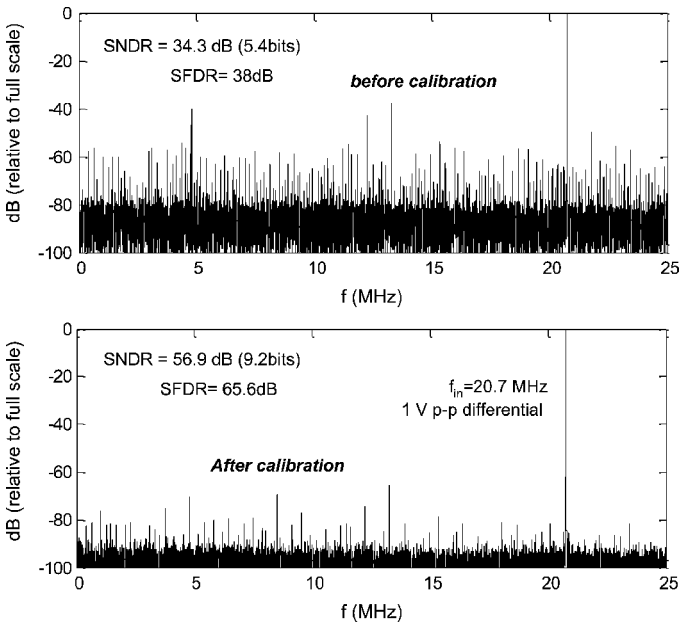

Fig. 19. FFT of ADC output before/after calibration with 20.7 MHz input tone, $f_s = 50$ MS/s.

voltage and/or migrating to a smaller technology. Although the digital calibration was implemented off-chip, the added power required if the calibration engine were on-chip would only be on the order of a few mW. To simplify the prototype, the reference voltages were also generated off-chip and their power is not included. However it is noted that the total average current demanded by ADC from the off-chip reference voltages was only 0.34 mA.

Figs. 18 and 19 show FFTs of the ADC output for input frequencies of 2.4 MHz and 20.7 MHz before and after calibration for $f_s = 50$ MS/s. The FFTs clearly illustrate the significant improvement in ADC performance afforded with calibration—more than 4 bits. The post-calibration FFT plots show heavy attenuation of even-order distortion terms, verifying the differential nature of the MDAC sampling topology of this work. Fig. 20 shows the variation of ADC SNDR and SFDR with input frequency, where it is seen that better than 9-bit ENOB (i.e., SNDR $>$ 56 dB) is maintained for the Nyquist bandwidth.

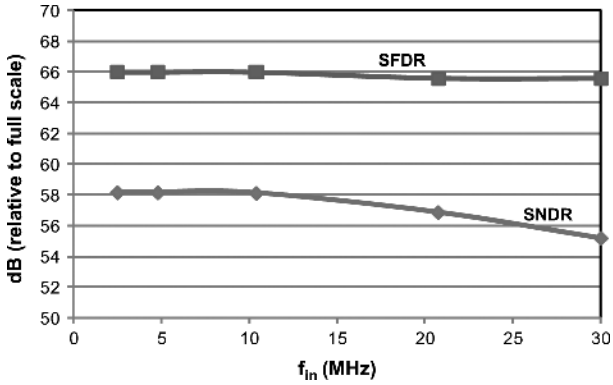

Fig. 20. ADC SNDR/SFDR variation with input frequency, $f_s = 50$ MS/s.

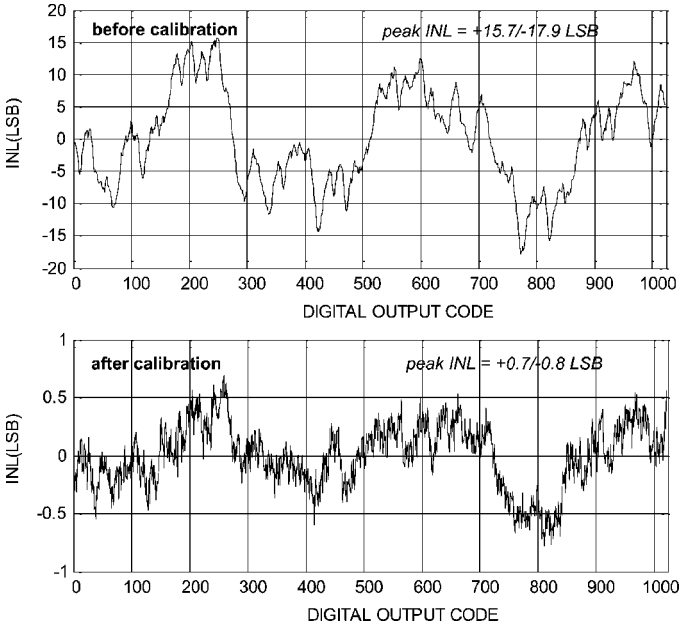

Fig. 21. ADC INL before and after calibration, $f_s = 50$ MS/s.

Figs. 21 and 22 show INL and DNL, respectively, of the ADC before and after calibration, where it seen that digital calibration significantly improves the INL of the ADC from $+15.7/-17.9$ LSB to $+0.7/-0.8$ LSB and DNL from $+1.6/-1$ LSB to $+0.35/-0.35$ LSB.

To evaluate the robustness of the system, all on-chip bias currents were varied by $\pm 10\%$ and the ADC resolution measured in each case without recalibrating the ADC (i.e., ADC calibration coefficients were only derived once at the nominal bias current). Measured results showed that the ENOB varied by less than 0.1 bits, indicating that frequent recalibrations may not be required. The ADC resolution was also checked with one week separation between measurements and without recalibrating, where the ENOB change over a week was negligible ($<$0.1-bit variation) with the same test setup.

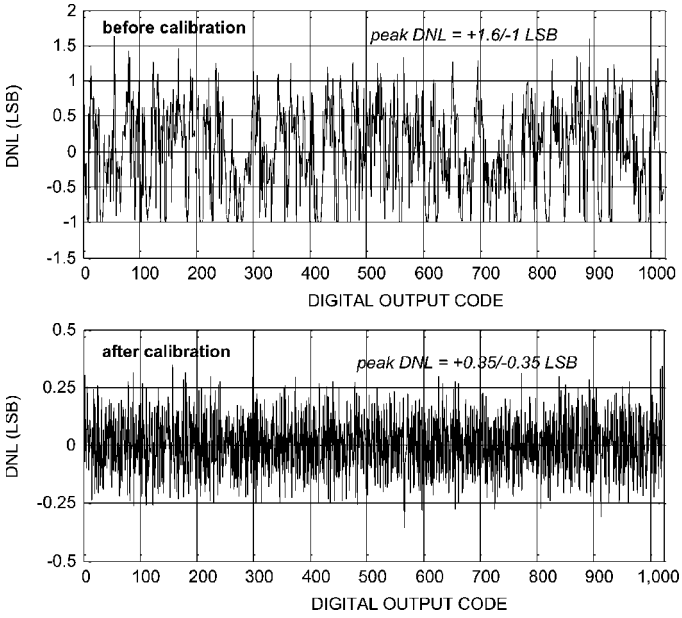

Fig. 22. ADC DNL before and after calibration, $f_s = 50$ MS/s.

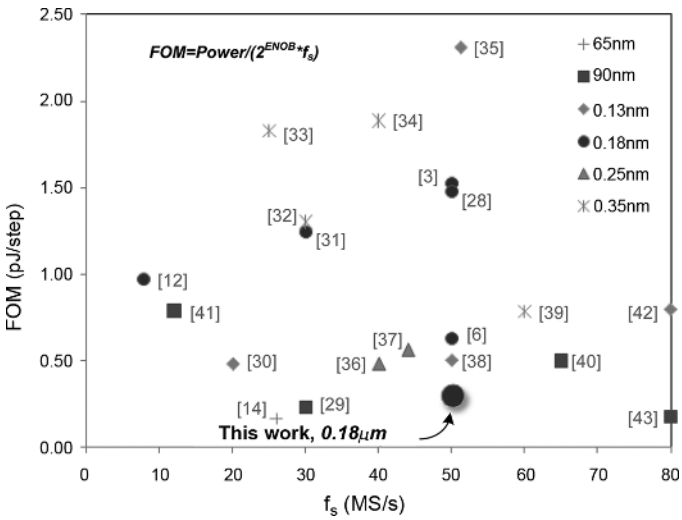

Fig. 23. Comparison of FOM of this work versus other recently published 10-bit ADCs.

Fig. 23 shows the figure of merit of the ADC of this work compared to other recently published 10-bit ADCs, where it is seen that the ADC of this work has among the best published figure of merits in the 10–80 MS/s range. Furthermore it is noted that among 0.18 μm 10-bit ADCs for the specified sampling rate range, this work achieves the lowest figure-of-merit. From Fig. 23 it is clear the techniques outlined in this work can be of great use in reducing ADC power.

VI. Conclusion

In this paper, a technique to significantly reduce pipelined ADC power was discussed. Low power was achieved by using a simple architecture consisting of a charge pump combined with a source-follower and digital calibration, which replaced the functionality of power-hungry opamp based pipeline stages found in prior works. A differential sampling technique was used which eliminated the need for an explicit CMFB circuit, thus enabling further power savings. A summary of key measurement results of this work are presented in Table I.

TABLE I
Summary of ADC Performance.

Technology	1.8V, 0.18μm CMOS
Input signal swing	1.0V p-p
Area	1.4mm^2
Sampling rate	50MS/s
SNDR	58.2 dB (peak)
SFDR	66dB (peak)
ENOB	9.4 (peak)
Power	9.9 mW
FOM	0.3 pJ/step

Appendix

From Fig. 5, during Φ_1 when a differential input of $V_{\text{in}+}, V_{\text{in}-}$ with a common-mode of $V_{\text{in\_CM}}$ and a common-mode offset of Δ_{VCM} is sampled, the charge sampled on node V_{x1} during Φ_1 is given by

$$Q_{\Phi 1_{V_{x1}}} = C[V_{\text{in\_CM}} - (V_{\text{in}+} + V_{\text{in\_CM}} + \Delta_{\text{VCM}})] + C_{\text{p\_S1}} V_{\text{in\_CM}} \quad (5)$$

$$\therefore\ Q_{\Phi 1_{V_{x1}}} = -C\Delta_{\text{VCM}} - CV_{\text{in}+} + C_{\text{p\_S1}} V_{\text{in\_CM}}. \quad (6)$$

Similarly, during Φ_1 the charge sampled on V_{x2} is given by

$$Q_{\Phi 1_{V_{x2}}} = -C\Delta_{\text{VCM}} - CV_{\text{in}-} + C_{\text{p\_S2}} V_{\text{in\_CM}}. \quad (7)$$

During Φ_2 switch S0 closes, resulting in $V_{x1} = V_{x2} = V_x$. Thus, the total charge on node V_x at the beginning of Φ_2 due to the events of Φ_1 is given by

$$Q_{\Phi 1\_V_x} = Q_{\Phi 1\_V_{x1}} + Q_{\Phi 1\_V_{x2}} = -2\Delta_{\text{VCM}} C - C(V_{\text{in}+} + V_{\text{in}}) + C_{\text{p\_SW}} V_{\text{in\_CM}} \quad (8)$$

where $C_{\text{p\_SW}} = C_{\text{p\_S1}} + C_{\text{p\_S2}}$. Since by definition $V_{\text{in}+} = -V_{\text{in}-}$:

$$\therefore Q_{\Phi 1\_V_x} = -2\Delta_{\text{VCM}} C + C_{\text{p\_SW}} V_{\text{in\_CM}}. \quad (9)$$

At the end of Φ_2 the total charge on node V_x is given by

$$Q_{\Phi 2\_V_x} = C_{\text{p\_SW}} V_x + C(V_x - V_{\text{DAC}+}) + C(V_x - V_{\text{buff}-}). \quad (10)$$

As charge is conserved at node V_x, (9) can be equated to (10), yielding

$$V_x = V_{\text{buff}-}\left(\frac{C}{2C + C_{\text{p\_SW}}}\right) + V_{\text{DAC}+}\left(\frac{C}{2C + C_{\text{p\_SW}}}\right) - 2\Delta_{\text{VCM}}\left(\frac{C}{2C + C_{\text{p\_SW}}}\right) + V_{\text{in\_CM}}\left(\frac{C}{2C + C_{\text{p\_SW}}}\right). \quad (11)$$

During Φ_1, the charge sampled on $V_{\text{buff}-}$ is given by

$$Q_{\Phi 1\_V_{\text{buff}-}} = C(V_{\text{in}-} + \Delta_{\text{VCM}}) + C_{\text{p\_buff}}(V_{\text{in}-} + V_{\text{in\_CM}} + \Delta_{\text{VCM}}). \quad (12)$$

During Φ_2, the charge sampled on $V_{\text{buff}-}$ is given by

$$Q_{\Phi 2\_V_{\text{buff}-}} = C_{\text{p\_buff}} V_{\text{buff}-} + C(V_{\text{buff}-} - V_x). \quad (13)$$

Using the fact that charge is conserved at node $V_{\text{buff}-}$ between Φ_1 and Φ_2 gives the following:

$$\begin{aligned} &C(V_{\text{in}-} + \Delta_{\text{VCM}}) \\ &\quad + C_{\text{p\_buff}}(V_{\text{in}-} + V_{\text{in\_CM}} + \Delta_{\text{VCM}}) \\ &\quad = C_{\text{p\_buff}} V_{\text{buff}-} + C(V_{\text{buff}-} - V_x). \end{aligned} \quad (14)$$

Substituting (11) into (14), the expression for the output voltage, $V_{\text{out}-}$, during Φ_2, is given by

$$V_{\text{out}-} = -A_{\text{buff}} \left[V_i \left(\frac{2+X}{1+X} \right) - V_{\text{DAC}+} \left(\frac{1}{1+X} \right) - (V_{\text{in\_CM}} + \Delta_{\text{VCM}}) \left(\frac{X}{1+X} \right) \right] \quad (15)$$

where

$$X = \frac{C_{\text{p\_SW}}}{C} + 2\frac{C_{\text{p\_buff}}}{C} + \frac{C_{\text{p\_SW}} C_{\text{p\_buff}}}{C^2} \quad (16)$$

A_{buff} is the gain of the unity-gain buffer (which is approximately one), and by definition $V_i = V_{\text{in}+} = -V_{\text{in}-}$.

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Imran Ahmed (S'00–M'08) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, Ontario, Canada, in 2002, 2004, and 2008, respectively.

He is a co-founder of Kapik Integration, Canada, a provider of design services and IP in high performance circuits. At Kapik he is involved in developing mixed-signal circuits such as data converters, digitally assisted analog, and reconfigurable systems. Between 2000 and 2004 he held several internships at Snowbush Microelectronics, Toronto, where he worked on various leading-edge mixed-signal circuits. From August to November 2007, he was an intern at Broadcom Netherlands, where he worked on developing low-power pipelined ADC architectures. He is the author of the book *Pipelined ADC Design and Enhancement Techniques* (Springer, 2010).

Dr. Ahmed received First Place in the operational category and Best Overall Submission in the 2005 DAC/ISSCC Student Design Competition. His work at ESSCIRC 2007 received the Young Scientist Award. He is also the recipient of the 2008 Analog Devices Outstanding Student Designer Award.

Jan Mulder received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1994 and 1998, respectively.

From 1998 to 2000, he was with Philips Research Laboratories, Eindhoven, The Netherlands. In 2000, he joined Broadcom Netherlands, Bunnik, The Netherlands, where he has been involved in analog and mixed-signal IC design. He has published over 50 papers in technical journals and conference proceedings. He holds more than 35 U.S. patents in circuit design. He is the author of the book *Dynamic Translinear and Log-Domain Circuits* (Kluwer, 1999) and co-editor of the book *Research Perspectives on Dynamic Translinear and Log-Domain Circuits* (Kluwer, 2000).

Dr. Mulder was a co-recipient of the Jan van Vessem Award for Best European Conference Paper at ISSCC 2004.

David A. Johns (S'81–M'89–SM'94–F'01) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, Ontario, Canada, in 1980, 1983, and 1989, respectively.

In 1988, he was hired at the University of Toronto where he is currently a full Professor. He has ongoing research programs in the general area of analog integrated circuits. His research work has resulted in more than 80 publications as well as the 1999 IEEE Darlington Award. Together with academic experience, he also has spent a number of years in the semiconductor industry and was a co-founder of a successful IP company called Snowbush Microelectronics.

Dr. Johns has served as a guest editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and an associate editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS as well as being a member of the SSCS Adcom from 2002 to 2008. His homepage is located at http://www.eecg.toronto.edu~johns.