A Low-Power CT Incremental 3rd Order ΣΔ ADC for Biosensor Applications

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***Abstract*—This paper proposes a 3rd order single-loop continuous-time incremental sigma-delta analogue-to-digital converter (ADC) for time-multiplexed signals. Incremental sigma-delta modulation is used to address medium to high resolution requirements of multi-channel applications, while a 3rd order continuous-time implementation is investigated as an alternative for low-power solutions. A prototype of the proposed modulator, running at 320 kHz, has been fabricated in a 0.15-µm CMOS technology, while the synchronization circuitry to allow incremental operation was built on-board. Measurement results show that the ADC achieves 65.3 dB peak SNR, 64 dB peak SNDR and 68.2 dB dynamic range over a 2 kHz bandwidth. The modulator's power dissipation is 96 µW from a 1.6 V power supply. This translates into the best figure-of-merit when compared to recently published continuous-time alternatives, while being competitive with respect to state-of-the-art discrete-time counterparts.**

***Index Terms*—A/D conversion, incremental ΣΔ ADC, continuous-time.**

I. Introduction

MANY multi-channel sensor applications, such as biomedical acquisition systems for neuropotential signals [1], [2], require low power analogue-to-digital converters (ADCs) covering bandwidths from kilohertz to megahertz and resolutions in the range of 9 to 14 bits. These systems are generally integrated together with complex digital signal processing cores, which favors a sub-micron technology implementation. At the expense of more digital processing, sigma-delta (ΣΔ) ADCs take advantage of oversampling and noise shaping techniques in order to achieve high-resolution and relax the matching required between analog components, when compared to Nyquist counterparts. Unfortunately, traditional ΣΔ ADCs are dynamic systems with memory and, thus, they cannot be directly used in time-multiplexed environments. Incremental ΣΔ (IΣΔ) ADCs are, on the other hand, well suited for such type of applications, acting as high-resolution Nyquist-rate converters.

IΣΔ ADCs were introduced in [3] and have gained increased attention during last years [1], [2], [4]–[9], targeting medium to high-resolution multi-channel applications. In particular, high-order architectures are especially attractive from a power consumption perspective, as they reduce the number of cycles per conversion, N. While high-order loop-filter topologies have been used in discrete-time (DT) IΣΔ ADCs' implementations [2], [7], [8], only first-order topologies architectures have been proposed for continuous time (CT) IΣΔ ADCs' implementations [1], [9]. On the order hand, high-order CT topologies have been employed in several traditional ΣΔ ADCs [10], [11] to exploit their advantage in terms of power dissipation. This advantage stems from the absence of switches in a CT loop filter which relaxes the settling and bandwidth requirements of the active blocks, thus leading to a reduction in power consumption. Even though a sampling occurs at the output of the multiplexer (MUX) preceding a multi-channel ADC, CT IΣΔ ADCs would still be able to benefit from the CT advantages, as the loop filter processes each sampled input in a continuous-time fashion. So far, high-order CT IΣΔ ADCs have not been implemented but only been investigated in [12] for single-loop (SL) architectures and in [6] for cascaded counterparts. Compared to high-order DT IΣΔ ADCs [2], [7], [8], a CT implementation would benefit from the aforementioned advantages possibly leading to a low-power implementation. However, it would also impose difficulties which are not present in a DT implementation, such as wider integrators' coefficients spread and increased sensitivity to excess-loop-delay and jitter. Compared to first-order CT IΣΔ ADCs [1], [9], a high-order CT architecture would benefit from a lower N at a cost of increasing the complexity in both the CT loop filter and the digital filter. By reducing N, it would then be possible to decrease the required sampling frequency, possibly relaxing the integrators' bandwidth as well as the sensitivity to jitter. In this paper, a 3rd order single-loop CT IΣΔ ADC implementation is presented to evaluate the benefits of combining a high-order topology with a continuous-time approach and to demonstrate its feasibility for low-power time-multiplexed multi-channel applications. Although not treated in this publication, the proposed IΣΔ ADC could also serve as the groundwork to build high-order CT alternatives of more elaborated and power efficient structures, which employ the IΣΔ ADC as a building block [13]–[15]. The proposed CT IΣΔ ADC's target application is an acquisition system for electrocorticography (ECoG)-based brain-computer-interfaces (BCIs). BCIs capture brain's neuropotentials that reveal the user's intention to act or to communicate [16], [17], enabling individuals with motion impairments or communication disorders to restore such abilities. This capture can be made by means of either a non-invasive, when using electroencephalographic (EEG) activity, or an invasive method, when using ECoG activity or single-neuron activity within the brain. ECoG-based BCIs are particularly attractive since they impose less clinical risks than single-neuron recordings [18] while providing better spatial resolution and requiring less training than EEG counterparts. Specifically, the high-γ ECoG band ($40 - 180$ Hz)

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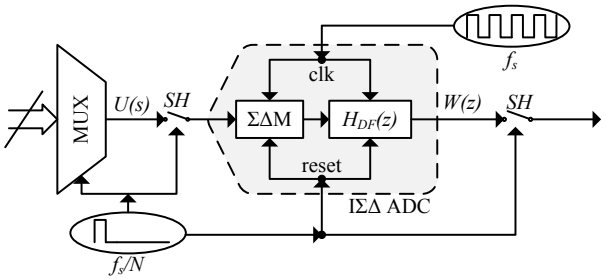

Fig. 1. Multi-channel SL IΣΔ ADC block diagram.

has received increased interest and has been used to decode movement direction [19] and semantic information [17]. The proposed ADC's targets the digital recording of such band with 12-bit resolution and 4 Ksamples/sec sample rate so as to cover 8-channels with 500 samples/sec per channel.

The paper is organized as follows. Section II provides the system level overview and describes the operation of the proposed IΣΔ ADC. The details of the modulator's circuit implementation are presented in Section III. Section IV describes the measurement setup along with the necessary on-board blocks to enable the incremental-mode of operation. Measurement results highlighting the performance of the proposed modulator and comparison with state-of-the-art counterparts are given in Section V. Finally, Section VI concludes the paper.

II. System Architecture

A. System Overview

A block diagram of an IΣΔ ADC in a multi-channel environment, together with the input channel multiplexor and the necessary sample and hold (SH) circuits is shown in Fig. 1. From a system level perspective, the main difference that distinguishes IΣΔ ADCs from traditional ΣΔ ADC counterparts is that they can be used in a multi-channel environment, processing time-multiplexed signals. This is obtained by resetting both the modulator's and the digital filter's states every time a new conversion takes place, and provides a one-to-one mapping between input and output. At the beginning of every conversion, the input signal of the selected channel, $U(s)$, is sampled and the modulator's states, as well as the digital filter, are reset. The signal is then hold for a period of N/f_s while the ADC performs the conversion at f_s frequency. The number of cycles, N, that the ADC runs can be seen as the equivalent of the oversampling ratio (OSR) in traditional ΣΔ ADCs. After N cycles have passed, a valid result is obtained from the output of the digital filter $H_{DF}(z)$ and a new conversion can take place.

Besides the advantage of being suitable for multi-channel environments, IΣΔ ADCs have some differences and limitations compared to traditional ΣΔ counterparts. The main limitation is that, as shown in [20], traditional ΣΔ ADCs have improved signal-to-quantization-noise (SQNR) performance with respect to equivalent IΣΔ ADCs in all situations but at very low OSRs. Differences in the design methodology include the digital filter realization, as shown in the following section, and stability considerations. As the modulator process a held input signal, its stability have to be assured by considering a DC input.

TABLE I
Coefficient values of the modulator shown in Fig. 2

c_1	7.0042	d_1	2
c_2	0.7137	d_2	1
c_3	0.354	d_3	-0.5
a_1	0.5	b_1	0.05

B. Design Methodology

The block diagram of the proposed CT IΣΔ ADC is shown in Fig. 2. A brief summary of the system level design for a 3rd order CT IΣΔ ADC [12] is provided here. In order to evaluate the advantages of a high-order CT architecture, a 3rd order loop filter has been chosen to reduce the number of necessary cycles, N. With respect to previous IΣΔ ADCs, only first order architectures have been implemented when using CT loop filters while up to third order have been proposed for DT IΣΔ counterparts. Furthermore, cascade-of-integrators in feed-forward (CIFF) configuration with input signal feed-forward has been used to relax the signal swing in the integrators path and minimize the performance degradation due to coefficient variations. With the exception of [7], this has been the preferred configuration for all other implementations and is specially attractive in this work due to the wide integrators' coefficient spread when employing a CT loop filter. All previous incremental implementations, but [2], have used a single bit implementation. At a cost of a less aggressive noise-transfer-function (NTF), a single-bit implementation has been chosen in this work as it minimizes the digital filter complexity and avoids the use of linearisation techniques in the feedback digital-to-analogue converter (DAC). In CT implementations, however, the use of a single-bit DAC will increase the sensitivity to jitter and excess-loop-delay (ELD), unless properly assessed. Accordingly, a switched-capacitor-resistor (SCR) [21] coding scheme with a mean lifetime value, τ, equal to $1/10\,\mathrm{T_s}$ is employed here so as to enhance the modulator's immunity to jitter and ELD.

The NTF was chosen using [22], and features an out-of-band gain (OBG) of 1.5 and all zeroes at DC. Furthermore, transient simulations were used to scale the loop filter coefficients and assure that all internal states are bounded between the input full-scale value, $\pm U_{\mathrm{FS}}/2$, and impulse invariant transformation (IIT) was used to perform continuous to discrete time (CTDT) transformations. The modulator's coefficients, assuming a normalized sampling rate of 1 ($T_S = 1$), are listed in Table I.

One particular difference of high-order CT IΣΔ ADCs with respect to DT IΣΔ ADCs is the design of the digital filter [12]. Although they employ the same principle, the use of a CT implementation with SCR feedback coding scheme will result in a different transfer function. As in DT implementations, the digital filter transfer function can be obtained by setting an upper limit of the ADC quantization error based on the bounded output of the last integrator. Accordingly, the digital

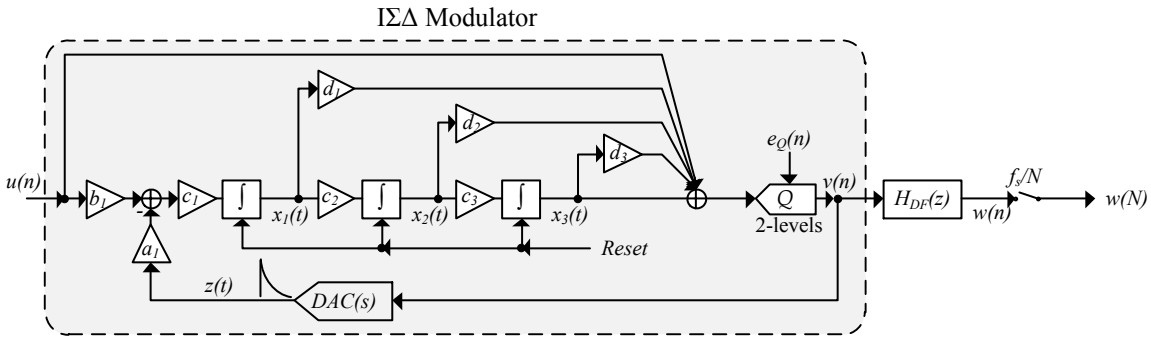

Fig. 2. Block diagram of the proposed SL CT IΣΔ ADC.

filter has been designed so that the ADC's quantization error is equal in magnitude to the DT equivalent of the last integrator's output, $x_3(n)$. Taking this into account, IIT has been used in order to design the digital filter and obtain the DT equivalent of $x_3(n)$ as well as the modulator's output, $v(n)$. The digital filter transfer function, $H_{DF}(z)$, that satisfies this requirement is given by:

$$H_{DF}(z) = \left(\frac{\alpha}{(z-1)} + \frac{\beta}{(z-1)^2} + \frac{\gamma}{(z-1)^3}\right) k \quad (1)$$

where

$$\alpha = \frac{1}{8}\left(8\,\tau^2\left(1 - \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right) - 4\,\tau + 1\right) \quad (2)$$

$$\beta = -\frac{1}{2}\left(2\,\tau\left(1 - \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right) - 2 + \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right) \quad (3)$$

$$\gamma = \left(1 - \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right) \quad (4)$$

$$k = \tau a_1\, c_1\, c_2\, c_3 \quad (5)$$

a_1, c_1, c_2 and c_3 are loop filter coefficients and τ is the mean lifetime value of the SCR-DAC. The least-significant-bit (LSB) quantization error can be found by considering that the ADC's quantization error is equal in magnitude to the DT equivalent of the last integrator's output, $x_3(n)$, at sampling times $n = N$. Accordingly, the LSB quantization error is obtained by scaling the output $x_3(N)$ to the ADC's full-scale input signal, $\pm U_{\mathrm{FS}}/2$. Its value, assuming a maximum range for $x_3(N)$ also bounded between $\pm U_{\mathrm{FS}}/2$, will be given by:

$$V_{LSB} = \frac{6\,U_{\mathrm{FS}}}{b_1\, c_1\, c_2\, c_3\, N^3} \quad (6)$$

where U_{FS} is the full-scale input signal and b_1 is a loop filter coefficient. From (6) the theoretical effective number of bits (ENOB) of the IΣΔ ADC, when a differential input signal with amplitude $\pm U_{\max}/2$ is considered, can be estimated as:

$$\mathrm{ENOB} = \log_2\left(\frac{U_{\max}}{V_{LSB}}\right) \quad (7)$$

As it can be appreciated from (7), setting the loop filter coefficients b_1 and $c_{1..3}$ to one would result in significant gainings. However, this transfer function does not lead to stable systems for single-bit modulators with order greater than two. This could be counteracted by the use of multibit quantizer, at a cost of more power due to the use of a flash ADC, linearisation techniques in the feedback DAC and more complex digital filter. This behaviour is similar to traditional ΣΔ counterparts, where a pure-differential NTF, $\left(1 - z^{-1}\right)^L$ for an L$^{\text{th}}$ order modulator, does not result in stable systems for single-bit modulators of order greater than two [23]. Put it in another way, for a linear model with a pure-differential NTF, the ENOB would increase proportionally to N^L, for an L$^{\text{th}}$ order architecture. However this increment will be deteriorated, in single-bit high-order IΣΔ ADCs by the use of a less aggressive NTF and the coefficients' scaling so as to assure stability.

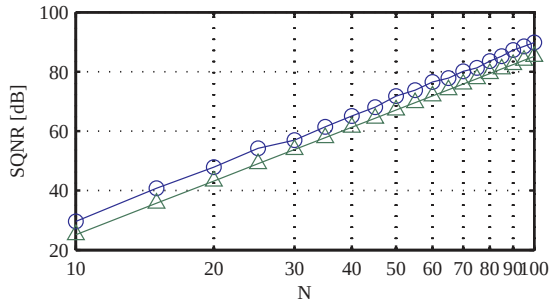

Fig. 3. Simulated SNDR of IΣΔ ADC (○), and theoretical SNDR derived from (7) (△) vs. number of cycles (N). Input signal power: $P_{sig} = -6$ dBFS.

As it is shown in Fig. 3, the theoretical SQNR derived from (7) is compared against system level simulations, when the number of cycles N is swept. It is worth to notice a slight difference between both traces, which stems from the fact that (6) takes into account a worst-case scenario while the quantization noise might be less than such value. These results were used to select a number of cycles N equal to 80 so as to provide considerable margin for performance degradation due to thermal noise and circuit non-idealities. In order to cover the required 2 kHz bandwidth, the proposed IΣΔ ADC is run at 320 kHz featuring a SQNR of around 83 dB at -6 dBFS which translates into a quantization level of -89 dBFS. Prior to the final circuit implementation, extensive simulations were performed at system level in Matlab/Simulink environment and at block level in Cadence using co-simulations with behavioral Verilog-A/Verilog-AMS models and transistor level blocks.

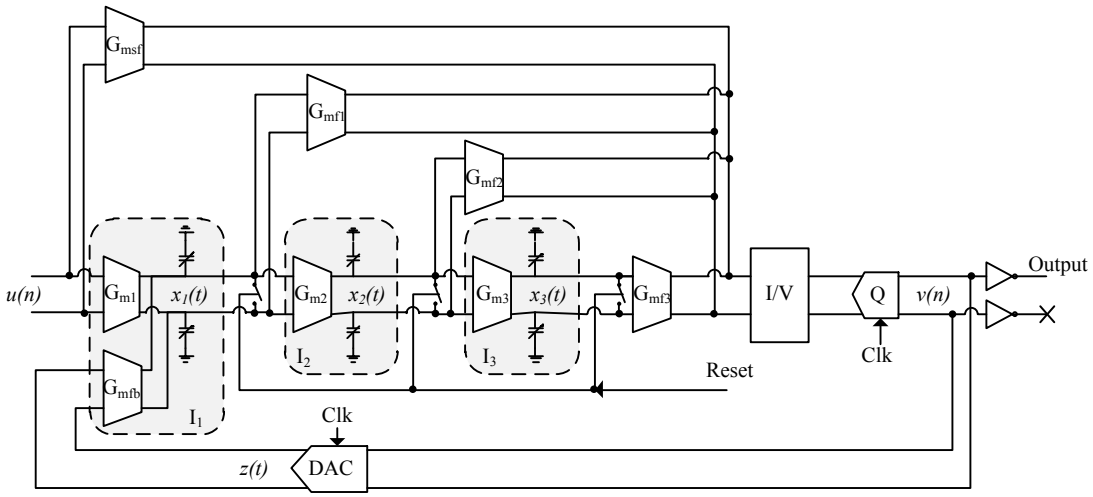

Fig. 4. Block diagram of implemented CT IΣΔ modulator.

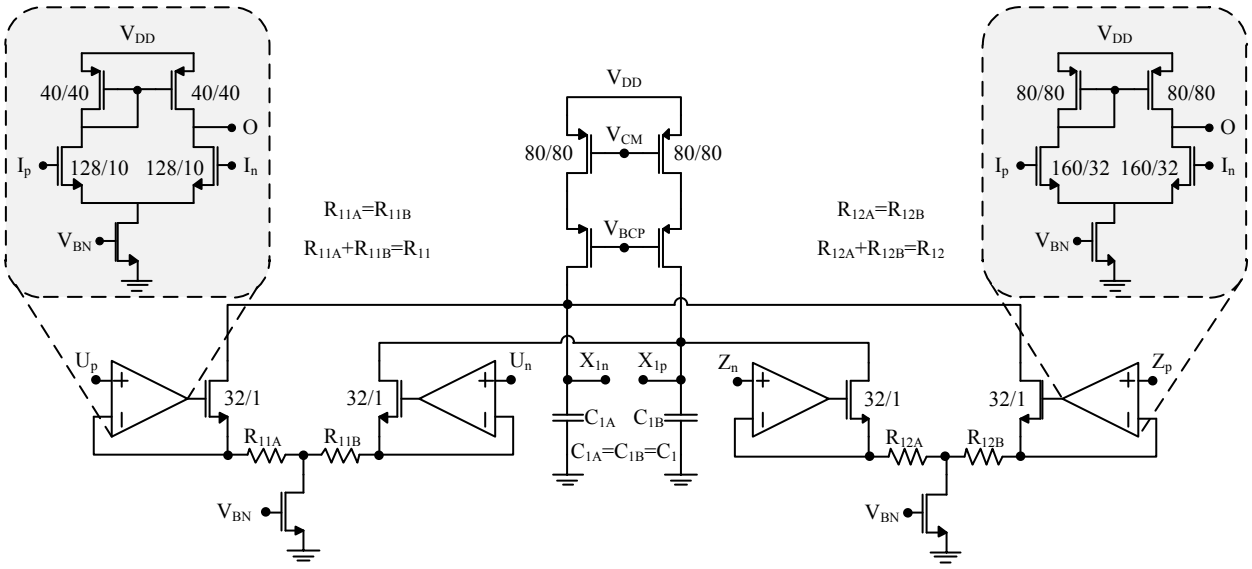

Fig. 5. Schematic of the first integrator.

III. Circuit Design and Implementation

The block diagram of the implemented IΣΔ modulator is shown in Fig. 4. The modulator was fabricated in a $0.15\ \mu\text{m}$ CMOS process, operating from a $1.6\ \text{V}$ supply voltage. The digital filtering is performed off-chip but has been synthesized and physically implemented so as to estimate its area and power consumption.

A. Loop Filter

The first integrator is one of the most critical blocks in the modulator as any non-ideality in this block will appear without suppression at the modulator's output [24]. Although active RC-integrators are generally preferred due to their high-linearity, the use of G_mC integrators has also been explored [25] [26] in order to reduce the modulator's power consumption. As shown in [25], G_mC integrators could potentially benefit from relaxed unity-gain bandwidth requirements in the G_m cell with respect to the OpAmp in a RC-integrator implementation, specially if driven by pulses from the SCR DAC. Moreover, the high input impedance of the G_m cell would also make this integrator easier to drive compared to RC-integrator counterparts. Taking this into consideration, a gain-boosted G_mC integrator was selected for the first stage in this implementation, showing sufficient performance to meet the target requirements.

1) First Integrator: Telescopic cascode structure sharing a PMOS cascode load was selected, as shown in Fig. 5, for both $G_{m\text{fb}}$ and G_{m1}, due to its lower noise and power consumption compared to folded counterparts. Each cell's transconductance is set by means of resistive source degeneration applied to their respective input differential pairs, thus, being approximately equal to $1/R_{11}$ and $1/R_{12}$ for the feed-forward and feedback cells, respectively. In order to enhance the circuit linearity, large transconductance transistors were used in the differential pair together with gain-boosting opamps. These transistors, as

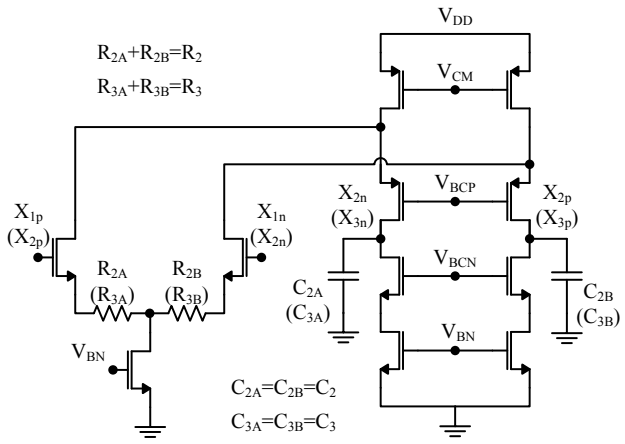

Fig. 6. Schematic of the second and third integrators.

well as the differential pair in the gain-boosting opamps, are operated in weak inversion having a large width-to-length ratio, (W/L). In order to minimize the noise contribution, single tail current sink is used, as its noise will appear at the outputs as common-mode noise and all PMOS loads' transconductance is reduced. The MOS devices flicker noise contribution is also minimized by using large length transistors.

One of the main drawbacks of telescopic structure is its reduced signal swing which, in this implementation, get worsened by the use of single tail current. However, thanks to the CIFF modulator's configuration, this is not an issue in this design, as the integrator's output signal swing is small enough to satisfy the linearity requirements. The DC gain of $G_{m\mathrm{fb}}$ and G_{m1} is 95 dB and 75 dB respectively, while having a total power consumption, including biasing, of $27.4\,\mu\mathrm{A}$.

2) Second and Third Integrators: Due to the noise-shaping characteristics of the loop filter, the requirements for the second and third integrators are relaxed with respect to the first integrator, accordingly, linearity and noise performance can be traded by lower power consumption. As shown in Fig. 6, these stages are implemented as folded cascode structures to accommodate a marginal signal swing increment of approximately 8% and 15% between the first integrator's output, $x_1(t)$, and the second and third integrators' outputs, $x_2(t)$ and $x_3(t)$, respectively. Moreover, resistive source degeneration is used, similarly to the first integrator, to set the transconductance to approximately $1/R_2$ and $1/R_3$ for the second and third integrator, respectively. Both integrators achieve a DC gain of approximately 70 dB, while consuming $5.8\,\mu\mathrm{A}$ and $4.6\,\mu\mathrm{A}$ respectively, including their biasing circuits.

3) Common-Mode Feedback: The integrators' common-mode feedback (CMFB) circuit is shown in Fig. 7. The common-mode input voltage in a G_m cell [27] can be obtained from the node C between the two source degeneration resistors and, in turn, be used to set the common-mode output voltage of the preceding stage. In this implementation, the common-mode voltages are sensed at the inputs of $G_{m\mathrm{f1}}$, $G_{m\mathrm{f2}}$ and $G_{m\mathrm{f3}}$. As gain boosting is not utilized in these stages, the voltage in node C will be approximately equal to $(V_{OP}+V_{ON})/2-V_{GS}$, inducing V_{GS} volts difference between the input voltage of the CMFB opamp, and the resulting common-mode voltage output. In order to counteract this effect, a level shifter has been introduced between the common-voltage set node, $V_{\mathrm{CM\_REF}}$, and the input of the CMFB opamp, $\mathrm{I_N}$. The dominant pole provided by the integrating capacitors is sufficient to ensure enough phase margin in the CMFB loop of the second and third integrators. In the first integrator, however, the phase margin is degraded by the input capacitance of the PMOS sources and a "crossover network" [28], formed by R_c and C_c, had to be added to effectively detach the amplifier from the feedback loop at high frequencies and maintain the loop stability.

4) Integrator's Constant Tuning: The capacitors employed in the loop filter are metal-insulator-metal (MiM) while high-resistivity polysilicon is used for the resistors. Characterization data from these components shows that the integrators' coefficients can suffer a maximum spread of approximately $\pm 40\%$. In order to counteract such deviation, each integrating capacitor is realized by a fix capacitor, C_{FIX}, plus a capacitor array [29], controlled by an externally supplied 4-bit binary word, $Ctrl\,[0\colon 3]$, as depicted in Fig. 8. The fix capacitor is composed by 16 C_{LSB} capacitors with the nominal value of the integrating capacitor set at the middle value of the array, $C_{\mathrm{FIX}} + 7\,C_{\mathrm{LSB}}$. This results in a tuning range and step [30] of $\pm 46.8\%$ and 4.3%, respectively, which is enough for a successful first-pass manufacturing. To minimize component mismatch, both C_{var} capacitors connected to the positive and negative output terminals are splitted in unit size elements which are randomly distributed in a matrix, surrounded by dummy elements. The capacitance value of the unit size elements for the second and third integrators is equal to C_{LSB} (869.5 fF), giving a total of 31 unit size elements per capacitor C_{var} and 62 capacitors in the array, which are arranged, together with two dummy elements, in a 8×8 matrix. As the capacitance value for the first integrator is two times the one used in the second and third integrators, two of the previous mentioned matrices are connected in parallel.

B. Feedback DAC

The implementation of the single-bit SCR feedback DAC [25], together with the feedback transconductance of the first integrator, $G_{m\mathrm{fb}}$, is depicted in Fig. 9. The operation of this DAC can be divided into two phases, the reset phase, which occurs on the clock's rising edge, Φ_1, and the exponential discharge phase, which occurs on the clock's falling edge, Φ_2.

1) In the reset phase, the right and leftmost plates of the bottom capacitor C_B are respectively connected to the common-mode input voltage V_{CM} and to $V_{\mathrm{DAC}} + V_{\mathrm{CM}}$, effectively sampling the voltage V_{DAC}. The top capacitor C_T is, in turn, discharged by connecting its plates to V_{CM}. Moreover, the DAC differential output driving the integrator's transconductance is set to zero by short-circuiting their terminals to V_{CM}.
2) At the beginning of the exponential discharge phase, the leftmost plate of C_T is connected to $V_{\mathrm{DAC}}+V_{\mathrm{CM}}$, hence, raising the voltage of node A to $V_{\mathrm{DAC}} + V_{\mathrm{CM}}$. The leftmost plate of C_B is, on the other hand, connected

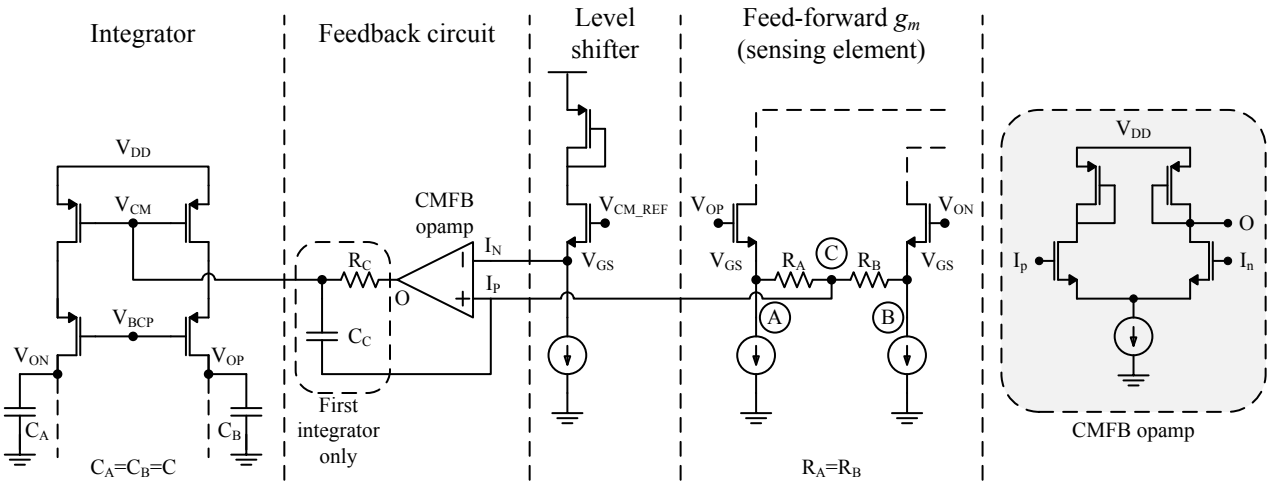

Fig. 7. Simplified CMFB circuit used in all integrators.

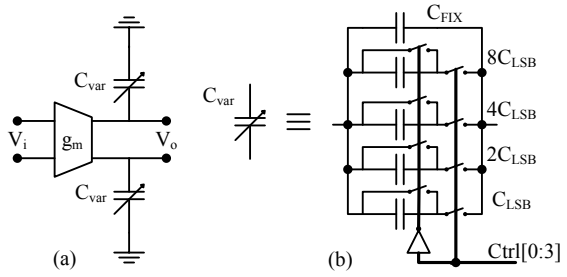

Fig. 8. Integrator's constant tuning. (a) G_mC integrator. (b) Tunable capacitor array.

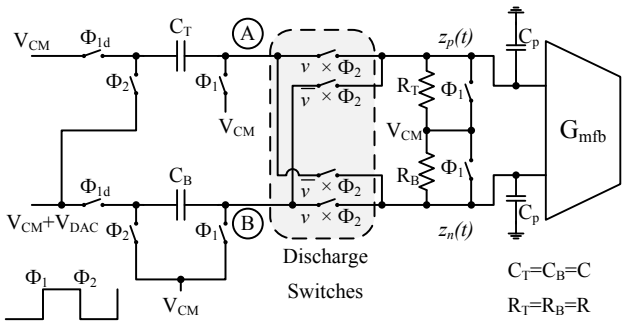

Fig. 9. SCR-DAC implementation and G_{mfb} block diagram of the first integrator.

to V_{CM}, lowering the voltage of node B to $V_{\mathrm{DAC}} - V_{\mathrm{CM}}$. Both capacitors are then discharged to V_{CM} via the top and bottom resistors. The polarity of such discharge, hence the polarity of the DAC output signal, $z_p(t) - z_n(t)$, will depend on the quantizer's output, v, which controls the four discharge switches.

The single-ended value of the discharge pulse will be influenced by both the on resistance, R_{on}, of the discharge switches and the parasitic capacitances of G_{mfb}, C_{p}, and it can be approximated as:

$$z_{\mathrm{SE}}(t) \approx V_{\mathrm{DAC}} \frac{C}{C + C_{\mathrm{p}}} \, \mathrm{e}^{-\frac{t}{(C+C_{\mathrm{p}})(R+R_{\mathrm{on}})}} \tag{8}$$

While the on resistance of the discharge switches is small compared to the discharge resistor, R, and can be disregarded, special attention has to be paid to the parasitic capacitance C_{p}. As the input transistors of G_{mfb} have been sized so as minimize flicker noise, their parasitic capacitance will load the DAC's output and, therefore, should be considered when calculating its pulse shape.

C. Current Summation and Quantizer

The current summation block, together with the quantizer are depicted in Fig. 10. The input signal feed-forward path plus the feed-forward coefficients, d_1 to d_3, are implemented using V/I converters by means of resistor degenerated G_m cells. The output scaled currents of these cells are added at the nodes A and B of the summation block. In this block, the cascode transistors M_{2a} and M_{2b} keep the voltage of node A and B constant, helping to increase the linearity of the G_m cells [31]. The added current is then folded and converted into voltage, through the active loads M_{3a} and M_{3b}, to drive the quantizer.

A dynamic latched comparator [32] is used to implement the quantizer. The decision circuit offers the advantage of low power dissipation, since there is no static current consumption, and low offset, as the dominant offset contribution is due to the input differential pair instead of the cross-coupled devices. Moreover, an SR-latch is used to keep the output stable over the full clock cycle. Time domain simulations show that its conversion time is significantly lower than the required time of $0.5\,\mathrm{T_S}$.

D. Digital Filter

As shown in Section II-B, one of the differences between traditional and incremental $\Sigma\Delta$ ADCs is the digital filter transfer function. Although the digital filter developed in (1)

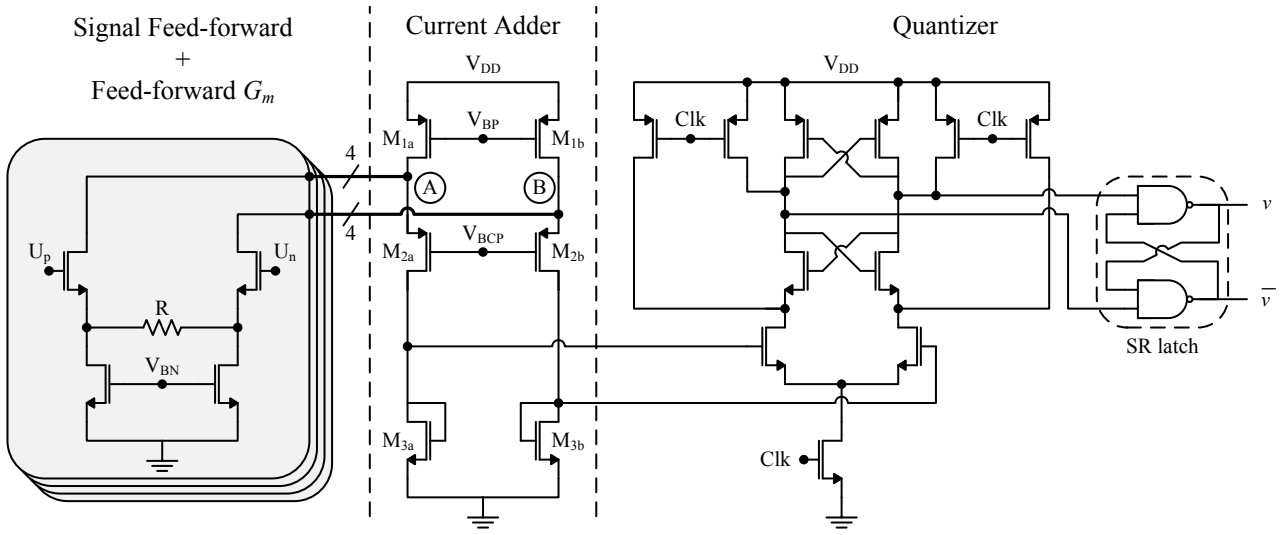

Fig. 10. Current summation and quantizer.

provides a good system level approximation, it does not take into consideration non-idealities that appear in circuit level implementation which results in a suboptimal solution. The design of an optimal filter for noise limited IΣΔ ADCs was mathematically derived in [33], and implemented in [2], for DT IΣΔ ADCs. In this work, optimization tools are employed as an alternative approach for the digital filter design, when considering the non idealities of the modulator's implementation. The digital filter matching the ideal analog transfer function given in (1) is a sum of cascade of integrators which process N samples coming from the ΣΔ modulator. This filter, when operating in transient mode, can instead be treated as a N-length finite impulse response (FIR) filter with the appropriate coefficients [34]. Recalling that the digital filter is active until a new reset occurs, at instant $n = N$, its output can be described by the difference equation $w(n) = k_0 v(n) + k_1 v(n-1) + \ldots + k_{N-1} v(n-N+1)$. Such difference equation is equivalent to the transfer function of an FIR filter of length N, input $v(n)$, output $w(n)$ and coefficients $k_0 \cdots k_{N-1}$. These coefficients can be obtained by computing the N-length impulse response of the transfer function in (1). So as to maximize the IΣΔ ADC's performance, the proposed method uses the MATLAB optimization algorithm *fmincon* [35] to find the optimum N coefficients of the FIR filter. Such algorithm attempts to find a constrained minimum of a scalar function (called the objective function) of several variables starting at an initial estimate. The coefficients obtained from (1) are then set as the initial estimate, while the variables to be optimized are the FIR coefficients. This approach uses as objective the inverse of the average improvement, in signal-to-noise-ratio (SNR), of the new filter with respect to the original one. The average SNR improvement is obtained from several measurements before the modulator is overloading. The optimized filter's impulse response agrees qualitatively with the results presented in [2], obtaining a performance improvement of $0.5\,\mathrm{dB}$ in the SNR and $1.3\,\mathrm{dB}$ in the signal-to-noise-plus-distortion-ratio (SNDR).

Although not fabricated, the optimized FIR filter has been synthesized and implemented at layout level in order to estimate its area and power consumption. Power aware design methodologies have been used from system level down to the physical implementation in order to obtain a digital filter with a marginal power contribution to the IΣΔ ADC. Post-layout simulation results show that the implemented FIR filter consumes $3.8\,\mu\mathrm{W}$ in 3071 gates, occupying a total area of $550 \times 330\,\mu\mathrm{m}^2$.

IV. Measurement Setup

The measurement setup used to characterize the ADC is shown in Fig. 11. This setup can be utilized to test the ΣΔ ADC in both the traditional mode of operation as well as in the incremental one. In order to operate it in the incremental mode, necessary blocks, such as a synchronization circuit and appropriate signal conditioning were built on-board, as described in the following subsection. An audio signal source (Agilent U8903A) with a SNDR better than $90\,\mathrm{dB}$ drives the test PCB. The required $320\,\mathrm{kHz}$ clock signal is generated by an arbitrary function generator. The output digital stream of the modulator is captured by a logic analyzer (Tektronix TLA614) with $65\,\mathrm{kB}$ memory depth. This stream is then imported into Matlab where it is filtered by the FIR filter of Section III-D. A fast-Fourier-transform (FFT) is performed using a Blackman window [36] to compute the performance metrics according to [37]. A custom Labview software setup has been created to control both the external audio source and the logic analyzer and perform the necessary amplitude and frequency sweeps for characterization.

A. Test board

A simplified block diagram of the PCB used to test the chip is shown in Fig. 11. Apart from the IΣΔ modulator DUT, the PCB has three main blocks: a signal source, a signal conditioning circuit and a synchronization circuit.

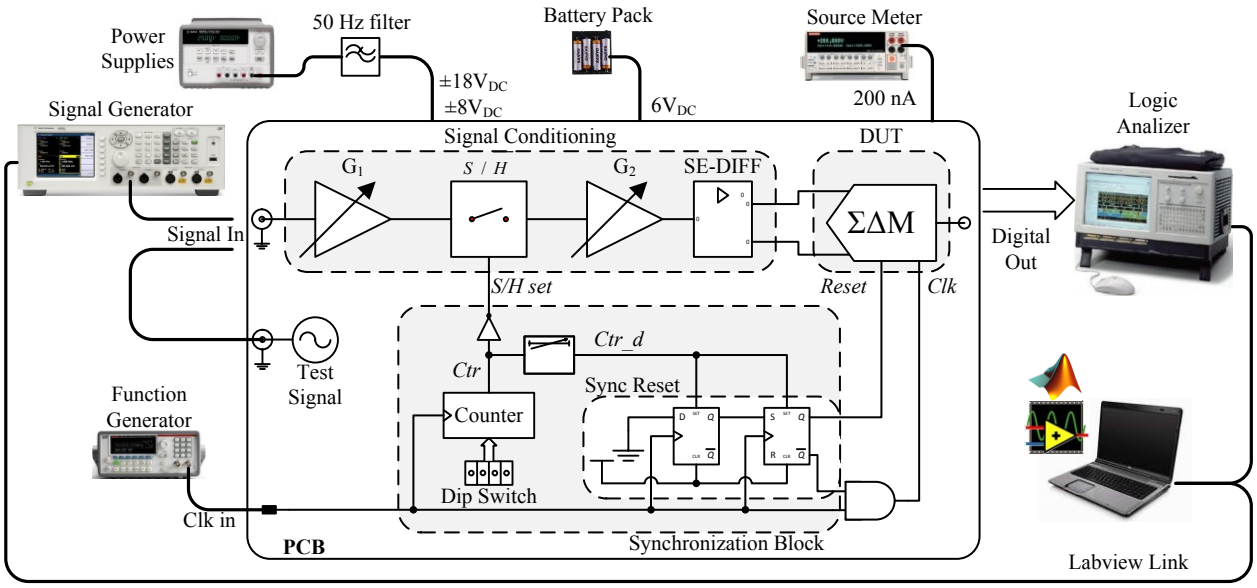

Fig. 11. Simplified block diagram of measurement setup.

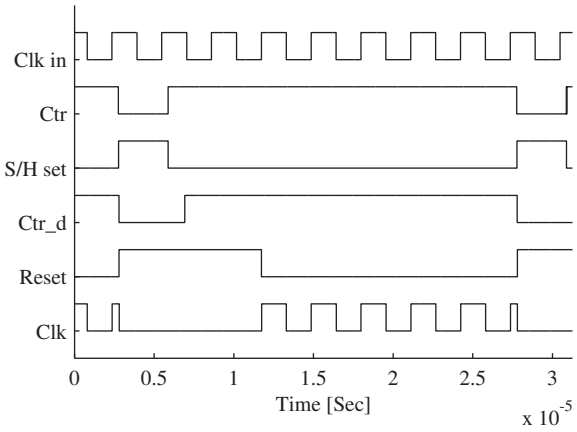

Fig. 12. Signals' timing measurement in synchronization block (counter dip-switch has been set to seven for clarity).

1) Test Signal Source: A sinusoidal signal source was implemented on the PCB in order to perform initial tests and to provide an alternative option to an external signal source. Such source is based on a modified version of a Wien-bridge oscillator which outputs a 3 V_{RMS} signal and features total-harmonic distortion (THD) better than 90 dB. The oscillation frequency is manually set by switching a capacitor bank.

2) Signal Conditioning: The purpose of this block is to sample-and-hold (S/H) the input test signal (*S/H* sub-block) and perform single-ended to differential conversion (SE-DIFF sub-block) while maintaining an adequate amplitude through the sub-blocks G_1 and G_2. Moreover, all components have been carefully selected so as to satisfy the characterization noise and distortion requirements. Each of these sub-blocks can also be bypassed, allowing the modulator not only to be tested in the proposed incremental mode of operation with and without S/H, but also in traditional mode.

3) Synchronization Circuit: As it can be appreciated from Fig. 1, in an IΣΔ ADC, the sample-and-hold, reset and clock signals need to be synchronized. Accordingly, a synchronization block, implemented with discrete logic, has been created for this purpose. A dip-switch selectable 8-bit binary down counter IC is driven by the ADC's clock and outputs a pulse every time the selected count has reached zero. As shown in Fig. 12, this pulse will, on the falling edge, asynchronously assert the reset signal and set the S/H into sample mode for one period. On the rising edge, the S/H enters into hold mode, but the modulator's reset signal is kept asserted, by means of a delay circuit, to give the held signal enough time to settle. Afterwards, the reset is deasserted synchronously through the reset synchronization block. During the reset period, the modulator's clock signal is inhibited which reduces the power consumption and aids to keep the resetted internal states undisturbed.

V. Measurement Results

An experimental prototype of the core 3rd order CT IΣΔ modulator has been fabricated in $0.15\,\mu\text{m}$ CMOS using six metallization layers. Fig. 13 shows the chip die photo of the IΣΔ modulator along with the test board. Excluding pads, the modulator occupies an area of $1.2\,\text{mm} \times 0.85\,\text{mm}$.

The measured output spectrum of a single-tone-test for a $-7.2\,\text{dBFS}$ input signal at $497\,\text{Hz}$, where $0\,\text{dBFS}$ refers to $0.7\,V_{pp}$, is shown Fig. 14. Up to approximately this amplitude, the thermal noise dominates over the harmonics level. For larger input amplitudes, distortion begins to becomes the limiting factor. The plot in Fig. 15 presents the measured SNR and SNDR versus the input signal amplitude at $497\,\text{Hz}$ showing a peak SNR of $65.3\,\text{dB}$ and a peak SNDR of $64\,\text{dB}$ @ $-3.3\,\text{dBFS}$. Moreover, the measured dynamic range (DR) is $68.2\,\text{dB}$. As shown in Fig. 16, similar SNR/SNDR characterizations have been performed for different frequencies over

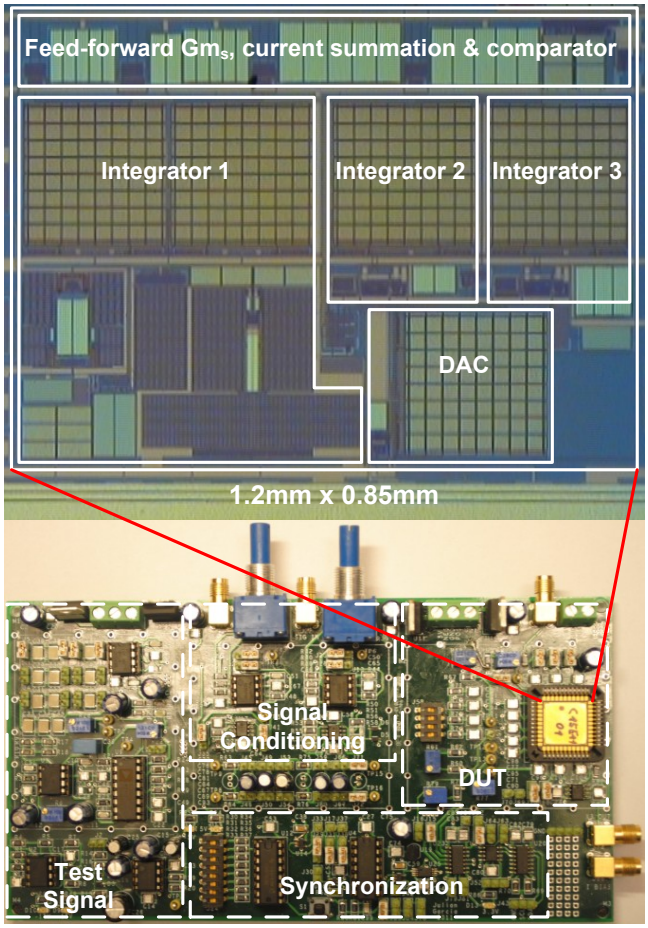

Fig. 13. Chip die photo and test board.

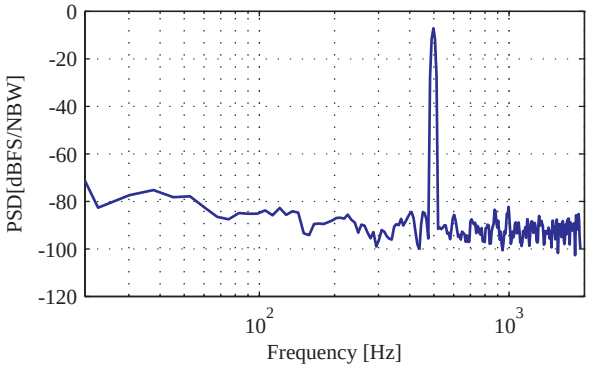

Fig. 14. Power spectral density plot for a -7.2 dBFS input signal @ 497 Hz.

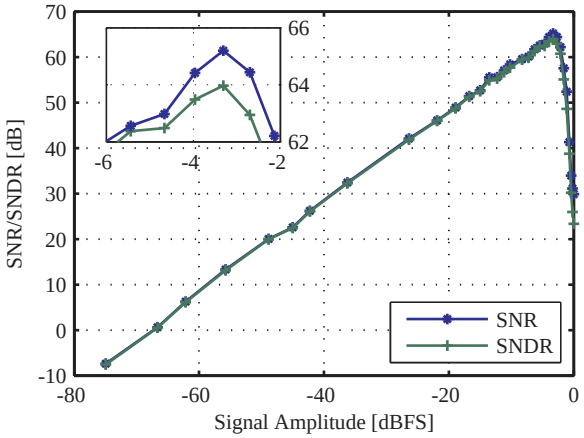

Fig. 15. Measured SNR and SNDR versus the input signal amplitude at 497 Hz.

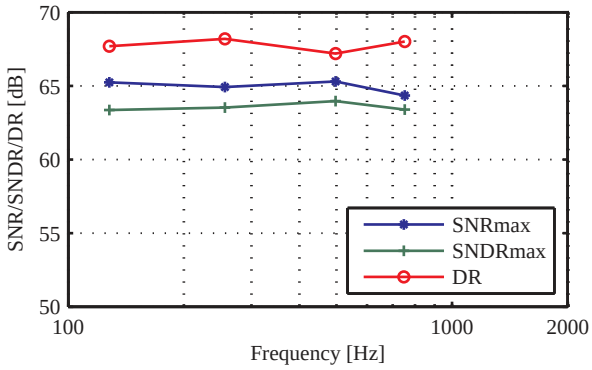

Fig. 16. Measured peak SNR and SNDR and DR over the bandwidth.

the bandwidth of operation while computing the peak SNR and SNDR, as well as the dynamic range. As it can be appreciated, the performance metrics suffer no significant degradation over the measured frequencies.

A summary of the measured performance is presented in Table II. The measured power consumption of the modulator, excluding output drivers, is 83 µW from the analog blocks, and 13 µW from the mixed-signal blocks and the clock distribution, which results in a total power dissipation of 96 µW from a 1.6 V power supply. According to post-layout simulations, 26.1 µA is consumed in the first integrator, 5.1 µA and 3.9 µA in the second and third integrators respectively, 12.7 µA in all four feed-forwards transconductances plus the summation circuit and 5.6 µA in the biasing circuits. The digital filter has an estimated power dissipation of 3.8 µW.

As it is possible to appreciate, there is an 18 dB performance drop between the ideal performance of the IΣΔ ADC (SQNR $\approx$ 83 dB), that is only limited by quantization noise, and the measured 65 dB SNR. Part of such degradation was anticipated before tape-out, obtaining 80 dB and 70 dB from Cadence transient simulations with and without transient noise activated, respectively. This translates into a 3 dB degradation when comparing the ideal performance against the performance when circuit level non-idealities, excluding devices' noise, are present. Moreover, a further 10 dB drop is caused by devices' noise, which was expected as the ΣΔ modulator was designed to operate in a power constrained environment, trading a higher device's noise for a lower current consumption. When comparing the achieved resolution with the post-layout, noise limited, simulation performance (SNR $\approx$ 70 dB), an unexpected 5 dB drop was found, mainly due to increment in the ADC's noise floor. Further inspection after tape-out revealed that devices' mismatches in the gain-boosting OpAmp's differential pairs of the feedback transconductance, $G_{m\mathrm{fb}}$, were most likely the main cause for such degradation. Under

TABLE II
MEASURED PERFORMANCE SUMMARY

Signal Bandwidth	2 kHz
Sampling Frequency	320 kHz
Dynamic Range	68.2 dB
peak SNR	65.3 dB
peak SNDR	64 dB
Power (Modulator)	96 µW
Supply Voltage	1.6 V
Technology	0.15 µm 1.8 V CMOS
Active Area (Modulator)	1.02 mm^2

TABLE III
SNDR VS. ADC'S BANDWIDTH

Signal Bandwidth [Hz]	Cycles	SNDR [dB]
2K	80	64
4K	40	60.3
8K	20	48.9

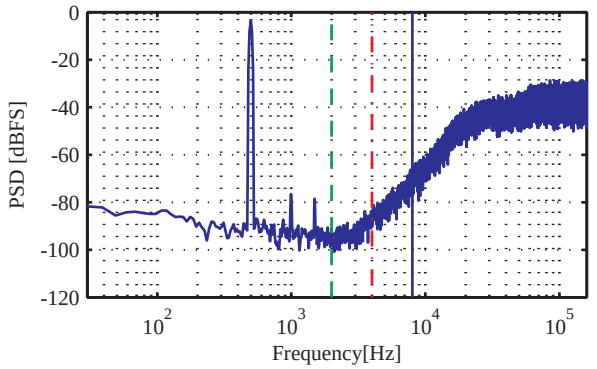

Fig. 17. Power spectral density of modulator's output operating in traditional mode for a −3.5 dBFS input signal @ 498 Hz. [Bandwidth references: (−−): 2 kHz, (−·−): 4 kHz, (—): 8 kHz].

mismatch conditions, the DC gain of the first integrator was significantly degraded, leading to an increment of the ADC's input referred noise both due to the devices' noise contribution as well as from noise induced through the power supply and biasing pins. As the process only allowed a maximum device length of 10 µm, each transistor (W/L = 160/32) in the aforementioned differential pair consisted of a stack of four transistors with W/L = 160/8, increasing, as a consequence, their layout and matching complexity.

One of the features of IΣΔ ADCs is their scalability in terms of bandwidth, resolution and power consumption [7], [9]. For the implemented IΣΔ ADC, scalability is presented by increasing the ADC's bandwidth at a cost of a reduction in performance. From Fig. 1, it can be seen that the sample rate of the ADC is given by the period of the reset signal, N/f_s, while the resolution depends on the number of cycles, N. As a consequence, one can trade bandwidth by resolution just by increasing or decreasing N. Table III shows the measured peak SNDR versus the ADC's bandwidth, from 2 kHz up to 8 kHz. The significant drop in performance when extending the bandwidth from 4 kHz to 8 kHz can be explained with the aid of Fig. 17, which shows a power spectral density (PSD) of the modulator operating in traditional mode, along with the different measured bandwidths. Here, it is possible to appreciate that, when extending the bandwidth from 4 kHz to 8 kHz, not only circuit noise but also quantization noise will degrade the ADC performance.

A performance comparison of recently published IΣΔ ADCs is given in Table IV. The figure-of-merit (FOM) used for comparison is given by:

$$\mathrm{FOM_{SNDR}} = \frac{\mathrm{Power}}{2 \times \mathrm{BW} \times 2^{\frac{\mathrm{SNDR}-1.76}{6.02}}} \tag{9}$$

where BW is the ADC's bandwidth. In order to obtain a fair comparison, only the modulator's power consumption has been taken into account in all cases, otherwise noted. The FOM of the proposed ADC, when covering a bandwidth of 4 kHz, has also been added to the comparison. As it can be seen, this modulator obtains the best FOM with respect to recent CT IΣΔ ADCs and a competitive FOM with respect to recently published DT IΣΔ ADCs, except for one mode of operation of the scalable IΣΔ ADC presented in [7]. It is worth to mention that only IΣΔ ADCs have been included in this comparison, thereby, excluding both traditional ΣΔ modulators and possible extensions or "enhancements" applied to IΣΔ ADCs [13]–[15]. While the groundwork has been presented, demonstrating the feasibility and competitive FOM of high-order CT IΣΔ ADCs for low-power multi-channel applications, several improvements could be introduced in order to enhance the proposed ADC performance in future implementations. From a system-level point of view, extended counting [13] or extended range [15] approach could be introduced to extend the ADC resolution and, as a consequence, to reduce the required number of cycles per conversion, N. Improvements at the block-level may include the use of a different DAC coding scheme, such as switched-capacitor-switched-resistor (SCSR) [38], which can obtain similar jitter immunity performance and may reduce the power consumption of the first integrator. Finally, from a circuit level perspective, state-of-art power conscious solutions, similar to [10] or [11], can be employed to further reduce the power consumption.

VI. CONCLUSION

An incremental ΣΔ ADC for neuropotential sensor applications has been designed and fabricated in a 0.15 µm CMOS technology. A 3rd order CT ΣΔ modulator has been employed to take advantage of low number of cycles per conversion and relaxed bandwidth requirements of the active blocks, thus, making it suitable for low-power multi-channel applications. The proposed CT IΣΔ ADC achieves an SNR/SNDR of 65.3/64 dB and a dynamic range of 68.2 dB. The modulator consumes 96 µW from a 1.6 V power supply while the digital filter consumes an estimated 3.8 µW. Comparison with state-of-the-art reveals that the ADC obtains the best FOM with respect to recent CT alternatives while being competitive when compared to DT counterparts.

TABLE IV
PERFORMANCE COMPARISON OF RECENT IΣΔ ADCS

	This Work[a]	This Work[b]	[8] JSSC	[2] CICC	[7][d] ISCAS	[7][d] ISCAS	[1] JBCAS	[9] ESSCIRC
Year	2011	2011	2006	2010	2010	2010	2009	2010
Implementation	CT	CT	DT	DT	DT	DT	CT	CT
BW (Hz)	2000	4000	7.5	21739	1670	1.67	1000	250
F_s (kHz)	320	320	7.68	10000	-	-	2048	512
SNR (dB)	65.3	61.7	-	83.7	89.9	86.5	-	-
SNDR (dB)	64	60	110.12[c]	81.5	88.9	84.7	56	58.95
Power (μW)	96	96	300[d]	6800	83	0.967	75.9	20
V_{DD} (V)	1.6	1.6	3	1.8	1.8	1.8	3.3	-
Technology (μm)	0.15 CMOS	0.15 CMOS	0.6 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS	0.5 CMOS	0.5 CMOS
FOM_{SNDR} (pJ/conv.)	18.5	14.7	76.3	16.1	1.09	20.6	73.6	55.2

[a] ADC covering 2 kHz bandwidth.
[b] ADC covering 4 kHz bandwidth.
[c] SNDR measurement not available. Approximation taken from INL measurements.
[d] Power consumption of decimation filter included in this design.
[e] Frequency scalable ADC. Performance metrics taken at both ends of its scalability.

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