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A Low-Power Delta-Sigma Capacitance-to-Digital Converter for Capacitive Sensors

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ABSTRACT This paper proposes a low-power delta–sigma capacitance-to-digital converter (CDC) for a capacitive sensor. The input of the capacitive sensor employs a zoomed-in technique with the offset capacitor to extend the input capacitance range. The proposed CDC uses a third-order switched capacitor delta–sigma modulator to provide a digital output, based on a cascade of integrators with a feed forward (CIFF) structure. The current-starved operational transconductance amplifiers (OTAs) are applied in the delta–sigma modulator's first integrator to improve the current efficiency and reduce the power consumption. An auto-zeroing technique is used in the OTAs to reduce their offset and noise. The circuit was implemented in a 0.18-μm CMOS technology and occupies an area of 0.496 mm^2. The measurable capacitance range of the CDC can be varied from 0 to 8 pF. In a measurement time of 0.8 ms, the delta–sigma CDC achieved a 12.7 effective number of bits while consuming 18.6-μA current from a 2-V supply voltage.

INDEX TERMS Capacitive sensors, delta-sigma modulation, low power.

I. INTRODUCTION

Capacitive sensors are designed to measure the electrical capacitance modulated by a physical or chemical parameter of interest [1], [2]. They are widely used in measurement and control systems such as pressure sensors, liquid sensors, and humidity sensors [3]–[6]. In these applications, it is important to have small capacitive sensors, which limits the measurable capacitance to below 1 pF. The ability to meet this limit requires a high accuracy interface circuit with a short measurement time. Several methods have been introduced for use in capacitive sensors [7]–[9]. A period modulation-based capacitive sensor interface converts the sensing capacitor to a time interval, which can be easily digitized using a simple digital counter. However, a high-frequency clock is needed to digitize the output time, which increases power consumption [7]. Pulse-width modulated capacitive sensors [8] have good linearity, low temperature, and short measurement time, but they provide low resolution. In [9], a differential successive-approximation (SAR) topology was employed in a CDC for capacitive pressure sensing. This achieved a high resolution; however, it included a differential SAR control logic and two binary-weighted DACs. With an increase in resolution, the capacitance of the binary-weighted DAC increased exponentially. This increase caused large power consumption, increase in the area of the capacitor, and significant mismatch issues.

This study proposes a low-power delta-sigma capacitance-to-digital converter (CDC) for capacitive sensors [10]. To increase the signal-to-quantization noise ratio, the designed CDC employs a three-order delta-sigma modulator based on a cascade of integrators with a CIFF structure. In contrast, the multi-stage noise shaping (MASH) modulators in [11]–[13] are vulnerable to mismatch effects. The current-starved operational transconductance amplifiers (OTAs) are applied in the delta-sigma modulator's first integrator to improve its current utilization and reduce power consumption and an auto-zeroing technique is adopted for the OTAs to reduce the offset and noise. The combination of these techniques enables the proposed CDC to achieve high resolution and low-power consumption and makes it very suitable for capacitive sensor applications.

The remainder of this paper is organized as follows. Section II describes the operating principle of the capacitive sensor. Section III discusses the architecture of the CDC. Section IV provides a detailed description of the circuits used in the CDC. Section V presents the measurement results of the chip, and Section VI concludes the paper.

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II. CAPACITIVE SENSOR

Fig. 1 shows the block diagram of the capacitive sensors studied in this paper. It consists of a CDC, a timing and control module, and three on-chip capacitor arrays comprising the sensing capacitor C_X, the reference capacitor C_{ref}, and the offset capacitor C_{off}.

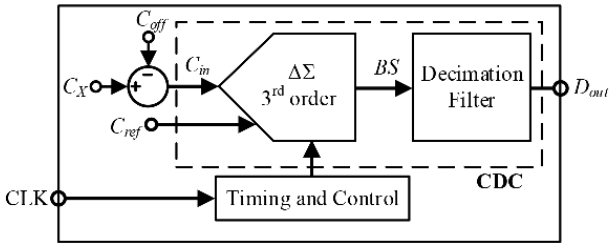

FIGURE 1. Block diagram of the capacitive sensor.

Because the sensing capacitor C_X may have a large baseline value, the variable capacitance modulated by physical or chemical parameters of the capacitive sensor is very small. To overcome this obstacle, Xia and Nihtianov [14] proposed a ''zoom-in'' technique in which an offset capacitor C_{off} is used to subtract the baseline capacitance from the sensing capacitor C_X to extend the input capacitance range and largely relax the dynamic-range requirements for the CDC. Therefore, the effective input capacitor C_{in} of the CDC can be expressed as

$$C_{in} = C_X - C_{off}. \tag{1}$$

In this work, the offset capacitor C_{off} can be programmed digitally from 0.032 pF to 8.160 pF in steps of 0.032 pF (C_b) by an 8 bits switched array, as shown in Fig. 2.

Then, the CDC digitizes the input capacitor C_{in} with respect to the reference capacitor C_{ref}, and produces a bitstream BS whose bit-density is proportional to the ratio of C_{in} and C_{ref}. According to [15], the bit-density can be expressed as

$$\mu = \frac{C_{in}}{2C_{ref}} + \frac{1}{2}. \tag{2}$$

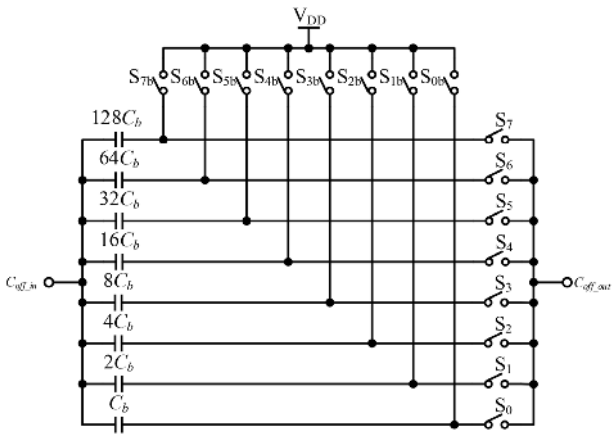

FIGURE 2. The offset capacitor array.

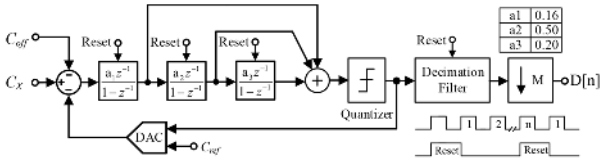

FIGURE 3. Simplified architecture of the CDC.

Finally, a decimation filter converts the bitstream into a digital number D_{out}. This digital number represents the relative input capacitor. The necessary timing for the CDC to ensure normal operation of the entire system is provided by the timing and control module.

III. SYSTEM ARCHITECTURE

The simplified architecture of the CDC is shown in Fig. 3. It comprises a third-order CIFF delta-sigma modulator and a decimation filter. The proposed modulator is an incremental delta-sigma modulator, which is particularly used to accurately convert narrowband signals [16]. All memory elements are reset at the beginning of each conversion cycle. Then, the input capacitor is applied to the input of the CDC for the first n clock cycles and the output signal will be derived after the first n clock cycles. Considering the influence of various non-ideal factors on circuit performance, a high-performance fourth-order sinc^4 filter is used to provide adequate noise suppression [17]. Its transfer function of the filter is given by

$$H(z) = \frac{1}{M^4}\left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^4, \tag{3}$$

where M is the decimation ratio.

The CDC was modeled using the delta-sigma toolbox in MATLAB. The design procedure can be found in the following steps:

–First, choose the delta-sigma modulator order, structure, and order of the sinc filter. In this work, the CDC employs a third-order CIFF delta-sigma modulator, the sinc filter is fourth-order, and the sampling frequency is 250 kHz.

–Second, find the required number of cycles. The required minimum oversampling ratio (OSR), i.e., the number of clock cycles, is 93 for a third-order modulator to achieve 13-bit resolution [18].

–Third, simulate the whole system in MATLAB and check the achievable resolution.

–Fourth, if the required resolution is not achieved, increase the number of clock cycles until the desired resolution is achieved.

Considering some non-ideal factors, a modest number of clock cycles to achieve 13-bit resolution was 200 in this work. Dynamic-range scaling was performed to ascertain the modulator coefficients (shown in Fig. 3) that would prevent overloading of the integrators and quantizers and achieve the required resolution.

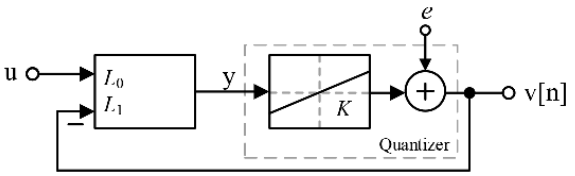

FIGURE 4. Generic representation of a high-order modulator.

A generic block diagram of a third-order (high-order) modulator is shown in Fig. 4 [19], where u is the modulator input, v[n] is the modulator output, y is the quantizer input, and e represents the quantization error of the modulator. In this block diagram, the quantizer (assuming it is not overloaded and it is busy, so that e is uniform) was modeled as a system with gain K.

The term $L_1(z)$ is expressed as

$$L_1(z) = \frac{a_1(z-1)^2 + a_1a_2(z-1) + a_1a_2a_3}{(z-1)^3}. \tag{4}$$

Therefore, the noise transfer function is derived as follows:

$$\mathrm{NTF}(z) = \frac{1}{1 + KL_1(z)}. \tag{5}$$

According to the small signal analysis, the high-order modulator can be seen as a negative-feedback system. Therefore, the system's open loop transfer function can be expressed as follows:

$$\mathrm{OTF}(z) = K\frac{a_1(z-1)^2 + a_1a_2(z-1) + a_1a_2a_3}{(z-1)^3}. \tag{6}$$

Fig. 5 shows the loci of the roots as K falls from infinity to zero. As the gain decreases to $K = 2.6$, the system becomes unstable. Therefore, the gain K of the quantizer must be greater than 2.6 to ensure stability.

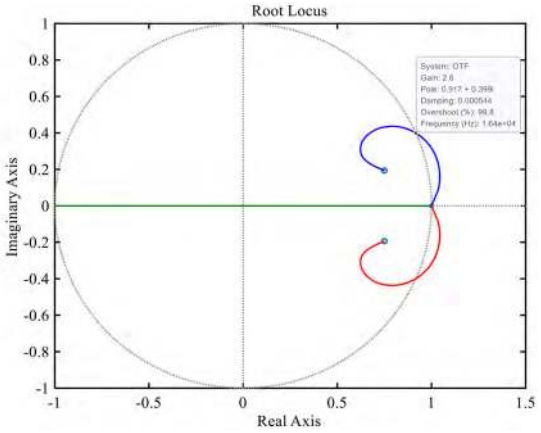

FIGURE 5. Root locus plot.

Fig. 6 shows the simulated signal-to-noise and distortion ratio (SNDR) curves of the third-order modulator. The peak SNDR is 84.2 dB. Compared with the traditional modulator (e.g., first-order), the higher order would achieve a high

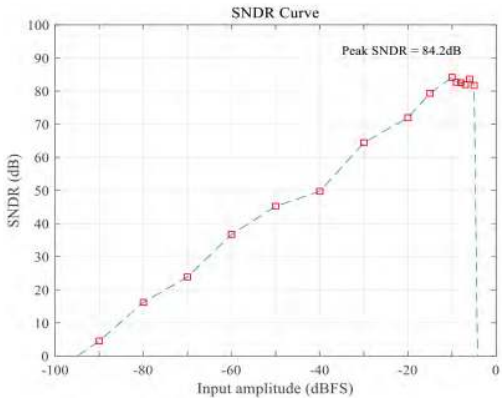

FIGURE 6. Simulated SNDR curves.

peak SNDR. However, the usable input range for a first-order modulator is $\pm C_{ref}$, which further decreases to $\pm$ 0.67 C_{ref} for a third-order modulator. A DC gain of at least 70 dB is required in the first integrator [20].

IV. CIRCUIT DESIGN AND IMPLEMENTATION

The third-order CDC was designed in a standard 0.18 μm CMOS process. Fig. 7 illustrates a switched-capacitor implementation of the CDC. Because the input to the CDC is a sequence, the modulator has to be more easily realized using discrete-time circuitry as compared with continuous-time circuitry [21].

To diminish the harm caused by the common-mode voltage of the sensors and achieve high accuracy, a fully differential circuit topology is used in this work. The sensing capacitors C_{X1} and C_{X2} directly serve as the sampling capacitors of the first integrator. The programmable offset capacitors C_{off1} and C_{off2} are cross-coupled to the sensing capacitor such that the effective input capacitance of C_{in} in the first stage is $C_X - C_{off}$. Under the control of two pairs of non-overlapping clocks signal S_1, S_{1d}, and S_2, S_{2d} in the delta-sigma cycle, these capacitors are switched between common-mode (CM) voltage (V_{CM}) and supply voltage (V_{DD}).

The reference capacitor C_{ref} is set to 0.4 pF. At this moment, the bit-density μ can be expressed as

$$\mu = \frac{\frac{1}{2}\left(C_{X1} - C_{off1} + C_{X2} - C_{off2}\right)}{2C_{ref}} + \frac{1}{2}. \tag{7}$$

Because the proposed CDC is implemented using the switched-capacitor modulator, the mismatch mainly originates from capacitor mismatch, which will reduce accuracy. Owing to the manufacturing errors and process factors, this is almost unavoidable. One method to overcome this is restricting the integrator output swings to decrease the influence; thus, the gain errors resulting from mismatch may be less obvious.

A. AUTO-ZEROING TECHNIQUE

In capacitive sensors, the major power consumption is due to the integrators of the CDC because the capacitor array

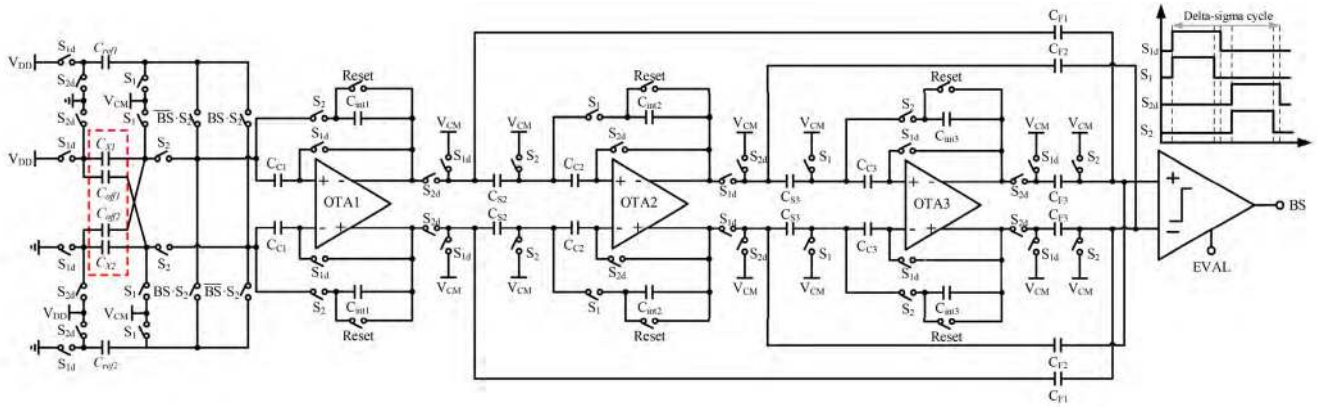

FIGURE 7. Circuit diagram of the CDC.

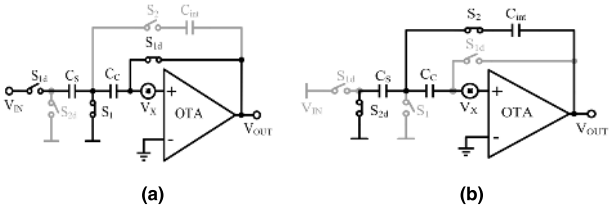

FIGURE 8. Operation of the first-stage integrator of the CDC. (a) Auto-zeroing phase, (b) integration phase.

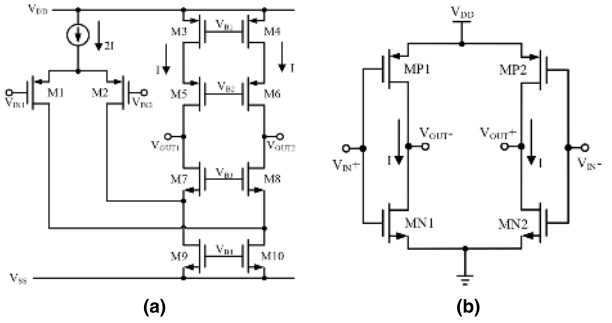

FIGURE 9. Circuit diagrams of two OTA types: (a) folded-cascode OTA, (b) inverter-based OTA.

does not consume static power. The integrators of the CDC are implemented in a switched capacitor. Fig. 8 shows the operation of the first-stage integrator (to simplify the analysis, it shows only half of the differential signal path).

To cancel the offset as well as the dynamic offset, V_X, an auto-zeroing technique is applied in these integrators [22]. In the auto-zeroing phase (Fig. 8a), the OTAs are configured in a unity-gain mode. The sensing capacitor C_X is connected to the power supply V_{DD}, and the capacitor C_C is charged simultaneously. At the end of the auto-zeroing phase, the charge on the capacitor C_C is

$$Q_1 = (V_{DD} - V_X(t_1))\, C_c. \tag{8}$$

In the integration phase (Fig. 8b), the charge is transferred from the capacitor C_C to the integrator capacitor C_{int}; therefore, the charge on the integrator capacitor C_{int} is

$$Q_1 = (V_{DD} - V_X(t_1) + V_X(t_2))\, C_c. \tag{9}$$

If the offset and noise V_X have no significance change during the auto-zeroing phase and integration phase, such that $V_X(t_1) = V_X(t_2)$, then the offset and noise will be eliminated, and this will improve the accuracy of the CDC.

B. CURRENT-STARVED CASCODED INVERTER-BASED OTA

The power consumption of a switched-capacitor integrator is usually dominated by the OTAs. Therefore, energy-efficient OTA implementation is a key for the overall energy efficiency of the CDC. Fig. 9 shows the circuit diagrams of two OTA types: the folded-cascode OTA [23] and inverter-based OTA [24].

In order to compare the current efficiency between the folded-cascode OTA (Fig. 9a) and the inverter-based OTA (Fig. 9b), the current-efficiency factor γ of an OTA is defined [25]:

$$\gamma = \frac{g_m}{I_{total}}, \tag{10}$$

where g_m is the transconductance of the OTA and I_{total} is the total current consumption of the OTA. Therefore, the current-efficiency factor γ_F of the folded-cascode OTA is

$$\gamma_F = \frac{g_m}{4I}. \tag{11}$$

In the inverter-based OTA, all the MOS transistors are biased in the sub-threshold region to realize ultra-low power consumption. The input differential pair transistors share the same bias current. Thus, the current-efficiency factor γ_C is

$$\gamma_C = \frac{g_{m,N} + g_{m,P}}{2I}, \tag{12}$$

where $g_{m,P}$ and $g_{m,N}$ are the transconductances of the inverter-based OTA when the input differential pair is PMOS or NMOS, respectively.

According to the above equations, the current-efficiency factor of the inverter-based OTA γ_C is four times better than that of the folded-cascode OTA once the transconductance $g_{m,P} = g_{m,N} = g_m$.

However, the inverter-based OTA is prone to process, voltage, and temperature (PVT) variations and has a poor

TABLE 1. Properties of the OTAs.

Item	Folded-cascode OTA	Inverter-based OTA
Low-power voltage	-	+
Power efficiency	-	+
DC gain	+	-
CM input range	-	+
Output swing	-	+
CMRR	+	-
PSRR	+	-

-: poor, +:good.

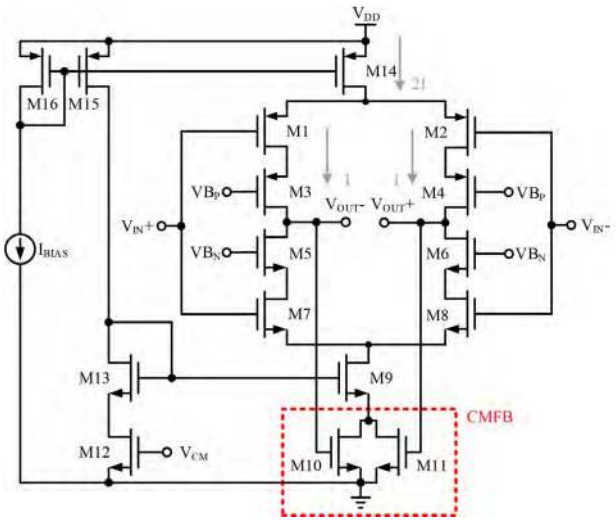

FIGURE 10. Current-starved cascoded inverter-based OTA with CMFB.

common-mode rejection ratio (CMRR), DC gain, and power supply rejection ratio (PSRR) [26]. Table 1 summarizes the properties of the folded-cascode OTA and inverter-based OTA. The properties clearly show that inverter-based OTA is the most attractive candidate for a low-voltage, low-power design.

To circumvent the above problem, this paper employs a current-starved cascoded inverter-based OTA with a common-mode feedback (CMFB) amplifier, as shown in Fig. 10.

The proposed OTA employs a cascoded structure (M3/M5 and M4/M6) to increase the OTA output impedance and improve the DC gain. Two differential cascoded inverters share a tail current source (M14 and M9) to increase the PVT tolerance and improve PSRR. However, the finite output impedance of the tail current source will limit the CMRR and reduce the output range. Such trade-offs require careful design of the circuit to reach an acceptable compromise.

Certainly, the CMFB amplifier is an indispensable component of the fully differential OTA in terms of stabilizing the output CM voltage. The traditional CMFB amplifier is a switched-capacitor CMFB amplifier. It does not limit the output swing of the OTA; however, there are four capacitors, which simplify the production of capacitor mismatch affecting the final CM output voltage. Additionally, more

TABLE 2. Prototype design data of OTAs (W/L in microns).

Instance	OTA1		OTA2		OTA3	
Name	W/L	M	W/L	M	W/L	M
M1,2	1.5/0.5	24	2.5/1.0	10	1.5/1.0	8
M3,4	4.0/0.5	32	2.5/1.0	12	1.5/1.0	14
M5,6	3.0/0.5	30	2.5/1.0	12	1.5/1.0	12
M7,8	2.0/0.5	26	2.5/1.0	4	1.5/1.0	2
M9	0.8/1.0	16	0.5/2.0	4	0.4/2.0	4
M10,11	0.4/5.0	8	0.22/20	2	0.22/20	2
M12	0.4/5.0	1	0.22/20	1	0.22/20	1
M13	0.8/1.0	1	0.5/2.0	1	0.4/2.0	1
M14	0.3/3.0	64	0.3/10	12	0.3/10	8
M15	0.3/3.0	4	0.3/10	3	0.3/10	2
M16	0.3/3.0	1	0.3/10	1	0.3/10	1

TABLE 3. OTA performance.

Item	OTA1	OTA2	OTA3
DC gain (dB)	78	81	83
Phase margin (deg)	82	80	80
Gain bandwidth (MHz)	12.5	2.5	2.7
Current (μA)	12	0.6	0.3
Load capacitance (fF)	2550	510	240

switches exist in the circuit. These introduce effects such as clock feedthrough and charge injection, which will damage the dynamic performance of the circuit; thus, the design requirements are harsh on the switches. Herein, the output CM voltage is held constant by the simplest CMFB amplifier. It comprises a differential pair, the current source of which comprises two transistors (M_{10} and M_{11}) in the linear region. Their drains are connected to cancel the differential signal, and the gates connect to the output. Obtaining an output voltage in the middle requires a large gate-source voltage ($V_{GS10,11}$). Therefore, it should a have small drain-source voltage ($V_{DS10,11}$) to not induce a large voltage drop. Conversely, transistors in the linear region are very linear; thus, it avoid the reduction of differential gain resulting from feedback.

The three integrators of the CDC have been implemented using the proposed OTA. Table 2 shows the size of the main transistors of the OTAs in the CDC. The bias current I_{BIAS} in the circuit is 200 nA. The performance of the proposed OTAs is summarized in Table 3, which is well above the requirement of the integrators in the CDC.

C. QUANTIZER

Fig. 11 depicts the circuit of the comparator (1-bit quantizer). The comparator comprises a preamplifier and a dynamic SR latch [27]. The EVAL (active low) is the clock signal of the comparator. This arrangement prevents kickback to the output of the third integrator. Table 4 shows the main component values of the comparator. The simulation result shows that the current consumption of the comparator is about 0.4μA.

V. MEASUREMENT RESULTS AND DISCUSSION

The proposed CDC circuit has been implemented in a standard 0.18 μm CMOS chip with an active area of

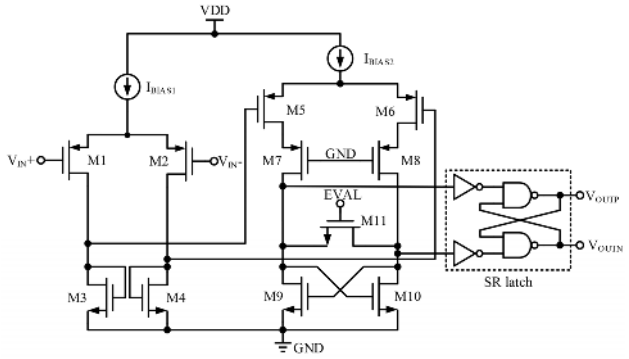

FIGURE 11. Comparator.

TABLE 4. Transistor dimensions of the comparator (W/L in Microns).

Instance Name	W/L	M
M1,2	15/0.25	1
M3,4	20/0.50	1
M5,6	15/0.25	1
M7,8	1.125/0.18	1
M9,10	6.75/0.18	1
M11	0.865/0.18	1

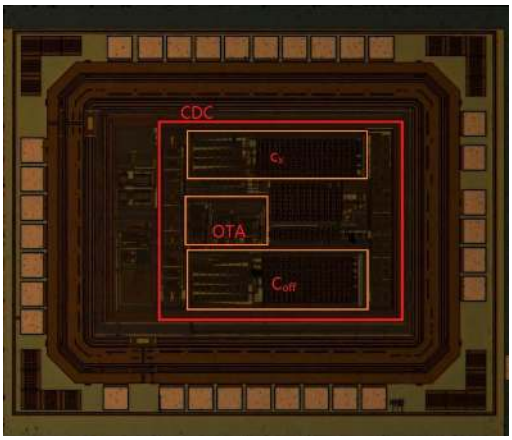

FIGURE 12. Chip micrograph.

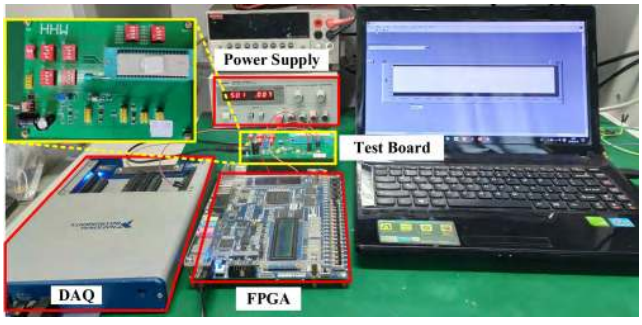

FIGURE 13. The measurement system setup.

0.496 mm^2 (Fig. 12). The chip consumed 18.6 μA current from a 2 V supply voltage.

Fig. 13 shows the measurement system setup, which is composed of a test board DAQ (National Instruments Data Acquisition), an FPGA (Altera DE2-115 Board), and a DC power supply (Agilent E3620A). An Altera DE2-115 board

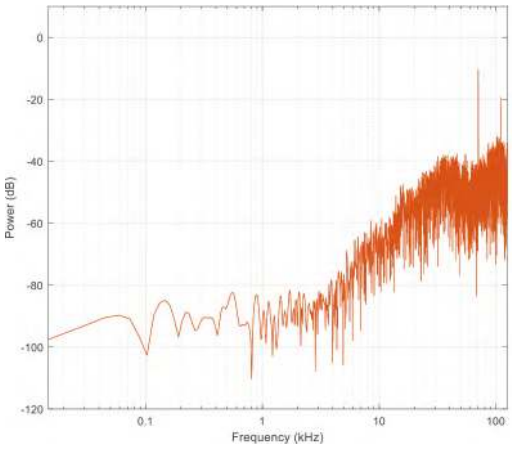

FIGURE 14. Measured spectrum of the bitstream (FFT of 2^{14} points).

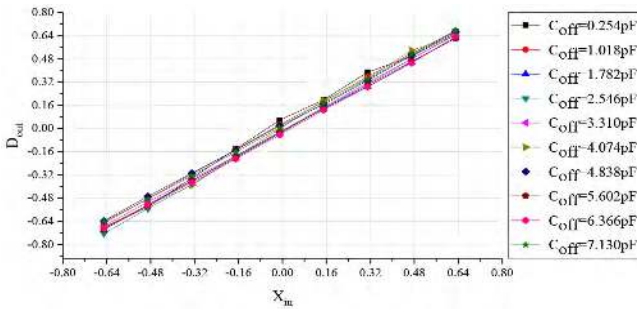

FIGURE 15. Measured digital output curve for different settings of the offset capacitors.

was used to provide the necessary timing for the CDC circuit to ensure normal operation of the entire system.

Fig. 14 presents the measured spectrum of the bitstream, demonstrating the third-order noise-shaping characteristic of the modulator. The proposed CDC achieved a resolution of 12.7 bits in a 0.8 ms measurement time.

To simplify the analysis, the equivalent input factor of the CDC is defined as

$$X_{in} = \frac{C_{in}}{C_{ref}}. \tag{13}$$

In this work, the equivalent input factor is designed from -0.65 to $+0.65$. Therefore, the effective input capacitor C_{in} is in the range of ± 0.26 pF as the reference capacitor C_{ref} is set to 0.4 pF. By programing the offset capacitor array C_{off}, the measurable capacitance range of the CDC can be varied from 0 pF to 8 pF. Fig. 15 shows the measured digital output D_{out} curve of one of the chips for different settings of the programmable offset capacitor.

The reported figure-of-merit (FoM) normalizes the energy consumption per measurement to the CDC's effective number of bits (ENOB), which can be calculated as

$$\text{FoM} = \frac{P_{power} \times T_{measurement}}{2^{\text{ENOB}}}, \tag{14}$$

where P_{power} and $T_{measurement}$ are the total power consumption and measurement time of the CDC, respectively. This FoM normalizes the energy consumption by dividing energy

TABLE 5. Performance summary of the delta-sigma CDC and comparison with other state-of-the-art devices.

Item	[7]	[8]	[24]	[28]	[29]	This Work
Year	2012	2013	2012	2014	2017	2019
CMOS Technology	0.35 µm	0.32 µm	0.35 µm	0.18 µm	0.35 µm	0.18 µm
Die area (mm^2)	0.51	0.52	2.6	0.2	6	0.496
Supply voltage (V)	3.3	3	3.3	1.6–2.0	3.3	2.0
Current consumption (µA)	64	28	4500	50	230	18.6
Architecture[1]	PM	PWM	3rd order ΔΣ	2nd order ΔΣ	3rd order ΔΣ	3rd order ΔΣ
Output data rate (kHz)	N.A.	N.A.	1250	512	200	250
Number of clock cycles	N.A.	N.A.	25	256	2000	200
Capacitance range (pF)	0–6.8	0–0.256	8.4–11.6	0.5–3.5	6–22	0–8
Measurement time (ms)	7.6	0.38	0.02	1	10.5	0.8
ENOB (bits)	13.5	6.8	13.8	14	16.7	12.7
FOM (pJ/Step)	139	283	20.9	4.91	74	4.47

[1] ΔΣ = delta-sigma modulation, PWM = pulse-width modulation, PM = period modulation.

consumption with the effective number of conversion steps. The ENOB is defined as

$$\text{ENOB} = \frac{\text{SNR} - 1.76}{6.02}, \tag{15}$$

where the signal-to-noise ratio, in units of dB, is defined by the following equation:

$$SNR = 20\log_{10}\left(\frac{C_{Range}}{2\sqrt{2}C_{Resolution}}\right), \tag{16}$$

where C_{Range} is the input range of the CDC and $C_{resolution}$ is the capacitance resolution of the CDC.

The performance of the interface circuit is summarized and compared with that of other state-of-the-art devices in Table 5. The measurement results show that the capacitive sensors based on a third-order CIFF delta-sigma modulator in this paper have good performances in terms of power consumption and measurement time. Compared with other designs, the proposed CDC discussed in this paper consumes much less power; its power consumption is only 37.2 μW, which is approximately 5.5 times better than that of [7] and 20 times better than that of [29]. Overall, the proposed CDC achieved a better FoM than other state-of-the-art CDCs described in previous work. This confirms the effectiveness of the techniques presented in this paper.

VI. CONCLUSION

A capacitive sensor with a low-power delta-sigma CDC has been designed and implemented in a 0.18 μm CMOS chip. The CDC employs a third-order CIFF incremental delta-sigma modulator with a current-starved cascoded inverter-based OTA. The proposed CDC employed a third-order modulator to achieve high resolution. The auto-zeroing technique is applied in the integrators of the CDC to cancel the offset as well as the dynamic offset. Simultaneously, a current-starved cascoded inverter-based OTA is employed in the integrator; this can yield a significant improvement in the energy efficiency of the system. Measurement results show that it achieves a resolution of 12.7 bits within a measurement time of 0.8 ms, while drawing only 18.6 μA from a 2 V supply. This represents an energy consumption of 4.47 pJ/step. However, the capacitor arrays have a certain parasitic capacitance. The parasitic capacitor needs to be charged and discharged during readout although it does not contribute any signal; this requires further study. This design allows the sensor to achieve excellent resolution within a very short measurement time with good energy efficiency, qualities that make the proposed CDC very suitable for capacitive sensor applications.

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