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A low power front-end architecture for SiPM readout with integrated ADC and multiplexed readout

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ABSTRACT: Silicon Photo-Multiplier (SiPM) detectors are becoming widely used for optical photon and, in conjunction with suited scintillators, for gamma detection in both medical imaging and particle physics experiments. The spatial resolution can be improved by using smaller SiPMs with a corresponding increase in front-end channels density. The timing resolution of the whole system is a function of the detector parameters and of the characteristics of the front-end electronics.

We present a low power front-end readout architecture which allows reading out several SiPMs though a single line in order to maximize the number of SiPMs. The design offers good timing performance and includes a simple charge digitizer in every channel.

Four different single-ended channel designs have been designed, submitted for fabrication and characterized electronically and with SiPMs. The timing performance is obtained by using a low input impedance, precise threshold setting of a leading edge discriminator and a programmable input dc potential to set the SiPM HV bias on a channel per channel basis. Programmable low- and high-pass filters should allow reducing baseline fluctuations and noise. A simple ADC is implemented by first integrating the signal current and then discharging it at a constant rate until the baseline is reached again. The current consumption of the single channel is typically less than 10 mA. The time and energy information are sent out on a single wire. In order to keep as low as possible the output cabling the signals from different channels can be multiplexed on the same cable. The processing of these signals (extraction of time, ADC amplitude determination and channel number decoding) is performed by an external FPGA.

The overall architecture, the front-end designs, and measurements with SiPMs are presented.

KEYWORDS: Front-end electronics for detector readout; Gamma detectors (scintillators, CZT, HPG, HgI etc)

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1 Silicon Photo-Multiplier readout

Silicon Photo-Multipliers (SiPMs) are excellent photon detectors and, combined with suited scintillators, they are becoming widely used as gamma rays detectors in medical imaging and high energy physics applications. The presented readout architecture, developed within the SUBLIMA European Project, is aimed to investigate the feasibility of a compact module with good spatial resolution in a 1 to 1 coupling configuration (between SiPMs and scintillators) and with an excellent time resolution (coincidence resolving time CRT < 300 ps), to allow for time of flight measurements.

In such a configuration, a better spatial resolution can be achieved using smaller scintillator elements at an increased channel count. The presented front-end architecture is designed to cope with a large number of channels so small power dissipation per channel is mandatory. An excellent time resolution is mainly achieved reducing the input impedance of every channel [1] and the biggest effort has been put in this direction. Each channel includes also the capability to tune the threshold using an internal DAC with a fine step of $\sim 250\,\mu$V. The typical non-homogeneity between SiPM gains can be compensate in each channel with a dedicated DAC which defines the DC input potential of the frontend, directly changing the SiPM over-voltage. Each channel bandwidth can be programmed independently: a low-pass filter reduces the white noise and a high-pass filter eliminates the baseline fluctuations from dark counts, typical of the SiPM detectors.

2 Channel architecture

The simplified channel overview is shown in figure 1. Each channel includes several amplifier stages, which work intrinsically also as a low-pass filter, a high pass filter and a leading edge discriminator (*Hit Logic* in the figure) [2]. The discriminator threshold can be set per-channel with an 11-bit Threshold-DAC, with 250μV step size. A 5-bit Input-DAC with 50 mV steps sets the DC input potential on a per-channel basis. The current signal from the SiPMs is integrated and digitized with an ADC. A digital block organizes the information from each channel (time, energy, channel ID) and sends it out on a single wire for processing by an external FPGA.

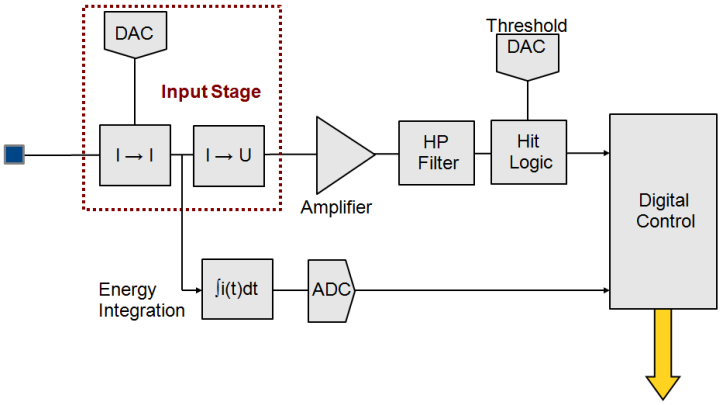

Figure 1. Simplified scheme of one channel. On the upper branch the current signal is converted into voltage, amplified and compared with a threshold defined from the DAC. On the lower one the current is integrated to give the energy information. Both results are then digitized and sent out from the digital control block.

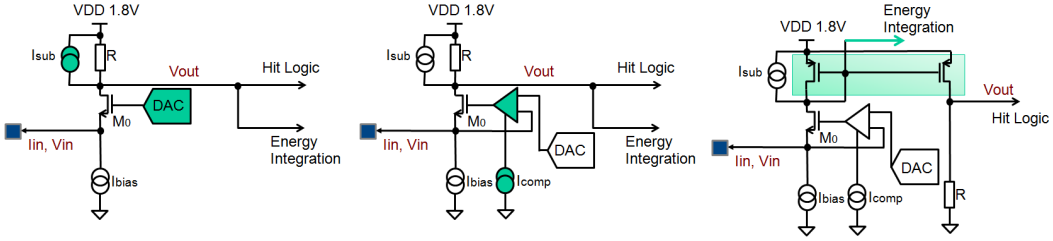

Figure 2. Left: grounded gate input stage. Center: regulated gate input stage. Right: regulated stage with current mirror.

2.1 Input stage design

Four different input stage designs have been implemented and characterized. We present here the main features avoiding a detailed description of each of them.

A classical method for reaching a low-impedance at the input node is to use a grounded gate stage: in this case the input impedance is limited by the characteristics of the cascode and the current flowing through it.

Starting from this simple idea, some features have been added to the input stage design.

Starting from this simple idea, some features have been added to the input stage design. The left side of figure 2 shows the classical scheme of a grounded gate input stage. A current source is placed in parallel to the gain resistor: the balance between the current flowing through the sources defines the output potential of the stage and, consequently, the dynamic range for the input signal. The gate voltage of the NMOS cascode M_0 is set with the Input-DAC to control the DC input potential. With this design the simulated input impedance can reach $\sim 25\,\Omega$, for a bias current of ~ 4 mA.

The second design (figure 2, center) includes a regulation circuit: a fast amplifier keeps the input DC potential at the voltage defined with the Input-DAC. An additional bias current is obviously needed, but the overall transconductance of the stage can be much higher, depending on the characteristics of the regulation circuit. The simulated input impedance reaches only $\sim 3\,\Omega$ at a total current of 8 mA per channel (at a supply voltage of 1.8 V).

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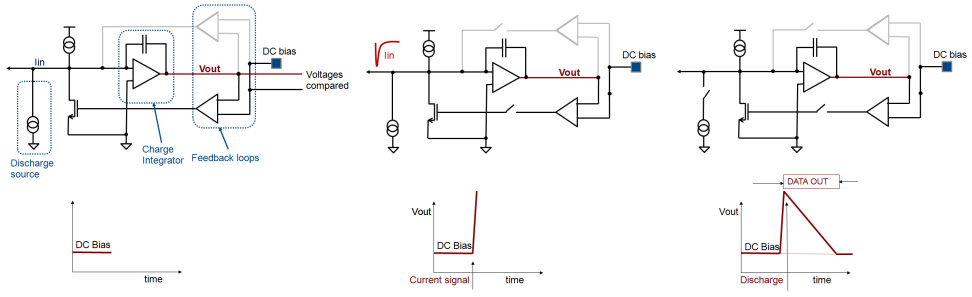

Figure 3. Energy integrator circuit: idle state (left), integration (center) the discharge (right) are shown.

The other two studied designs are similar to the previous ones, but they include a current mirror which allows placing the gain resistor on a second branch. The third one, not shown in the figure, has no compensation circuit for the DC input potential, while the fourth design, with its regulation circuit, is shown on the right side of figure 2. With this configuration is easily possible to obtain a higher voltage gain and a larger dynamic range. The voltage gain is in fact determined by the product between the mirror ratio and the resistor value and in our design it is fixed at ~ 200, with a mirror ratio of 2 and a 100 Ω resistor. The output voltage can in this case vary from very low values (a few hundreds mV, depending on the input stage setting) to the maximum $1.8V$ value, while in the previous design the maximum reachable output voltage is set by the gain resistor and the bias current and cannot be larger than ~ 1.5 V in our design.

Other regulation circuit designs can be found in [3–5].

2.2 Energy integration

The energy integrator converts the input charge to a time interval: the current from the SiPM (obtained from the amplified voltage signal in figure 2 left/center via a simple resistor or directly via the current mirror in figure 2 right) is collected on an integrator. After a programmable time (depending mainly on the crystal time constant) the integrating capacitor is discharged with a constant current. The discharge time is a measurement of the signal energy. Figure 3 shows a simplified schematic of the circuit:

- In the idle state the output potential of the integrator is kept at a reference level with a feedback circuit. An input current source is adjusted such that no current flows in the integrator. Two regulation circuits are actually present in the scheme (on gray in the figure), the second one needed for the stability of the system.

- When a signal from the SiPM is detected by the discriminator (in the timing path), the compensation circuits are turned off and the SiPM current is collected on the feedback capacitor.

- After a programmable time a constant current source is disconnected from the input so that the feedback capacitor is discharged at a constant rate. When the output voltage reaches again the reference voltage, the feedback circuits are turned on again. The time between ramp start and the end of the ramp is proportional to the input charge

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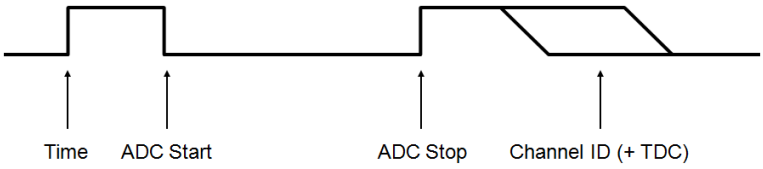

Figure 4. Output protocol simplified example.

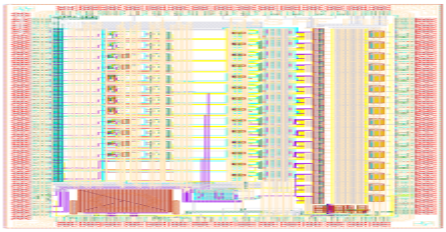

Figure 5. Test chip layout.

In our implementation, we have chosen discharge times of several 100 ns. This is comparable to integration windows required for LYSO readout ($\tau \sim 40$ ns) on one hand and allows using slow low power circuitry on the other hand. The total current consumption of this part is typically 150 μA.

2.3 Single-wired output protocol

Every channel includes a digital block which merges the energy and time information on a single wire. This information can then be processed by an external FPGA.

The single wire protocol (figure 4) is built as follows: the first rising edge occurs when the front-end electronics detects a signal over threshold. This timing critical edge must be sampled by the FPGA with a *ps* precision. After a programmable (but uncritical) time interval (when all charge has been collected), the integrator discharge is started automatically and the signal goes low. When the discharge is over the signal goes up again: this *interval*, to be sampled with *ns* precision, gives the energy information. The last part of the output signal is Manchester encoded and includes other information, like the ID of the firing channel or a parity bit.

The outputs of several channels can be multiplexed to a single line using this protocol. The digital control block in figure 1 must then do a channel arbitration and make sure that no partial data is transmitted. Lost hits can be messaged in an extended trailer.

3 Measurements and results

The test chip has been realized in UMC180 nm technology, the layout is shown if in figure 5.

All channel designs has been tested and characterized. In terms of energy resolution all the channels behave in a similar way, as expected. The input impedance measured at DC is consistent with the simulations: the regulated input stages have a very low input impedance of $\sim$ 7–8 Ω, while the simple cascode stages have an impedance one order of magnitude larger ($\sim 70\,\Omega$).

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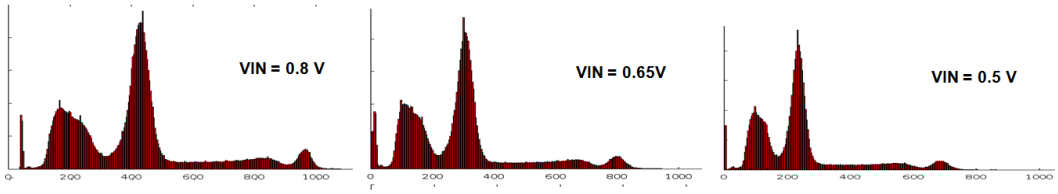

Figure 6. ^{22}Na energy spectra measured at different input dc potentials.

The channels have been connected to large area SiPMs (4×4 mm) which are optically glued to 22 mm long LYSO scintillators. Spectra taken with a ^{22}Na source for three settings of the Input-DAC are shown in figure 6.

As expected, the SiPM gain can be adjusted linearly. Given the simplicity of the approach, the measured *FWHM* of the 511 keV peaks of $\sim 15\%$ is a very encouraging preliminary result which can probably still be improved.

The time resolution could not yet been determined due to a mismatch between the chosen gains in the timing and the energy channel: For high SiPM bias voltages required for good timing, the ADC unfortunately saturates so that no energy cuts can be applied and coincident events cannot be clearly identified. This is fixed in a new design iteration with a lower integrator gain and wider gain setting range. Using a small SiPM overvoltage with a bias current of only 50 μA per SiPM (of 16 mm^2 area), the measured CRT (FWHM in coincidence) is 750 ps.

Acknowledgments

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