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A Low-Power High-Speed Dynamic Comparator With a Transconductance-Enhanced Latching Stage

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ABSTRACT Low-power, high-speed dynamic comparators are highly desirable in the design of high-speed analog-to-digital converters (ADC) and digital I/O circuits. Most dynamic comparators use a pair of cross-coupled inverters as the latching stage, which provides strong positive feedback, to accelerate the comparison and reduce the static power consumption. The delay of the comparator is mainly determined by the total effective transconductance of the latching stage. The delay not only limits the maximum operating frequency but also extends the period of the metastable state of the latching stage; hence, it increases energy consumption. However, at the beginning of the comparison phase, the conventional latching stage has two transistors with zero gate-to-source voltage, which degrade the total effective transconductance of the latching stage. In this paper, a novel low-power, high-speed dynamic comparator with a new latching stage is presented. The proposed latching stage uses separated gate-biasing cross-coupled transistors instead of the conventional cross-coupled inverter structure. The simple proposed latching stage improves its effective total transconductance at the beginning of the comparison phase, which leads to a much faster comparison and lowers energy consumption. The comparator is analyzed and compared to its prior type in terms of delay and power consumption via simulations and measurements. The experimental results demonstrate that the proposed comparator operates from a 1.2-V supply and consumes 110-fJ energy per comparison, with sampling speeds up to 2 GS/s.

INDEX TERMS Dynamic comparator, high-speed, low-power, two-stage comparator.

I. INTRODUCTION

The latch-based dynamic comparator is a crucial module in analog-to-digital converters (ADC) [1]–[3], high-speed digital I/O circuits [4], memory sensing amplifiers [5] and analog built-in-self-testing (BIST) circuits [6]. Compared with static comparators, dynamic comparators utilize positive feedback and dynamic bias; therefore, have higher speed and lower static power consumption [7].

The conventional single-stage dynamic comparators directly stack the input transistors with the cross-coupled latch circuit; hence, they require large voltage headroom [8]. Moreover, they suffer from severe kickback noise introduced by the capacitive paths from the output nodes to the input nodes, and there is a challenging tradeoff between speed and power consumption. Several design techniques for low-voltage, low-power dynamic comparators have been reported, including the charge-steering technique [9], techniques using body-driven transistors [10], and supply boosting methods [11]. As an alternative, the two-stage dynamic comparator topology employs a fully dynamic preamplifier as the input stage, which is separated from the latching stage [5]. This structure has less stacking, so it is more suitable for low-voltage operation. In addition, it reduces the kickback noise by providing additional shielding between the input and the output and enables independent optimization of the input stage (which mainly affects the offset) and latching stage (which mainly affects the speed). Several modified

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two-stage comparators have been reported to achieve faster speed and lower power consumption. In [12], positive feedback is introduced in the preamplifier of the two-stage comparator to strengthen the regeneration, which reduces the delay. However, it suffers from higher kickback noise than the conventional two-stage comparator. A common-mode insensitive dynamic comparator is presented in [13]. The latch is activated with an intentional delay to reduce power consumption. However, it suffers from a larger required area and higher kickback noise. The two-stage comparator in [14] employs a dynamic bias preamplifier, which only partially discharges the internal nodes and reduces the energy consumption. However, its delay is larger than that of the conventional structure. In [15], an additional positive feedback and a special clocking pattern are used in the preamplifier to improve the preamplifier gain.

All of the aforementioned dynamic comparators employ similar cross-coupled latching stages. In [16], we show that the delay and energy consumption can be greatly reduced by using a novel transconductance-enhanced latching stage. The proposed latching stage provides separated gate-biasing to the cross-coupled transistors, which improves the effective total transconductance at the beginning of the comparison phase; hence, it achieves higher speed and lower power consumption. In this paper, we present the detailed analysis of the novel two-stage dynamic comparator using the transconductance-enhanced latching stage. Various dynamic comparator circuits were designed and simulated in a 0.18-μm CMOS process for comparison in terms of delay and power consumption. In addition, the proposed comparator was fabricated and measured, and the measured results verify that the proposed comparator operates from a 1.2-V supply and consumes 110 fJ per comparison with sampling speeds up to 2 GS/s.

The remainder of the paper is organized as follows. Section II presents the operation and delay analysis of the conventional two-stage comparators. The proposed comparator and design considerations are described in Section III. The simulation and measurement results are presented in Section IV, and the paper is concluded in Section V.

II. CONVENTIONAL TWO-STAGE DYNAMIC COMPARATOR

Fig. 1 presents the conventional two-stage dynamic comparator. It consists of a preamplifier stage and a latching stage. The low-tail current of the preamplifier stage is preferred to reduce the input offset voltage. The latching stage is usually optimized to have a large operational current to enhance the speed. The operation of the comparator is as follows. During the reset phase when $CLK = 0$, M4 and M5 are on, and M10 and M11 are off. Therefore, nodes D_n and D_p are charged to VDD, which causes nodes OUT_p and OUT_n to discharge to the ground through M8 and M9. In the comparison phase, when $CLK = VDD$, M10 and M11 are on, and M4 and M5 are off. Nodes D_n and D_p start to discharge with two different discharging currents, depending on the corresponding

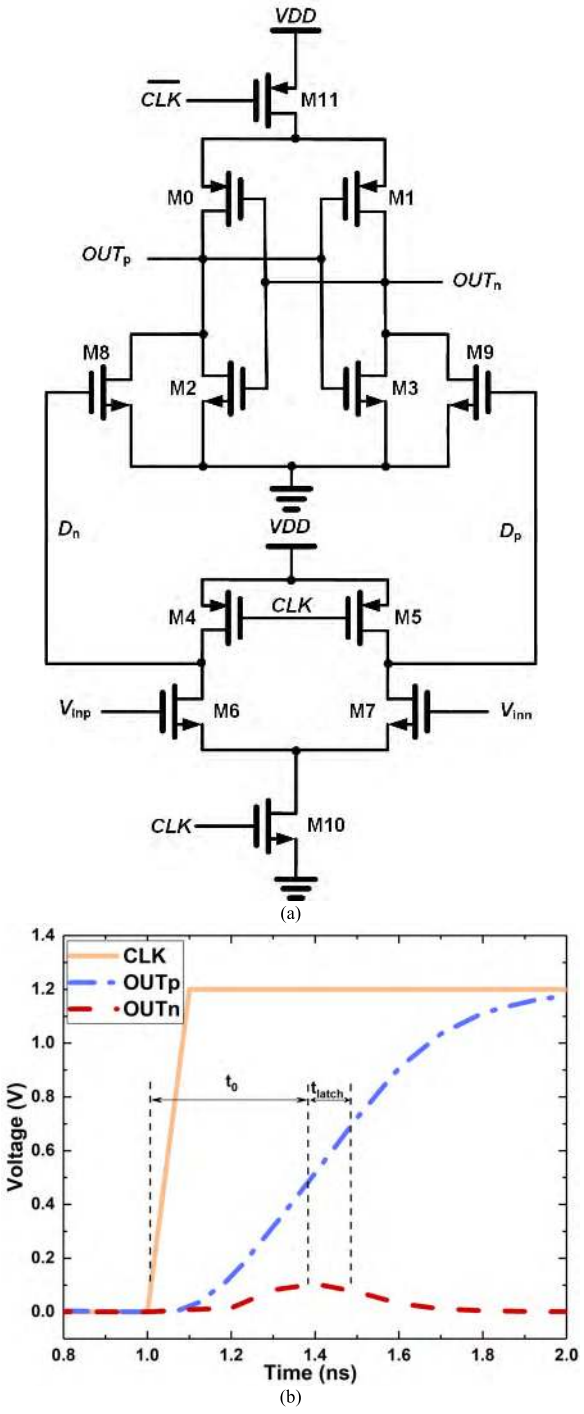

FIGURE 1. (a) Conventional two-stage dynamic comparator and (b) its typical waveforms.

input voltage (V_{inn} and V_{inp}). The voltage difference between D_n and D_p builds up the initial differential voltage at the output nodes (OUT_p and OUT_n), which is further amplified by the strong positive feedback of the cross-coupled latching structure. The two-stage structure has several advantages, including lower kickback noise, better suitability for low-voltage operation and more flexible trade-off between speed and offset.

The delay of the comparator is defined as the time that the output difference takes to reach $0.5VDD$ and can be divided into two parts: t_0 and t_{latch}, as shown in Fig. 1 (b). t_0 is the period from the rising edge of $CLK$to the time when OUT_{p} and OUT_{n} are charged to V_{THN}. During this period, the pMOS transistors M0 and M1 are in the saturation region, while the nMOS transistors M2 and M3 are off. Therefore, the total transconductance of the latch is approximately equal to the transconductance of M0 and M1, and t_0 can be calculated from (1).

$$t_0 = \frac{V_{\text{THN}}C_{\text{OUT}}}{I_{\text{p}}} = \frac{V_{\text{THN}}C_{\text{OUT}} \cdot 2\mu_{\text{p}}C_{\text{OX}}\frac{W_{\text{p}}}{L_{\text{p}}}}{g_{\text{mp}}^2} \approx \frac{V_{\text{THN}}C_{\text{OUT}} \cdot 2\mu_{\text{p}}C_{\text{OX}}\frac{W_{\text{p}}}{L_{\text{p}}}}{g_{\text{m,eff}}^2} \tag{1}$$

where C_{OX} is the gate oxide capacitance, μ_{p} is the hole mobility, V_{THN} is the threshold voltage of M2 and M3, C_{OUT} is the load capacitance at the output nodes, I_{p} is the current that passes through M1, g_{mp} is the transconductance of the pMOS transistor M1, W_{p} and L_{p} are the channel width and length of M1, respectively. $g_{\text{m,eff}}$ is the effective total transconductance of the inverter consisting of M1 and M3, and is given by

$$g_{\text{m, eff}} = g_{\text{mp}} + g_{\text{mn}} \tag{2}$$

where g_{mn} is the transconductance of the nMOS device of the inverter. Since the nMOS transistor M3 is off during this period, g_{mn} is negligible.

The second part of the delay t_{latch}, which is defined as the time between the end of t_0 and the time when the differential voltage of the output nodes reaches $V_{\text{DD}}/2$, is the latching delay of two cross-coupled inverters. t_{latch} is given by

$$t_{\text{latch}} = \frac{C_{\text{OUT}}}{g_{\text{m,eff}}} \cdot \ln\frac{\Delta V_{\text{out}}}{\Delta V_0} = \frac{C_{\text{OUT}}}{g_{\text{m,eff}}} \cdot \ln\frac{V_{\text{DD}}/2}{\Delta V_0} \tag{3}$$

where ΔV_0 is the initial voltage difference between the two output nodes at $t = t_0$. During this period, all the transistors of the cross-coupled inverters are turned on. Therefore, the effective total transconductance of the inverter can be expressed as

$$g_{\text{m, eff}} = g_{\text{mp}} + g_{\text{mn}} = \mu_{\text{p}}C_{\text{OX}}\frac{W_{\text{p}}}{L_{\text{p}}}(|V_{\text{GSP}}| - V_{\text{THP}}) + \mu_{\text{n}}C_{\text{OX}}\frac{W_{\text{n}}}{L_{\text{n}}}(V_{\text{GSN}} - V_{\text{THN}}) \tag{4}$$

The total delay of the comparator can be expressed as

$$t_{\text{delay}} = \frac{V_{\text{THN}}C_{\text{OUT}} \cdot 2\mu_{\text{p}}C_{\text{OX}}\frac{W_1}{L_1}}{g_{\text{m,eff}}^2} + \frac{C_{\text{OUT}}}{g_{\text{m,eff}}} \cdot \ln\frac{V_{\text{DD}}/2}{\Delta V_0} \tag{5}$$

Note that enhancing the total transconductance $g_{\text{m,eff}}$ is an effective method to reduce the delay, particularly for t_0 when the comparator first enters the comparison phase. However, for the conventional two-stage dynamic comparator, only the pMOS transistors in the latch are on during t_0, so the nMOS transistors make no contribution to $g_{\text{m,eff}}$, which leads to a lower regeneration speed at the beginning of the comparison phase. Furthermore, this phenomenon causes a longer time of the metastable state of the cross-coupled inverters and results in higher energy consumption.

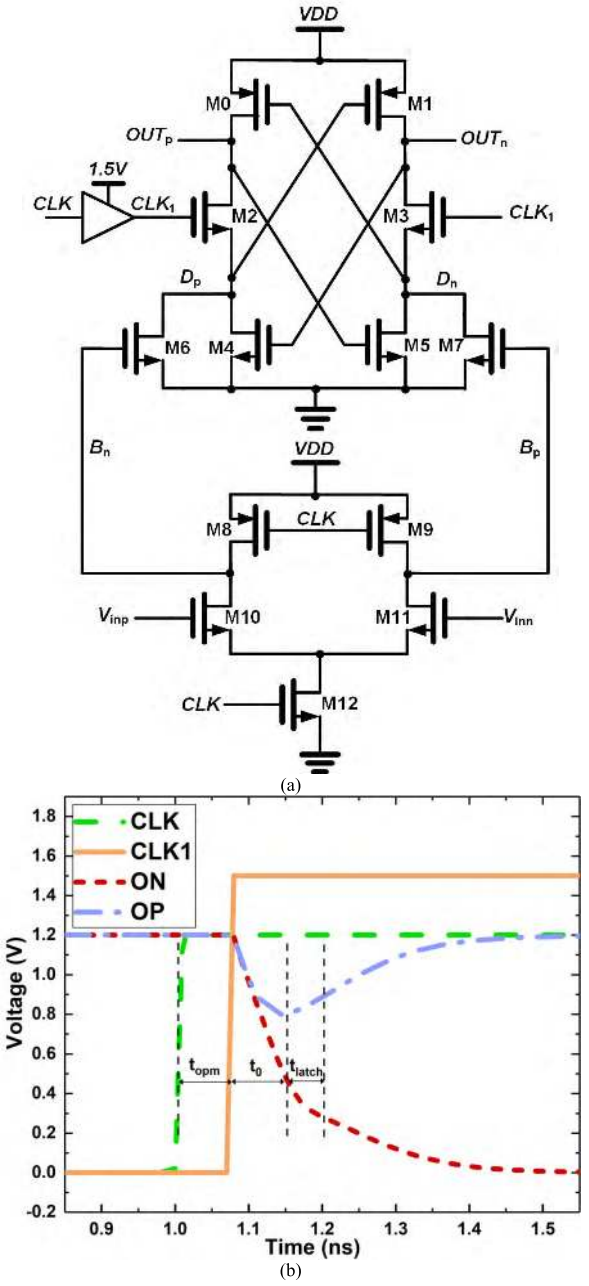

FIGURE 2. (a) Schematic of the proposed dynamic comparator and (b) its typical waveforms.

III. PROPOSED DYNAMIC COMPARATOR

A. CIRCUIT DESCRIPTION

Fig. 2 presents the schematic of our proposed dynamic comparator with a new latching stage and its typical waveforms. CLK_1 is the level-shifted signal of CLK with 95 ps delay.

In the reset phase, when $CLK = 0$, nodes B_n and B_p are charged to VDD, M6, M7, M0 and M1 are on, and M2 and M3 are off. Nodes D_n and D_p are discharged to ground via transistors M6 and M7, and nodes OUT_p and OUT_n are charged to VDDvia transistors M0 and M1.

In the reset phase, compared with other cross-coupled structures that bias only two transistors in the strong-inversion region and leave the other two transistors in the cut-off region, all cross-coupled transistors M0, M1, M4 and M5 in the proposed regenerative structure are biased in the strong-inversion region. At the beginning of the comparison phase, as described below, the proposed regenerative stage has a much higher effective total transconductance than the conventional structure, which accelerates the regeneration speed. Furthermore, the faster comparison leads to a shorter metastable period of the cross-coupled inverters, which reduces the energy consumption. CLK_1 is delayed by t_{opm} in purpose, so that M2 and M3 are turned on later to minimize the short current through M6 and M7 at the rising edge of CLK.

The delay of the proposed dynamic comparator is expressed as

$$t_{delay} = t_{opm} + t_0 + t_{latch} \tag{6}$$

In the period of t_0, OUT_p and OUT_n are discharged from VDD, while D_p and D_n are increasing from GND. Therefore, all transistors (M0-1 and M4-5) of the cross-coupled inverters are on and working in the triode region at first. The effective total transconductance of the latch is given by

$$g_{m,eff} = g_{mn} + g_{mp} = \mu_n C_{OX} \left(\frac{W}{L}\right)_n V_{dsn} + \mu_p C_{OX} \left(\frac{W}{L}\right)_p |V_{dsp}| \tag{7}$$

where V_{dsn} and V_{dsp} are the drain-to-source voltages of the nMOS and pMOS transistors in the latch, respectively. Equation (5) shows that $g_{m,eff}$ linearly depends on the drain-to-source voltages of the transistors of the latch. After CLK_1 increases to VDD, switches M2 and M3 are turned on; hence, $OUT_{p/n}$ are rapidly discharged to $D_{p/n}$, which causes a rapid increase in V_{dsn} and $|V_{dsp}|$. For the conventional cross-coupled latch, only pMOS transistors are on and working in the saturation region. Its $g_{m,eff}$ is given by

$$g_{m,eff} = g_{mp} = \mu_p C_{OX} \left(\frac{W}{L}\right)_P (|V_{GSP}| - V_{THP}) \tag{8}$$

Therefore, $g_{m,eff}$ of our proposed latch structure increases much faster than the conventional cross-coupled latch at the beginning of the comparison phase. Fig. 3 presents the transient simulation results of $g_{m,eff}$ of the conventional and proposed two-stage dynamic comparators. For a fair comparison, both circuits are optimized to achieve an offset of approximately 7 mV, designed with similar transistor sizes of the latch circuit, and simulated with identical input signals. The effective total transconductance of the proposed structure increases much faster and higher than its counterpart,

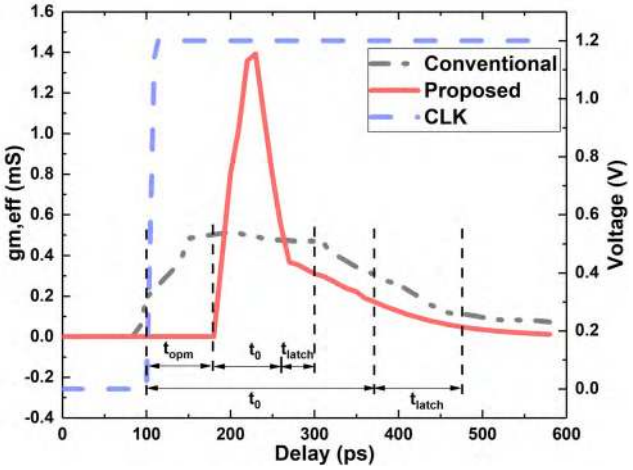

FIGURE 3. Simulated $g_{m,eff}$ of the conventional and proposed comparators.

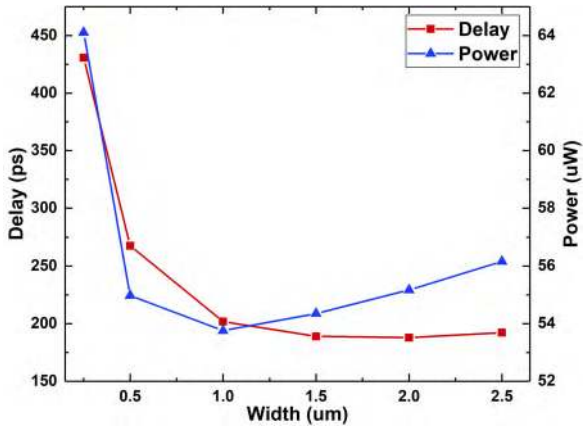

FIGURE 4. Simulated delay and power consumption of the proposed comparator versus the width of switches M2 and M3.

and its peak value is improved to approximately 3×. This advantage makes our proposed dynamic comparator achieves faster comparison, shorter period of the metastable state and lower energy consumption.

B. DESIGN CONSIDERATIONS

Some design issues must be considered in the design of the proposed comparator. The most unique part of this structure is the modified cross-coupled latch and associated switches M2-3. In the comparison phase, M2-3 are turned on, and the drain-to-source voltage of these switches must be minimized to enable a full discharge of the output nodes. Therefore, a pair of nMOS switches with a boosted control voltage is used. The boosted control voltage is set to be $VDD + 0.3$ V. Since the parasitic capacitance of M2-3 is a part of the load capacitance, a trade-off between switch-on resistance and parasitic capacitance must be considered. Fig. 4 shows the simulated delay and power consumption of the proposed comparator with different widths of switches M2-3. When the width of M2-3 is larger than 1 μm, increasing the width cannot help to significantly reduce the delay but causes

higher power consumption. Therefore, we set the width of M2-3 to 1 μm.

The control signal CLK_1 is a boosted and delayed signal generated from CLK, and the delay between CLK and CLK_1 is defined as t_{opm}, as previously mentioned. A shorter t_{opm} may lead to a higher short current through M6 and M7, whereas a longer t_{opm} may lead to a significant degradation of speed. The delay t_{opm} is determined by the transistor sizes of the level shifter in Fig. 2 (a). The delay and energy consumption with different t_{opm} is simulated, as shown in Fig. 5. We make a tradeoff between energy consumption and speed and set t_{opm} to 95 ps according to the simulation results.

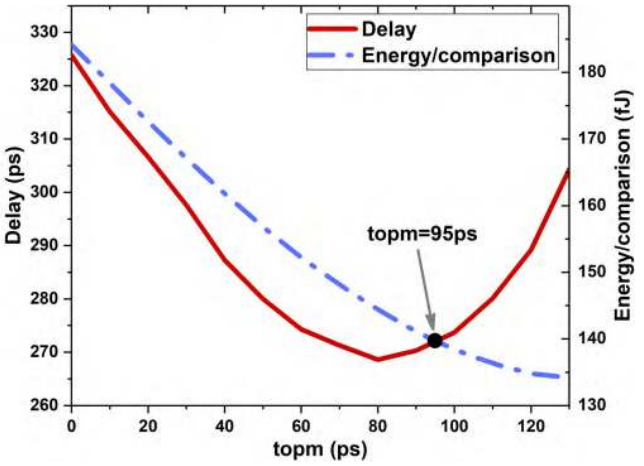

FIGURE 5. Simulated delay and energy consumption versus t_{opm}.

TABLE 1. Transistor sizes in the proposed dynamic comparator.

Transistor ID	Size of transistor (μm)
M0-1	2/0.18
M2-3	1/0.18
M4-5	0.5/0.18
M6-7	2/0.18
M8-9	1.8/0.18
M10-11	4/0.18
M12	0.44/0.18

IV. EXPERIMENTAL RESULTS

To compare the new and conventional double-tail comparators, all circuits were simulated in 0.18-μm CMOS technology with 1.2 V supply voltage and 20 fF load capacitance. For a fair comparison, the transistor dimensions of the comparators were optimized to obtain an equal offset standard variation of 7 mV at an input common-mode voltage (V_{cm}) of 1.1 V. The clock frequency was set at 500 MHz. The transistor sizes of the proposed comparator are presented in Table 1. To verify the low-power and high-speed feature of the proposed comparator, we also fabricated and measured the proposed comparator. The microphotograph and layout of the proposed comparator are shown in Fig. 6. The circuit was laid out in a fully symmetric fashion to avoid the static offset voltage caused by the layout mismatch. We used an Agilent E8267C Vector Signal Generator to generate the clock signal, and a Keysight 6626A Precision Power Supply to generate the

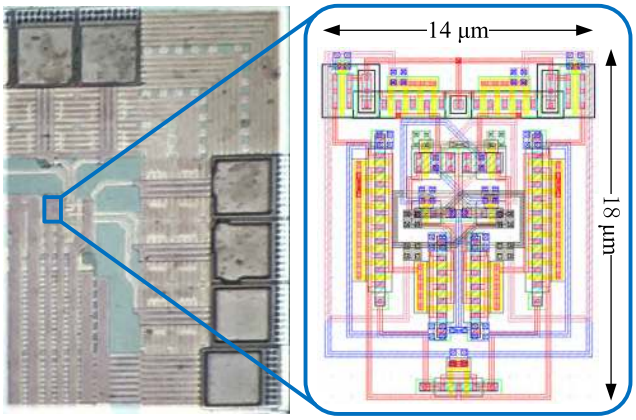

FIGURE 6. Microphotograph and layout of the proposed comparator.

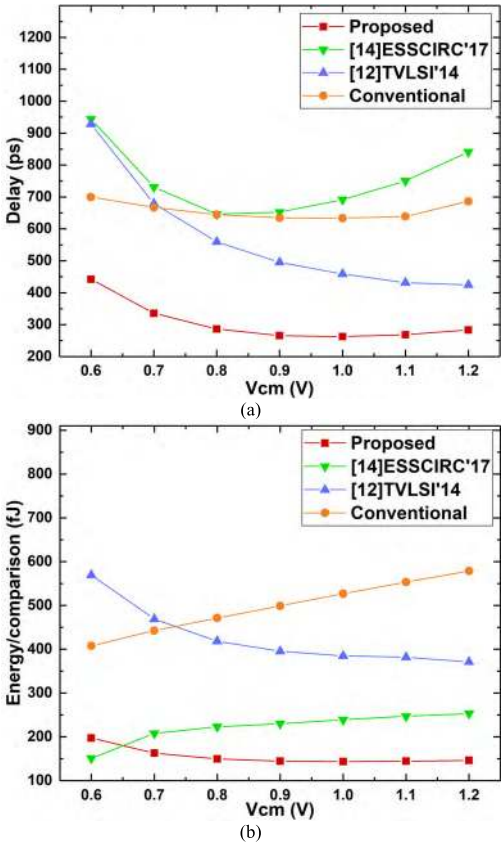

FIGURE 7. (a) Postlayout simulated delay and (b) energy consumption versus V_{cm} ($VDD = 1.2$ V; $V_{id} = 50$ mV).

input voltages. The output of the comparator was measured by a Keysight DSO90254A Oscilloscope.

A. SIMULATION RESULTS

Figs. 7 (a) and (b) show the postlayout simulated delay and energy consumption versus V_{cm} at $V_{id} = 50$ mV, respectively. The proposed comparator is faster than the others by more than 150 ps. Meanwhile, the energy consumption of the proposed comparator is comparable to that of the comparator in [14] and only approximately 30% of that of the conventional circuit and comparator in [12]. Since the proposed

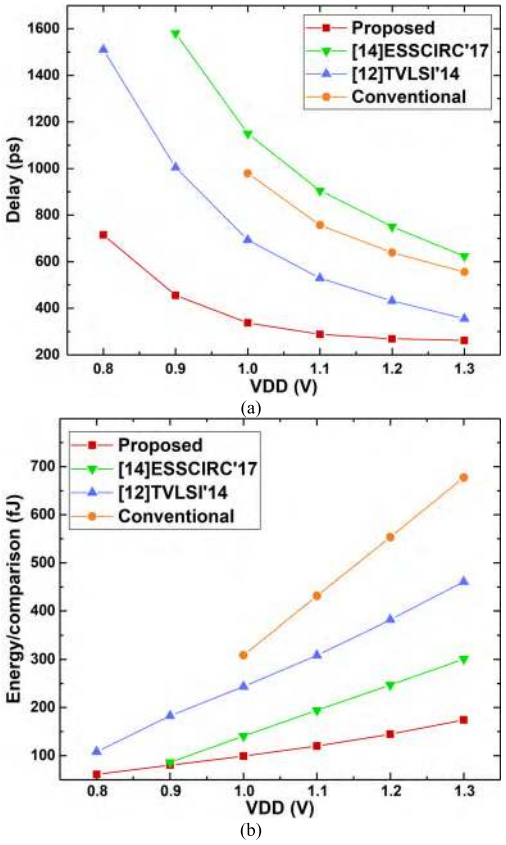

FIGURE 8. (a) Postlayout simulated delay and (b) energy consumption versus *VDD* (V_{id} = 50 mV; V_{cm} = *VDD* - 0.1 V).

comparator uses a conventional input stage, the performance improvements are due to its novel latching stage.

Fig. 8 (a) and (b) present the postlayout simulation results of the delay and energy consumption of the mentioned dynamic comparators versus the *VDD*variation at V_{id} = 50 mV and V_{cm} = *VDD* – 0.1 V. Fig. 8 (a) shows that in comparison with the other three structures, the delay and energy consumption of the proposed dynamic comparator is significantly reduced in low-voltage supplies, which makes it more suitable for low-voltage low-power applications than the other structures. For example, the proposed comparator can operate with 0.8-V supply and 500-MHz sampling frequency at the cost of 55 fJ/conversion with 710 ps delay.

Fig. 9 depicts the dependence of the comparator delay on the differential input voltage at *VDD* = 1.2 V and multiple input common-mode voltages. The delay remains moderate and comparable for the input common-mode voltage in the range of 0.7–1.1 V. It decreases with the decrease in differential input voltage. Fig. 10 shows the standard deviation of the offset of the proposed comparator, which is 7.3 mV using Monte Carlo simulations for a run of 300 samples. Based on our simulation results, Table 2 presents the comparison between the proposed and three other two-stage dynamic comparators. The proposed comparator achieves the smallest power consumption, delay, and area with the same offset budget and similar transistor sizing as its counterparts.

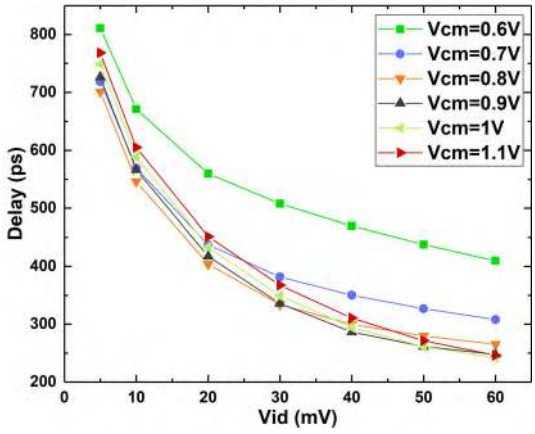

FIGURE 9. Postlayout simulated delay versus V_{id} (*VDD* = 1.2 V; V_{cm} = 0.7 V).

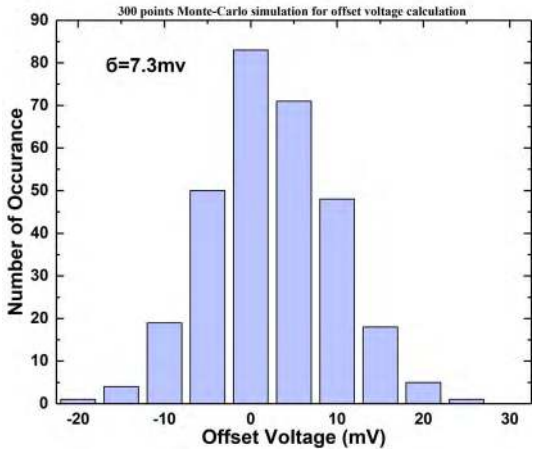

FIGURE 10. Monte Carlo simulation results of the offset in the proposed comparator.

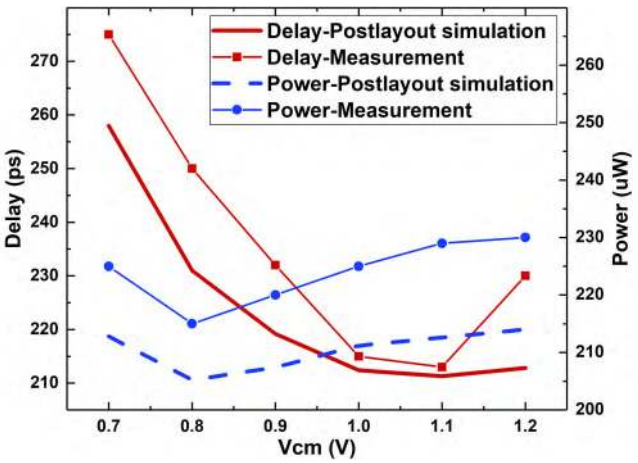

FIGURE 11. Delay and energy consumption versus V_{cm} (V_{id} = 0.1 V; *VDD* = 1.2 V; the operating frequency is 2 GHz).

B. MEASUREMENT

Fig. 11 presents the measured and simulated delay and power consumption at 2 GHz operating frequency and 0.1 V input differential voltage. In the input common-mode voltage range

TABLE 2. Performance comparison based on our simulations.

	Conventional [5]	TVLSI'14 [12]	ESSCIRC'17 [14]	Proposed
Operating frequency (MHz)	500	500	500	500
Average power(μW)	276.62	190.88	123.51	72.2
Delay(ps)	638.91	431.74	750.13	268.6
Estimated area (μm^2)	1407	877	541	252
Offset(mV)	7.11	7.26	7.25	7.3

TABLE 3. Comparison between the proposed comparator and other comparators.

	TCAS-I'13 [18]*	TVLSI'14 [12]†	Microelectron. J. '14 [17]†	EL'15 [13]†	TVLSI'18 [15]*	Proposed*
Supply voltage (V)	5	1.2	1	1.2	1.8	1.2
Maximum operating frequency (Hz)	33.3 M	2.5 G	1G	1.25	0.5 G	2 G
Offset (mV)	50.57 uV	7.8	11	7.78	2	7.3†
Area (μm^2)	64000	392	180	-	530	252
Energy per conversion (fJ)	23000	560	51	480	460	112.5
Technology (nm)	500	180	180	130	180	180

*Measurement results.

†Simulation results.

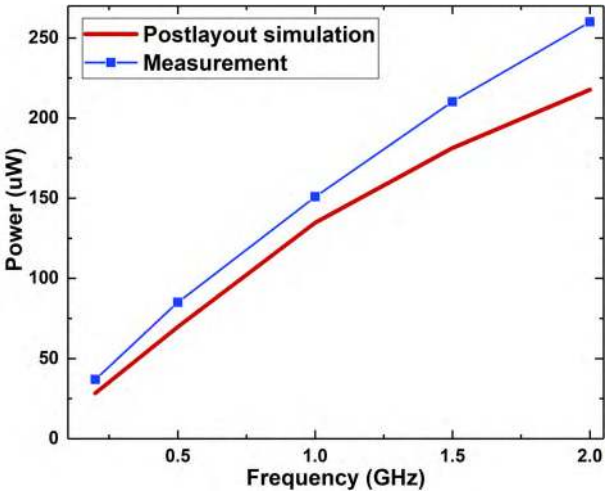

FIGURE 12. Power consumption versus the operating frequency (V_{id} = 0.1 V; VDD = 1.2 V; the operating frequency is 2 GHz).

of 0.7-1.2 V, the delay is less than 275 ps, and the average power consumption is approximately 225 μW. Fig. 12 shows the measured and simulated power consumption at different operating frequencies. The proposed comparator maintains the feature of low power consumption at different frequencies. The test results are basically consistent with the simulation results. Table 3 presents the performance comparison of the proposed and other dynamic comparators. The proposed comparator achieves a low-power behavior with high speed and small area. The dynamic comparator in [12] has a higher maximum operating frequency of 2.5 GHz (from simulation results), but its energy consumption is approximately 5× higher than that of our proposed comparator. The comparator in [17] has lower energy consumption (from the simulation results) but suffers from a lower speed and a larger offset voltage.

V. CONCLUSION

We presented a new dynamic comparator with a novel transconductance-enhanced latching stage, which is suitable for low-power high-speed operation. The cross-coupled transistors in the proposed latch structure are biased in the strong inversion region during the reset phase, which improves the total effective transconductance of the latch at the beginning of the comparison phase and significantly decreases the delay and energy consumption. Postlayout simulations and measurement results confirm that the delay and energy consumption of the proposed comparator are strongly reduced compared to those of the conventional comparator structures. In addition, this simple structure is area-efficient and can work at a low supply voltage.

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