Hindawi
Wireless Communications and Mobile Computing
Volume 2018, Article ID 9130910, 10 pages
https://doi.org/10.1155/2018/9130910

Research Article

A Low Power Impedance Transparent Receiver with Linearity Enhancement Technique for IoT Applications

Sizheng Chen, Tingting Shi, Lei Ma, Cheng Kang, Na Yan, and Hao Min

State Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China

Correspondence should be addressed to Na Yan; yanna@fudan.edu.cn

Received 3 November 2017; Revised 8 March 2018; Accepted 12 April 2018; Published 14 May 2018

Academic Editor: Christian Fager

A low power receiver with impedance transparent RF front end is presented. By using the 4-path passive mixer and the active feedback of LNA, the baseband impedance profile is further transferred to receiver input. While a LO-defined input matching is formed by RF front end, the linearity of entire receiver chain is improved. Furthermore, derivative superposition technique is employed to cancel the distortion of the CMOS LNA. A 3rd-order active-RC filter is designed with current-efficient feedforward compensated OTA. And a digital-to-time converter (DTC) assisted fractional-N all-digital phase-locked loop (ADPLL) is codesigned with receiver to meet the IoT requirements. The presented receiver is fabricated in 55 nm CMOS technology with an active area of 2.3 mm^2 and power consumption of 20 mW. Measurement results show that the receiver achieves 5.3 dB NF with 78 dB gain from 0.6 to 1 GHz, the RX out-of-band IIP3 is +8 dBm, and in-band IIP3 is −10 dBm, and the ADPLL achieves −94 dBc/Hz in-band PN and −120.5 dBc/Hz at 1 MHz offset.

1. Introduction

The need for low power and low cost transceivers has been growing with the expansion of portable wireless devices and wireless sensor networks. Because of big market potential and design challenges, narrow-band (NB) receivers have become the focus of industry and academic researches recently. Modern wireless protocols are released, such as the emerging NB-IoT [1] and the IEEE 802.11ah [2], to support IoT applications. Additionally, NB-IoT has been included as an important part of future fifth-generation (5G) mobile communication [3].

Different techniques are proposed in recent researches to realize the low power and low cost receiver for IoT protocols. Because of the superior performance (better noise and linearity) of NB LNAs, multiple narrow-band receivers are employed to cover the entire band of the operation. To provide high-Q frequency selectivity, each NB RX uses off-chip components, which increases the entire area and cost [4]. Reconfigurable receiver is able to select signals over a wide operation band. And one of the common challenges of these receivers is out-of-band interference. Academic researches have focused on using passive mixer to suppress the out-band blockers. A mixer-first receiver has an excellent linearity at the cost of large power dissipation and poor LO-to-RF isolation [5]. Others proposed a noise-cancelling receiver to achieve very low noise figure by employing two paths of downconversion which increases the hardware complexity [6], but extra calibration is needed to provide precise gain and phase matching.

In this work, an impedance transparent receiver architecture is proposed which only uses one downconversion path. The proposed reconfigurable RF front end employs an active feedback LNA to transfer the baseband filter character to the input of receiver, which can attenuate out-of-band interferers. By using the impedance mapping of passive mixer and the feedback of LNA, a LO-defined input matching is formed. To further improve the linearity of RX, a linearity enhancement technique called "derivative superposition [7]" is employed in the CMOS LNA.

This paper proposes a low power impedance transparent receiver with linearity enhancement technique. The description of the system architecture is given in Section 2; the design of the building blocks is shown in Section 3; the measured results are described in Section 4 and conclusions are provided in Section 5.

Table 1: Main specifications of receiver for IoT protocols.

Parameters	NB-IoT
RF frequency	699~915 MHz
Channel bandwidth	180 kHz
Max. receive level	−25 dBm
Sensitivity	<−109 dBm
Noise figure	<7 dB
P-1dB	>−25 dBm
OB-IIP3	>+7.75 dBm*
In-band IIP3	>−15.4 dB

*Range 2 of NB-IoT protocol.

2. System Description

2.1. System Specifications for the Receiver. Based on the IoT protocols [8], main specifications of the receiver are summarized in Table 1. Low power and low cost are the key features of IoT application. And the system specifications are briefly reviewed as follows.

2.1.1. Noise Figure. Sensitivity level of a receiver is very key requirement in a communication system because most of the other specifications are defined based on it. For the NB-IoT application with 180 kHz transmission bandwidth, the sensitivity level is around −109 dBm. The $\mathrm{SNR}_{\mathrm{min}}$ is 2.5 dB to cover all possible TBS (Transport Block Set) with QPSK modulation and code rate 1/3. Based on the requirements above, the noise figure of the receiver can be expressed as

$$\begin{aligned}\mathrm{NF} &= \mathrm{Sensitivity} \\ &\quad - \left(-174\,\mathrm{dBm} + 10\log \mathrm{BW} + \mathrm{SNR}_{\mathrm{min}}\right) - I_M.\end{aligned} \tag{1}$$

I_M is implementation and production margin. BW is the transmission bandwidth in Hz. Assuming I_M is 3 dB, it can be calculated that NF = 6.94 dB.

2.1.2. Nonlinearity. For RX nonlinearity, there are in-band and out-of-band IIP3 requirements. The in-band IIP3 of the RX is corresponding to the 1-dB compression point (P1dB). Since the maximum input level of the NB-IoT receiver is −25 dBm, the P1dB is −25 dBm. So the in-band IIP3 is −15.4 dB, which is 9.6 dB higher than P1dB. The out-of-band IIP3 is determined by out-of-band blocking parameters. According to [8], the interferer power is −30 dBm in range 2 (60~85 MHz frequency offset from desire signal), while the signal power is 6 dB above the reference sensitivity (about −109 dBm). The IIP3 estimated with 2.5 dB SNR is as follows (where P_{signal} is the power of signal):

$$\mathrm{OB\text{-}IIP3} = \frac{3P_{\mathrm{in}} - \left(P_{\mathrm{signal}} - \mathrm{SNR}\right)}{2} = 7.75\,\mathrm{dBm}. \tag{2}$$

For the sensitivity requirement of the protocol, LNA-first architecture should be employed. Compared with mixer-first receiver, the LNA is added for two reasons.

(1) LO-to-RF isolation can be improved by adding the LNA, which is one of the most challenging things in mixer-first receiver. The allowable emission level within receiver band is in range of −60 to −80 dBm. For example, according to [9], the LO leakage of mixer-first RX is about −48 dBm without calibration in 28 nm CMOS technology.

(2) Providing a gain in first stage is a power efficiency method to realize high sensitivity receiver. Due to lack of LNA, lots of current is burned in baseband transimpedance amplifier (TIA) to make the NF less than 8 dB in mixer-first receiver [5].

Because of the narrow-band profile, the 1/f noise and DC offset could degrade the sensitivity. A passive mixer is employed for its superiority on 1/f noise. And a DC offset cancellation circuit is designed.

Besides, it is difficult to achieve both high linearity and low power for RF front end, especially without the help of off-chip device (e.g., SAW, BAW). Compared with traditional method of using passive mixer at LNA output only, the proposed receiver is further mapping the impedance of mixer to the RX input with active feedback LNA to realize the input LO-defined impedance matching. The in-band of RX could be a problem due to the incremental gain of LNA. So the derivative superposition technique is utilized to cancel this distortion in LNA.

2.2. Receiver Architecture. The proposed receiver architecture is a suitable solution for IoT applications as shown in Figure 1, consisting of an impedance transparent receiver front end, a 3rd-order active-RC filter, a fractional-N frequency synthesizer, and SPI interface to configure the system. The local frequency generator consists of a divide-by-two circuit to generate a 25% duty-cycle LO from an on-chip all-digital phase-locked loop. A DTC-assisted fractional-N ADPLL with a TDC is employed in this work. Self-biased CMOS inverters are used to provide rail-to-rail swing to the gate of passive mixer. Compared with the traditional 50% duty-cycle LO, the 25% duty-cycle LO scheme [9] provides isolation timely between I- and Q-current-path. Therefore, conversion gain reduction and subsequent NF increase are prevented.

2.3. Noise Analysis of Receiver RF Front End. The receiver RF front end comprises an LNA, two separate passive mixers for in-phase (I) and quadrature-phase (Q), and a single-pole filter as a TIA which changes the current signal to voltage signal. The passive mixer is implemented with 4 nMOS transistors, which are connected with the output of LNA. According to [10], the output of 4-path passive mixer can be written as

$$\begin{aligned}S_{\mathrm{MIXER,current}} &= \sum_{n=-\infty}^{+\infty} a_n e^{jn\omega_{\mathrm{LO}}(t-(T/4)i)} \\ a_n &= \frac{1}{4} e^{-jn(\pi/4)} \sin c\left(\frac{n\pi}{4}\right).\end{aligned} \tag{3}$$

$S_{\mathrm{MIXER,current}}$ is the current gain of 4-path passive mixer and a_n is the coefficients of the Fourier series. The receiver conversion gain and NF can be calculated as follows:

$$A_{\mathrm{RX\_RF}} = \frac{1}{2} \cdot g_{m,\mathrm{LNA}} \cdot \frac{Z_{\mathrm{O,LNA}}\left(\omega_{\mathrm{LO}}\right)}{Z_{\mathrm{O,LNA}}\left(\omega_{\mathrm{LO}}\right) + R_{\mathrm{sw}}} \cdot a_{-1} \cdot R_F \tag{4}$$

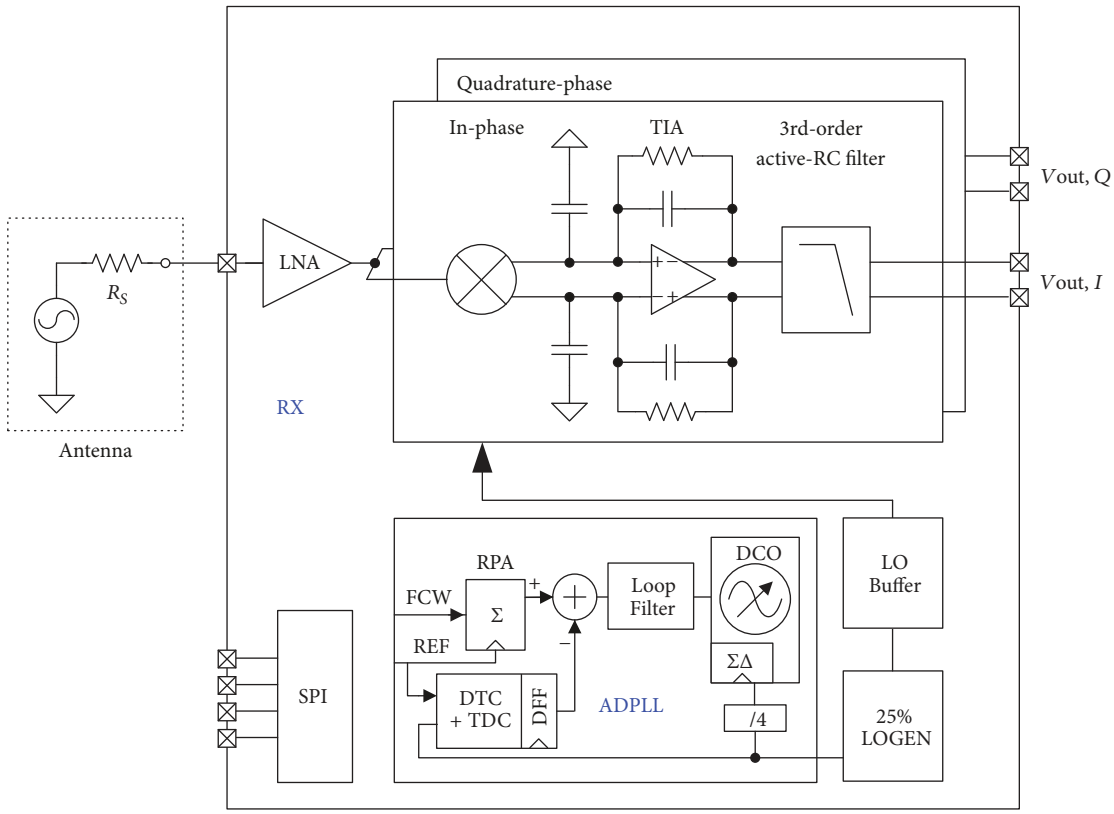

Figure 1: Proposed receiver architecture.

$$\mathrm{NF} = 1 + \frac{\overline{I_{n,\mathrm{LNA}}^2}}{kTR_S \cdot g_{m,\mathrm{LNA}}^2} + \frac{R_{sw} \cdot R_F}{R_S \cdot A_{\mathrm{RX\_RF}}} \left(\sum_{n=0}^{+\infty} \frac{a_{-n}}{Z_{\mathrm{O,LNA}}(n\omega_{\mathrm{LO}}) + R_{\mathrm{sw}}} \right)^2 + \frac{\overline{V_{n,\mathrm{TIA}}^2} \left(1 + R_F/C_{\mathrm{O,LNA}}\right)^2}{4kTR_S \cdot A_{\mathrm{RX\_RF}}^2} + \frac{R_F}{R_S \cdot A_{\mathrm{RX\_RF}}^2}. \quad (5)$$

$g_{m,\mathrm{LNA}}$ is the transconductance of the LNA. $Z_{\mathrm{O,LNA}}$ and $\overline{I_{n,\mathrm{LNA}}^2}$ are, respectively, the output impedance and output current noise of the LNA. R_{sw} is the mixer switch on-resistance. And R_F is the feedback resistance of TIA. The OTA noise is modeled by $\overline{V_{n,\mathrm{TIA}}^2}$ as shown in Figure 2. Since the thermal noise of passive mixer switches is white noise, all parts of harmonics of the LO will be folded into baseband which is shown in third part of (5). From this equation, we can see that the LNA stage decreases the noise contribution from mixer and TIA.

2.4. Impedance Transparent Profile. Compared with conventional architecture of just employing passive mixer at LNA output, the high-Q filtering profile of passive mixer is further transferred to the input of the receiver in our proposed RF front end. So it can relax the requirement on LNA linearity while achieving a relatively low NF. To figure out how the impedance transparent affects the linearity of the RX, the benefit of a filter is added before or after LNA is analyzed as shown in Figure 3.

To simplify analysis, only the nonlinearity of LNA and mixer are considered. The filter has two rejections as shown in Figure 4, H_{blocker1} and H_{blocker2} for different blockers at F_{blocker1} and F_{blocker2}. A_1 and A_2 represent the amplitudes of the two blockers. For a memoryless nonlinear system, the input/output characteristic can be modeled as a polynomial [11].

Then output IM3 of this cascaded receiver stages (LNA and mixer) is as follows:

$$A_{\mathrm{IM3,baseband}} = \underbrace{G_{\mathrm{LNA}} G_{\mathrm{MIXER}} \frac{A_1^2 A_2}{A_{\mathrm{IIP3,LNA}}^2}}_{\text{Output IM3 of LNA}} + \underbrace{G_{\mathrm{LNA}}^3 G_{\mathrm{MIXER}} \frac{A_1^2 A_2}{A_{\mathrm{IIP3,MIXER}}^2}}_{\text{Output IM3 of MIXER}}. \quad (6)$$

G_{LNA} and G_{MIXER} are the gain of the LNA and the mixer stage, respectively. In case one, the filter is added after the LNA. The resulting IM3 is as follows:

$$A_{\mathrm{IM3,baseband}} = \underbrace{G_{\mathrm{LNA}} G_{\mathrm{MIXER}} \frac{A_1^2 A_2}{A_{\mathrm{IIP3,LNA}}^2}}_{\text{Output IM3 of LNA}} + \underbrace{\frac{G_{\mathrm{LNA}}^3 G_{\mathrm{MIXER}}}{H_{\mathrm{blocker1}}^2 H_{\mathrm{blocker2}}} \frac{A_1^2 A_2}{A_{\mathrm{IIP3,MIXER}}^2}}_{\text{Output IM3 of MIXER}}. \quad (7)$$

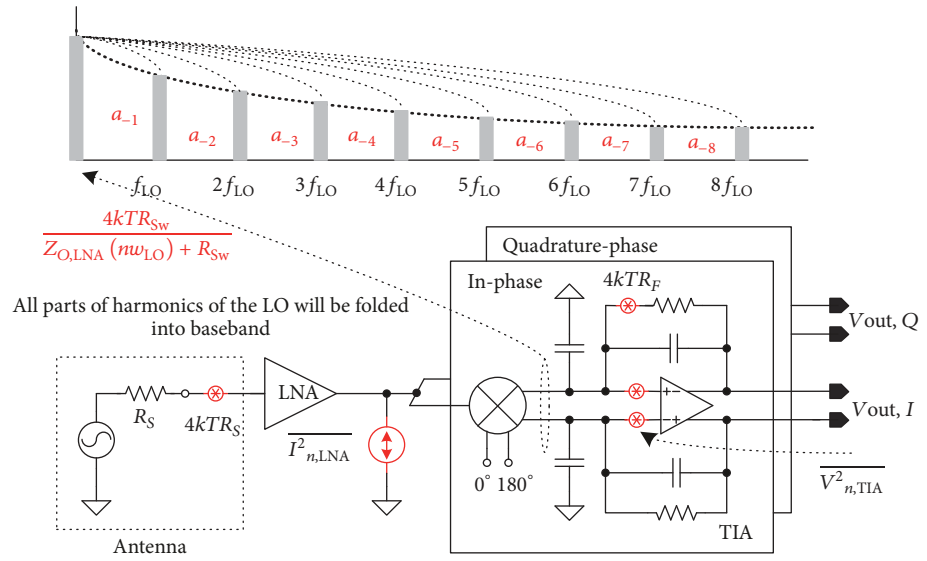

Figure 2: Noise sources inside the RF front end.

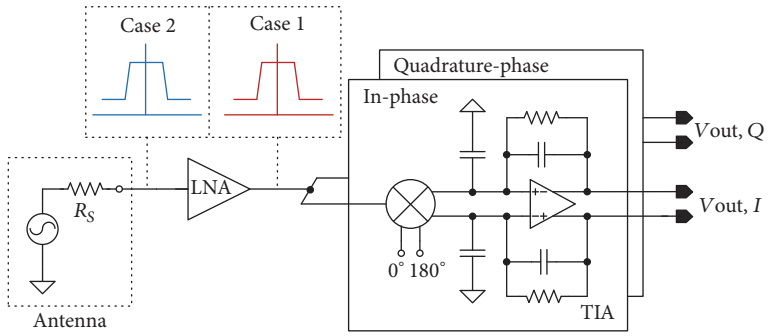

Figure 3: Two cases to analyze the effect of impedance transparent.

From (7), we can see that blockers are not attenuated at the input of LNA. But the IM3 levels from the mixer stage are significantly reduced, which helps to improve the IM3 level by a few dB. Therefore, the RX IIP3 is limited by LNA stage in this case. By adding the filter in case two, the IM3 at baseband is calculated as

$$A_{\text{IM3,baseband}} = \underbrace{\frac{G_{\text{LNA}}G_{\text{MIXER}}}{H^2_{\text{blocker1}}H_{\text{blocker2}}}\frac{A_1^2A_2}{A^2_{\text{IIP3,LNA}}}}_{\text{Output IM3 of LNA}} + \underbrace{\frac{G^3_{\text{LNA}}G_{\text{MIXER}}}{H^2_{\text{blocker1}}H_{\text{blocker2}}}\frac{A_1^2A_2}{A^2_{\text{IIP3,MIXER}}}}_{\text{Output IM3 of MIXER}}. \quad (8)$$

In this case, it can be shown that IM3 level from both the LNA stage and mixer stage is attenuated. So the IIP3 of the entire receiver is significantly improved. If the blocker IM3

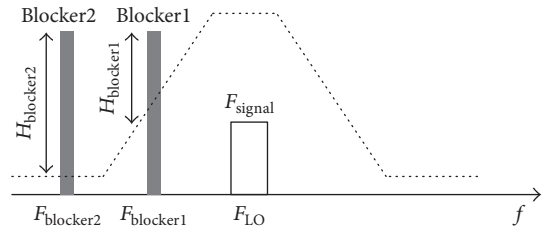

Figure 4: The rejection of the filter for two different blockers.

improvement due to the smaller voltage swing is ΔIM_3, the entail IIP3 improvement is

$$\Delta\text{IIP3 (dB)} = H_{\text{blocker1}}\text{ (dB)} + \frac{1}{2}H_{\text{blocker2}}\text{ (dB)} + \frac{1}{2}\Delta\text{IM}_3\text{ (dB)}. \quad (9)$$

If the blocker 1 is attenuated by 10 dB and blocker 2 is attenuated by 6 dB, while ΔIM_3 is 3 dB, the IIP3 improvement is about 14.5 dB.

In our proposed receiver front end, an active feedback LNA is used to further map the bandpass filtering characteristic of 4-path passive mixer to the input of RX, which has the same effects as case 2. So it has a suitable tradeoff between noise and out-of-band attenuation early in the receiver chain.

According to N-path filtering theory, the frequency response of the filter is centered at the LO frequency. Because of the reciprocal character of passive mixer, the RF signal is down converted to baseband. After being shaped by baseband load, it is up converted back to RF, which transfers the load response to LO frequency. The input impedance of the mixer can be calculated as follows (where R_{sw} is the switch on-resistance, $Z_{baseband}$ is the baseband impedance, and R_{sh} is equivalent resistance of harmonic mixing) [5]:

$$Z_{mixer}(\omega) = R_{sw} + \frac{2}{\pi^2} Z_{baseband}(\omega - \omega_{LO}) \| R_{sh}. \quad (10)$$

So the LNA load impedance can be shown to be consisting of the output impedance of LNA and the baseband impedance upconverted by the passive mixer. The input stage of receiver is a CMOS LNA with a shunt-shunt feedback [12]. With the negative feedback, the impedance properties at the baseband can be mapped to the LNA input as

$$R_{in} = \frac{1/g_{m2} + R_{F,LNA}}{1 + g_{m1} \cdot R_{L,LNA} \| Z_{mixer}(\omega)}. \quad (11)$$

$R_{F,LNA}$ and $R_{L,LNA}$ are feedback resistance and load resistance of LNA, respectively. g_{m1} and g_{m2} are the transconductance of main amplifier transistor and feedback transistor, respectively. $Z_{mixer}(\omega)$ is the input impedance of passive mixer, which has a bandpass impedance characteristic. Since the input resistance of active feedback LNA is inversely proportional to the LNA gain, making the baseband impedance further transferred to the LNA input. The in-band impedance is matched to 50 Ohms, making the input impedance matched at LO frequency only; thus the power of out-of-band blockers are reflected at RX input. The reduction in the voltage gain out of band causes the impedance to increase instead which means that the shape of the impedance is inverse to the shape of the impedance at the output of the LNA. Simulated s-parameters and input impedance of the front end using steady-state analysis are shown in Figure 5.

3. Building Block Designs

3.1. LNA. Comparing with mixer-first receiver, LNA-first architecture has better noise and LO-to-RF isolation performance. And impedance transparent character is discussed in Section 2.2. A feedback buffer is added between the LNA output and input, which is used to further map the bandpass filtering characteristic of 4-path passive mixer to the input of LNA. Since the receiver noise figure is dominated by the LNA, it should be carefully designed. According to [12], the noise figure of LNA can be calculated as

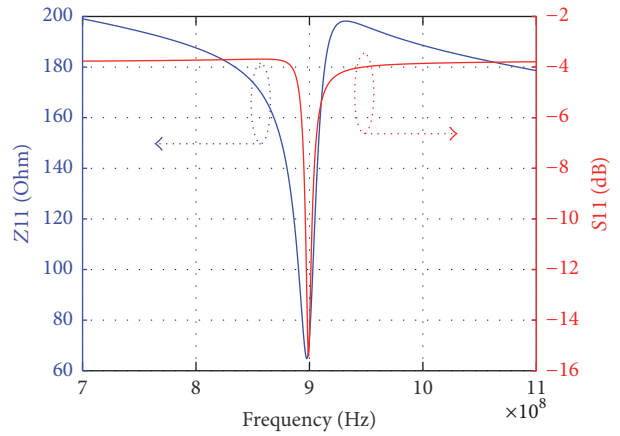

Figure 5: Simulated Z11 and S11 of receiver RF front end.

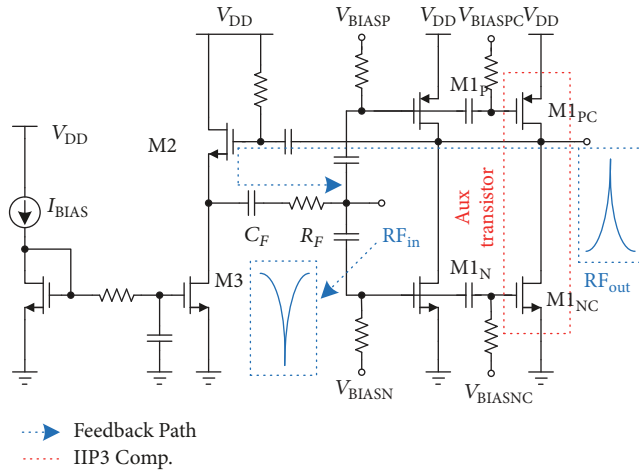

Figure 6: Schematic of the presented CMOS LNA.

$$\begin{aligned} F &= F_{RS} + F_{M1} + F_{RF} + F_{M2} + F_{RL} + F_{MB} \\ &= 1 + \frac{\gamma_1 R_S}{g_{m1}} \left(\frac{2 + A_V}{1 + A_V} \right)^2 + \frac{R_F}{R_S (1 + A_V)^2} \\ &\quad + \frac{\gamma_2}{1 + A_V} \left[1 - \frac{R_F}{R_S (1 + A_V)} \right] \\ &\quad + \frac{1}{g_{m1} R_S A_V} \left(\frac{2 + A_V}{1 + A_V} \right)^2 \\ &\quad + \gamma_B g_{mB} R_S \left[1 - \frac{R_F}{R_S (1 + A_V)} \right]^2. \end{aligned} \quad (12)$$

There is a negative item in the equation above, so the noise factor can be optimized with the degree of freedom brought by the active feedback. The layout parasitic is also significantly affecting the NF. The noise of gate resistances is directly amplified to the output; low resistance metal layers should be used for gate connections.

As shown in Figure 6, main amplifier with CMOS structure is used in LNA, which increases 2x current

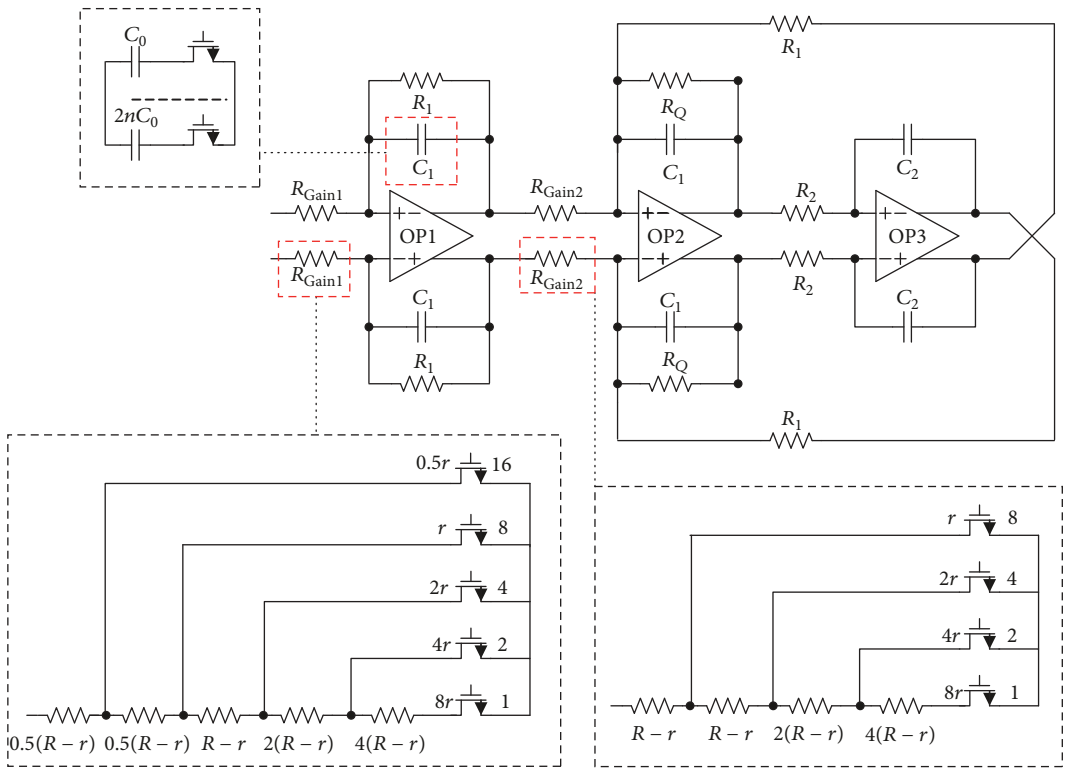

Figure 7: The proposed architecture of 3rd-order Butterworth low-pass active-RC filter.

efficiency. CMOS LNA can also cancel out the second order nonlinearity by properly sizing. A linearization technique called "derivative superposition" [7, 15] is used to improve the linearity of LNA because it determines the linearity of whole RX. The third derivatives (g3) of drain current from the main and auxiliary transistors are added to cancel distortion. Because g3's sign is different at the moderate and strong inversion region, zero g3 can be created by proper biasing the transistors. The auxiliary inverter only contains weak-inversion transistors, resulting in much smaller power consumption than the common feedforward technique.

3.2. Filter. Figure 7 is the proposed 3rd-order Butterworth low-pass filter. The filter consists of two main stages. For higher linearity, the Tow-Thomas biquad filter is arranged after a first-order filter. Programmable resistor and capacitor arrays are designed to adjust gain and compensate for process variations.

Feedforward compensated amplifier has less power dissipation than miller-compensated opamps when reaching the same design index [16]. A typical two-stage feedforward compensated amplifier is used in this work, as shown in Figure 8. To further lower power and area, local common-mode feedback circuit is applied. To meet the demand of ripple (<0.2 dB), the GBW of op1, op2, and op3 in Figure 6 are 400 MHz, 200 MHz, and 200 MHz, respectively.

For high gain filter, it is necessary to eliminate input DC offset. The DC offset cancellation (DCOC) circuit is shown in Figure 9. The low-pass feedback circuit will make the filter indicate high-pass feature at relatively low frequency.

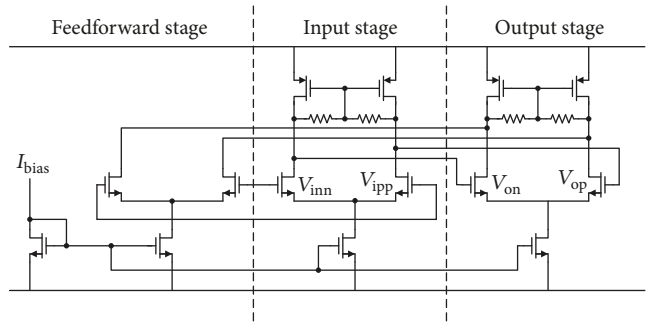

Figure 8: Schematic of two-stage feedforward compensated opamp.

3.3. ADPLL. Based on the blocking requirement, the codesign between the RF front end and ADPLL is necessary. The LO phase noise at 1 MHz offset should be less than −116 dBc/Hz with 6 dB margin. Both of the effects of reciprocal mixing of the blocker and the white noise introduced to signal band are considered. A DTC-assisted fractional-N ADPLL is employed with a time-amplified TDC, as shown in Figure 10. The TDC employs time amplifier (TA) realizing fine resolution. DTC is used with phase prediction algorithm to reduce the detection range of TDC. $\Delta\sum$-DTC

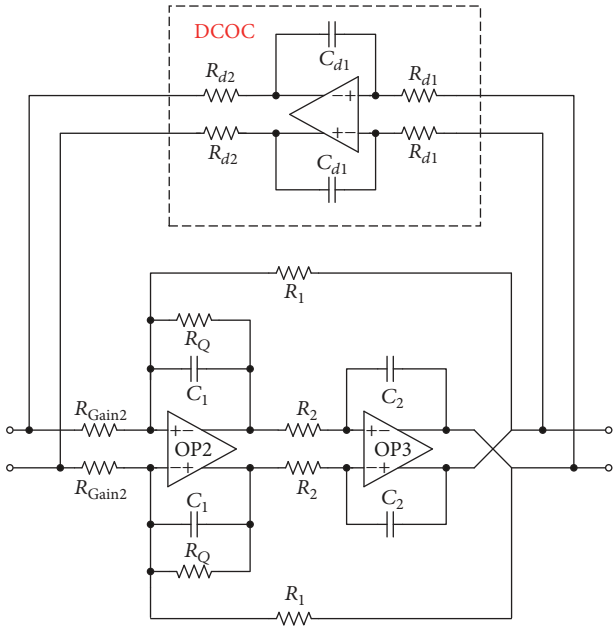

Figure 9: DCOC circuit of two-stage low-pass filters.

can be cascaded with DTC to suppress the spur induced by DTC quantization. Autocontroller algorithm and gear-shift technique helps to reduce the locking time to less than 20 us.

TDC and DCO are the most power-consuming blocks in the traditional ADPLL, so some techniques are used to lower power dissipation of these parts. Firstly, TDC snapshot is utilized to reduce the sampling rate from CKV to CKVS (=FREF), and the DTC can reduce the TDC detection range, which contributes to a prominent power reduction. Secondly, a low-supply structure DCO is designed in this work, which consumes just 900 uW at 1.5–2.05 GHz. A TA-TDC is designed to achieve high quantization to improve in-band phase noise. The DCO is followed by an inductor-less 2x divider to provide a reasonable input frequency for the phase digitization circuits. The divider generates four 90°-spaced phases.

4. Measured Results

This chip is fabricated in SMIC 55 nm 1P7M CMOS technology. Figure 11 shows the die photograph of the receiver. The core area of the chip is 2.3 mm × 1 mm, and the ADPLL occupied 1 mm × 1.2 mm due to the inductor of DCO.

As shown in Figure 12, the in-band phase noise is about −95 dBc/Hz and the out-band phase noise is about −120 dBc/Hz at 1 MHz frequency offset, which can satisfy the requirement of NB-IoT protocol [8]. The rms jitter is about 1.1 ps which is integrated from 1 kHz to 10 MHz. The whole power consumption of ADPLL is about 4 mW.

The measured S11 of the receiver with different LO frequency is shown in Figure 13. Using the SPI the ADPLL was set up to LO frequency, respectively (1.2 GHz/1.4 GHz/1.6 GHz/1.8 GHz/2 GHz). Then the LO power was expected as 5 dBm. And the received signal is swept from *F*LO −100 MHz to *F*LO +100 MHz. It shows that S11 < −10 dB over a 0.6–0.9 GHz RF range. The matching point is tunable with LO frequency and forms a narrow-band matching character which can improve the linearity of the receiver.

Figure 14 shows the measured baseband noise figure of the receiver. We measured a minimum noise figure of 5.3 dB at 1 MHz with the LO frequency of 900 MHz. Both the simulated and measured NF are in good agreement. The simulated result is about 1 dB lower than the measured one. The NF discrepancy is mainly due to layout parasitic which can lower the transconductance of LNA and the inaccuracies of the noise model in simulation.

The OB-IIP3 is measured at LO frequency of 900 MHz. Two blockers with −25 dBm input power are injected. IIP3 is measured at different frequency offsets. Figure 15 shows the test result of the OB-IIP3. It shows that due to the effect of impedance mapping, with the increase of the offset frequency, IIP3 increases. The highest point of linearity is mainly limited by the on-resistance of mixer and the linearity of LNA. The slope of the change in linearity is mainly limited by the capacitance size before the TIA. The in-band IIP3 is about −10 dBm, and the out-band IIP3 is +8 dBm at 60 MHz offset.

The OB-IIP2 is measured at LO frequency of 900 MHz as the IIP3 test method. Two blockers with −25 dBm input power are injected. And two blockers are separated by 1 MHz, with an offset from LO frequency. Figure 16 shows the test result of the IIP2. It shows that, due to the effect of impedance mapping, with the increase of the offset frequency, IIP2 increases. The out-band IIP2 is greater than +39 dBm without any calibration. This IIP2 is limited by the mixer mismatch and second nonlinearity of the gain stages. Since a CMOS LNA architecture is used in this work, IIP2 is improved in the proposed receiver. The measured result of this impedance transparent receiver is summarized in Table 2 with comparisons of prior arts. The proposed low power RX architecture has a suitable noise figure and linearity for IoT application and shows a good out-of-band blocker tolerance.

5. Conclusion

A low power impedance transparent receiver for IoT application is proposed in this paper. A reconfigurable receiver with tunable channel filtering and narrow-band input matching at RX input is presented. Passive mixer and active feedback LNA are used in the receiver to further map the baseband impedance to RF input. A 3rd-order active-RC filter is employed in the receiver for meeting the IoT requirements. The filter achieves a relatively low power with the use of current-efficient feedforward compensated OTA. Digital controlled resistor and capacitor arrays are flexible for gain and bandwidth tuning. A DTC-assisted fractional-*N* ADPLL is employed with a time-amplified TDC. By utilizing blocker filtering and derivative superposition techniques, the proposed RX achieves NF of 5.3 dB with +8 dBm OB-IIP3

Table 2: Comparison with prior arts.

Parameter	This work	[13]	[14]	[5]	[6]
Selective input matching	Yes	No	No	Yes	Yes
Architecture	LNA with active feedback	Balun LNA	Current mode LNA	Mixer first	Noise cancelling
Operation frequency	0.6~1 GHz	0.75~0.96 GHz	1.0–5.2 GHz	0.1–2.4 GHz	0.08–2.7 GHz
Gain	78 dB	20~104 dB	23 dB	40–70 dB	72 dB
Noise figure	5.3 dB	5.1/4 dB	6.5 dB	7 dB @ 2 GHz	1.9 dB
IB-IIP3	−10 dBm	−6.2 dBm @ Min Gain	-	−67 dBm	−18 dBm
OB-IIP3	+8 dBm	-	−1.5 dBm	+25 dBm	+13.5 dB
IIP2	39 dBm	45 dBm @ Min Gain	-	+56 dBm	+85 dBm
Technology	55 nm CMOS	180 nm CMOS	130 nm CMOS	65 nm CMOS	40 nm CMOS
Core power	16 mW RX +4 mW ADPLL	25 mW @1.7V	13 mW RX +22 mW LO	37–70 mW	35.1–78 mW

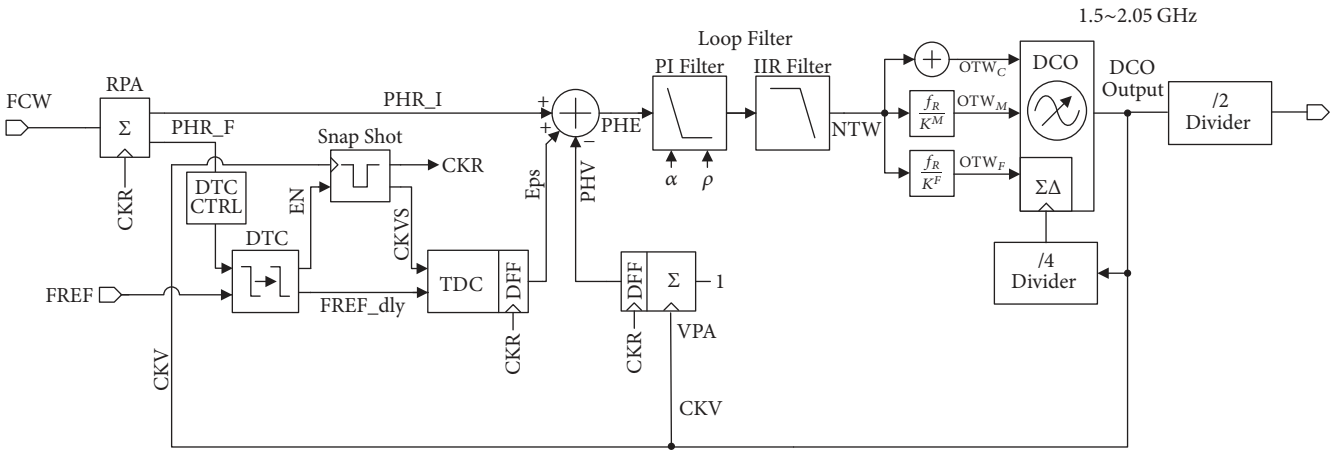

Figure 10: ADPLL architecture.

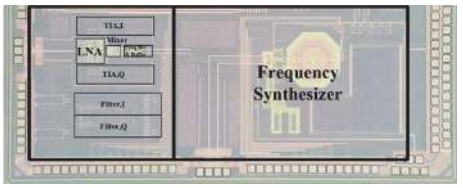

Figure 11: Die photograph of the chip in 55 nm CMOS.

Figure 12: Measured phase noise of the frequency synthesizer.

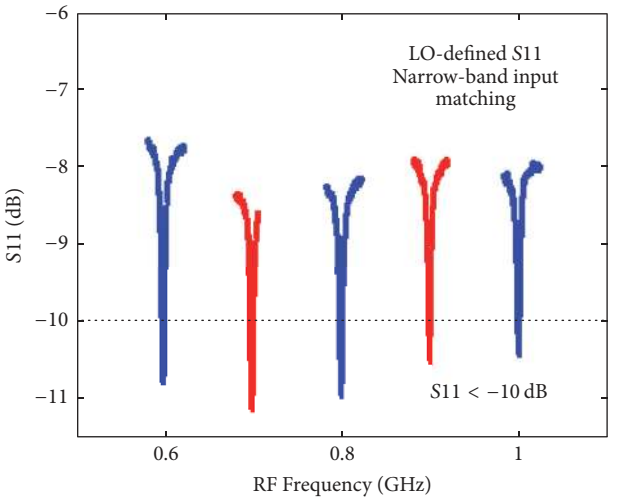

Figure 13: Measured S11 of the receiver with different LO frequency.

while consuming 16 mW. The ADPLL in-band phase noise is about −95 dBc/Hz and the out-band phase noise is about −120 dBc/Hz at 1 MHz frequency offset, while consuming

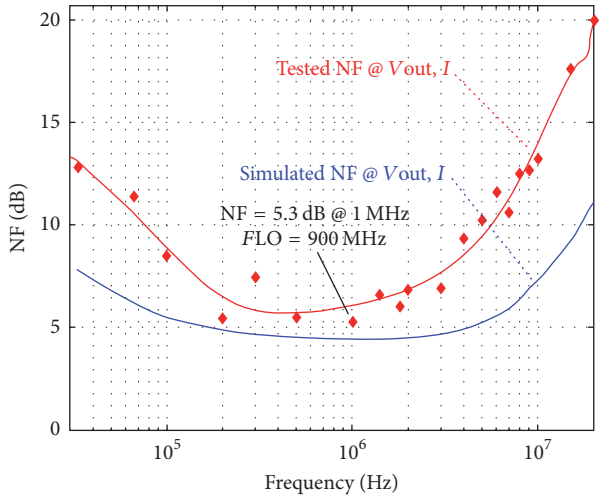

Figure 14: Measured baseband noise figure of the receiver (*FLO* = 900 MHz).

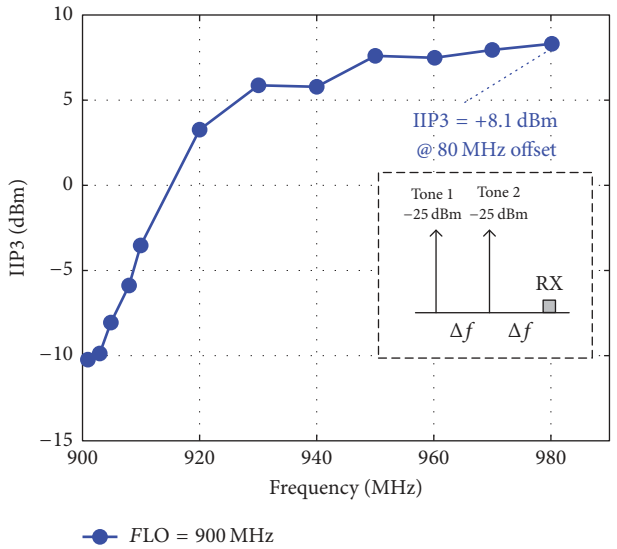

Figure 15: Measured IIP3 at 900 MHz for different frequency offsets.

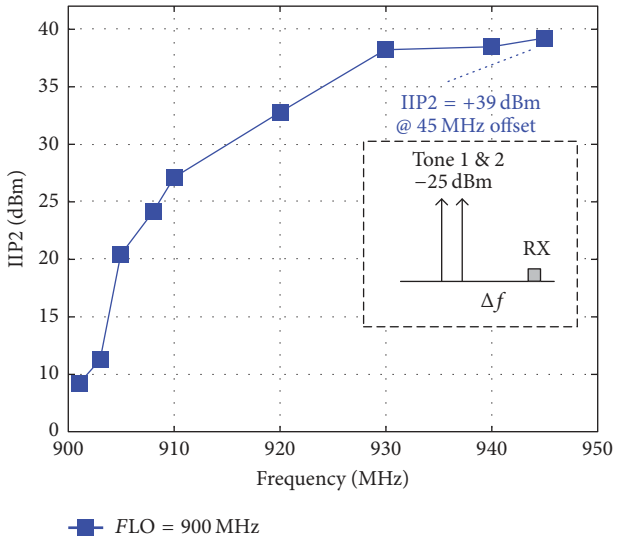

Figure 16: Measured IIP2 at 900 MHz for different frequency offsets.

4 mW. The proposed receiver architecture can be used for low power IoT application, such as IEEE 802.11ah and NB-IoT.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

This work is supported by National Natural Science Foundation of China (nos. 61574045 and 61774048), National Science and Technology Major Project (no. 2016ZX03001012-003), and National High Technology Research and Development Program (no. 2015AA016601-005).

References

[1] R. Ratasuk, B. Vejlgaard, N. Mangalvedhe, and A. Ghosh, "NB-IoT system for M2M communication," in *Proceedings of the 2016 IEEE Wireless Communications and Networking Conference, WCNC 2016*, April 2016.

[2] M. Park, "IEEE 802.11ah: Sub-1-GHz license-exempt operation for the internet of things," *IEEE Communications Magazine*, vol. 53, no. 9, pp. 145–151, 2015.

[3] J.-P. Bardyn, T. Melly, O. Seller, and N. Sornin, "IoT: The era of LPWAN is starting now," in *Proceedings of the 42nd European Solid-State Circuits Conference, ESSCIRC 2016*, pp. 25–30, September 2016.

[4] H. Hedayati, W.-F. A. Lau, N. Kim, V. Aparin, and K. Entesari, "A 1.8 dB NF blocker-filtering noise-canceling wideband receiver with shared TIA in 40 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1148–1164, 2015.

[5] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, 2010.

[6] D. Murphy, A. Hafez, A. Mirzaei et al., "A blocker-tolerant wideband noise-cancelling receiver with a 2dB noise figure," in *Proceedings of the 59th International Solid-State Circuits Conference (ISSCC '12)*, pp. 74-75, San Francisco, Calif, USA, February 2012.

[7] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 571–580, 2005.

[8] Technical Report for BS and UE Radio Transmission and Reception (Release 13), document TS 36.802, 3GPP.

[9] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "The Blixer, a wideband balun-LNA-I/Q-mixer topology," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2706–2715, 2008.

[10] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2353–2366, 2010.

[11] R. Behzad, *RF Microelectronics*, vol. 2, Prentice Hall, New Jersey, USA, 1998.

[12] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, "Low-area active-feedback low-noise amplifier design in scaled digital CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2422–2433, 2008.

[13] Z. Song, X. Liu, X. Zhao, Q. Liu, Z. Jin, and B. Chi, "A Low-Power NB-IoT Transceiver With Digital-Polar Transmitter in 180-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2569–2581, 2017.

[14] J. Kim and J. Silva-Martinez, "Low-power, low-cost CMOS direct-conversion receiver front-end for multistandard applications," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2090–2103, 2013.

[15] Y. S. Youn, J. H. Chang, K. J. Koh, Y. J. Lee, and K. H. Yu, "A 2GHz 16dBm IIP3 low noise amplifier in 0.25μm CMOS technology," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 452–507, San Francisco, CA, USA.

[16] N. Krishnapura, A. Agrawal, and S. Singh, "A high-IIP3 third-order elliptic filter with current-efficient feedforward-compensated opamps," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 4, pp. 205–209, 2011.