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A Low-Power Integrated Circuit for Adaptive Detection of Action Potentials in Noisy Signals

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Abstract—**The advent of microelectrode arrays allowing for the simultaneous recording of 100 or more neurons is leading to significant advances in science and medicine. However, the amount of data generated by these arrays presents a technical challenge if these systems are ever to be fully implanted for neuroprosthetic applications. We have developed an algorithm to perform real-time data reduction by detecting action potentials, or "spikes," embedded in a noisy signal. This algorithm is simple enough to be implemented in a mixed-signal integrated circuit consuming less than 60 μW of power. Experimental results from a chip show that the circuit is able to adaptively set a spike detection threshold above the background noise level of a signal.**

Keywords—**Spike detection, integrated circuit, neural recording, low-power circuit design, neuroprosthesis, CMOS**

I. Introduction

There is an increasing need in science and medicine for technologies that allow for the simultaneous recording of action potentials, or "spikes," from populations of tens or hundreds of neurons. Recent advances in microelectrode array technology have allowed researchers perform up to 100 parallel extracellular recordings in close proximity [1], [2]. However, the electronic circuitry necessary to amplify and process the signals from 100 or more electrodes is still too bulky and power hungry for implantation with the electrode array.

While recent advances have been made in the design of low-power neural signal amplifiers [3]-[5], little has been done to address the inevitable data bottleneck that comes with a multielectrode recording system. Consider the case of a 100-channel neural recording system where each channel is amplified and then passed to an analog-to-digital converter that digitizes each channel at 30 kSamples/sec with a resolution of 10 bits. The data rate of this 100-channel system is 30 Mbit/sec. This data must be delivered transcutaneously to an external receiver via an RF or optical link. Transmitting data at this rate would likely require a transmitter that dissipates power at a level unsafe for small implants, since small levels of chronic heat dissipation (80 mW/cm^2) can lead to tissue damage [6].

When one considers the nature of typical neural signals, it is clear that far too much information is being transmitted in the above example. For many scientific and neuroprosthetic applications, the only relevant information is the presence and timing of action potentials. Cortical neurons exhibit firing rates around 10 Hz, and in a 100-channel system, the "address" of each spike can be encoded in a 7-bit number representing its electrode of origin. If we transmit an address only when a spike occurs, our data rate can be reduced to an average of 7 kbit/sec, which could easily be transmitted from an implanted low-power RF transmitter operating at a moderate carrier frequency.

The remaining problem is how to perform this data reduction from a noisy analog waveform to identified spikes in a small, low-power device. The amplitude of spikes recorded extracellularly can vary widely from one electrode to the next depending on the relative position and orientation of the recording site and the axon carrying the impulse. Additionally, background noise caused by distant neural activity, electrode noise, and electronic noise in the preamplifier can vary with time, temperature, and electrode position.

In this paper, we present an algorithm for the automatic detection of spikes in a noisy waveforms by adapting a threshold that stays above the background noise level. We implement this algorithm as a low-power CMOS integrated circuit and report on its performance.

II. Adaptive Spike Detection Algorithm

For the development of our adaptive spike detection algorithm, we assumed the input signal to be a linear combination of bandlimited Gaussian noise and transient action potential signals having a duration of approximately 1.0 msec. We assume that the signal from the extracellular recording electrode has been high-pass filtered by a preamplifier so that low-frequency local field potentials (LFPs) in the 0.1-30 Hz range have been attenuated. (It is common practice to use a low-frequency cut-off between 100 Hz and 300 Hz for spike recordings.)

We define a spike detector as a system that produces a logical "true" output when a spike is present and produces a logical "false" output when a spike is not present. The goal of our spike-detection algorithm is to adaptively set a detection threshold that is low enough to capture action potentials, but high enough to reject occasional peaks in the background noise. We are assuming Gaussian background noise having a mean of zero. (Since the signal has been high-pass filtered, any dc offset has been removed.) Therefore the noise is entirely described by its rms value, which is equivalent to its standard deviation, σ.

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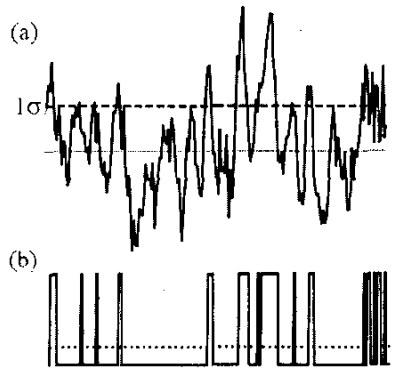

Fig. 1. (a) If Gaussian noise is passed through a comparator having a threshold set to the rms value of the noise (1σ), the resulting digital signal (b) made up of 0's and 1's has a dc level (dotted line) of 0.159.

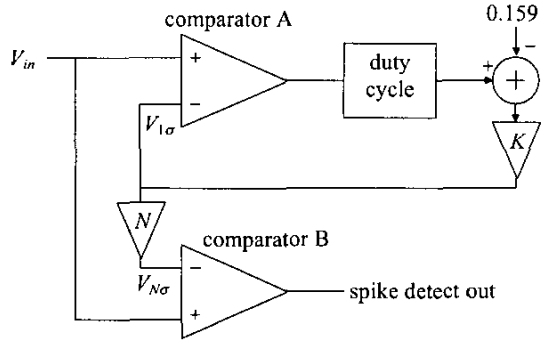

Fig. 2. Block diagram of the adaptive spike detection algorithm.

If we can measure the rms level σ of the background noise, we can set a threshold to some positive multiple of σ and reject all but a vanishingly small fraction of the background noise. For example, with a threshold of 5σ, the probability of Gaussian noise triggering the spike detector is approximately 3×10^{-7}.

To develop a method for measuring σ, we observe that if a threshold is set at σ, the probability of Gaussian noise exceeding this threshold is 0.159. Fig. 1(a) shows a noise waveform and a threshold level of 1σ. After comparing the noise with this threshold, we get a digital waveform having a *duty cycle* (i.e., the fraction of time the waveform is high) of 0.159 [see Fig. 1(b)]. The duty cycle is proportional to the dc level of this digital waveform, and we can use this signal as feedback to servo a reference voltage to the 1σ level of the waveform.

Fig. 2 shows a block diagram of the proposed adaptive spike detection algorithm. Comparator A is used in a feedback loop (with a gain of K) that servos the duty cycle of its output to 0.159, thus setting $V_{1\sigma}$ to the rms level of the input waveform. This voltage is then amplified by a constant N typically having a value of five or greater. The resulting voltage $V_{N\sigma}$ is used as the threshold level for Comparator B. Thus, the circuit performs spike detection using a specified multiple of the background noise rms value.

The presence of spikes in the waveform will lead to errors in our estimate of the noise rms level since the $V_{1\sigma}$ feedback loop does not distinguish between spikes and background noise. However, if the spikes are approximately ac balanced (as most biphasic spike waveforms are) and occur relatively infrequently, they should have little effect on the rms noise estimate. In cortical neurons, for example, firing rates around 10 Hz are common, and action potentials recorded extracellularly have a duration of approximately 1 msec, so spikes are present only about 1% of the time. Nevertheless, a more precise analysis of this source of error should be undertaken in the future.

We expect this algorithm to work well for background noise which is not precisely Gaussian, although this has not yet been tested. By selecting N to be sufficiently large, a conservative threshold can be set for noise that deviates from a true Gaussian distribution.

III. Circuit Implementation

We implemented the adaptive spike detection algorithm in a CMOS integrated circuit with the goal of minimizing power consumption and chip area. We used a commercially-available 1.5-μm 2-metal, 2-poly CMOS process available through MOSIS. The circuit was completely integrated, using no off-chip components.

A schematic of the adaptive spike detection circuit is shown in Fig. 3. Comparators A and B are implemented using standard regenerative latch-and-hold topologies [7]. The duty cycle of comparator A is calculated using an operational transconductance amplifier (OTA) to realize a g_m-C low-pass filter. By biasing this OTA in the subthreshold region, cutoff frequencies below 1 Hz may be achieved [8]. The high-frequency oscillations of the digital waveform are attenuated leaving only the dc level, which is proportional to the duty cycle of the waveform. By taking a "running average" of the duty cycle using this leaky integrator, the circuit is able to adapt to time-varying levels of background noise. The time constant of this filter sets the adaptation time constant.

An *n*MOS differential pair is used to compare the output of the low-pass filter to the reference voltage $V_{duty} = 0.159V_{DD}$, which corresponds to a low-pass filter output indicating Comparator A is operating at the 1σ threshold level. Current from one leg of the differential pair is mirrored using a *p*MOS current mirror and driven into two resistors in series. These resistors convert the current into two voltages: $V_{1\sigma} = IR$ and $V_{5\sigma} = 5IR$. To save chip area, these resistors were implemented as *n*MOS transistors operating in the deep triode (linear) region. By sizing the transistors appropriately, a drain-to-source resistance R of approximately 10 kΩ was obtained.

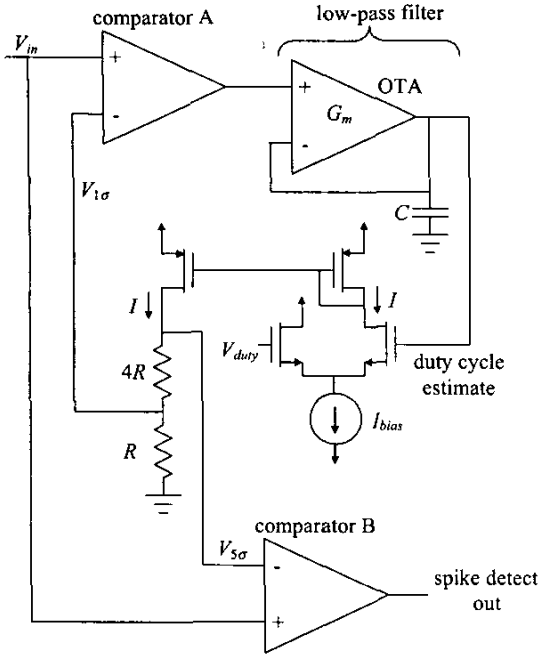

Fig. 3. Schematic of the adaptive spike detection circuit.

Since latch-and-hold comparators were used, a clock signal must be provided to trigger comparisons and then reset the comparators. We used a clock frequency of 6 kHz, corresponding to a period of 0.167 msec. This sub-millisecond period ensures that the circuit will not miss a spike.

IV. Results

A. Comparator Precision

Before testing the adaptive spike detector, we first characterized the comparators independently. A significant source of error in CMOS integrated circuits is device mismatch [9]. Two transistors fabricated side-by-side with identical dimensions will not behave identically due to random variations in size and implanted charge introduced in the fabrication process. In our circuit, device mismatch affects the precision of our comparators. Ideally, the output of a comparator should switch when the difference between the two input voltages crosses zero. Real comparators exhibit an small offset voltage that varies from one circuit to the next across a chip.

We measured the input-referred offset voltage of 20 fabricated comparators to assess the minimum resolution at which these circuits could reliably operate. The measured input-referred offset voltage of 20 comparators (four each on five separate chips) varied from -0.45 mV to +3.35 mV. The mean offset voltage was +1.75 mV, and the standard deviation was 1.12 mV.

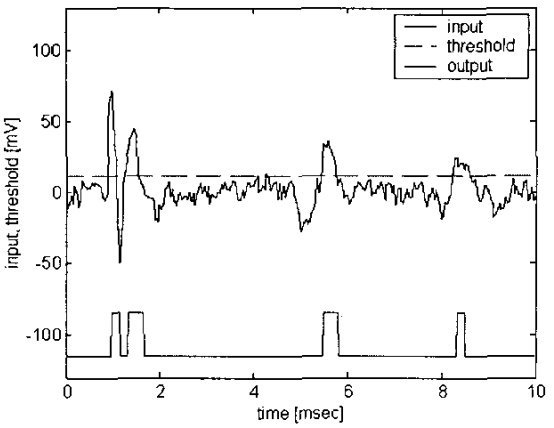

Fig. 4. Measured output of adaptive spike detection chip for input amplitude of 70 mV.

Neural signals recorded extracellularly typically have rms noise levels in the range of 5-10 μV [10], so clearly the signal from the recording electrode must be amplified before this spike detection circuit. In a complete system, a low-noise preamplifier would also bandlimit the signal appropriately to remove LFPs. We have previously designed low-noise, power-efficient CMOS preamplifiers for neural recording applications [3], but we do not include a preamplifier in the circuit reported here. To overcome the comparator offsets, a preamplifier with a gain of at least 10^3 (60 dB) should be used.

B. Adaptive Spike Detector

We tested the adaptive spike detector using a synthetic waveform programmed into an arbitrary waveform generator (Agilent 33120A). The test waveform consisted of three "typical" extracellular action potentials embedded in a background of Gaussian noise, and represented the output from a preamplifier in a complete neural recording system. The waveform was bandlimited at 7.5 kHz using a 3-pole low-pass filter. The first 10 msec of the test waveform is shown as the input waveform in Fig. 4. The rest of the waveform consisted only of noise. The waveform was 80 msec in length and was played in a loop so the burst of three spikes appeared periodically at a rate of 12.5 Hz.

We applied this waveform to the input of the adaptive spike detector. The amplitude of the waveform was set so that the largest spike had an amplitude of 70 mV and the background noise had an rms value of 5.5 mV. (Assuming a preamplifier with a gain of 60 dB, this corresponds to a spike amplitude of 70 μV and a noise rms value of 5.5 μV at the electrode.) Fig. 4 shows the input waveform along with the value of $V_{5\sigma}$ and the output of Comparator B. The adaptive spike detector successfully sets the threshold to an appropriate level to detect spikes but reject noise.

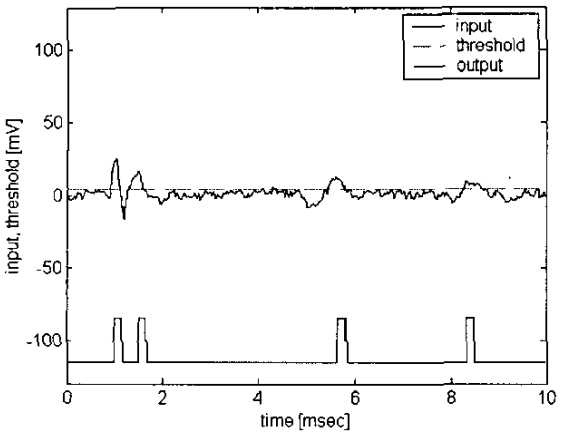

Fig. 5. Output of adaptive spike detection chip with amplitude of 23 mV.

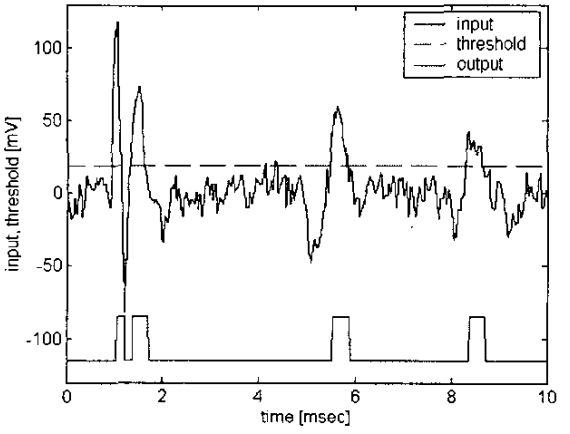

Fig. 6. Output of adaptive spike detection chip with amplitude of 116 mV.

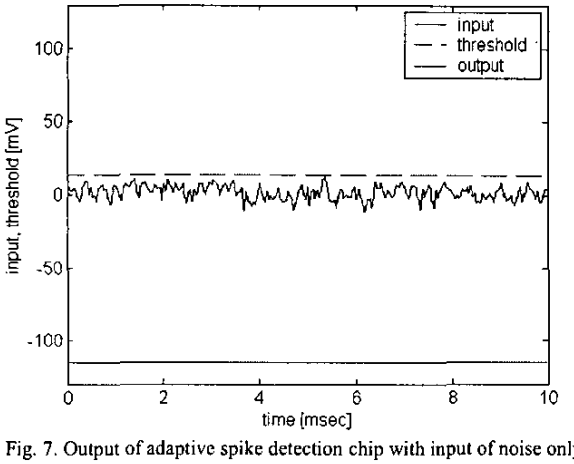

Fig. 7. Output of adaptive spike detection chip with input of noise only.

The amplitude of the input waveform (largest spike) was varied from 23 mV to 116 mV (and the rms noise level varied from 1.8 mV to 9.2 mV). Figs. 5 and 6 show the results of two of these experiments. The circuit functions correctly as the amplitude of the background noise changes by a factor of five. Fig. 7 shows the response of the circuit to a waveform containing only noise and no spikes. The algorithm succeeds in rejecting the noise completely despite occasional peaks in the Gaussian waveform. (In Figs. 4-7, the 0-5V digital output voltage is scaled down for clarity.)

The circuit consumes 0.094 mm^2 of chip area in a 1.5-μm process, and its power consumption is 57 μW when run from a 5 V power supply. The two comparators consume 91% of this power, so future work will focus on reducing their power dissipation.

V. Conclusion

We have presented a novel algorithm and circuit for the automatic detection of spikes in neural recordings. Our circuit was completely integrated in a commercially-available CMOS process. The small size and low power operation of this circuit make it compatible with fully-implanted multi-electrode applications. Although it detects spikes successfully, this circuit is incapable of distinguishing between spikes of different shapes, and thus cannot be used for spike sorting. It may be possible to develop more sophisticated circuits that would report certain characteristics of detected spikes and allow for spike sorting.

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