A Low-power Level-Crossing ADC for Biosignal Acquisition

A Low-power Level-Crossing ADC for Biosignal Acquisition

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Abstract. A large number of redundant signals will be generated when the traditional Nyquist sampling method is used to acquire a biological signal, leading to a system's energy loss. A new level-crossing analog-to-digital converter (LC-ADC) with non-uniform sampling and fixed window structure is presented, with fewer data and low power consumption features. The circuit uses a 6-bit capacitive DAC to quantize the input signal, avoiding the error accumulation of the 1-bit capacitive DAC structure, and a nanoamp CMOS current bias circuit to provide a very low quiescent current for the comparator, further reducing power consumption. The structure was verified in a 0.18μm CMOS technology. The results indicate that the total power dissipation is 0.26uw@500Hz, the signal-to-noise distortion ratio (SNDR) is 59dB@500Hz, and ENOB reached 9.51bit, which is suitable for the acquisition of low-frequency biological signals.

1. Introduction

As people pay more and more attention to their health, wearable medical devices with real-time monitoring of human health indicators such as blood pressure, heart rate, and respiratory rate have become the next hot spot for smart terminals. ADC is an indispensable module in the data acquisition system of wearable medical devices, which mainly collects bio-signals such as ECG and EEG. Usually, the frequency of the ECG signal is below 1KHz, while the EEG signal is around 100Hz. The biosignals are weakly changing for a long time and have a sudden characteristic, which can only change sharply in a short period and has a strong sparsity. Using the traditional Nyquist sampling method for uniform sampling in time creates a large number of redundant signals causing system energy to be wasted in data conversion, transmission, and storage. Data compression is an excellent method of reducing sensor devices' energy, storage, and transmission requirements [1], so non-uniform analog-to-digital converters have become a new research hotspot in wearable medical devices.

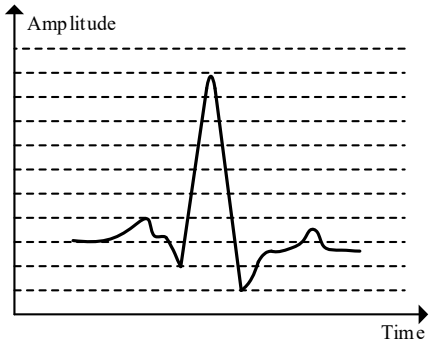

Figure 1. LC sampling

The LCADC is a non-uniformly sampled analog-to-digital converter, introduced in 1966 [2][3], which solves the above problem. In contrast to conventional Nyquist sampling, it quantizes the signal's amplitude uniformly, as shown in Figure 1. It only generates a sample when the signal exceeds a given quantization value and records the interval between two successive samples. The conversion result of LC-ADC consists of a digital code for the voltage amplitude and the time interval.

Conventional LC-ADC can be divided into the floating window and fixed window depending on how the window voltage is detected. A floating window [4][5] means that the window voltage changes with the input signal, always ensuring the input voltage is within the window. A comparator with a common high-mode input range is required to maximize the input signal swing. Therefore, this architecture requires higher power consumption. Fixed window means [6][7][8][9]: fixing the input threshold voltages of the two comparators to form a fixed window, generating a sample whenever the input signal exceeds the threshold voltage, and controlling the feedback signal to add and subtract the superposition with the input signal to obtain the residual signal, ensuring that the residual signal is always in the window. This architecture does not require high-input common-mode range comparators and can reduce overall power consumption. Literature [8] uses a 1-bit capacitive DAC to implement a fixed window structure, which has the advantage of a simple design and low power consumption. However, the circuit generates errors after each sample, affecting sampling accuracy after many accumulations. Literature [9] uses an integrator to implement the function of a 1-bit DAC, which overcomes the error accumulation problem existing in Literature [8]. Still, this structure has high power consumption and is unsuitable for working in a low-power environment.

This paper proposes a novel fixed window structure LC-ADC based on the concept of N-bit DAC, which uses 6-bit capacitive DAC to achieve the addition and subtraction superposition of the input signal, ensuring that the residual signal is constantly in between the window voltages. This structure overcomes the error accumulation problem of the 1-bit capacitive DAC because the accumulated error exceeds 1LSB, and the error is eliminated by triggering the sampling. The capacitive DAC does not consume static power, which can improve the sampling accuracy of the ADC without increasing additional power consumption.

2. System Framework

Figure 2(a) shows an Architecture diagram of the presented n-bit LC-ADC, which mainly includes a 6-bit capacitive DAC, comparator, counter, etc. The V_H and V_L are the threshold voltage of the comparator, $and\, V_H - V_L = 1LSB$ constitutes the window voltage interval. The common-mode voltage V_M is equivalent to $(V_H - V_L)/2$. The V_{SP} pulse indicates the sampling pulse, and the UD signal represents the input signal phase.

An example waveform is shown in Figure 2(b). When the input signal V_{IN} is in ascending phase, the residual signal V_{RES} increase. When V_{RES} is larger than V_M, the direction discriminator comparator COM2 generates a CMPD pulse, which controls UD Logic and generates the UD signal (UD=1). The MUX is based on the UD signal. Select the input signal for comparison with V_H. When V_{RES} and V_H level crossings, Cc Logic generates a V_{SP} pulse, and the counter performs an addition operation. Finally, the output of the counter and non-overlapping jointly control the output voltage of the 6-bit capacitor DAC and the input signal for subtraction operation so that the residual signal VRES is folded down. Similarly, when the input signal turns into descending phase, the system operation flow is the same as above.

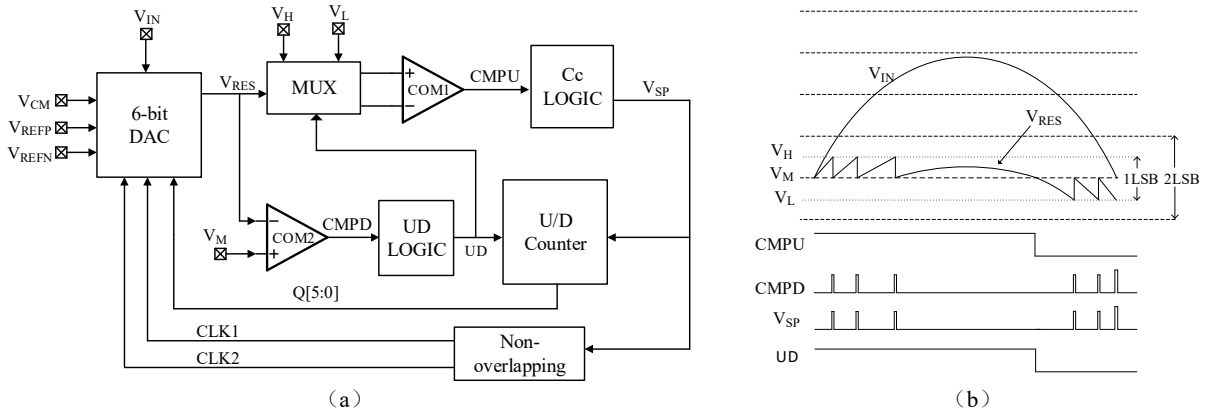

Figure 2. (a)Architecture diagram of the presented n-bit LC-ADC, (b) Example waveforms

3. Circuit design

3.1. 6-bit capacitive DAC

The circuit of the 6-bit capacitive DAC is shown in Figure 3, through which the input signals are superimposed so that the residual signal V_{RES} is always between the two threshold voltages. The V_{CM}, V_{REFP}, and V_{REFN} are reference voltages. The CLK1 and CLK2 are non-overlapping signals to avoid race contention affecting the sampling accuracy. The a, b, and c are switching control signals for DAC, which can be expressed as

$$a = \mathrm{Q[5:0]} \cdot \mathrm{CLK1} \tag{1}$$

$$b = \overline{\mathrm{Q[5:0]}} \cdot CLK1 \tag{2}$$

$$c = CLK2 \tag{3}$$

Where Q [5:0] is the output of the counter.

The work of the DAC can be divided into two main phases: tracking and updating. When DAC is in the tracking phase, CLK1=0, CLK2=1 (for 1 means the switch is closed), and switch c is closed so that all lower pole plates of the capacitor array are attached to the V_{CM}, at which point and the value of V_{RES} is

$$V_{RES} = \frac{1}{2} V_{IN} + V_{DAC} \tag{4}$$

V_{DAC} indicates the output voltage of DAC. When the value of V_{RES} reaches 0.5LSB, CLK1 changes to 1, and DAC switches to the update phase. At this time, switches a and b charge the lower plate of each capacitor array with V_{REFP} or V_{REFN} according to the value of Q [5:0]. The CLK1 drops back low to indicate that the capacitor array has been charged. When CLK2 goes high again, the output voltage of the capacitor array V_{DAC} changes to a set value and is superimposed on the input signal, eventually collapsing the V_{RES} waveform and starting a new round of tracking the input signal.

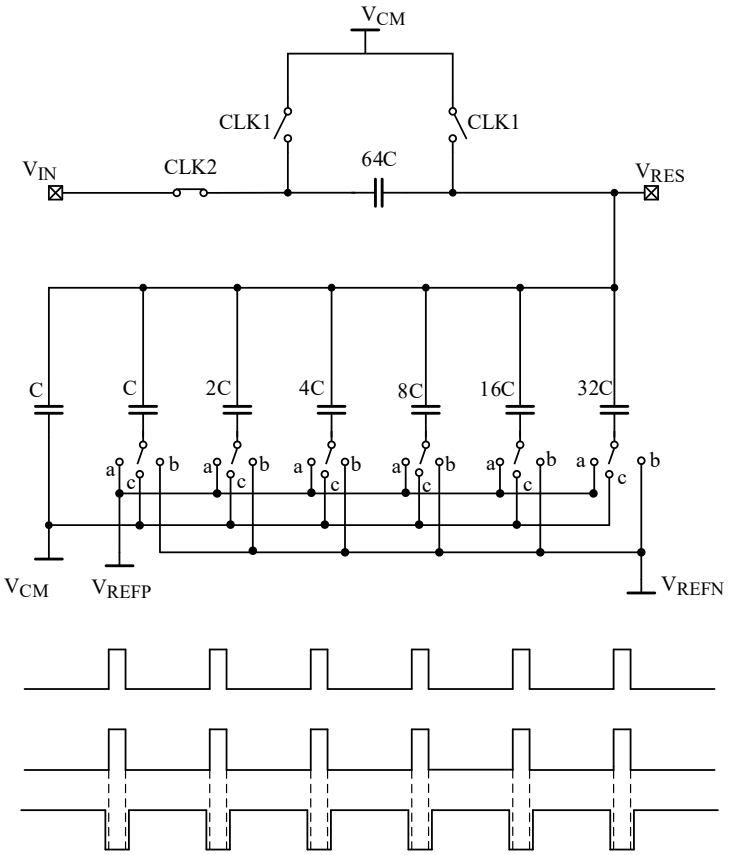

Figure 3. 6-bit DAC and control signals

3.2. Comparator

The LC-ADC proposed in this paper is an asynchronous non-uniform sampled ADC, so the static comparator monitors whether the input signal is in real time if the threshold voltage is exceeded.

The power dissipation of a static comparator accounts for a significant portion of the overall power consumption, so the key to a low-power design is to minimize its power consumption. Figure 4 shows the static comparator. The left part is a nanoamp CMOS current bias circuit[10] that provides a very low operating current for the comparator. The MP9 is equivalent to a diode, equivalent to two diodes connected in parallel, drain-substrate, and source-substrate, respectively, where the source and drain are used as the anode and the substrate the cathode. The role of the diodes is to clamp the V_{GS} voltages of MN6 and MN7 so that they are in the sub-threshold region to generate nano-amperes of bias current.

All MOS in the circuit is operated in the subthreshold region to decrease power dissipation. The second section shows that two comparators with different performances are needed in this paper. The propagation delay of the direction discriminant comparator COMP2 can be much weaker than the window voltage discriminant comparator COMP1. Since the transmission delay of the comparator is negatively related to the G_M, the performance of the comparator can be reduced by lowering the current, thus saving the static power dissipation. The design adopts a three-stage structure. The first stage uses a diode connection of NMOS as a fully differential amplifier for the load. The second stage is a high-gain amplifier which enlarges the input signal difference and converts the differential output to a single-ended one. The final stage uses a Class AB output to increase the swing of the system. Normally, the second stage turns the third stage off and does not consume power. The third stage draws current from the power supply only when level crossing occurs.

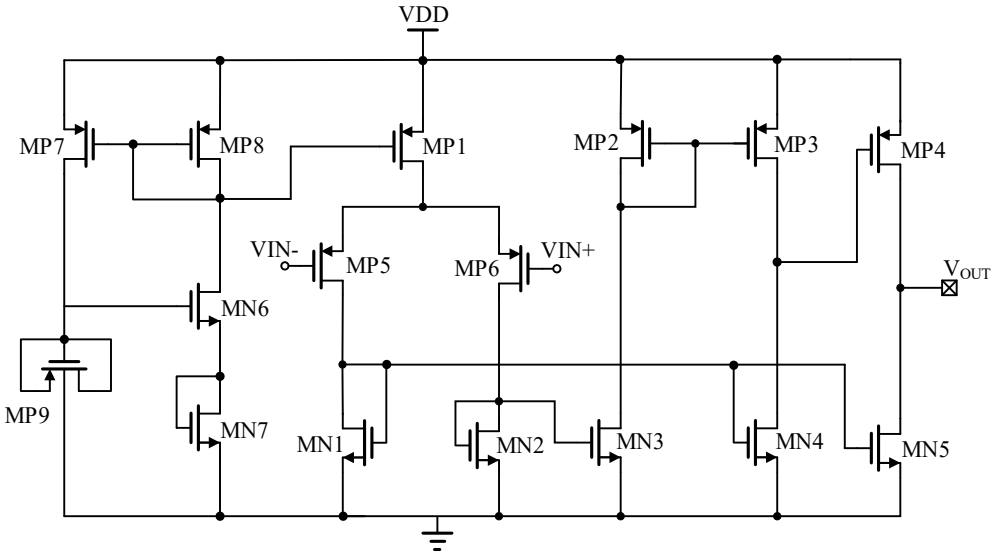

Figure 4. Comparator and bias circuit

3.3. Cc Logic Circuit

The Cc Logic circuit is modified from[11], shown in Figure 5. The CMPU signal comes from comparator COM1, which is normally low and only goes high when a sample occurs. The ack comes from the counter, meaning the sampled signal has been converted to a 6-bit digital code. The Reset indicates the reset signal, and V_{SP} is the pulse signal generated when the level crossing.

When no sampling occurs, TG is on, and M3 is off, allowing the CC Logic circuit to read the output voltage of comparator COM1. When signal sampling occurs, V_{RES} exceeds the preset window value, and the comparator output CMPU begins to rise. When the CMPU crosses the threshold voltage of the inverter in SR1, the output of SR1 is set to 1, then TG is turned off, and M3 is turned on via SR2. When the output of SR1 is delayed by the Delay module[12], the output of SR1 is reset to zero. After the Cc Logic circuit completes one sampling, the module is disabled until ACK returns a high level, TG is switched on, and the whole circuit resets into normal operation mode in preparation for the next signal processing.

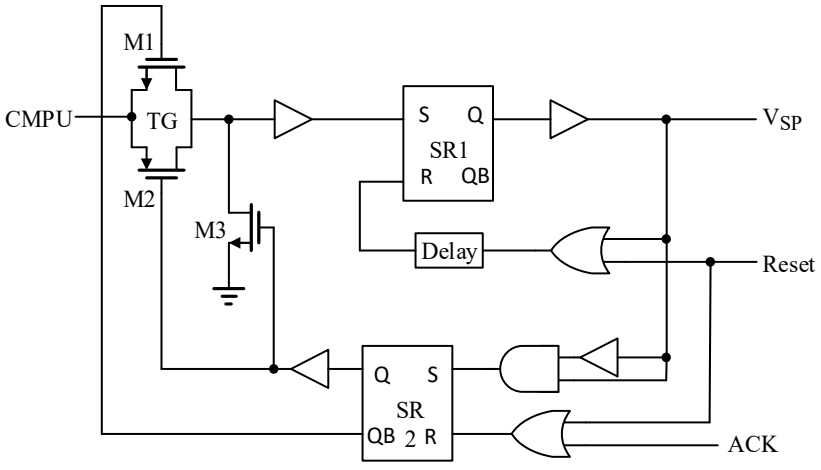

Figure 5. Cc logic circuit

4. Circuit simulation result

This work uses a 0.18μm CMOS process, a supply voltage of 0.8V, and an input signal in the frequency range of 10Hz-1.5KHz. The layout of the presented LC-ADC is shown in Figure 6.

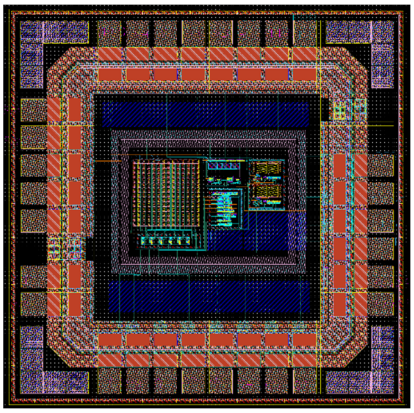

Figure 6. The layout of the presented LC-ADC

This work was simulated and verified using Cadence Spectre, and MATLAB was used for signal interpolation and reconstruction. In the simulation, the window voltage of the comparator 1LSB is equal to 12.5 mV. However, equation (4) shows that the DAC shrinks the input signal by one time, so the window voltage needs to be doubled when the signal is reconstructed. When the input is 500Hz sinusoidal signal, the amplitude is 0-0.8V, the LC-ADC output spectrum is shown in Figure 7, the SNDR is 59dB@500Hz, and ENOB reached 9.51bit.

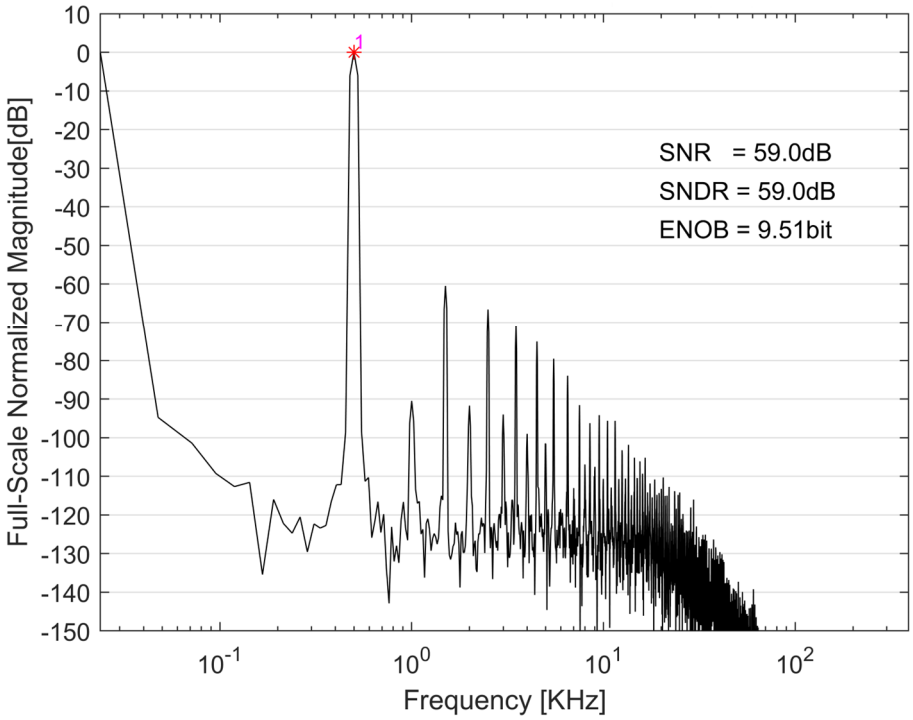

Figure.7 The LC-ADC output spectrum for a 500 Hz sine inputs

The amplitude of the input signal is 0-0.8V, and its frequency is scanned from 5Hz to 1.5KHz. As shown in Figure 8, the SNDR ranges from 51.5dB to 61.9 dB.

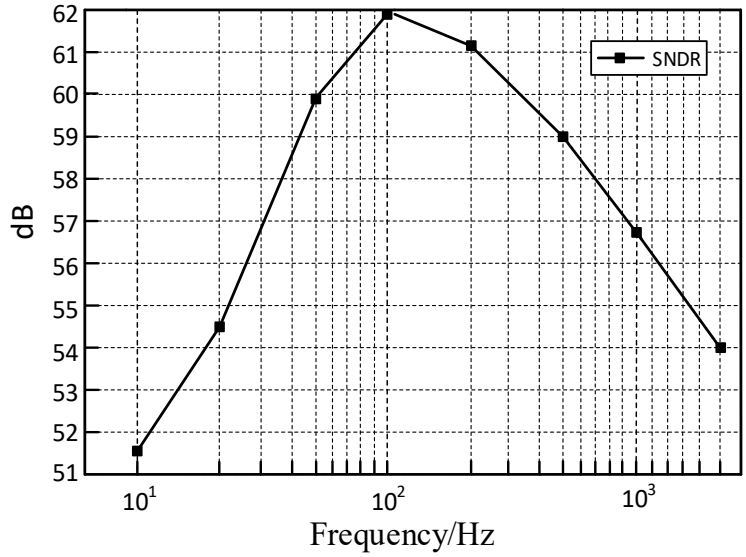

Figure 8. The SNDR curve for input frequency scanning from 5Hz to 1.5KHz

The values of analog-and-digital power consumption in the circuit versus frequency are shown in Figure 9, and superimposing the two yields a total power consumption of 139.3-513.6 n W. As the input signal rises, the working times of each module in the circuit increase in unit time, resulting in a positive correlation between overall power consumption and frequency.

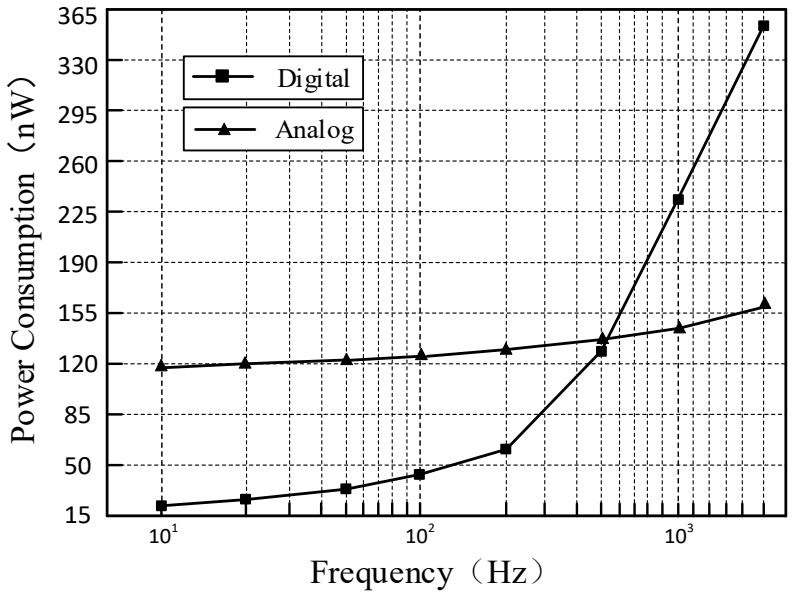

Figure 9. Power consumption curve for input frequency scanning from 5Hz to 1.5KHz

The performance summary of this paper compared with other asynchronous LC-ADCs is shown in Table 1, with some improvement in power consumption and SNDR. Although the bandwidth is reduced, it is satisfied for common biosignal acquisition.

Table 1. Performance summary and comparison with other asynchronous LC-ADCs

	[6]	[7]	[9]	This work
Technology (μm)	0.18	0.18	0.028	0.18
Supply(V)	0.8	0.55-1	0.65	0.8
Bandwidth (KHz)	3.3	1	40000	1.5
SNDR (dB)	40-49	39-49	32-42	51.5-61.9
Power (μW)	0.31-0.58	0.0042-0.544	8	0.139-0.513

5. Conclusion

This paper proposes a new LC-ADC with a fixed window structure, using a 6-bit capacitive DAC to ensure that the residual signal is always between the window voltages, which improves the SNDR and decreases the power consumption of the conventional event-driven mode converter. Simulation results show that the high effective bit count can be guaranteed in the range of 10Hz-1.5KHz, which is suitable for low-frequency biosignal acquisition.

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