

# A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications

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**Abstract**—There is a need among scientists and clinicians for low-noise low-power biosignal amplifiers capable of amplifying signals in the millihertz-to-kilohertz range while rejecting large dc offsets generated at the electrode–tissue interface. The advent of fully implantable multielectrode arrays has created the need for fully integrated micropower amplifiers. We designed and tested a novel bioamplifier that uses a MOS–bipolar pseudo-resistor element to amplify low-frequency signals down to the millihertz range while rejecting large dc offsets. We derive the theoretical noise–power tradeoff limit—the noise efficiency factor—for this amplifier and demonstrate that our VLSI implementation approaches this limit by selectively operating MOS transistors in either weak or strong inversion. The resulting amplifier, built in a standard 1.5- $\mu\text{m}$  CMOS process, passes signals from 0.025 Hz to 7.2 kHz with an input-referred noise of 2.2  $\mu\text{Vrms}$  and a power dissipation of 80  $\mu\text{W}$  while consuming 0.16  $\text{mm}^2$  of chip area. Our design technique was also used to develop an electroencephalogram amplifier having a bandwidth of 30 Hz and a power dissipation of 0.9  $\mu\text{W}$  while maintaining a similar noise–power tradeoff.

**Index Terms**—Analog integrated circuits, biosignal amplifier, low noise, low-power circuit design, neural amplifier, noise efficiency factor, subthreshold circuit design, weak inversion.

## I. INTRODUCTION

THERE IS a great demand for technologies that enable neuroscientists and clinicians to observe the simultaneous activity of large numbers of neurons in the brain. Multielectrode neural recordings are becoming standard practice in basic neuroscience research, and knowledge gained from these studies is beginning to enable clinical and neuroprosthetic applications. Recent advances in MEMS technology have produced small (less than 4 mm in any dimension) arrays of microelectrodes containing as many as 100 recording sites [1], [2]. Next-generation neural recording systems must be capable of observing 100–1000 neurons simultaneously, in a fully implanted unit.

While integrated electronics have been developed for small-scale amplification of the weak bioelectrical signals [3]–[15], existing circuits typically have unacceptable noise levels or consume too much power to be fully implanted in large quantities. Implantable bioamplifiers must dissipate little power so that surrounding tissues are not damaged by heating. A heat flux of only 80  $\text{mW}/\text{cm}^2$  can cause necrosis in muscle

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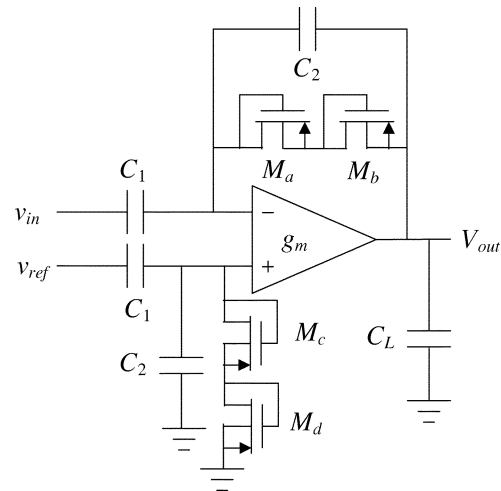


Fig. 1. Schematic of neural amplifier.

tissue [16], so for small chronic implants, power dissipation should not exceed a few hundred milliwatts. For a 1000-electrode system, this results in a maximum power dissipation much less than 1 mW per amplifier, and this does not include power required by other components in the implanted system such as telemetry.

Due to electrochemical effects at the electrode–tissue interface, dc offsets of 1–2 V are common across differential recording electrodes [17]. Typical neural action potentials, or spikes, have amplitudes up to 500  $\mu\text{V}$  when recorded extracellularly, with energy in the 100-Hz–7-kHz band [6], while low-frequency local field potentials (LFPs) have amplitudes as high as 5 mV and may contain signal energy below 1 Hz [8]. Some existing VLSI bioamplifier designs use off-chip capacitors in the nanofarad range to obtain a low-frequency cutoff that passes LFP signals while rejecting large dc offsets [7], [8], [10], [11]. This approach is not feasible for large numbers of implanted electrodes. If we restrict ourselves to a 15 mm  $\times$  15 mm die for a 1000-channel system, then each amplifier must consume less than 0.225  $\text{mm}^2$  of silicon area.

This paper reports on the design and testing of a fully integrated amplifier suitable for recording biological signals from the millihertz range to 7 kHz. We show that this amplifier rejects dc offsets at the input and offers the best power–noise tradeoff of any biosignal amplifier reported.

## II. NEURAL AMPLIFIER DESIGN

Fig. 1 shows the schematic of our bioamplifier design. This circuit was first described in [18]. The midband gain  $A_M$  is set by  $C_1/C_2$ , and for the case where  $C_1, C_L \gg C_2$ , the bandwidth

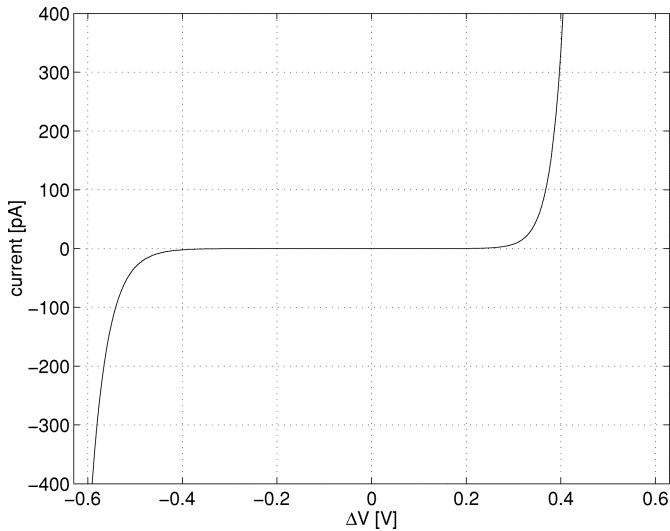


Fig. 2. Measured current–voltage relationship of MOS-bipolar element ( $M_a$ – $M_d$  in Fig. 1) [19].

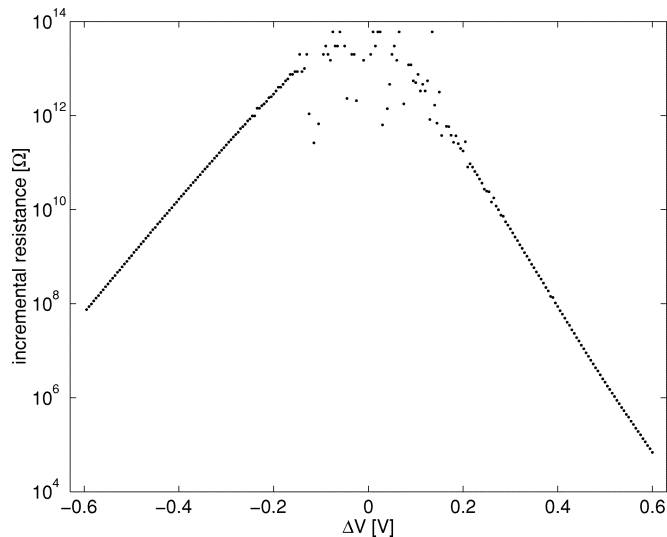


Fig. 3. Incremental resistance of single MOS-bipolar element. For low voltages, the incremental resistance exceeds  $10^{12} \Omega$ .

is approximately  $g_m/(A_M C_L)$ , where  $g_m$  is the transconductance of the operational transconductance amplifier (OTA).

#### A. MOS-Bipolar Pseudoresistor Elements

Transistors  $M_a$ – $M_d$  are MOS-bipolar devices acting as pseudoresistors. With negative  $V_{GS}$ , each device functions as diode-connected pMOS transistor. With positive  $V_{GS}$ , the parasitic source–well–drain p–n–p bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT [19] (see Fig. 2). Each transistor was sized  $4 \mu\text{m} \times 4 \mu\text{m}$ . For small voltages across this device, its incremental resistance  $r_{inc}$  is extremely high (see Fig. 3). For  $|\Delta V| < 0.2 \text{ V}$ , we measured  $dV/dI > 10^{11} \Omega$ . It was difficult to measure  $dV/dI$  accurately in this region due to the low current, which was near the limit of our measurement capabilities.

We use two MOS-bipolar devices in series to reduce distortion for large output signals. The low-frequency cutoff  $\omega_L$  of the ac-coupled amplifier is given by  $1/(2r_{inc}C_2)$ . Despite the long

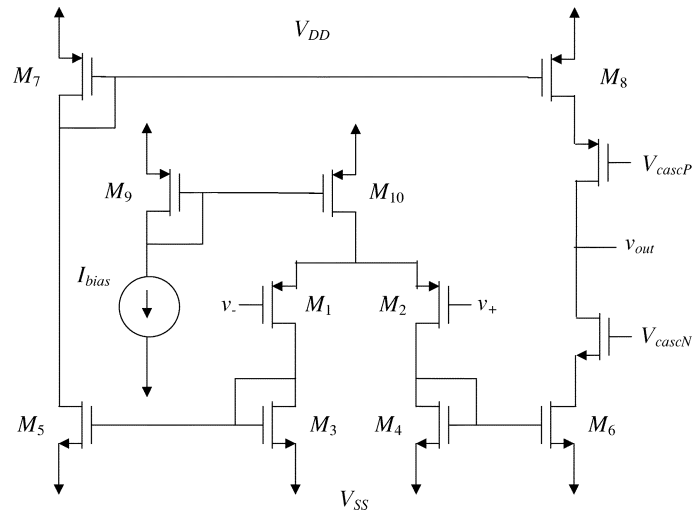


Fig. 4. Schematic of OTA used in neural amplifier.

time constant, a large change in the input causes a large voltage across the MOS-bipolar elements, reducing their incremental resistance and giving a fast settling time. Recent bioamplifier designs have used transistors biased in the subthreshold region to approximate large-valued resistors [13], [14]. This technique yields similar results but requires additional biasing circuitry. Another design uses diode-connected nMOS transistors as pseudoresistors to achieve an equivalent resistance of greater than  $10^{10} \Omega$ , though it is not stated whether a body–source connection is used to create a diode-connected bipolar transistor [15].

#### B. Low-Noise Low-Power OTA Design

Fig. 4 shows a schematic of the current-mirror OTA used in the bioamplifier. The bias current and cascode bias voltages were generated by standard circuits [20], and the power consumption of these biasing circuits was not included in our power measurements since an arbitrary number of OTAs can share the generated voltages. Although the circuit topology is a standard design suitable for driving capacitive loads, the sizing of the transistors is critical for achieving low noise at low current levels. The bias current  $I_{bias}$  is set to  $8 \mu\text{A}$ , giving devices  $M_1$ – $M_8$  drain currents of  $4 \mu\text{A}$ . At this current level, each transistor may operate in weak, moderate, or strong inversion depending on its  $W/L$  ratio. For each device, we calculate the moderate inversion characteristic current  $I_S$  [21], given by

$$I_S = \frac{2\mu C_{ox} U_T^2}{\kappa} \cdot \frac{W}{L} \quad (1)$$

where  $U_T$  is the thermal voltage  $kT/q$ , and  $\kappa$  is the subthreshold gate coupling coefficient. Note that  $\kappa$  has a typical value of 0.7 and is equivalent to  $1/n$ , where  $n$  denotes the reciprocal of the change in surface potential  $\psi_{sa}$  for a change in gate-to-body voltage  $V_{GB}$  [21], [22].

The inversion coefficient (IC) for each transistor may then be calculated as the ratio of drain current to the moderate inversion characteristic current, as follows:

$$IC = I_D/I_S. \quad (2)$$

A device having  $IC > 10$  operates in the strong inversion region and has a transconductance proportional to the square root

TABLE I  
OPERATING POINT OF OTA TRANSISTORS FOR NEURAL AMPLIFIER

| Devices              | $W/L$ ( $\mu\text{m}$ ) | $I_D$ ( $\mu\text{A}$ ) | Inversion Coefficient | $g_m/I_D$ ( $\text{V}^{-1}$ ) | $V_{EFF} = V_{GS} - V_t$ (V) |
|----------------------|-------------------------|-------------------------|-----------------------|-------------------------------|------------------------------|
| $M_1, M_2$           | 800.0/4.0               | 4.0                     | 0.43                  | 20.6                          | -0.076                       |
| $M_3, M_4, M_5, M_6$ | 12.0/44.8               | 4.0                     | 110                   | 2.5                           | +0.770                       |
| $M_7, M_8$           | 6.4/12.8                | 4.0                     | 171                   | 2.0                           | +0.960                       |
| $M_9, M_{10}$        | 20.0/20.0               | 8.0                     | 171                   | 2.0                           | +0.960                       |
| $M_{\text{cascN}}$   | 12.0/3.2                | 4.0                     | 7.8                   | 8.1                           | +0.200                       |
| $M_{\text{cascP}}$   | 6.4/3.2                 | 4.0                     | 43                    | 3.9                           | +0.481                       |

of drain current. A device having  $IC < 0.1$  operates in the weak inversion (subthreshold) region and has a transconductance proportional to drain current [22], [23]. For devices operating in moderate inversion ( $10 > IC > 0.1$ ), both strong and weak inversion expressions overestimate transconductance. For low-power circuit design, we use the EKV model, which is valid in all regions of inversion [24]. We estimate  $g_m$  by

$$g_m \approx \frac{\kappa I_D}{U_T} \cdot \frac{2}{1 + \sqrt{1 + 4 \cdot IC}}. \quad (3)$$

Table I shows the dimensions and operating conditions of each transistor in the circuit. The input devices  $M_1$  and  $M_2$  are drawn with identical sizes, and we denote their transconductance as  $g_{m1}$  and their width-to-length ratio as  $(W/L)_1$ . Similarly, transistors  $M_3$ – $M_6$  are the same size  $(W/L)_3$  and have transconductance  $g_{m3}$ . The pMOS current mirror transistors  $M_7$  and  $M_8$  have size  $(W/L)_7$  and transconductance  $g_{m7}$ .

Analysis of this circuit reveals the input-referred thermal noise power to be

$$\overline{v_{ni, \text{thermal}}^2} = \left[ \frac{16kT}{3g_{m1}} \left( 1 + 2 \frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}} \right) \right] \Delta f. \quad (4)$$

If we size our devices such that  $g_{m3}, g_{m7} \ll g_{m1}$ , we can minimize the noise contributions of devices  $M_3$ – $M_8$ . This can be accomplished by making  $(W/L)_3, (W/L)_7 \ll (W/L)_1$ , thus, pushing devices  $M_3$ – $M_8$  into strong inversion where their relative transconductance  $g_m/I_D$  decreases as  $1/\sqrt{ID}$ . As shown in Table I, by operating  $M_1$  and  $M_2$  in the subthreshold regime, we achieve a high  $g_m/I_D$  ratio so that  $g_{m1}$  is much greater than  $g_{m3}$  and  $g_{m7}$ . We are operating near the maximum achievable  $g_m/I_D$  ratio of  $\kappa/U_T$  (approximately  $27 \text{ V}^{-1}$ ), which is reached in deep weak inversion.

In practice, we cannot decrease  $g_{m3}$  and  $g_{m7}$  arbitrarily without danger of instability. If the total capacitance seen by the gate of  $M_3$  (or  $M_4$ ) is denoted as  $C_3$ , then the OTA has two poles at  $\omega_p = g_{m3}/C_3$ . Similarly, there is a pole at  $g_{m7}/C_7$  caused by the pMOS mirror. To ensure stability, these pole frequencies must be several times greater than the dominant pole,  $g_{m1}/C_L$ . This criterion becomes easier to satisfy as  $C_L$  is made larger, so it becomes necessary to consider area limitations and bandwidth requirements. In our design, we decreased  $(W/L)_3$  and  $(W/L)_7$  as much as possible, trading off phase margin for lower input-referred noise. We designed our amplifier to have a phase margin of  $52^\circ$ . Transistors  $M_3$ – $M_8$  are narrow devices that require relatively large gate overdrive voltages, as shown in the last column of Table I, so output signal swing

considerations or finite power-supply voltages may also limit the designer's ability to decrease  $g_m$ .

Flicker noise, or  $1/f$  noise, is a major concern for a low-noise low-frequency circuit. We minimize the effects of flicker noise by using pMOS transistors as input devices and by using devices with large gate areas. Flicker noise in pMOS transistors is typically one to two orders of magnitude lower than flicker noise in nMOS transistors as long as  $|V_{GS}|$  does not greatly exceed the threshold voltage [21], [25] and flicker noise is inversely proportional to gate area. All transistors should be made as large as possible to minimize  $1/f$  noise. However, as devices  $M_3$ – $M_8$  are made larger,  $C_3$  and  $C_7$  increase, leading once again to a reduced phase margin. As  $M_1$  and  $M_2$  are made larger, the OTA input capacitance  $C_{in}$  increases. The input-referred noise of the bioamplifier can be related to the OTA input-referred noise by

$$\overline{v_{ni, \text{amp}}^2} = \left( \frac{C_1 + C_2 + C_{in}}{C_1} \right)^2 \cdot \overline{v_{ni}^2} \quad (5)$$

where  $C_1$  and  $C_2$  are the feedback network capacitors shown in Fig. 1. Since  $C_{in}$  contributes to a capacitive divider that attenuates the input signal, any increase in  $C_{in}$  increases the input-referred noise of the overall circuit [26]. An optimum gate area for  $M_1$  and  $M_2$  can be found to minimize  $1/f$  noise.

Lateral p-n-p transistors can be built in standard CMOS technology for low-frequency applications, and exhibit lower  $1/f$  noise than MOS transistors [27]. We did not use p-n-p devices for the input transistors  $M_1$  and  $M_2$  because the base current would have to flow through the MOS-bipolar devices. This dc current would bias the pseudoresistors toward an operating point with lower incremental resistance and raise the low-frequency cutoff. The inherently high  $g_m/I_C$  ratio of bipolar transistors makes them unsuitable for devices  $M_3$ – $M_8$  in our OTA design, as shown in (4).

### C. Noise Efficiency Factor

Since we are interested in minimizing noise within a strict power budget, we must consider the tradeoff between power and noise. The noise efficiency factor (NEF) introduced in [7] quantifies this tradeoff:

$$\text{NEF} = V_{ni, \text{rms}} \sqrt{\frac{2I_{\text{tot}}}{\pi \cdot U_T \cdot 4kT \cdot \text{BW}}} \quad (6)$$

where  $V_{ni, \text{rms}}$  is the input-referred rms noise voltage,  $I_{\text{tot}}$  is the total amplifier supply current, and BW is the amplifier bandwidth in hertz. An amplifier using a single bipolar transistor (with no  $1/f$  noise) has an NEF of one; all practical circuits have higher values.

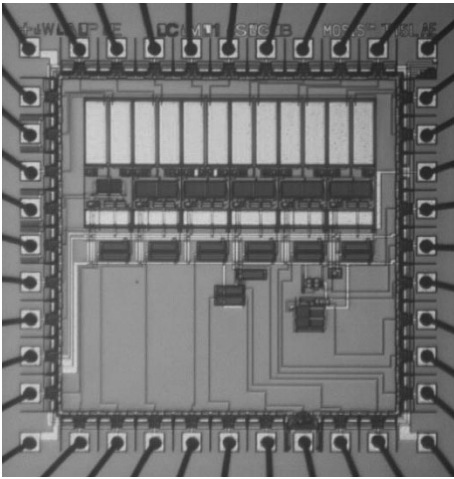


Fig. 5. Microphotograph of  $2.2 \times 2.2$  mm chip containing six neural amplifiers.

Substituting the expression for amplifier thermal noise (4) integrated across the bandwidth BW into (6) and assuming  $g_{m3}$ ,  $g_{m7} \ll g_{m1}$ , we find

$$\text{NEF} = \sqrt{\frac{4I_{\text{tot}}}{3U_T g_{m1}}} = \sqrt{\frac{16}{3U_T} \left( \frac{I_{D1}}{g_{m1}} \right)} \quad (7)$$

where  $I_{D1}$  is the drain current through  $M_1$ , which is 1/4 of the total amplifier supply current. From this expression, it is clear that if we wish to minimize the NEF, we must maximize the relative transconductance  $g_m/I_D$  of the input devices  $M_1$  and  $M_2$ . In weak inversion,  $g_m/I_D$  reaches its maximum value of  $\kappa/U_T$ , so we make  $(W/L)_1$  very large to approach subthreshold operation with microamp current levels. Using a more accurate model for thermal noise valid in weak inversion [21] yields

$$\text{NEF} = \sqrt{\frac{4}{\kappa U_T} \left( \frac{I_{D1}}{g_{m1}} \right)}. \quad (8)$$

In weak inversion, the expression for NEF reduces to

$$\text{NEF} = \sqrt{\frac{4}{\kappa^2}} \cong 2.9 \quad (9)$$

assuming a typical value of  $\kappa = 0.7$ . This is the theoretical NEF limit for an amplifier with this circuit topology constructed from MOS transistors, assuming current mirror ratios of unity. In practice, the NEF will be limited by stability constraints on  $g_{m3}$  and  $g_{m7}$ , as discussed earlier, and by  $1/f$  noise.

### III. EXPERIMENTAL RESULTS

We fabricated the amplifier in the AMI ABN 1.5- $\mu\text{m}$  two-metal two-poly CMOS process. We designed the amplifier for a gain of 100, setting  $C_1$  to 20 pF and  $C_2$  to 200 fF. Both  $C_1$  and  $C_2$  were built as poly-poly capacitors for maximum linearity. The bandwidth-limiting load capacitor  $C_L$  was built as an nMOS capacitor with a value of 17 pF. One amplifier circuit uses  $0.16 \text{ mm}^2$  of silicon area, and 67% of this area is taken up by capacitors. A die photograph of a  $2.2 \text{ mm} \times 2.2 \text{ mm}$  chip containing six amplifier variants is shown in Fig. 5.

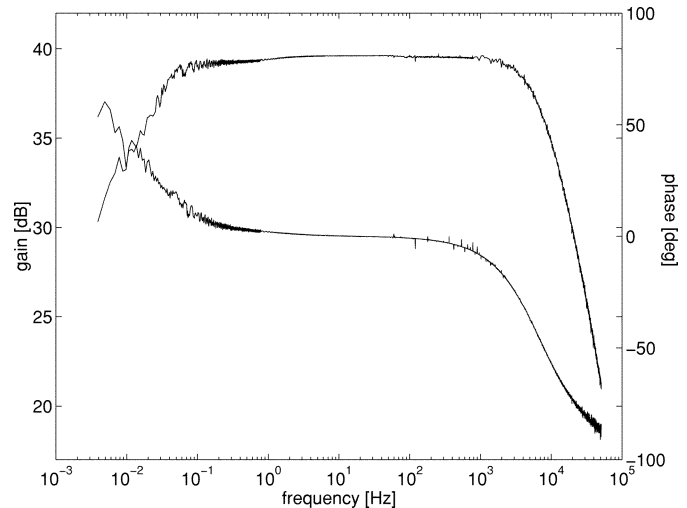


Fig. 6. Measured transfer function of amplifier. Midband gain is 39.5 dB, and single-pole rolloff occurs at 7.2 kHz. Low-frequency rolloff occurs at 0.025 Hz.

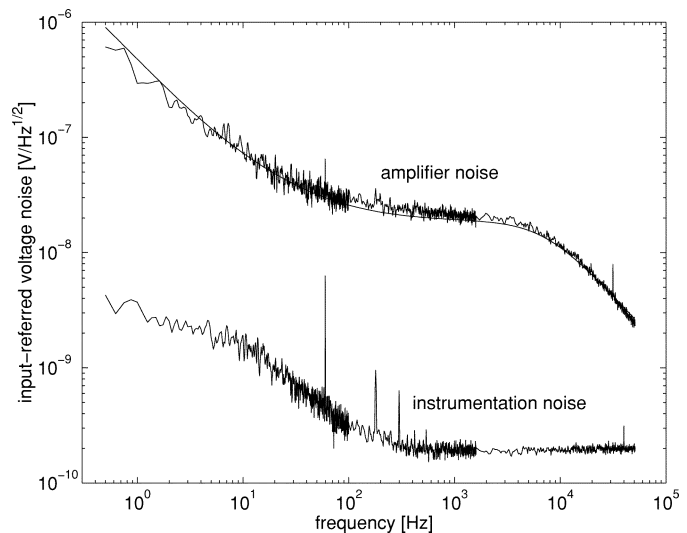


Fig. 7. Measured and simulated (smooth curve) amplifier input-referred voltage noise spectrum. Integration under this curve yields an rms noise voltage of  $2.2 \mu\text{Vrms}$ .

#### A. Testbench Results

Fig. 6 shows the measured amplifier transfer function from 0.004 Hz to 50 kHz. The midband gain is 39.5 dB, which is slightly lower than our design specification of 40 dB. This discrepancy is likely caused by fringing fields on the small  $C_2$  capacitors, yielding a larger capacitance than drawn. The low-frequency cutoff  $f_L$  is approximately 0.025 Hz. This corresponds to a MOS-bipolar element incremental resistance  $r_{\text{inc}} > 10^{13} \Omega$ .

Fig. 7 shows the measured input-referred voltage noise spectrum. The thermal noise level is  $21 \text{ nV}/\sqrt{\text{Hz}}$  and the  $1/f$  noise corner occurs at 100 Hz. Integration under this curve from 0.5 Hz to 50 kHz yields an rms noise voltage of  $2.2 \mu\text{Vrms}$ . This noise measurement was confirmed by recording the output noise waveform and dividing by the gain to generate an input-referred noise waveform whose rms value is  $2.2 \mu\text{Vrms}$  (see Fig. 8). Surprisingly,  $1/f$  noise is not the dominant noise source in the circuit. If  $1/f$  noise were eliminated entirely,

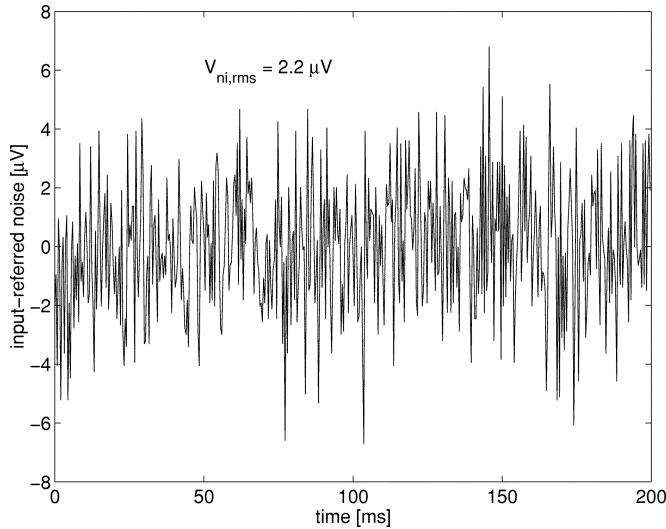


Fig. 8. Measured amplifier input-referred noise (i.e., output noise divided by amplifier gain). The rms value is  $2.2 \mu\text{V}$ , which agrees with the noise spectrum measurements in Fig. 7.

the circuit would have an input-referred noise of  $2.1 \mu\text{Vrms}$ . The low noise corner is due partially to the use of pMOS input devices with large gate areas, as discussed in Section II, but also to the relatively high thermal noise level of  $21 \text{ nV}/\sqrt{\text{Hz}}$ . This noise level is acceptable because of the low bandwidth of the circuit and the requirement that the input-referred noise only be lower than the typical extracellular neural background noise of  $5\text{--}10 \mu\text{Vrms}$  over this bandwidth [28].

Table II summarizes these and other measurements along with simulation results. We achieved noise simulations that closely matched experimental data by using SPICE BSIM3v3 Level 49 transistor models with  $1/f$  noise coefficients of  $\text{KF} = 6 \times 10^{-27}$  (pMOS),  $\text{KF} = 3 \times 10^{-25}$  (nMOS), and  $\text{AF} = 1$  (pMOS and nMOS). The smooth curve in Fig. 7 shows the simulated noise spectrum. The measured NEF of our amplifier is 4.0, which is near the theoretical limit of 2.9 calculated in (9).

Distortion stays below 1% total harmonic distortion (THD) for inputs less than 16.7 mV peak-to-peak (larger than typical extracellular neural signals). If we calculate dynamic range assuming a distortion limit of 1% (a conservative definition), our dynamic range is 69 dB. We also fabricated an alternate circuit using only single MOS-bipolar pseudo-resistor elements instead of two elements in series (see Fig. 2). This amplifier exhibited 1% THD for a 12.0-mV peak-to-peak input, resulting in a lower dynamic range of 66 dB.

The common-mode rejection ratio (CMRR) and the power-supply rejection ratio (PSRR) were measured and both exceeded 80 dB. Crosstalk was measured between amplifiers adjacent on the chip, and was  $-64$  dB or less. The input-referred offset voltage was measured for four amplifiers and varied between 180 and  $550 \mu\text{V}$ .

Fig. 9 shows the power-noise performance of our amplifier compared with estimated NEF values from previously published bioamplifiers [3]–[11]. (Only simulation results were presented in [12], and although circuits were built and tested in [13]–[15],

TABLE II  
SIMULATED AND EXPERIMENTAL CHARACTERISTICS OF NEURAL AMPLIFIER

| Parameter                               | Simulation           | Measured             |
|---|----------------------|----------------------|
| Supply voltage                          | $\pm 2.5 \text{ V}$  | $\pm 2.5 \text{ V}$  |
| Supply current                          | $16 \mu\text{A}$     | $16 \mu\text{A}$     |
| Gain                                    | 40 dB                | 39.5 dB              |
| Bandwidth                               | 7.5 kHz              | 7.2 kHz              |
| Low-frequency cutoff                    | 0.130 Hz             | 0.025 Hz             |
| Input-referred noise                    | $2.1 \mu\text{Vrms}$ | $2.2 \mu\text{Vrms}$ |
| Noise efficiency factor                 | 3.8                  | 4.0                  |
| THD (16.7 mVpp input)                   | not simulated        | 1.0%                 |
| Dynamic range (1% THD)                  | not simulated        | 69 dB                |
| CMRR (10 Hz – 5 kHz)                    | $\geq 42 \text{ dB}$ | $\geq 83 \text{ dB}$ |
| PSRR (10 Hz – 5 kHz)                    | $\geq 42 \text{ dB}$ | $\geq 85 \text{ dB}$ |
| Crosstalk ( $f = 1 \text{ kHz}$ )       | not simulated        | $-64 \text{ dB}$     |
| Area (in $1.5\text{-}\mu\text{m}$ CMOS) | n/a                  | $0.16 \text{ mm}^2$  |

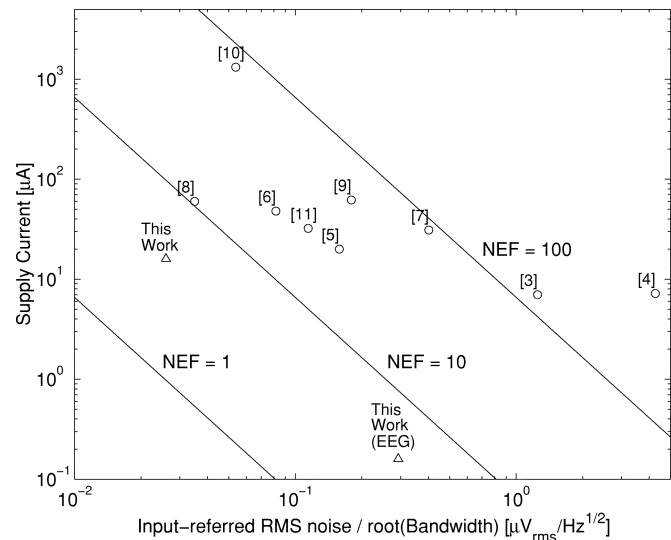


Fig. 9. Supply current versus normalized noise for amplifiers in [3]–[11] (circles) and the amplifiers described in this paper (triangles). Lines indicate constant NEF contours.

no noise measurements were reported.) The amplifier presented here exhibits a significantly better NEF than existing designs.

### B. Biological Test Results

We used the bioamplifier described above as a preamplifier in a simple neural recording experiment to verify operation of the circuit when connected to a neural electrode. We recorded spontaneous neural activity in rat olfactory cortex using a platinum-tipped extracellular microelectrode (Bionic Technologies, Salt Lake City, UT). Due to the unshielded wires connecting the electrode array to the amplifier circuit, we observed strong interfering signals at 60 Hz and approximately 50 kHz. We used two single-pole filters after the bioamplifier circuit to attenuate frequencies below 300 Hz and above 30 kHz. Fig. 10 shows an action potential recorded from this system referred to the amplifier input. The peak-to-peak signal and noise levels recorded with our low-power system match those obtained using a commercially available rack-mount biosignal amplifier system (Bionic Technologies).

TABLE III  
OPERATING POINT OF OTA TRANSISTORS FOR EEG AMPLIFIER

| Devices              | $W/L$ ( $\mu\text{m}$ ) | $I_D$ ( $\mu\text{A}$ ) | Inversion Coefficient | $g_m/I_D$ ( $\text{V}^{-1}$ ) | $V_{EFF} = V_{GS} - V_t$ (V) |
|----------------------|-------------------------|-------------------------|-----------------------|-------------------------------|------------------------------|
| $M_1, M_2$           | 800.0/4.0               | 0.032                   | 0.0034                | 27.1                          | -0.206                       |
| $M_3, M_4, M_5, M_6$ | 6.4/470.0               | 0.032                   | 17                    | 5.8                           | +0.304                       |
| $M_7, M_8$           | 6.4/104.0               | 0.032                   | 11                    | 7.0                           | +0.242                       |
| $M_9, M_{10}$        | 20.0/20.0               | 0.064                   | 1.4                   | 15.4                          | +0.059                       |
| $M_{\text{caseN}}$   | 12.0/3.2                | 0.032                   | 0.063                 | 25.7                          | -0.092                       |
| $M_{\text{caseP}}$   | 6.4/3.2                 | 0.032                   | 0.34                  | 21.5                          | -0.017                       |

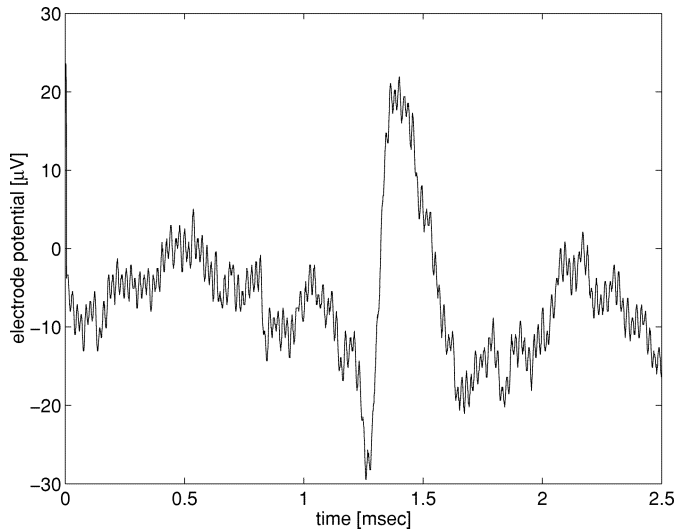


Fig. 10. Action potential from rat olfactory cortex recorded extracellularly using fully integrated CMOS amplifier. Waveform is referred to the amplifier input.

#### IV. ELECTROENCEPHALOGRAM (EEG) AMPLIFIER DESIGN

As a further demonstration of our amplifier design technique, we redesigned the neural signal amplifier demonstrated above for low-frequency biosignal applications such as EEGs or brain-surface electrodes. Electrical recordings from the scalp or brain surface show signal energy primarily below 30 Hz since individual neural action potentials cannot be observed from this distance. We modified our previous amplifier design to achieve a bandwidth extending from below 1 Hz to 30 Hz while maintaining a low NEF and a gain of 40 dB.

In order to lower the amplifier bandwidth, we increased the load capacitance  $C_L$  from 17 to 50 pF. Layout area considerations prevented us from increasing  $C_L$  beyond this value. The low value of  $g_m$  required to produce a 30-Hz bandwidth dictated a bias current of 32 nA for the differential pair transistors. Table III lists the dimensions and operating point of each transistor in the OTA. Transistors  $M_3$ – $M_8$  were drawn extremely long and narrow so that strong inversion operation could be achieved in the current mirrors at nanoampere current levels.

This amplifier was fabricated in the same 1.5- $\mu\text{m}$  CMOS process described in Section III. Table IV summarizes the simulated and measured results for this amplifier. The EEG amplifier exhibited a bandwidth of 30 Hz at a power dissipation of 0.9  $\mu\text{W}$  and an input-referred rms noise voltage of 1.6  $\mu\text{Vrms}$ . Despite low-frequency operation where  $1/f$  noise power is high, an NEF of 4.8 was achieved by using high- $g_m/I_D$  operation for the

TABLE IV  
SIMULATED AND EXPERIMENTAL CHARACTERISTICS OF EEG AMPLIFIER

| Parameter                         | Simulation           | Measured             |
|-----------------------------------|----------------------|----------------------|
| Supply voltage                    | $\pm 2.5$ V          | $\pm 2.5$ V          |
| Supply current                    | 128 nA               | 180 nA               |
| Gain                              | 40 dB                | 39.8 dB              |
| Bandwidth                         | 30 Hz                | 30 Hz                |
| Low-frequency cutoff              | 2.2 Hz               | 0.014 Hz             |
| Input-referred noise              | 2.4 $\mu\text{Vrms}$ | 1.6 $\mu\text{Vrms}$ |
| Noise efficiency factor           | 6.0                  | 4.8                  |
| THD (12.4 mVpp input)             | not simulated        | 1.0%                 |
| Dynamic range (1% THD)            | not simulated        | 69 dB                |
| CMRR (1 Hz – 100 Hz)              | $\geq 88$ dB         | $\geq 86$ dB         |
| PSRR (1 Hz – 100 Hz)              | $\geq 80$ dB         | $\geq 80$ dB         |
| Area (in 1.5- $\mu\text{m}$ CMOS) | n/a                  | 0.22 $\text{mm}^2$   |

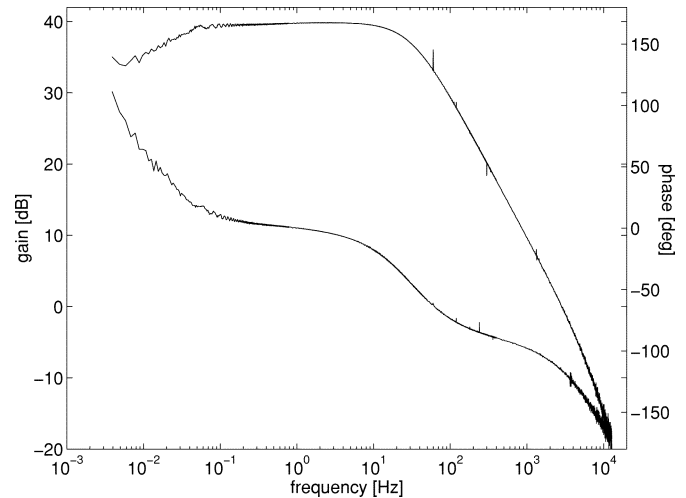


Fig. 11. Measured transfer function of EEG amplifier. Midband gain is 39.8 dB, and single-pole rolloff occurs at 30 Hz. Low-frequency rolloff occurs at 0.014 Hz.

input differential pair and low- $g_m/I_D$  operation for the current mirrors. Fig. 11 shows the measured transfer function of this amplifier. Fig. 12 shows the measured input-referred voltage noise spectrum. The  $1/f$  noise corner frequency occurred at 2.3 Hz due to the relatively high thermal noise levels.

The chip area consumed by the EEG amplifier (0.22  $\text{mm}^2$ ) was slightly greater than the neural amplifier since a larger value of  $C_L$  was used. The measured dynamic range of 69 dB matches the performance of the neural amplifier, and the CMRR and PSRR exceeded 80 dB. The input-referred offset voltage was measured for four amplifiers and varied between 110 and 380  $\mu\text{V}$ .

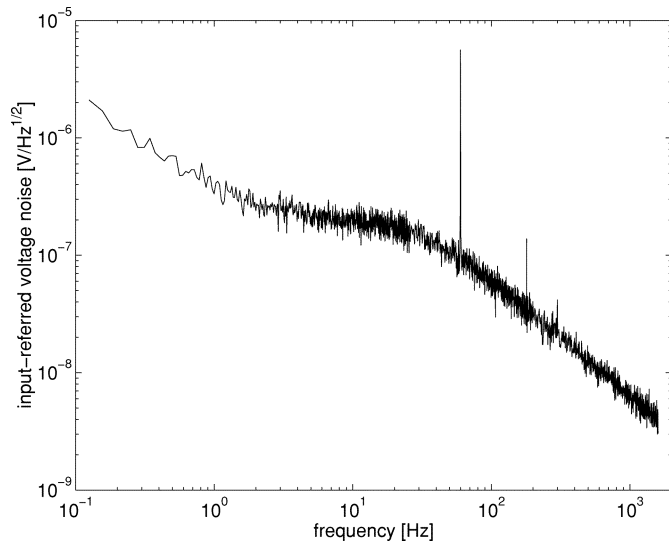


Fig. 12. Measured EEG amplifier input-referred voltage noise spectrum. Integration under this curve yields an rms noise voltage of  $1.6 \mu\text{V}_{\text{rms}}$ .

## V. CONCLUSION

An  $80\text{-}\mu\text{W}$  fully integrated CMOS biosignal amplifier with an input-referred noise of  $2.2 \mu\text{V}_{\text{rms}}$  over a  $7.2\text{-kHz}$  bandwidth has been demonstrated. The amplifier rejects dc offsets commonly encountered in microelectrode recording applications, but passes low-frequency signals in the millihertz range while using no off-chip components. By taking advantage of the high  $g_m/I_D$  ratio of devices operating in subthreshold, we were able to achieve the best power-noise tradeoff reported among biosignal amplifiers. A 1000-channel amplifier would consume only  $80 \text{ mW}$  and fit on a  $13\text{-mm} \times 13\text{-mm}$  silicon die in a  $1.5\text{-}\mu\text{m}$  process (pads excluded), allowing for large-scale implantable neural recording systems. We applied the same design approach to an EEG amplifier application and achieved a similar NEF at a much lower bandwidth and power dissipation.

A complete multichannel recording system will also require an analog multiplexer (MUX) and analog-to-digital converter (ADC) with milliwatt power dissipation. For systems with large numbers of channels, the hardware required for serialization and digitizing of neural signal data may become the dominant source of power consumption. Low-power MUX and ADC design will be essential for fully implanted neural recording systems.

The low-frequency ac coupling provided by the MOS-bipolar element may also have applications in the baseband circuitry of direct-conversion RF receivers. The direct-conversion architecture is attractive for low-power fully integrated receivers, but device mismatch and substrate coupling lead to large dc offsets that may be much larger than the received signal [29]. The amplifier presented in this article achieves ultralow-frequency ac response while completely rejecting large dc offsets, and may be of use in integrated direct-conversion systems.

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