A Low-Power Sub-GHz RF Receiver Front-End With Enhanced Blocker Tolerance

by

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Abstract

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Sub-GHz wireless systems have become a popular choice for Internet-of-Things (IoT) applications due to their lower cost, lower power consumption and longer transmission range compared to their 2.4 GHz counterpart. This thesis presents a class-AB sub-GHz RF receiver front-end for low power IoT applications. By exploiting transistors' class-AB operation in both the RF and baseband sections, the receiver front-end achieves a very low sensitivity and an elevated blocker tolerance while keeping a low power consumption. Such performance makes the receiver fully compliant with the short-range (e.g. IEEE 802.15.4) application and also suitable for the emerging long-range (e.g. LoRa) application. The proposed RF receiver front-end has been implemented in 0.13um CMOS technology, operates in the 868/915MHz ISM bands, and exhibits an in-band gain of 50dB, noise figure of 2.7dB, out-of-band IIP3 of +2dBm, out-of-band IIP2 of +37dBm, out-of-band P1dB of -10.5dBm, while draining 2.1mA from a 1.2V supply.

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List of Acronyms

ADC Analog-to-Digital Converter

BW Bandwidth

DUT Device Under Test

IIP2 Input-Referred Third-order Intercept Point

IIP3 Input-Referred Second-order Intercept Point

IM Intermodulation

IoT Internet of Things

LNA Low Noise Amplifier

LO Local Oscillator

LP-WAN Low-Power Wide Area Networks

LR-WPAN Low-Rate Wireless Personal Area Network

NF Noise Figure

NMOS N-Channel MOSFET

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

OP-AMP Operational Amplifier

OTA Operational Transconductance Amplifier

PER Packet Error Rate

PCB Printed Circuit Board

PMOS P-Channel MOSFET

RF Radio Frequency

SFDR Spurious Free Dynamic Range

SMA SubMiniature Version A

SNR Signal-to-Noise Ratio

TIA Trans-Impedance Amplifier

Chapter 1

Introduction

1.1 Motivation

The emerging development of Internet of Things (IoT) has opened up a huge market for sub-GHz applications in areas such as sensor networks, smart cities and personal health monitoring systems. Sub-GHz wireless systems have several advantages over their 2.4GHz counterparts including longer operation range and lower power consumption, which make them a popular choice for IoT applications. The trend in recent works [4], [5] for IoT receiver design is to primarily target ultra-low power consumption (sub-mW) while sacrificing the performance in sensitivity and linearity (i.e., the radio spurious free dynamic range SFDR). Though a low power consumption is important for battery-powered systems, worse sensitivity reduces the operative range by making such solutions not compliant with low power wide area networks (LP-WAN) [6]. Moreover, a reduction in linearity compromises the co-existence with other devices, especially in the presence of large interferers.

To address the above issues, this thesis aims to design a sub-GHz RF receiver front-end which deeply relies on class-AB operation to enhance its sensitivity and blocker resilience while keeping the overall power consumption low. Existing sub-GHz wireless standards include the IEEE 802.15.4 for short-range applications and LoRa for long-range applications. However, since LoRa does not release its PHY level specification to the public, the receiver front-end in this thesis will mainly target the IEEE 802.15.4 standard. Nevertheless, a low sensitivity performance will make the receiver suitable for any long-range application in general.

1.2 Thesis Outline

Chapter 2 - IEEE 802.15.4 Receiver System: This chapter overviews the IEEE 802.15.4 standard, compares different receiver architectures, discusses roles of critical design blocks in the receiver, and derives receiver's specifications based on the standard.

Chapter 3 - Design Solution: This chapter discusses the proposed receiver front-end architecture and the topology selection, implementation, and design trade-offs for its design blocks including the Low Noise Amplifier (LNA), Mixer, Trans-Impedance Amplifier (TIA) and Channel Selection Filter. Transistor level design and element sizing are examined. Simulation results of critical design parameters including the transfer function, input impedance matching, noise figure, and linearity are also provided.

Chapter 4 - Measurement Results: This chapter discusses lab measurement methods to verify the performance of the chip prototype, shows measurement results of the chip prototype, and compares the performance of the chip prototype with the state-of-the-art works.

Chapter 5 - Conclusion: This chapter highlights the achievements of this thesis and discusses future work.

Chapter 2

IEEE 802.15.4 Receiver System

2.1 IEEE 802.15.4 Overview

IEEE 802.15.4 is a specification for low-rate wireless personal area networks (LR-WPANs) [7]. It is specifically tailored for battery powered applications where low-power and low cost are the main requirements. It defines the physical layer (PHY) and media access control layer (MAC) for LR-WPANs. It serves as a basis for many other standards such as MiWi and Zigbee, which further extend the specification by developing upper layers not defined in IEEE 802.15.4. Zigbee is a popular IEEE 802.15.4-based standard for IoT applications. It simplifies the communication protocol which reduces the system complexity and implementation cost. The minimum requirement to meet the Zigbee standard (IEEE 802.15.4) is also more relaxed compared to other short-range wireless standards such as WLAN and Bluetooth (IEEE 802.11). Zigbee devices are very power-efficient because of their low duty cycle (<1%). They spend most of the time in the power-saving mode and wake up only every once in a while (e.g., a few milliseconds every minute) to transmit or receive signals [8]. As a result, Zigbee devices are able to operate on battery power for months or even years without battery replacement. Due to its low data rate (20kb/s), Zigbee is not meant for applications like Internet connection or file transmission. However, a low data rate is best suited for cost-efficient and power-efficient applications that only require the device to perform simple tasks like sensor readings [9].

Zigbee devices can operate in either sub-GHz (868MHz, 915MHz) or 2.4GHz ISM bands. The 865MHz band and 915MHz bands are used in Europe and North America, respectively, while the 2.4GHz bands can be used worldwide. Devices based on the sub-GHz standard have several advantages compared to their 2.4GHz counterpart. The worldwide applicability of

2.4GHz band is attractive for a wide range of applications, therefore the device has to co-exist in the same band with others operating on different standards such as WLAN and Bluetooth. This inevitably increases the design complexity for the transceiver to ensure a robust operation under strong interference. The sub-GHz standard, on the other hand, has a more relaxed co-existence situation. Sub-GHz signals also have a longer transmission range and are better at penetrating objects, another benefit compared to the 2.4GHz signals.

2.2 IEEE 802.15.4 Sub-GHz Radio Specification

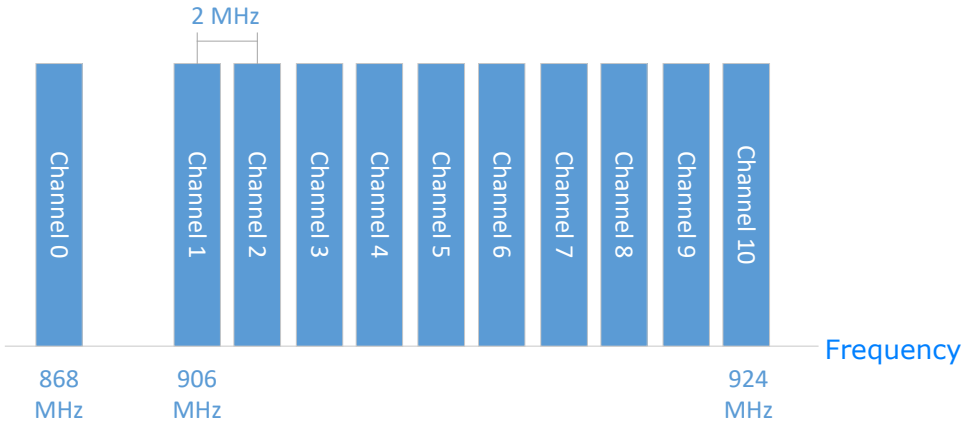


Figure 2.1: IEEE 802.15.4 Sub-GHz Channels

The IEEE 802.15.4 specification assigns a total of 11 signal channels in sub-GHz bands, as shown in Fig. 2.1. Channel 0 is in the 868MHz band with a bandwidth of 600KHz, and Channel 1-10 are in the 915MHz band with a bandwidth of 1.2MHz. The center frequencies of these channels are defined as follows:

$$\begin{aligned} Fc &= 868.3MHz, \quad \text{for k = 0} \\ Fc &= 906 + 2\,(k-1)MHz, \quad \text{for k = 1, 2, ..., 10,} \\ &\text{where k is the channel number} \end{aligned} \tag{2.1}$$

Fig. 2.2 shows the in-band blocker mask, which specifies the location and power of in-band interferers. The signal power in the adjacent channels is the same as the signal of interest, and the signal power in the alternate channels is 30dB higher than the signal of interest. Notice that only one interferer is expected to show up at a given time. While this blocker mask is a specification that must be met to be standard compliant, having better blocker tolerance allows

a device to operate in a more challenging environment. This is especially critical since out-of-band blockers are not specified in the standard and they are usually much stronger than in-band blockers.

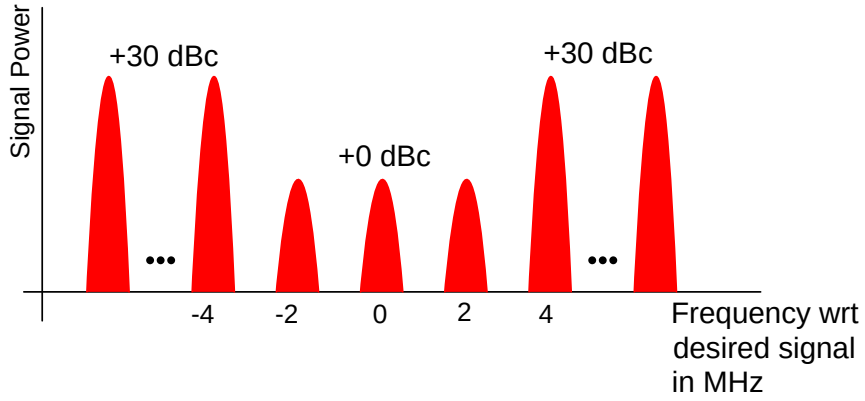


Figure 2.2: Blocker Mask

Receiver sensitivity is defined as the minimum input signal power that yields a specified packet error rate (PER), and should be smaller than -92dBm as per the specification. IEEE 802.15.4 sub-GHz signals use BPSK modulation, and the SNR at the output of the receiver should be higher than 6dB for a <1% PER. To ensure such output SNR, it is important to determine the maximum allowable SNR degradation from the input to the output of the receiver. This can be characterized by the noise figure:

$$\begin{aligned} NF &= SNR_{in} - SNR_{out} \\ &= \text{Sensitivity - Input Noise - } SNR_{out} \text{ (in dB)} \end{aligned} \tag{2.2}$$

The input noise is the noise generated from a source resistor integrated over the bandwidth of interest:

$$P_{noise\_in} = KTB \tag{2.3}$$

where K is Boltzmann constant, T is temperature in Kelvin, and B is signal bandwidth

From (2.3) the input noise is calculated to be -113dBm. Plug this value into (2.2), the noise figure is calculated to be 15dB. This means that the receiver can afford to have a 15dB SNR degradation and is still able to detect the signal.

Another important evaluation criteria for a robust receiver is its ability to survive in the presence of interferers. This can be characterized by the linearity performance. Due to the non-linear

characteristics of semiconductor devices, when two or more signal tones go through a circuit, they will produce an intermodulation (IM) product. The third-order intermodulation product (IM3) usually deserves the most attention because they are close to the input tones and can appear within the desired channel. For example, two strong out-of-band blockers may produce an IM3 higher than the noise floor overlapping the signal of interest. When this happens, the IM3 will greatly degrade the overall SNR resulting in signal detection failure.

The input-referred third-order intercept point (IIP3) specifies the input power level at which the IM3 intersects the fundamental tone and can be found as:

$$IIP3 = Pin + \frac{(Pin - IM3_{in})}{2} \tag{2.4}$$

Where P_{in} is the power of the fundamental tone, and $IM3_{in}$ is the power of the input-referred third-order intermodulation product

Unfortunately the standard does not specify the linearity requirement, therefore it can only be inferred from the specification. Assuming that P_{in} in (2.4) is the power of the alternate channel blocker (-62dBm) and $IM3_{in}$ is equal to the noise floor (Sensitivity - SNR), IIP3 is calculated to be -44dBm. This means that if the receiver achieves an IIP3 higher than -44dBm, the overall SNR of the receiver will not be limited by the non-linearity.

The last major factor that may degrade the SNR of the receiver is the image of the desired signal, as illustrated in Fig. 2.3. Suppose that the desired signal is Δf away from the LO, the

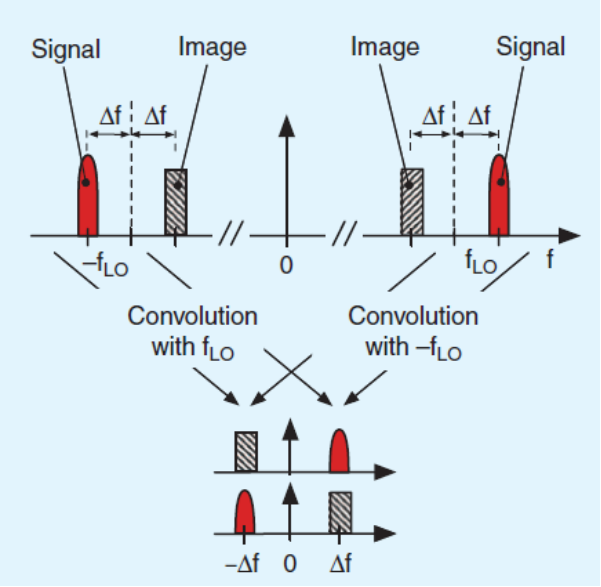


Figure 2.3: Image Before and After Down-Conversion [1]

signal which is Δf away from the LO on the opposite side is called the image of the desired signal. After down-conversion, the image will sit at the same intermediate frequency (IF) as the desired signal which effectively reduces the overall SNR. Again, the standard does not specify the image rejection requirement. But with proper selection of the IF frequency (e.g. <1MHz), the signal in the adjacent channel can be purposely made to be the image of the desired signal. This ensures that the image is of the same power as the desired signal and the minimum image rejection requirement in this case is 6dB.

The following table summarizes the minimum requirements for the receiver operating on the IEEE 802.15.4 sub-GHz specification:

Table 2.1: Sub-GHz Receiver Specifications

Channel 0	@868 MHz, 600 KHz bandwidth
Channel 1-10	@902 MHz - 928 MHz, 1.2 MHz bandwidth
Channel Spacing	2 MHz
Adjacent Channel Rejection	0 dB
Alternate Channel Rejection	30 dB
Receiver Sensitivity	-92 dBm
Noise Figure	15 dB
IIP3	-44 dBm
Image Rejection	6 dB
SNR	6 dB for < 1% PER

2.3 Receiver Architecture

Various RF receiver architectures have been developed over the past years. As different applications have different requirements on the cost, performance and power consumption, a certain architecture may be more suitable than the other. In this section, two modern receiver architectures, Direct-Conversion and Low-IF, will be compared based on their compatibility with the IEEE 802.15.4 sub-GHz standard.

To understand the operation of an RF receiver and the functionality of its building blocks, a typical receiver block diagram which can be used to represent either a Direct-Conversion or Low-IF structure is shown in Fig. 2.4. Since the desired RF input signal is very weak (e.g. -92dBm), a low-noise amplifier (LNA) is used to amplify such signal while adding minimum

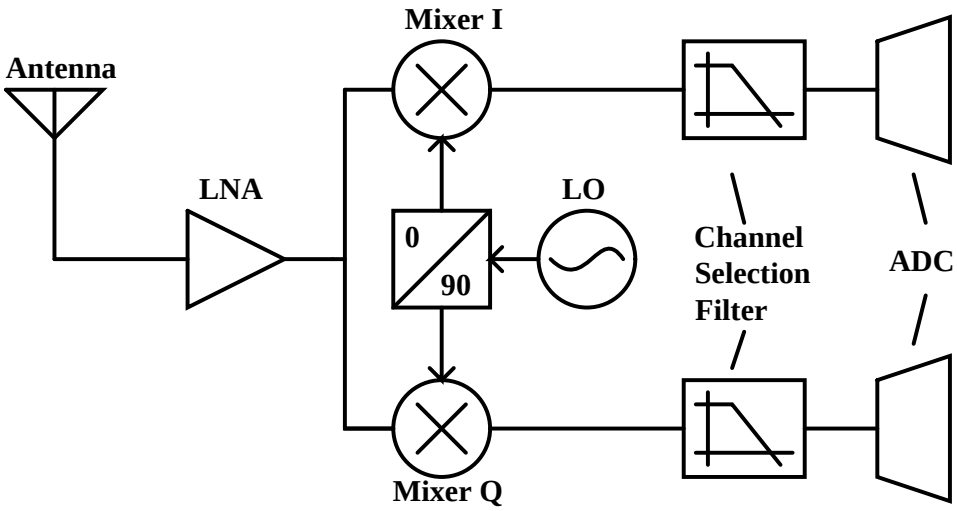


Figure 2.4: Typical Receiver Architecture

noise to it so that the overall SNR is not deteriorated. The LNA also needs to match its input impedance with the external source (e.g. antenna) to avoid signal reflection and ensure the maximum signal power delivery. Next, the in-phase (I) and quadrature (Q) mixers driven by quadrature clocks will down-convert the RF signal from carrier frequency to DC or a low IF, depending on whether a Direct-Conversion or Low-IF architecture is used. This is also known as the quadrature down-conversion scheme. A main advantage of using quadrature down-conversion is its image rejection capability. Suppose that the RF signal contains both the desired signal A_{sig} and its image A_{im}:

$$x_{RF}(t) = A_{sig}\cos((w_{LO}+w_{IF})t) + A_{im}\cos((w_{LO}-w_{IF})t) \tag{2.5}$$

After down-conversion, the two baseband signals on I and Q paths are:

$$x_I(t) = \frac{A_{sig}}{2}\cos(w_{IF}t) + \frac{A_{im}}{2}\cos(w_{IF}t) \tag{2.6}$$

$$x_Q(t) = -\frac{A_{sig}}{2}\sin(w_{IF}t) + \frac{A_{im}}{2}\sin(w_{IF}t) \tag{2.7}$$

Notice that the I and Q signals are 90° out of phase. If an additional 90° shift is introduced to the Q signal, it becomes:

$$x'_Q(t) = \frac{A_{sig}}{2}\cos(w_{IF}t) - \frac{A_{im}}{2}\cos(w_{IF}t) \tag{2.8}$$

It is clear that by adding (2.6) and (2.8), not only the desired signal is reconstructed, the image is eliminated as well.

Finally, since interferers are also down-converted to the baseband along with the desired signal, a channel selection filter is used to attenuate such interferers. The idea is to present a relatively "clean" baseband signal to the ADC so that a low power low dynamic-range ADC can be used to convert the signal into the digital domain for further signal processing.

2.3.1 Direct-Conversion Receiver

Direct-Conversion receiver (DCR) is a special variant of Low-IF receiver where IF is chosen to be at DC. It is also called Zero-IF receiver for this reason. Since the baseband signal centers at DC, a low pass filter with low cut-off frequency and sharp roll-off slope can be used for channel selection, making this structure excellent in rejecting interferers. DCR also tends to be more power efficient because gain and filtering can happen at a low frequency. Despite its apparent advantages, DCR has some drawbacks that may prevent it from being used for certain applications.

The first problem is the self-corruption of asymmetric signals. Modern modulation schemes such as FSK, QPSK, GMSK, and QAM contain asymmetric spectrum around the carrier frequency. This asymmetric nature of the signal is problematic in DCR because the image of the signal is the signal itself. Due to this reason, the image cannot be filtered in the analog domain by an image rejection filter such as a complex filter. Instead, image rejection is performed in the digital domain through IQ recombination, as mentioned previously. The unfiltered image together with the desired signal result in a higher dynamic range requirement for the ADC. The image rejection performance in a DCR depends on the gain and phase matching between I and Q signals. This can be characterized by the image rejection ratio IRR which stands for the ratio between the signal power and image power after IQ recombination:

$$IRR = \frac{(1+\varepsilon)^2 + 2(1+\varepsilon)\cos\Delta\theta + 1}{(1+\varepsilon)^2 - 2(1+\varepsilon)\cos\Delta\theta + 1} \tag{2.9}$$

Where ε is the gain mismatch and $\Delta\theta$ is the phase mismatch.

IRR is ideally infinite, however a real system will inevitably experience some amplitude and

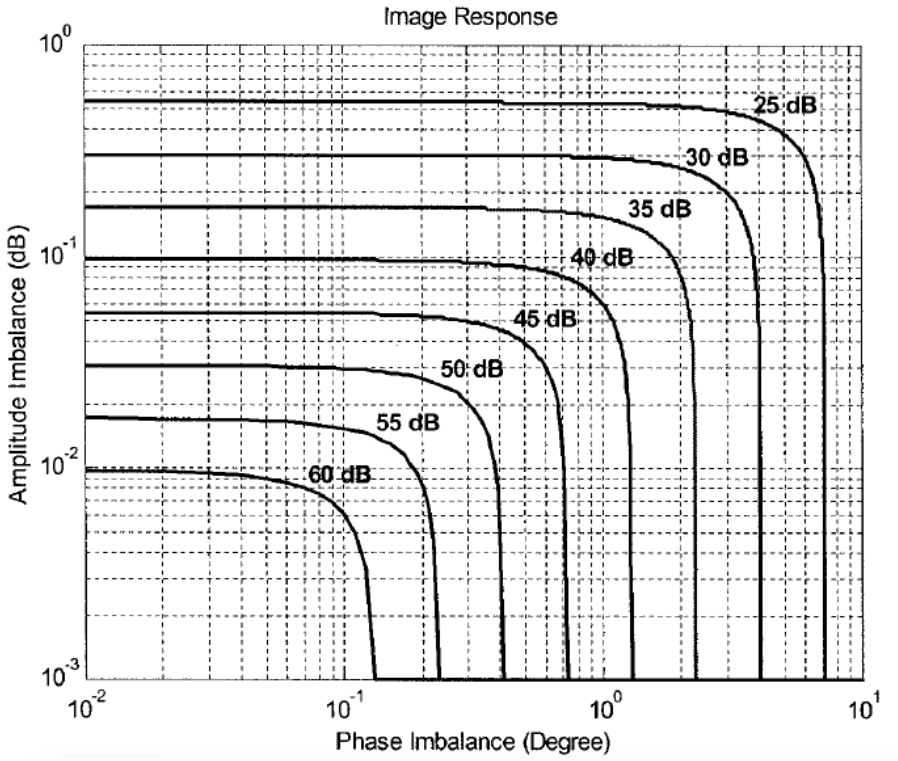


Figure 2.5: Image Rejection vs Amplitude and Phase Imbalance [2]

phase mismatch between the IQ signals which lead to a finite IRR. Fig. 2.5 shows the IRR with response to the amplitude and phase imbalance. For example, 1° phase mismatch and 0.5dB gain mismatch will result in a 25dB IRR.

The second problem is the DC offset due to LO self-mixing and 2^{nd} order distortion. LO self-mixing occurs when the LO signal leaks to the RF section through parasitic capacitors and re-mixes with the LO itself, creating a DC signal in the baseband [10]. Two tones can also create a low frequency beat near DC. Suppose that the RF signal contains two interferers at w_1 and w_2 with an amplitude of A: $V_{in}(t) = A\cos(w_1)t + A\cos(w_2)t$. Upon passing through a non-linear circuit such as LNA, the RF signal becomes:

$$\begin{aligned} V_{out} &= \alpha_1 V_{in}(t) + \alpha_2 V_{in}^2(t) \\ &= \alpha_1 A(\cos w_1 t + \cos w_2 t) + \alpha_2 A^2 \cos(w_1 + w_2)t + \\ &\quad \alpha_2 A^2 \cos(w_1 - w_2)t + ..., \end{aligned} \tag{2.10}$$

The low frequency component at $w_1 - w_2$ can show up in the baseband due to the mismatch in IQ mixers [10]. These DC signals are amplified along with the desired signal and can potentially saturate the receiver. In order to filter out such signals, a high-pass filter with very

low cut-off frequency should be introduced to the receiver. This not only damages the desired signal itself but also increases the system complexity as simple on-chip passive elements are infeasible to realize a low cut-off frequency near DC.

The last problem is DCR's sensitivity to the 1/f noise. The 1/f noise power is inversely proportional to frequency, making it particularly harmful for narrowband systems because a large portion of the signal band will fall into the 1/f regime, greatly degrading SNR.

In conclusion, DCR is best-suited for applications with a large signal bandwidth where the DC offset and 1/f noise can be remedied fairly easily without damaging the desired signal. But it is non-ideal for narrowband applications like IEEE 802.15.4.

2.3.2 Low-IF Receiver

Unlike a DCR where the IF is located at DC, a Low-IF receiver usually moves the IF away from DC up to a few MHz. The problems discussed above in the DCR also exist in the low-IF receiver but are not as severe. Since the baseband signal is now located at a higher frequency, the DC offset and 1/f noise can be remedied with a simple RC high pass filter without damaging the desired signal. The image rejection method by using IQ recombination in the digital domain is still feasible in low-IF receivers. Moreover, since the image is no longer the desired signal itself as in DCR, a complex filter can also be used for image rejection in the analog domain. The magnitude response of a N^{th} order complex filter can be described as:

$$|H(jw)| = \frac{1}{\sqrt{1+\left(\frac{w-w_c}{w_p}\right)^{2N}}} \tag{2.11}$$

where Wc is the center frequency, Wp is the pole location, and N is the filter order

Low-IF receivers operating on the IEEE 802.15.4 sub-GHz standard can choose an IF <1MHz so that the image becomes the signal in the adjacent channel which is of the same power as the desired signal. According to (2.11), a 3^{rd} order complex filter with a center frequency (IF in this case) of 800KHz and a cut-off frequency of 750KHz (for 1dB attenuation at the edge of the signal band) can attenuate the image by 20dB. Notice that such value can also be easily obtained by using IQ recombination even with a coarse matching condition (Fig. 2.5).

Overall, the low-IF structure better suits the IEEE 802.15.4 sub-GHz standard due to its insensitivity to the DC offset and 1/f noise.

2.4 Analog-to-Digital Converter

Modern RF receivers will place ADCs at the end of the receiver chain to convert the baseband analog signal into a digital form for further signal processing in the digital domain. Since an ADC's resolution is directly related to its power consumption, is it ideal if a low resolution ADC can be used for the conversion so that little overhead is added to the overall power budget. This requires the receiver front-end to filter out most of the interferers so as to reduce the signal's dynamic range upon arriving to the ADC. Table 2.2. shows the pre and post-filtered blocker mask for the IEEE 802.15.4 sub-GHz standard.

Table 2.2: Pre and Post Filtered Blockers

				alternate	adjacent	main	adjacent	alternate					
IF (MHz)	-9.2	-7.2	-5.2	-3.2	-1.2	0.8	2.8	4.8	6.8	8.8	10.8	12.8	14.8
Before filter (dBm)	-62	-62	-62	-62	-92	-92	-92	-62	-62	-62	-62	-62	-62
After filter (dBm)	-104.5	-98.1	-89.7	-77.1	-92.4	-92	-103.8	-87.6	-96.6	-103.4	-108.7	-113.1	-116.9

Table 2.2 assumes that the receiver chain provides a 3^{rd} order low-pass filtering with a cut-off frequency of 1.8MHz (for 1dB attenuation at the signal edge). The post-filtered signal is dominated by the blocker at -3.2MHz with a power of -77dBm, which sets the full-scale (FS) for the ADC. The SNDR of the ADC can then be found as:

$$SNDR = (FS + Creset\ Factor) - (Noise\ Floor - 10\ dB) \tag{2.12}$$

With a FS of -77dBm, crest factor of 3dB, noise floor of -113dBm, and an extra margin of 10dB, the SNDR of the required ADC is 50dB. This means that an ADC with 8-bit resolution should be used, according to the formula:

$$ENOB = \frac{(SNDR - 1.76)}{6.02} \tag{2.13}$$

The interferers beyond 14.8MHz will be filtered below the noise floor. This means that the sampling frequency of the ADC should be higher than 14.8MHz so that negligible amount of interferers will fold into the signal band. Finally, the power consumption of the ADC can be estimated based on the well-known figure-of-merit (FOM) [11]:

$$FOM = SNDR + 10\log\frac{BW}{Power} \tag{2.14}$$

The state-of-the-art ADC with a 2MHz bandwdith can achieve a 56.9dB SNDR with 820uW

power consumption [12]. Assuming that the ADC used in the receiver front-end achieves the same FOM as [12], the power consumption for such ADC (50dB SNDR) can be estimated based on (2.14) and is found to be 151uW. However, if the blockers are not filtered before arriving to the ADC, the ADC's full-scale will be dominated by the adjacent-channel blocker with a power of -62dBm. According to (2.12) and (2.14), the ADC in this case would require a SNDR of at least 63dB (the SNDR can be even higher due to unfiltered interferers folding in band after sampling) and consume 3mW. While the power consumption considered here is a very rough estimation, it nevertheless offers an insight into the choice of the receiver filtering profile. Therefore, the proposed receiver front-end will be designed to have a 3^{rd} order low-pass filtering capability.

Chapter 3

Design Solution

This section will discuss the proposed receiver front-end solution for the IEEE 802.15.4 sub-GHz standard. The topology selection and transistor level implementation for each of the blocks used in the receiver front-end will be presented including the LNA, Mixer, TIA and Channel Selection Filter. The function and performance of the proposed design blocks will be examined in detail together with theoretical analysis and simulation results.

3.1 Proposed Receiver Front-End

Recently, RF receivers exploiting class-AB LNA have shown to achieve a promising performance in power usage efficiency and blocker tolerance [13], [14]. The goal of the proposed solution is to extend the use of class-AB operation to the entire RF front-end. The structure of the proposed receiver is shown in Fig. 3.1. The LNA is followed by a pair of passive current mixers to implement a low-IF quadrature down conversion scheme. As typically happens in ultra-low power RF front-end, the LNA is single-ended. This choice reduces the power consumption of the RF section and avoids the use of an external balun, which would degrade the RX sensitivity with its insertion loss. The passive mixers, driven by a 25% duty-cycle clock, perform also a single-ended to differential conversion by making the remaining part of the receiver fully differential. An on-chip divider is designed to generate non-overlapping phases from an external LO. The receiver is completed by the analog baseband section where the down-converted current is sensed by a class-AB filtering TIA ac-coupled with a further filtering stage which makes the receiver fully compliant with the IEEE 802.15.4 blocker profile.

In the absence of large interferers, both the LNA and TIA will work in class-A drawing mini-

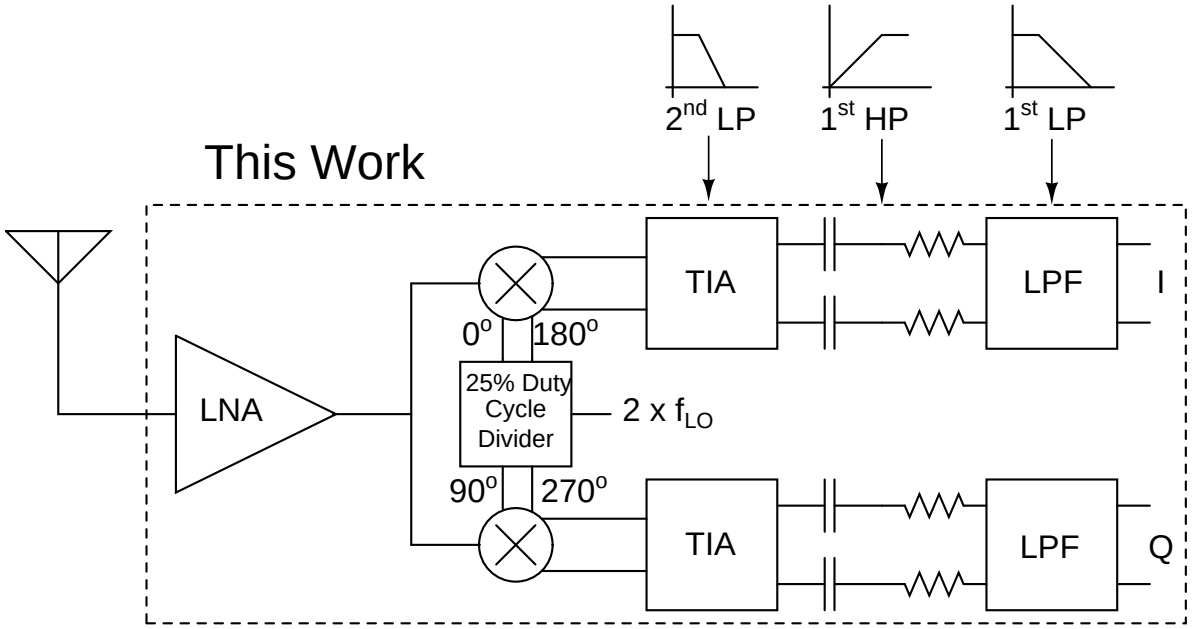


Figure 3.1: Proposed Receiver Front-End

mum current from the power supply. When large signals show up at the input of the receiver, both the LNA and TIA will operate in class-AB by handling the blockers without saturating the system. The LNA output and the TIA input are biased at the same dc value to ensure that nominally zero dc current flows through the mixer switches [15]. This eliminates the need for large decoupling capacitors at the input of the passive mixers to minimize the impedance seen by the LNA. As a result, the LNA experiences a low output voltage swing even in the presence of large blockers since its load is dominated by the low input impedance provided by the TIA, which is up-converted to the LNA output via the mixer [15]. This strategy avoids gain compression at the output of the LNA and improves linearity.

The TIA, with a 2^{nd} order filtering capability, is able to attenuate large out-of-band blockers at an early stage which greatly improves out-of-band linearity. The TIA together with the channel selection filter create an overall 3^{rd} order Butterworth filtering profile for the receiver front-end. Image rejection will be performed in the digital domain through IQ recombination. With an IF of 800KHz, the baseband signal spans between 200KHz and 1.4MHz. A high-pass filter with a cut-off frequency of as high as 200KHz is sufficient to filter the dc-offset and 1/f noise. The high-pass filter is realized with a passive RC circuit between the TIA and channel selection filter.

3.2 Low Noise Amplifier

3.2.1 LNA Overview

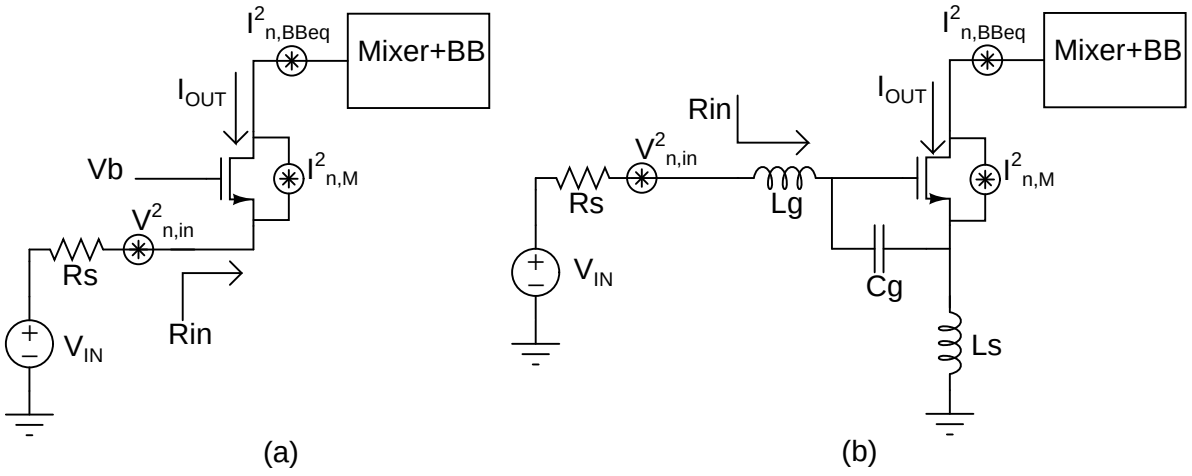


Figure 3.2: Common-Gate and Common-Source LNA

There are several challenges in the LNA design. As the first block in the receiver chain, it dictates the overall receiver noise performance. It is usually the most power consuming block in the receiver, therefore minimizing its power consumption is critical for low power applications. Since the LNA interfaces with pre-filtered RF signals, it should also be sufficiently linear in order to withstand large interferers. Over the past years, extensive studies have been done on LNA topologies to target various design requirements. However, most of the LNA topologies are built upon the two fundamental structures - the Common Gate (CG) and Common Source (CS) LNA (Fig. 3.2)[10].

Both LNAs in Fig. 3.2 have a current output and are loaded by a TIA via a mixer. In Both structures, a real input impedance R_{in} is synthesized to match with the 50Ω source resistor R_s over the bandwidth of interest. There are three main noise sources in both LNA structures. The first one is the voltage noise $V_{n,in}^2 = 4KTR_s$ from the source resistor R_s (which comes from the antenna and cannot be reduced). The second one is the transistor's current noise $I_{n,M}^2 = 4KT\gamma g_m$. And the last one is the up-converted baseband current noise $I_{n,BBeq}^2$, which is usually dominated by the TIA's input transistor noise. The noise coupling between I and Q paths can be ignored to simplify the noise calculation[16].

To determine the up-converted baseband noise, consider the model in Fig. 3.3. V_n^2 is the input-referred voltage noise of the opamp used in the TIA. $I_{n,BB}^2$ is the input-referred current noise of

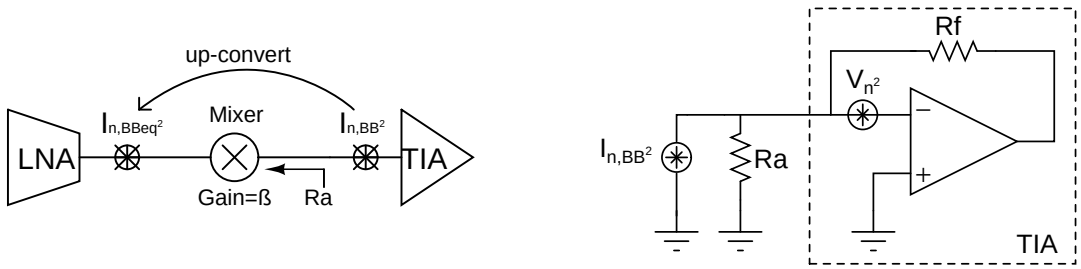


Figure 3.3: Up-Converted BB Noise Model

the TIA due to V_n^2. $I_{n,BBeq}^2$ is the up-converted current noise of the TIA that appears on the RF side. Ra is the source impedance of the TIA looking into the output of the mixer. And β is the mixer's conversion gain, which is equal to $\sqrt{2}/\pi$ when the mixer is driven by 25% duty-cycle clocks. The input-referred current noise of the TIA can be computed as [17]:

$$I_{n,BB}^2 = \frac{V_n^2}{(R_a \parallel R_f)^2} \tag{3.1}$$

Assuming that V_n^2 comes from the input transistor in the opamp, its value then becomes $4KT/g_{m,op}$ (where $g_{m,op}$ is the transconductance of the input transistor). Substitute it back into (3.1) and divide (3.1) by the mixer's gain, the up-converted baseband current noise becomes:

$$I_{n,BBeq}^2 = \frac{4KT\gamma}{g_{m,op}\beta^2(R_a \parallel R_f)^2} \tag{3.2}$$

Next, the transfer function, input impedance, and noise figure for the CG LNA are presented below.

Transfer function (CG):

$$\frac{I_{out}}{V_{in}} = \frac{g_m}{1+R_s g_m} = \frac{g_m}{2} \tag{3.3}$$

Input Impedance (CG):

$$R_{in} = \frac{1}{g_m} \tag{3.4}$$

The input impedance of the CG LNA is ideally constant over frequency. In reality, however, it changes with frequency when parasitic capacitance of the transistor is taken into account. Nevertheless, the CG LNA can still provide a relatively wide band input impedance matching. Since the input impedance is directly related to the trans-conductance (which in turn is related to the power consumption) of the LNA, there is no much freedom in choosing the power consumption of the CG LNA.

Noise Figure (CG):

$$NF = 1 + \gamma + \frac{4\gamma R_s}{g_{m,op}\beta^2 (R_a \parallel R_f)^2} \tag{3.5}$$

With $\gamma \approx 1$, the NF is at least 3dB. While the NF can be lowered by increasing g_m, doing so will violate the $R_s = 1/g_m$ input matching condition. There are techniques that allow one to increase g_m while maintaining the input matching condition, such as using a feedback or feed-forward loop in the conventional CG LNA [10]. However, this additional degree of freedom is paid with the price of increasing either the power consumption or the complexity of the loop.

The transfer function, input impedance, and noise figure for the CS LNA are presented below. The passive network at the input (Fig. 3.2(b)) not only provides impedance matching but also creates a Q boost on the transistor gate at resonance.

Transfer function (CS):

$$\frac{I_{out}}{V_{in}} = \frac{g_m Q}{2} \tag{3.6}$$

$$\text{Where } Q = \frac{1}{W_o C_g R_s}$$

Input Impedance (CS):

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_g} + \frac{g_m}{C_g} L_s \tag{3.7}$$

g_m/C_g (also known as w_t) and L_s synthesize the frequency-independent real part of the input impedance. At resonant frequency, L_s, L_g and C_g cancel out the imaginary part of the input impedance providing a narrow band matching to the source resistor. Unlike the CG LNA, the input impedance of the CS LNA does not correlate with the power consumption. Therefore, a low power design can be achieved for the CS LNA. The disadvantage of this topology is the large silicon area occupied by the passive elements, especially the integrated inductors. This problem becomes worse for sub-GHz applications, as even larger inductors are required to resonate with capacitors under 1GHz. This leads to a L_g too large to be integrated on-chip and therefore realizing it off-chip is the only option.

Noise Figure (CS):

$$NF = 1 + \frac{\gamma}{g_m R_s Q^2} + \frac{4\gamma}{g_{m,op}\beta^2 (R_a \parallel R_f)^2 g_m^2 Q^2 R_s} \tag{3.8}$$

Since the real part of the input impedance does not only depend on g_m, the noise can be designed to be arbitrarily small by increasing g_m. In addition, the Q boost on the transistor gate

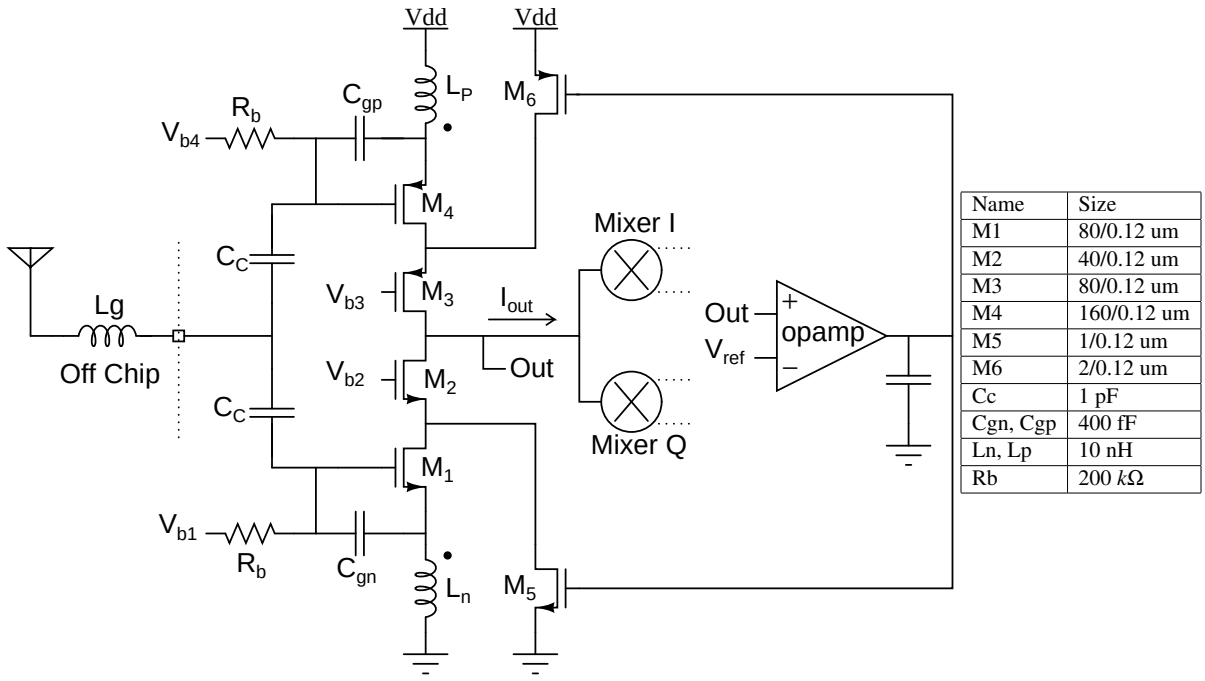
further reduces the noise by Q^2. Therefore, with the proper choice of design parameters, low noise and input matching can be achieved simultaneously.

Table 3.1 compares the performance of the CG and CS LNA. Since low noise and low power are the two key objectives for the target receiver design, plus IEEE 802.15.4 channels only span a narrow bandwidth (<100MHz), the CS LNA is a more suitable option.

Table 3.1: Common-Gate vs. Common-Source LNA

Topology	Gain	Input Impedance	Noise	Power
CG	Low	Wide Band	High (>3dB)	High due to 1/gm matching condition
CS	High	Narrow Band	Low (<3dB)	Low and can tradeoff with noise

3.2.2 Proposed LNA



Name	Size
M1	80/0.12 um
M2	40/0.12 um
M3	80/0.12 um
M4	160/0.12 um
M5	1/0.12 um
M6	2/0.12 um
Cc	1 pF
Cgn, Cgp	400 fF
Ln, Lp	10 nH
Rb	200 $k\Omega$

Figure 3.4: Class-AB PN Complementary LNA

The conventional CS LNA in Fig. 3.2(b) has been widely used for narrow band applications because of its high gain and low noise performance. Several techniques have been proposed to modify this classical topology to reduce its power consumption and increase its linearity. One of them is the current re-use technique where a NMOS stage and a PMOS stage share the bias current thereby increasing the effective g_m for a given bias current [18]. In the design proposed in [18] the structure was biased to operate only in class-A with a limited blocker

tolerance. Increasing the gate-source overdrive voltage can improve the linearity, but the bias current should be increased as well. To enhance blocker tolerance without sacrificing power consumption, the LNA can be biased in class-AB [13], [14].

The proposed LNA in Fig. 3.4 uses the PN complementary structure which simultaneously achieves current re-use and class-AB biasing. The complementary transistors M1 and M4 operate in the weak inversion region to maximize the g_m/I_d ratio. PMOS transistors are sized two times larger than NMOS transistors to compensate for their smaller mobility. To reduce the area of the design, Ln and Lp inductors are realized through an integrated transformer and coupled each other. The g_{mn}/C_{gn} and g_{mp}/C_{gp} ratios have been designed to be approximately the same so that a 1:1 transformer could be used thereby simplifying the layout and having a full symmetric structure. At sub-GHz frequencies, an off-chip inductor (L_g) is required to resonate the input network and provide the required input impedance matching. The LNA's dc output voltage is set through a current-mode feedback injecting into the source of M3 and M2. The current-mode approach simplifies the compensation of the feedback loop and reduces the parasitic capacitance introduced by the biasing network. The LNA consumes 550uA current.

Transfer function (Proposed LNA):

$$\begin{aligned} \frac{I_{out}}{V_{in}} &= \frac{g_{mp}Q_p + g_{mn}Q_n}{2} \\ \text{Where } Q_p = \frac{1}{W_o C_{gsp} R_s} &\text{ and } Q_n = \frac{1}{W_o C_{gsn} R_s} \end{aligned} \tag{3.9}$$

Clearly, the addition of PMOS input stage increases the transconductance gain.

Input Impedance (Proposed LNA):

$$\begin{aligned} Z_{inp} &= \frac{g_{mp}L_p}{C_{gp}} + sL_p + \frac{1}{sCgp} \\ Z_{inn} &= \frac{g_{mn}L_n}{C_{gn}} + sL_n + \frac{1}{sCgn} \\ Z_{in} &= sL_g + Z_{inp} \parallel Z_{inn} \end{aligned} \tag{3.10}$$

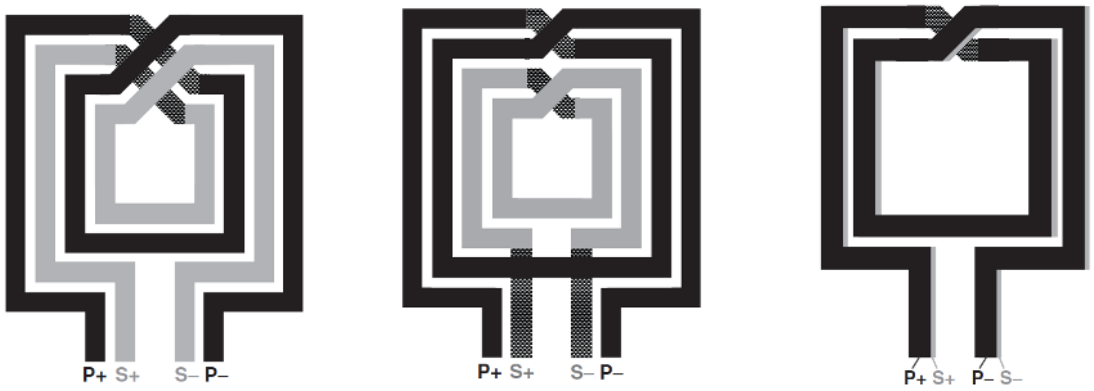
The input impedance of the proposed LNA can be viewed as two CS LNA input impedance placed in parallel. NMOS and PMOS input stages synthesize their respective real impedance R_{inp} and R_{inn} which together produce an equivalent 50Ω resistance to match with Rs. The remaining imaginary part is cancelled out with an external Lg at resonant frequency.

Noise Figure (Proposed LNA):

$$NF = 1 + \frac{\gamma}{R_s}\frac{g_{mp}+g_{mn}}{(g_{mp}Q_p+g_{mn}Q_n)^2} + \frac{4\gamma}{g_{m,op}\beta^2(R_a \parallel R_f)^2(g_{mp}Q_p+g_{mn}Q_n)^2R_s} \tag{3.11}$$

To understand the benefit of using the proposed structure on the noise figure, consider a special case where $g_{mp} = g_{mn} = g_m$ and $Q_p = Q_n = Q$. NF in this case is simplified to $1 + \frac{\gamma}{2g_mR_sQ^2} + \frac{\gamma}{g_{m,op}\beta^2(R_a \parallel R_f)^2g_m^2Q^2R_s}$. Compare this equation with (3.8), the noise from the active elements (second term) is reduced by half and the noise from the loading (third term) is reduced by four times. Indeed, in the proposed structure, the noise power from the active devices doubles due to the additional PMOS input stage, and the noise power from the loading remains the same. However, the signal power is quadrupled because the transconductance gain is doubled. Therefore, the overall noise figure of the proposed LNA is significantly lower than the conventional CS LNA.

3.2.3 Transformer Design



(a) Interleaved (b) Tapped (c) Stacked

Figure 3.5: Common Transformer Structures [3]

The LNA in [18] uses two on-chip inductors for Ln and Lp which occupies a large area. In the proposed LNA, these two inductors are replaced by an on-chip transformer. The total chip area is reduced as a result.

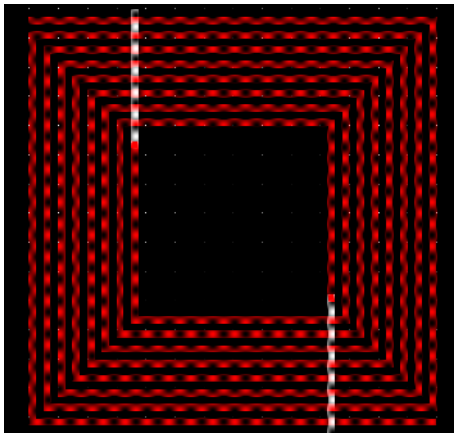
The performance of a transformer can be characterized by its magnetic coupling, self-inductance and self-resonant frequency. Magnetic coupling and self-inductance together create the overall inductance of a transformer coil. Self-resonant frequency is the frequency up to which the coil behaves as an inductor. It sets the maximum frequency at which the transformer can be used.

Three common transformer structures are shown in Fig. 3.5 and their respective performances are summarized in Table 3.2 [3].

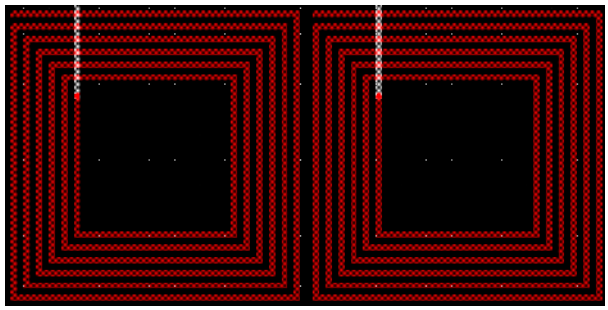
Table 3.2: Common Transformer Structures Comparison

Structure	Coupling	Self-Inductance	Area	Self-Resonance
Interleaved	> 0.7	Medium	Medium	Medium
Tapped	0.3 - 0.7	Low	Large	High
Stacked	0.9	High	Small	Low

Tapped structure has the highest self-resonant frequency because the two coils are separated thereby minimizing the inter-coil capacitance. Its downside is the poor magnetic coupling and large area occupation. The stacked structure allows two coils on different metal layers to stack on top of each other, which maximize the magnetic coupling and self-inductance and minimizes the area occupation. This structure, however, has a poor self-resonant frequency due to the increased capacitance between the two coils and from the bottom coil to the substrate. The interleaved structure has two interleaved coils constructed on the same metal layer, resulting in a fairly high magnetic coupling, medium self-inductance and medium self-resonant frequency. Since the interleaved structure allows perfect symmetry between the two coils, does not have any serious drawbacks, and has sufficiently good performance for LNA operating in sub-GHz, it becomes the structure of choice in the proposed LNA design.



(a) Transformer $270um \times 270um$



(b) Individual Inductors $230um \times 230um \times 2$

Figure 3.6: ASITIC - Transformer VS Individual Inductors

Once the transformer structure is determined, a fast simulator such as ASITIC can be used to quickly estimate the transformer's performance for a given set of geometry parameters. In Fig. 3.6(a), a 1:1 interleaved square transformer is constructed in ASITIC. The equivalent inductance of the two coils matches with Ln and Lp in Fig. 3.4.

Fig. 3.6(b) shows a realization of Ln and Lp with two square inductors using the same metal width and spacing as the transformer in Fig. 3.6(a). In addition, the two square inductors are sized to have the same self-inductance and quality factor as the two coils in the transformer in Fig. 3.6(a). Compared Fig. 3.6(a) and Fig. 3.6(b), using a transformer reduces the area occupation by approximately 31%.

While a fast simulator allows the designer to quickly characterize a transformer and determine its geometry parameters, it usually has a poor estimation on the transformer's actual performance. Hence, a more accurate EM simulator HFSS is used to accurately characterize the proposed transformer structure, as shown in Fig. 3.7.

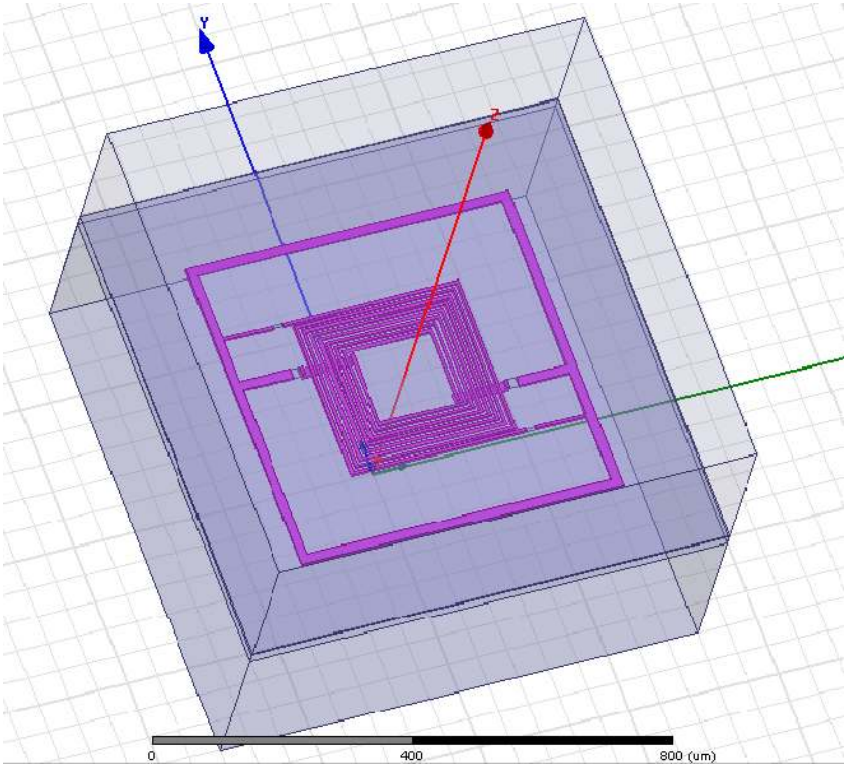


Figure 3.7: HFSS - Transformer

With the same geometry setting, simulation results of the transformers created by ASITIC and HFSS are compared in Fig. 3.8 - 3.10

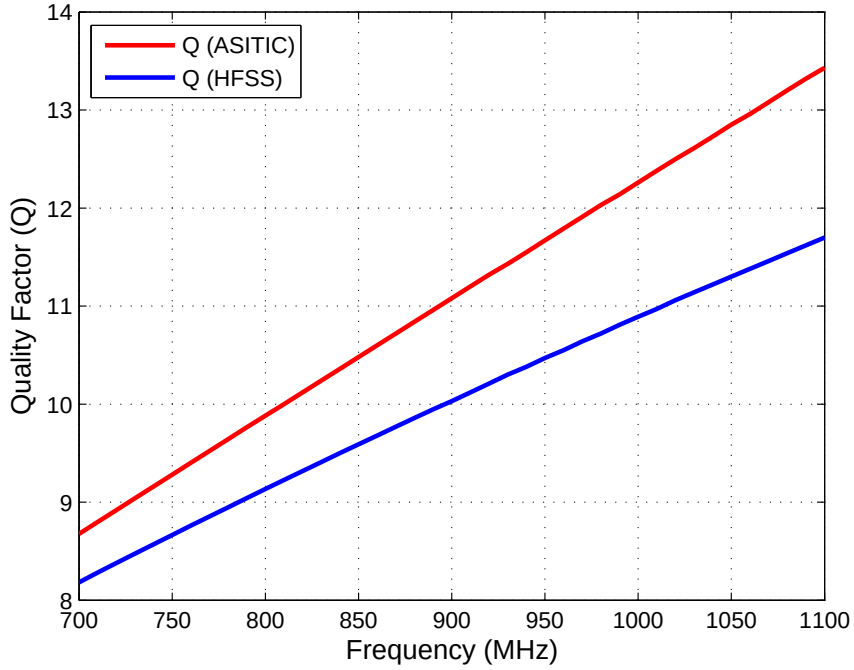


Figure 3.8: ASITIC vs HFSS - Quality Factor

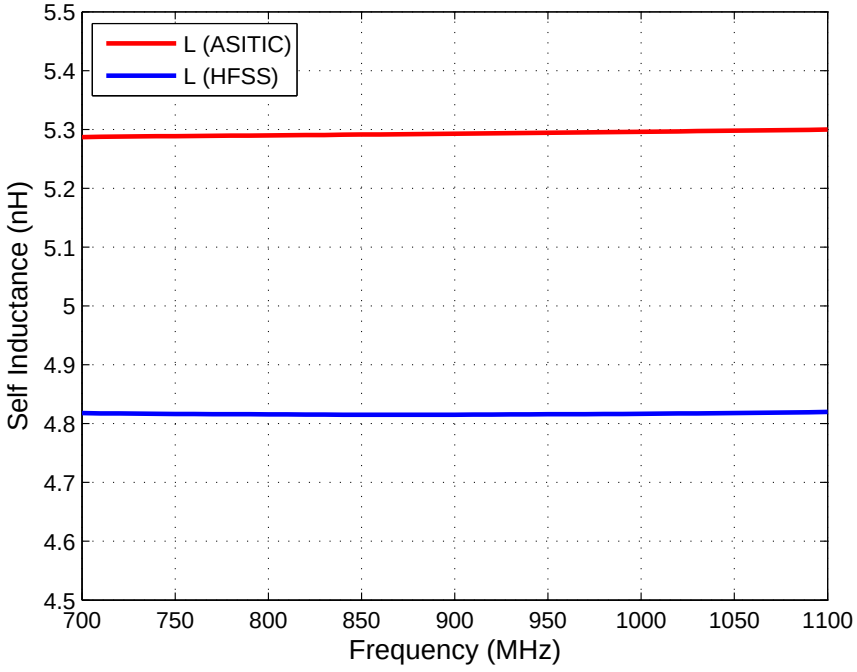


Figure 3.9: ASITIC vs HFSS - Self Inductance

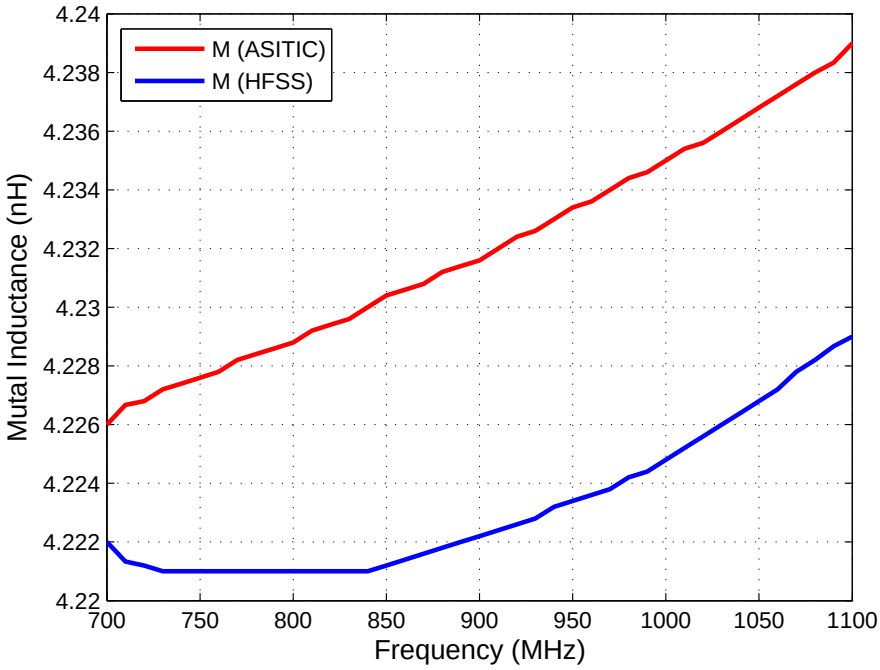


Figure 3.10: ASITIC vs HFSS - Mutual Inductance

Fig. 3.8 - 3.9 only shows the quality factor and self-inductance of one coil. The second coil has the same characteristics due to the symmetrical structure of the proposed transformer. Comparing the simulation results from the two simulators, it is clear that ASITIC overestimates the transformer's quality factor and self-inductance. To be conservative, the transformer model created by HFSS will be used in the receiver design.

3.2.4 Simulation of Proposed LNA

Fig. 3.11 shows the test bench for the proposed LNA simulation. An additional 300fF capacitor that captures the parasitic capacitance of the pad and package is added to the RF input. The LNA is loaded by a pair of ideal IQ mixers (switches) driven by 25% duty-cycle clocks. The baseband circuit is represented by an ideal 1^{st} order low-pass TIA with a $25k\Omega$ trans-impedance gain, 250Ω input impedance, and 2MHz cut-off frequency. To include the baseband noise in the simulation, a $2.5k\Omega$ noisy resistor $R_{n,BB}$ which represents the op-amp's input-referred noise is inserted in front of the op-amp. The noise from $R_{n,BB}$ is equivalent to the noise from an input differential transistor pair with a $800uS$ g_m . A transformer model obtained from the HFSS simulator is also included in the simulation. Simulation results are summarized

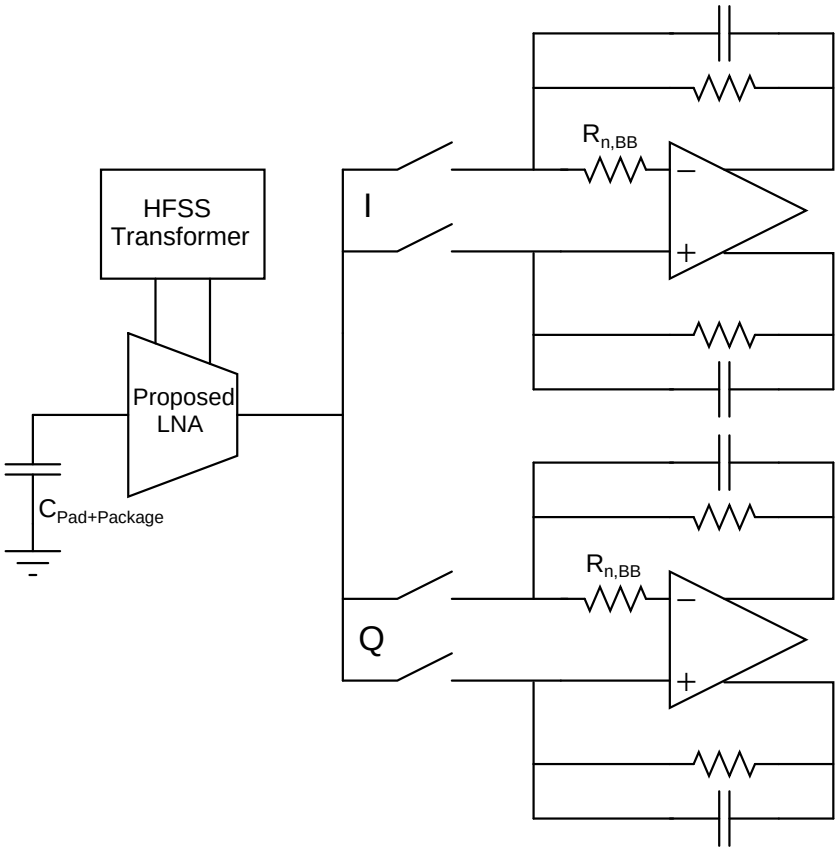


Figure 3.11: Proposed LNA Simulation Test Bench

in Fig. 3.12-3.19. The LNA achieves S_{11}<-10dB over 200MHz bandwidth, 45mS transconductance gain, and 1.8dB noise figure. The out-of-band IIP3 test is performed with two tones placed at [LO+10MHz, LO+19MHz] and an IIP3 of 0dBm is achieved. The out-of-band P1dB compression test is performed by placing a tone at LO+50MHz and sweeping its power until the gain drops by 1dB. The LNA achieves a P1dB of -10.5dBm. Fig. 3.18 and Fig. 3.19 show the drain currents of the NMOS and PMOS input stages in the proposed LNA in the presence of a blocker at LO+50MHz. When the blocker power is small (e.g. -40dBm), the LNA works in class-A (Fig. 3.18). When the blocker power is large (e.g. -15dBm), the LNA works in class-AB (Fig. 3.19).

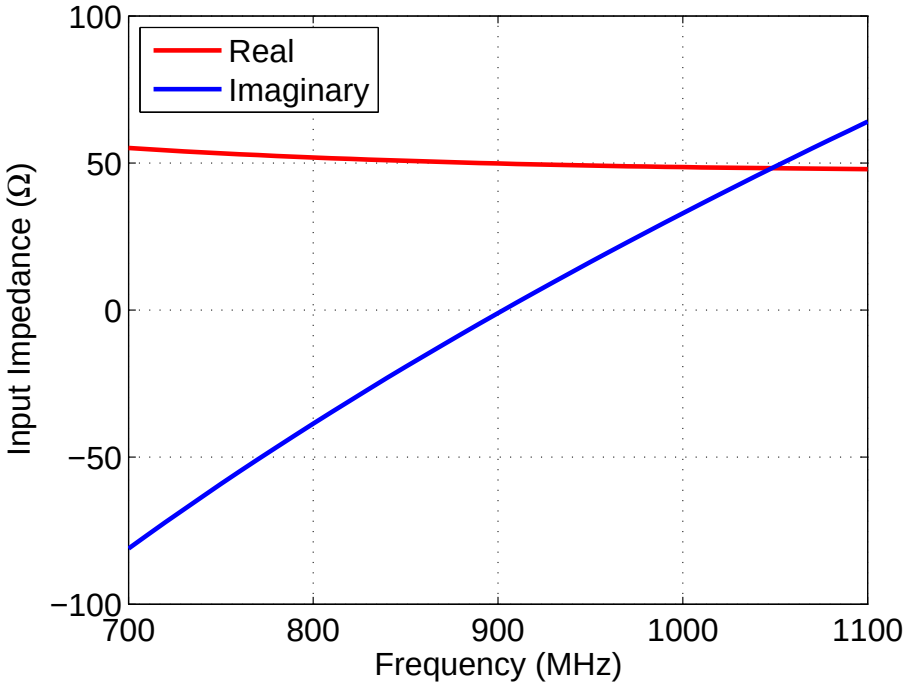


Figure 3.12: Proposed LNA: Input Impedance

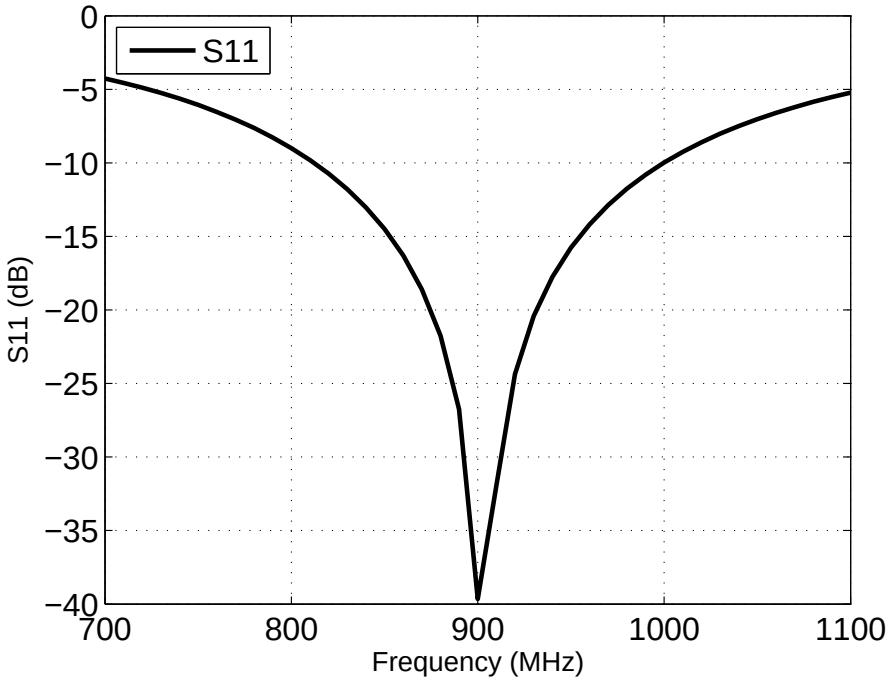


Figure 3.13: Proposed LNA: S11

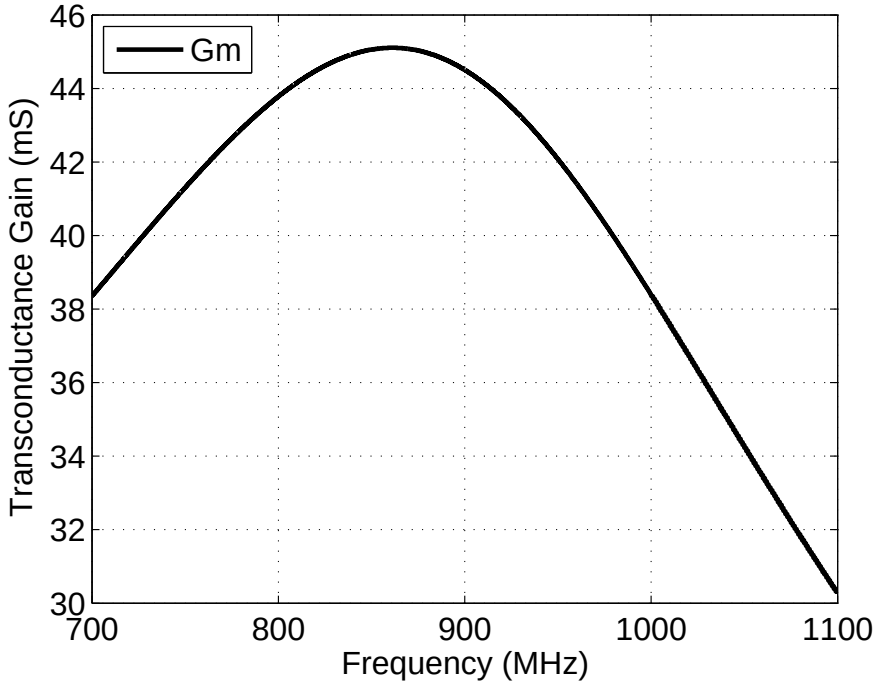


Figure 3.14: Proposed LNA: Transconductance Gain

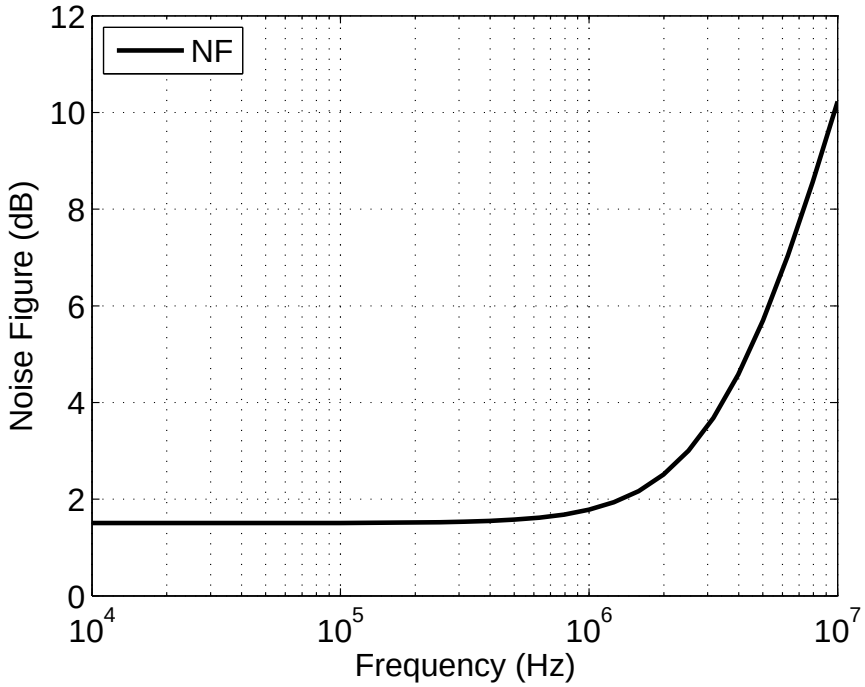


Figure 3.15: Proposed LNA: Noise Figure

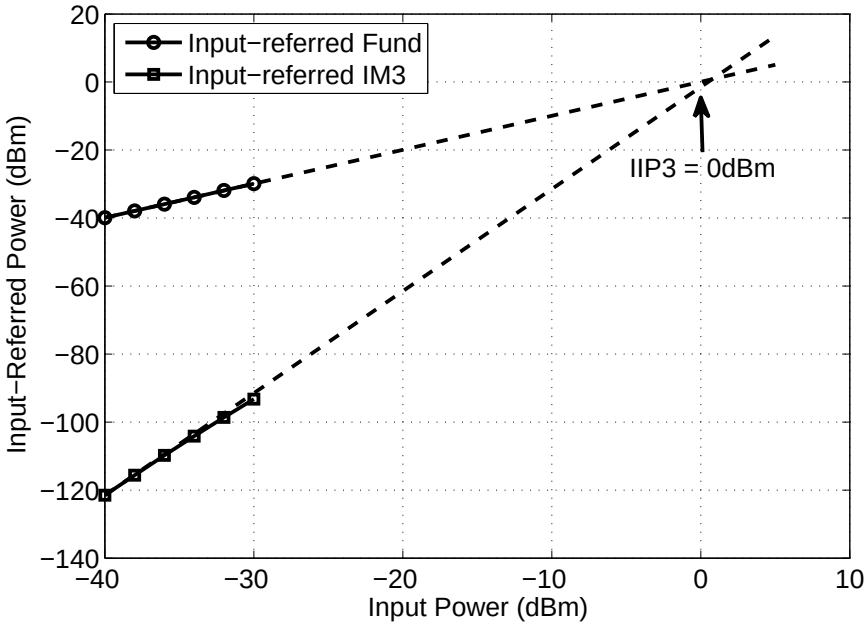


Figure 3.16: Proposed LNA: IIP3

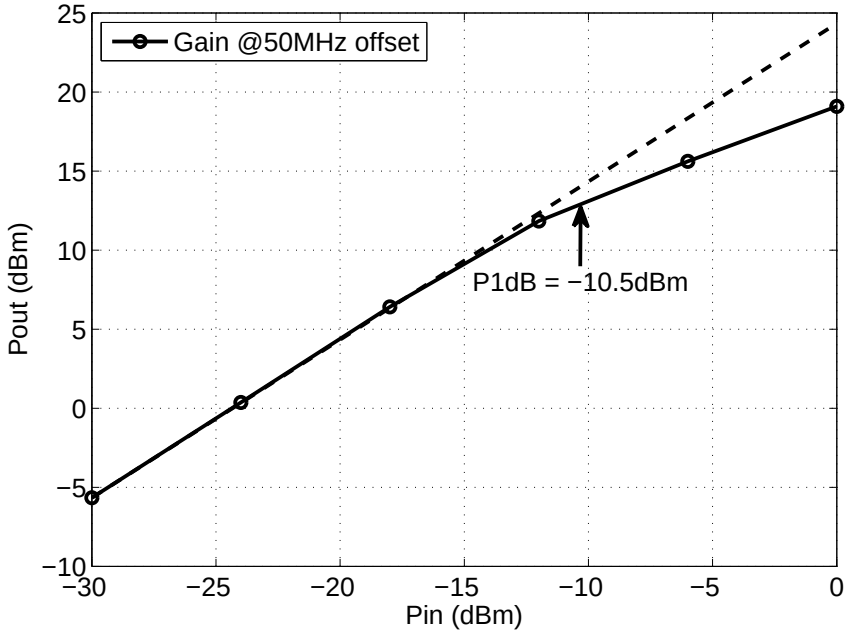


Figure 3.17: Proposed LNA: P1dB

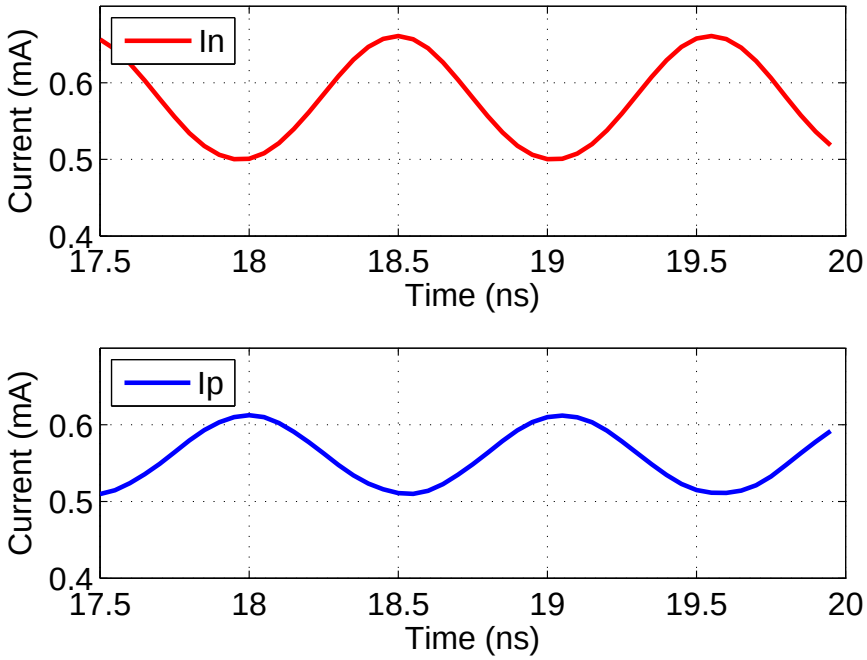


Figure 3.18: Proposed LNA: Class-A Operation

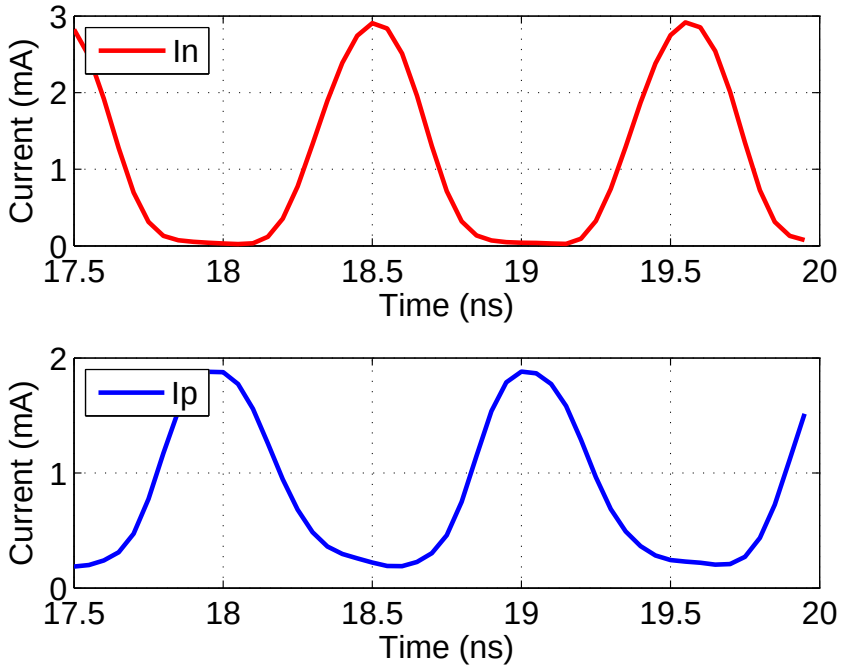


Figure 3.19: Proposed LNA: Class-AB Operation

3.3 Mixer

3.3.1 Mixer Overview

In RF receivers, the mixer is responsible for down-converting the RF signal to the IF by multiplying the RF signal with LO signals. Mixer topologies can be classified as active mixers and passive mixers. Active mixers are able to provide a high gain but they require active current biasing and hence consume power. Due to the high gain, the noise contribution from the following stages in the receiver chain are suppressed making active mixers a good choice for low noise applications. Passive mixers, on the other hand, does not provide gain because their transistors do not have active current biasing. However, they are well-suited for applications where low power is the primary objective. It has also been shown that passive mixers have a better linearity and flicker noise performance compared to their active counterparts [19], [20], [21], [22]. Therefore, a passive mixer will be used in the proposed receiver front-end.

3.3.2 Proposed Mixer

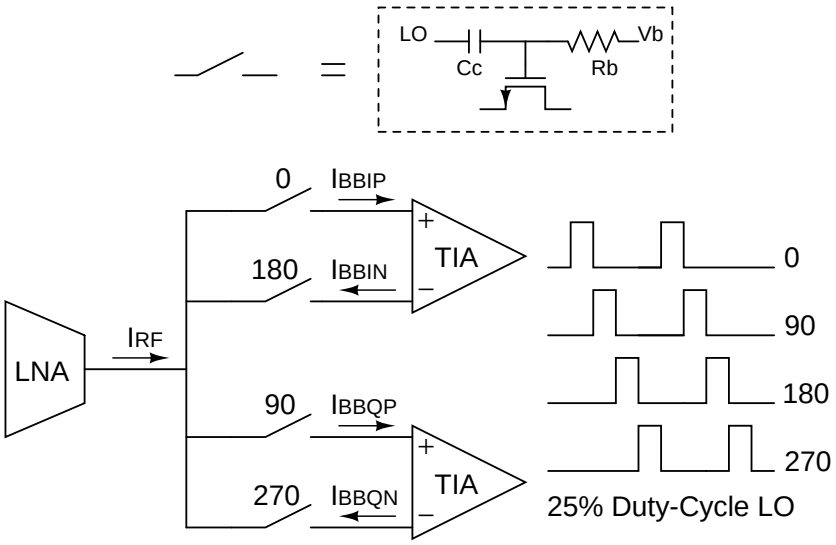


Figure 3.20: Single-balanced Current-driven Passive Mixer

The proposed mixer structure is the single-balanced current-driven passive mixer, as shown in Fig. 3.20. The mixer is driven by the LNA on the RF side and loaded by the TIA with a low input impedance on the baseband side. A single-balanced structure is used because the LNA is single-ended. Both end of the mixer are biased at the same DC level to ensure zero DC current

flowing through. NMOS transistors are chosen since they can achieve the same on-resistance as PMOS transistors with a smaller size. A smaller size also means a smaller capacitive loading for the LO generator. A series capacitor Cc isolates the transistor's gate bias from the LO generator thus allows gate bias control for threshold adjustment. The four single-balanced mixers driven by 25% duty-cycle quadrature clocks will down convert the single-ended RF signal to two differential baseband IQ signals. It has been shown that using 25% duty-cycle clocks can eliminate IQ cross-talk and also increase the conversion gain compared to using 50% duty-cycle clocks [23]. The conversion gain of a single mixer is:

$$H(s) = \frac{1}{2\pi}\frac{\sin(\pi d)}{2d} \tag{3.12}$$

Where d is the duty cycle of the LO signal and is 0.25 in this case. The conversion gain from RF to baseband on the I(Q) path (differentially) is therefore $\frac{\sqrt{2}}{\pi}$ (-6.94 dB).

The operation procedure for the proposed mixer is presented in Fig. 3.21 [24]. In Fig. 3.21(a), the LNA is modelled by a current source I_{rf} in parallel with a loading capacitor C_{lna}. Mixer A represents either the I or Q mixer. In Fig. 3.21(b), a duplicated mixer B is created and placed in parallel with the original mixer A. The two mixers are driven by the same LO. However, I_{rf} and C_{lna} are now separated and attached to the input of the two mixers respectively. This transformation does not alter the actual behaviour of the mixer if the switches are ideal. In Fig. 3.21(c), I_{rf} is down-converted to I_{BB} on the I(Q) path via mixer B. Only the $f_{rf} - f_{LO}$ component is significant in I_{BB} because higher order harmonics are filtered by the low-pass shaped Z_{BB}. The equivalent driving impedance Z_{eq} looking from the output of mixer A can be obtained through the switched-capacitor approach. Finally, a continuously time model capturing the transfer function of the mixer is obtained in Fig. 3.21(d).

Since the proposed mixer utilizes quadrature clocks with 25% duty-cycle, the conventional switched-capacitor approach which requires a 50% duty cycle clock is infeasible to evaluate Z_{eq}. To find Z_{eq} in this case, an evaluation procedure proposed in [24] is presented in Fig. 3.22. A test voltage Vx is placed on the I path output and a correlated test voltage jVx is placed on the Q path output. During a clock period, C_{lna} samples $\frac{V_x}{2}$ and $\frac{jV_x}{2}$ alternatively leading to an average charge transfer of $\frac{(1-j)C_{lna}V_x}{2}$ through the mixer. I_x can then be obtained by multiplying this value with the clock frequency. Finally, the differential driving impedance Z_{eq} becomes:

$$Zeq = \frac{1+j}{C_{lna}f_{lo}} \tag{3.13}$$

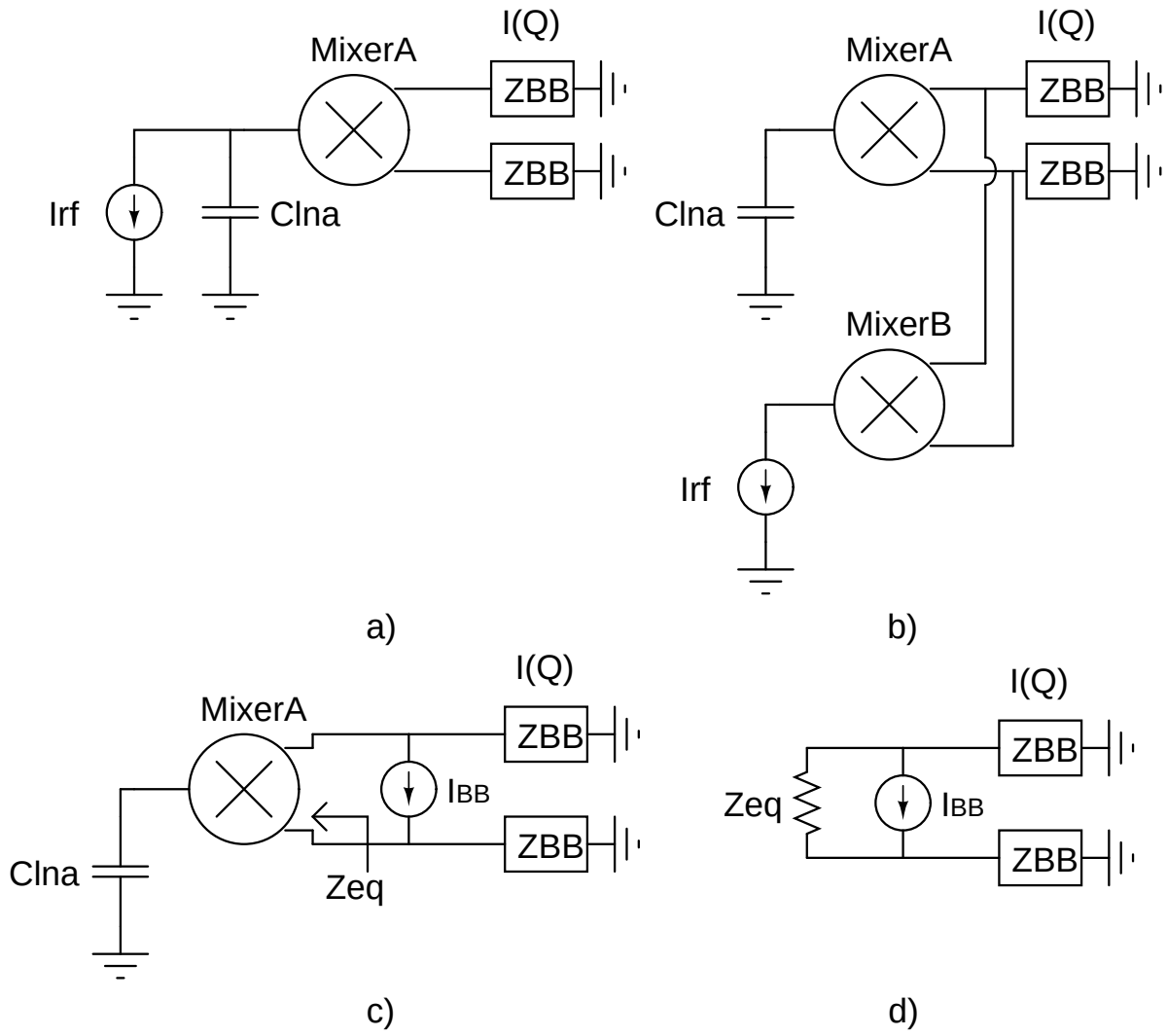


Figure 3.21: Derivation of CT model for mixer

Having obtained the equivalent continuous-time model for the proposed mixer, the value of the baseband loading can be determined for a certain conversion gain. With a 200fF C_{lna} and 900MHz f_{lo}, the magnitude of Z_{eq} is $7.86k\Omega$. If a conversion loss of 0.5dB due to the current partition between Z_{eq} and $2Z_{BB}$ is allowed, the TIA should be designed to have a $< 250\Omega$ input impedance (Z_{BB}).

The next step is to determine the transistor size for the mixer. First of all, as the LNA, Mixer and TIA form a current divider, the switch's on-resistance should be minimized to avoid loading the LNA which decreases the conversion gain. In addition, in the presence of large blockers, the LNA output will start to see a large swing which modulates the switch's on-resistance and decreases linearity. Therefore the switch should be sized large enough to maintain a high linearity under large blockers. However, a larger switch will also increase LO's capacitive load

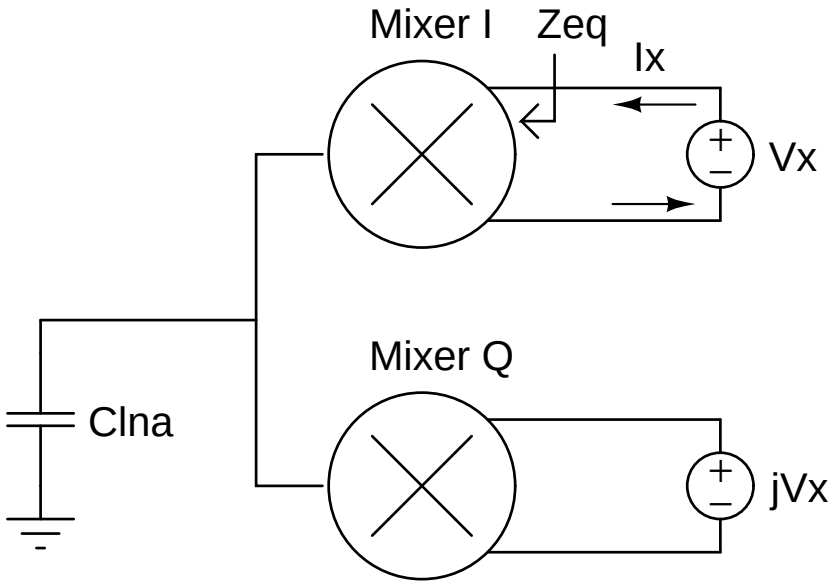


Figure 3.22: Equivalent Output Impedance for 25% Duty-Cycle LO

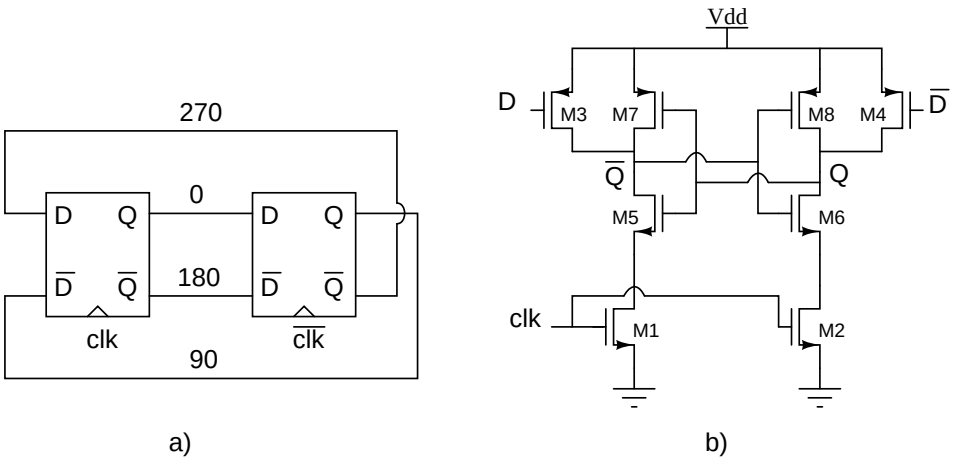
resulting in a higher power consumption on the LO side. Lastly, it has been shown that the noise from the switching transistors is inversely proportional to the LNA's output capacitance [24]. Therefore a larger switch size will increase the LNA's capacitive load and increase the noise figure. In conclusion, the conversion gain and linearity set the lower boundary for the switch size, while the noise performance and LO power consumption set the upper boundary.

Based on the above discussion, a transistor size of 24um is determined for a balanced noise and linearity performance. Simulation results with the LNA, mixer and TIA working together will be presented and discussed in section 3.6.

3.3.3 25% Duty-Cycle Divider

Since a voltage-controlled oscillator cannot provide quadrature clocks with 25% duty-cycle (which is required for the proposed mixer), a clock divider must be used. The clock divider and the latch is adopted from [25] and is shown in Fig. 3.23.

When clk is high, the latch senses the inputs and produces differential outputs. When clk is low, M1-2 are off, and one output keeps the high state as before while the other output is pulled up by the input. Since both outputs are high when clk is low, the latch produces asymmetrical outputs which gives the 25% duty-cycle behaviour. M5-6 are used to prevent direct current flow from Vdd to Gnd when clk is low and thus save power. Fig. 3.24 shows the operation of the clock divider which takes a 1.8GHz clock as input and produces 900MHz quadrature



a) b)

Name	Size
M1-2	2.4/0.12 um
M3-4	7.2/0.12 um
M5-6	1.2/0.12 um
M7-8	3.6/0.12 um

Figure 3.23: 25% Duty-Cycle Divider and Latch

clocks with 25% duty-cycle. The clock divider together with the buffers after it consumes 350uA current.

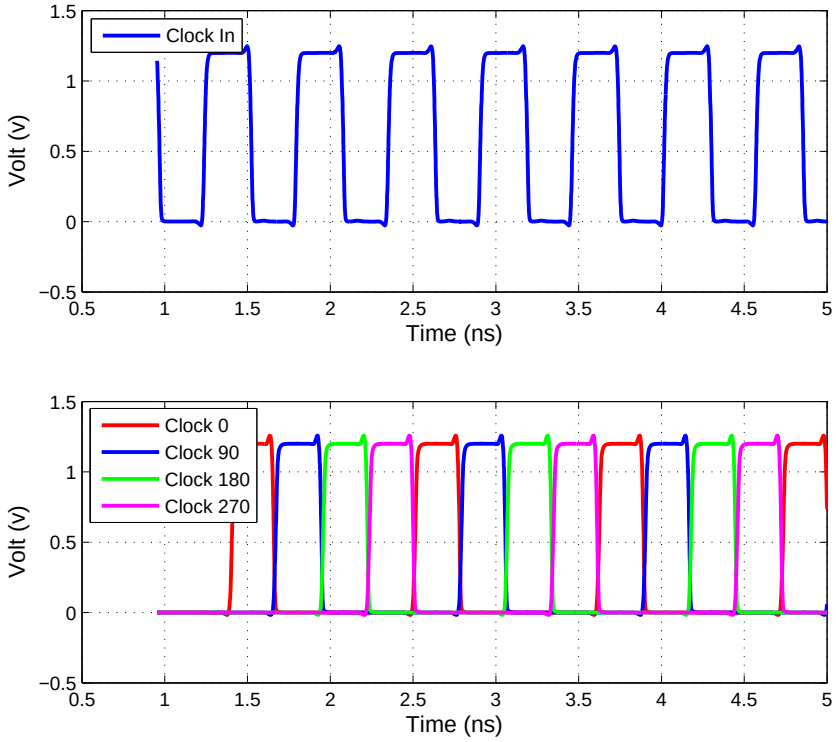


Figure 3.24: 25% Duty-Cycle Divider Outputs

3.4 Trans-Impedance Amplifier

3.4.1 TIA Overview

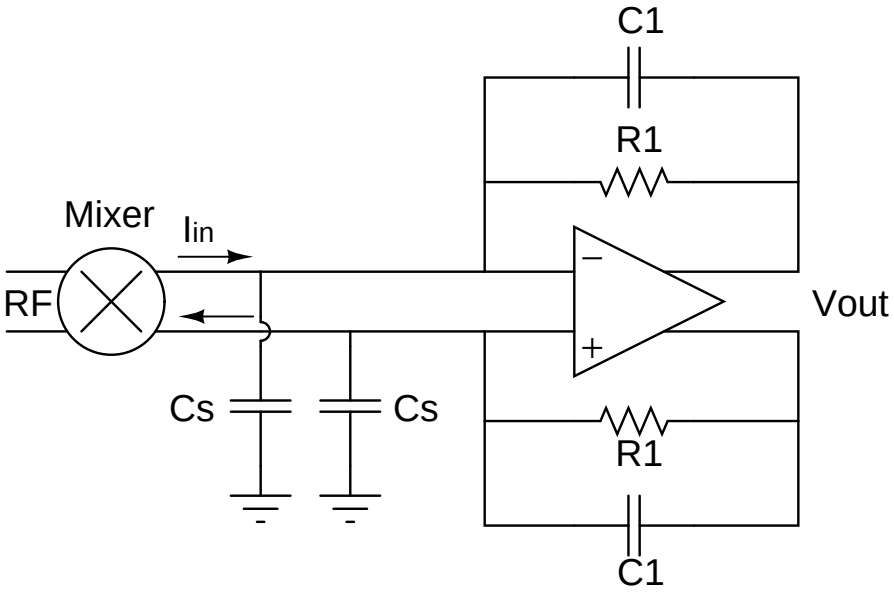


Figure 3.25: First Order Active RC TIA

In current-mode down-conversion receivers, a low-pass TIA is often used to sense the down-converted current signal and produces a voltage output. Since the TIA is the first baseband stage, its input impedance, noise and linearity can critically affect the performance of the overall chain. A low input impedance is necessary to ensure the theoretical conversion gain of the mixer by maximizing the signal transfer between the RF and BB. It also limits the voltage swing at the output of the mixer to reduce the modulation on the switch resistance when large blockers are present. The goal of the TIA design is to achieve a high gain in the signal band to suppress the noise coming from the following stages, and to provide a high attenuation in the stop band to reject large interferers.

A common TIA structure is the 1^{st} order active RC filter as shown in Fig. 3.25. This structure has a transfer function:

$$H(s) = -\frac{R_1}{1+sR_1C_1} \tag{3.14}$$

The trans-impedance gain is provided by the feedback resistor R_1. A real pole is created by R_1C_1 which achieves a 1^{st} order filtering. At low frequency, the input impedance is R_1 divided

by the loop gain of the amplifier and is ideally a virtual ground. At high frequency, a large shunt capacitor Cs maintains a low input impedance as the loop gain of the amplifier drops.

This simple structure suffers from several drawbacks. A 1^{st} order filter is insufficient to attenuate large interferers, which can potentially saturate the TIA. Therefore the gain of the TIA must be compromised in order to maintain a high linearity. A small gain is non-ideal since it not only increases the noise contribution from the following stages, but also increases the baseband area. In addition, a large capacitor Cs should be used to attenuate interferers at the input, which also increases the chip area.

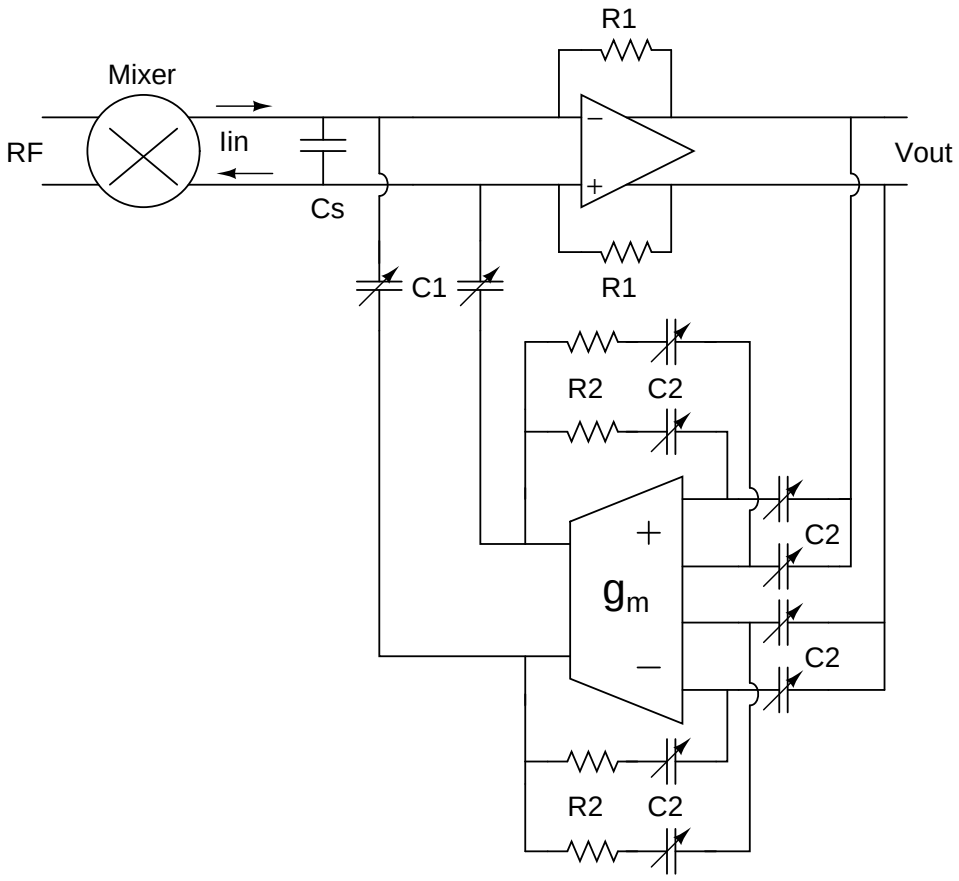
3.4.2 Proposed TIA

To improve the limitations of a single pole TIA, a TIA topology which exhibits a 2^{nd} order low-pass response and an excellent blocker cancellation capability has been proposed in [26] and is shown in Fig. 3.26. In the filter pass-band, the feedback path is open (since it's ac-coupled through capacitor C_1) and the current signal goes through the feed-forward Op-Amp with a trans-impedance gain of R_1. On the other hand, in the filter stop-band, the interferers are absorbed by the feedback path through the capacitor C_1. The two real zeros in the feedback network (created by C_1 and R_2C_2) become complex conjugate poles in the close-loop transfer function:

$$H(s) = -\frac{R_1}{s^2 R_1 R_2 C_1 C_2 + s R_1 C_1 + 1}$$

$$\begin{cases} w_o = \sqrt{\dfrac{1}{R_1 R_2 C_1 C_2}} \\ Q = \sqrt{\dfrac{R_2 C_2}{R_1 C_1}} \end{cases} \tag{3.15}$$

Therefore, the TIA can be configured as a 2^{nd} order Butterworth filter. As proposed in [26], the OTA in the TIA's feedback path has been implemented with a complementary topology operating in class-AB. As a result, the TIA can achieve a low power consumption and low noise during the sensitivity test and a high blocker tolerance in the presence of large blockers [26]. The noise and distortion contributed by the feedback network are negligible because they are high-pass shaped by C_1. Since C_1 is boosted by the feedback network, it is able to absorb



Name	Size
R_1	25 $k\Omega$
R_2	25 $k\Omega$
C_1	3.5 pF
C_2	3.5 pF
C_s	30 pF
g_m	4.4 mS

Figure 3.26: Proposed TIA

large interferers with a relatively small size. The shunt capacitor Cs can be sized small as well because it is only responsible for draining very far-away interferers in this case. Notice that, the particular low in-band noise of this topology allows the trans-conductance gain of the LNA to be limited to less than 40mS. This approach not only saves power in the LNA itself but also scales up the impedance level of the filter without saturating the receiver chain. A larger impedance reduces both the area of the baseband section and the power consumption in the output stage of the feed-forward Op-Amp.

The cut-off frequency of the TIA can be reconfigured by changing C_1 and C_2, which are implemented as 4-bit capacitor banks (Fig. 3.27). The capacitor bank uses binary-weighted capacitors with a unit size of 160fF. The switch is realized with a transmission gate and is placed at the side of the capacitor that sees a small swing (e.g input of the Op-Amp and OTA). According to (3.15), if C_1 and C_2 change by the same ratio α, the quality factor of the filter will remain the same while the cut-off frequency will change by $1/\alpha$.

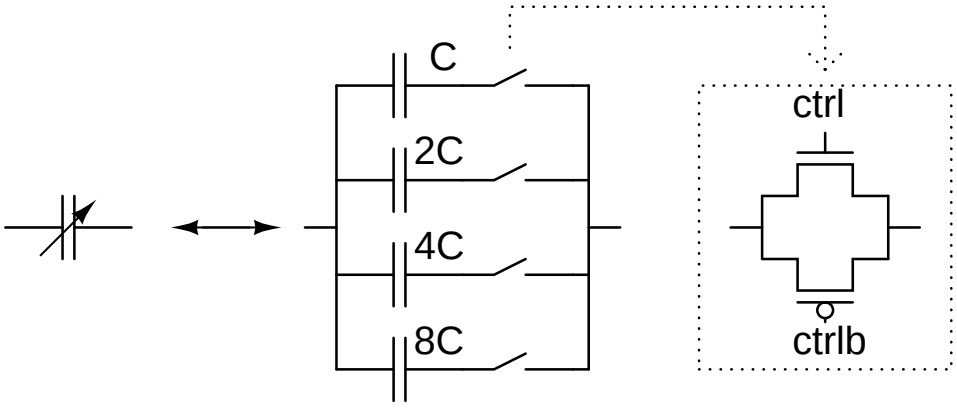


Figure 3.27: TIA: Capacitor Bank

The overall baseband circuit should provide a 3^{rd} order butterworth filtering profile as shown in Fig. 3.28

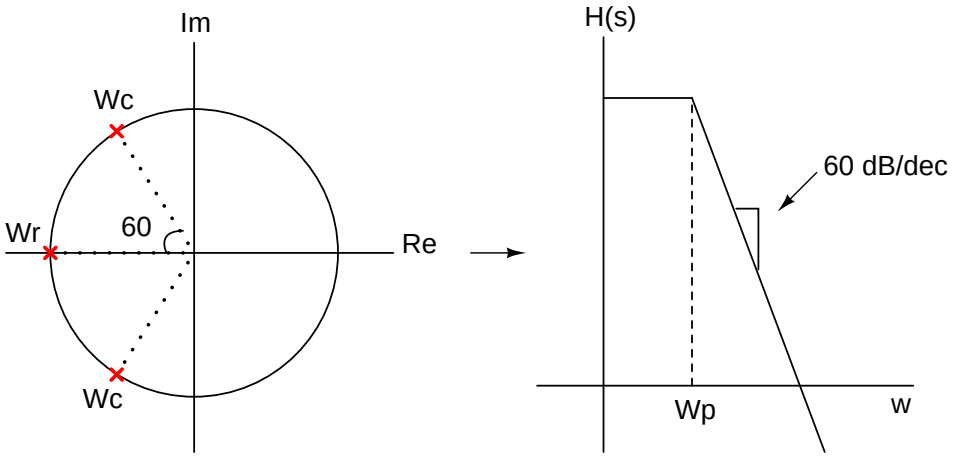


Figure 3.28: 3^{rd} Order Butterwroth Filter

The two complex conjugate poles can be realized in the TIA with the Q in (3.15) set to 1, and the remaining real pole can be created by a 1^{st} order active RC filter after the TIA.

The magnitude response of a N^{th} order butterworth low-pass filter is:

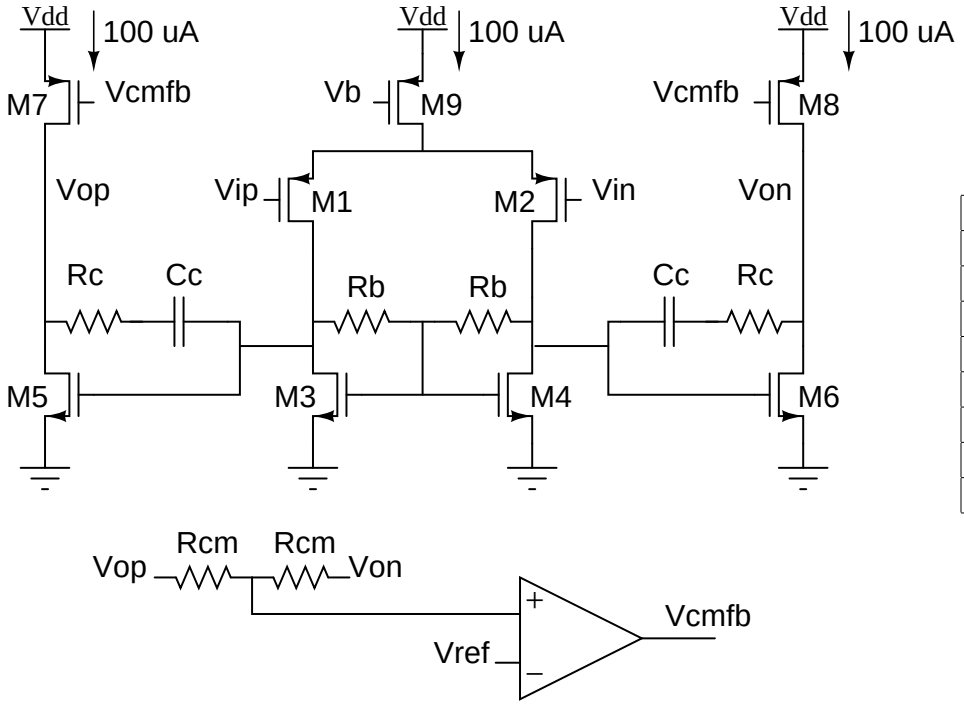
$$|H(jw)| = \frac{1}{\sqrt{1+\left(\frac{w}{w_p}\right)^{2N}}} \tag{3.16}$$

Where w_p is the cut-off frequency and N is the filter order

The nominal cut-off frequency of the filter is chosen to be 1.8MHz for a 1dB attenuation at the

edge of the signal band (1.4MHz). The trans-impedance gain is chosen to be $25K\Omega$ to achieve an over 50dB gain in the front-end. The rest of the circuit parameters can be calculated based on (3.15) and are shown in Fig. 3.26.

3.4.3 Operational Amplifier in Feed-Forward Path

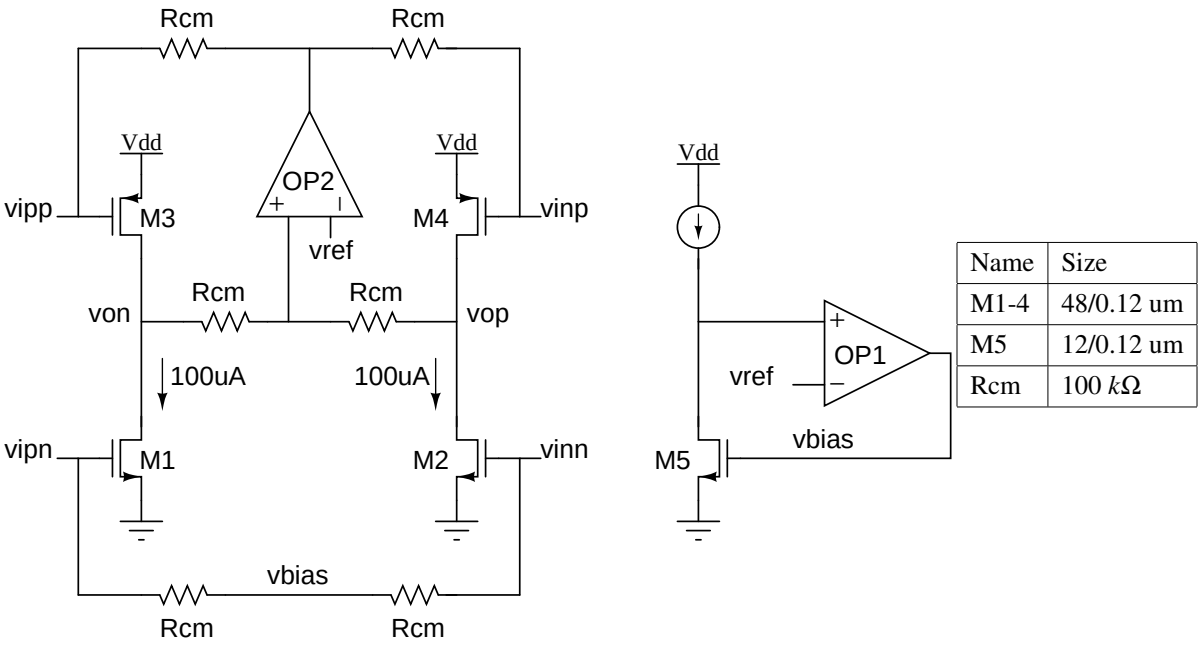


Name	Size
M1-2	28/0.2 um
M3-4	8/1 um
M5-6	16/1 um
M7-9	20/0.5 um
Cc	800 fF
Rc	3 $k\Omega$
Rb	100 $k\Omega$
Rcm	100 $k\Omega$

Figure 3.29: TIA: Operational Amplifier

Fig. 3.29 shows the implementation of the Op-Amp with a classical two-stage structure. M1 and M2 are biased in sub-threshold to maximize the gm/Id ratio and reduce the thermal noise. Transistor length for M3 and M4 is sized ten times larger than the minimum length to decrease the flicker noise. Miller compensation technique is realized through R_c and C_c and is introduced for stabilization purpose. The first stage common-mode is set by R_b, and the output common-mode is set by the common-mode feedback amplifier. The Op-Amp consumes 300 uA current.

3.4.4 Operation Transconductance Amplifier in Feedback Path



Name	Size
M1-4	48/0.12 um
M5	12/0.12 um
Rcm	100 $k\Omega$

Figure 3.30: TIA: Operational Trans-conductance Amplifier

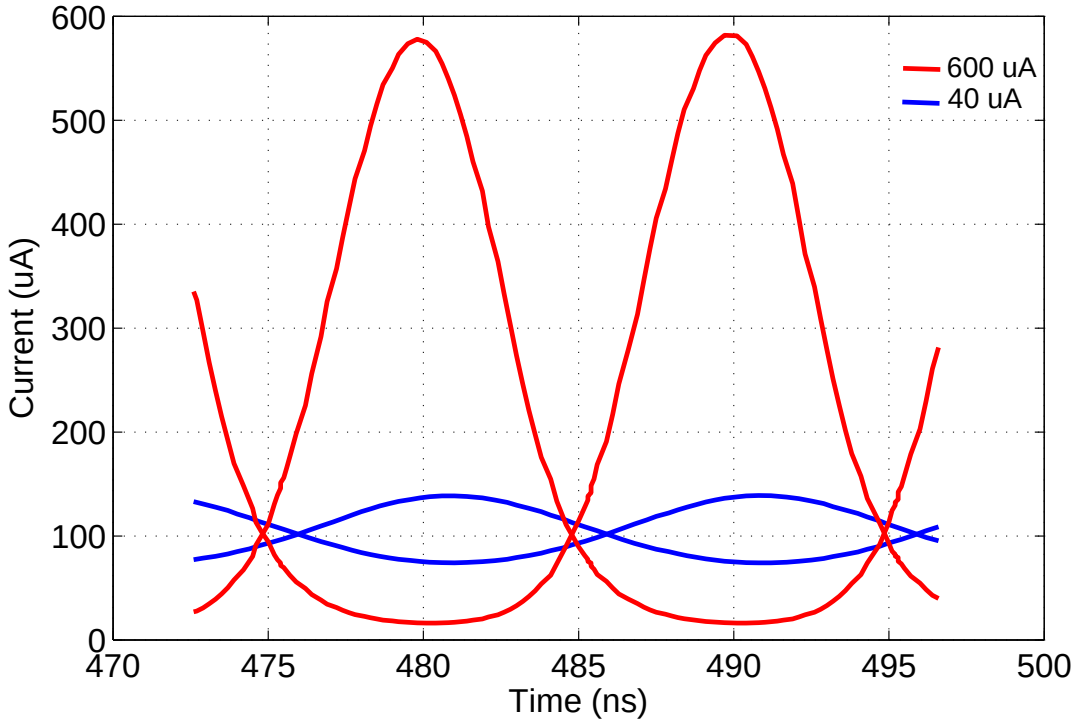
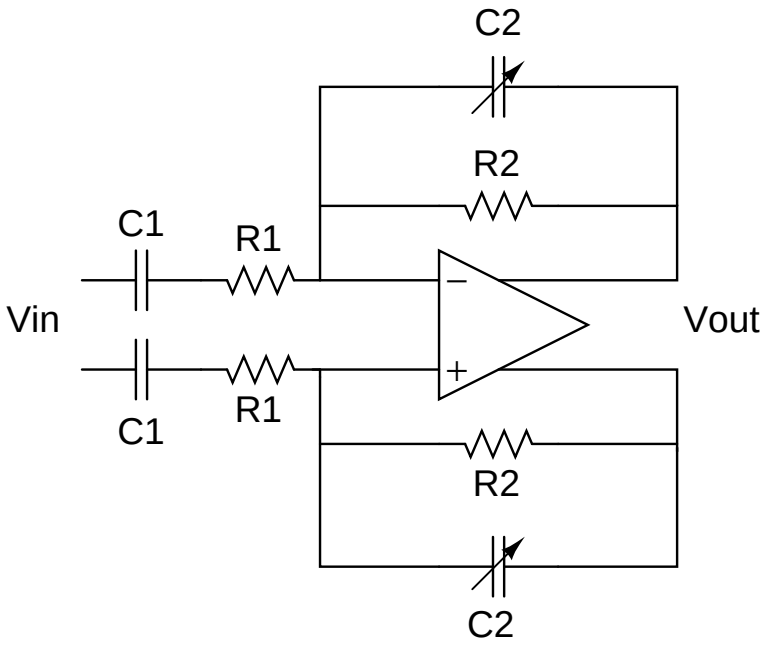


Figure 3.31: TIA: Class-A vs. Class-AB Operation

Fig. 3.30 shows the implementation of the OTA. NMOS devices are biased by OP1 while PMOS devices and the output common-mode are biased by OP2. Similar to the proposed LNA, the OTA uses the PN complementary structure which allows both PMOS and NMOS devices to share the same bias current thereby increasing the effective transconductance for a given bias current. To further increase the current usage efficiency, PMOS and NMOS devices are biased in class-AB which results in a low current consumption in the absence of blockers and a strong blocker cancellation capability in the presence of large blockers. The OTA consumes 200 uA current.

Fig. 3.31 shows the OTA's drain current (NMOS only) in the presence of a blocker located at 50MHz offset frequency. The blocker in this case is the down-converted interferer current showing up at the input of the TIA. When the blocker is small (e.g 40uA), the OTA still works in class-A and its drain current has a sinusoidal shape around the dc bias current (100uA). When the blocker is large (e.g 600uA), the OTA is forced to operate in class-AB, which allows it to produce a large output current to cancel the blocker.

3.5 Channel Selection Filter



Name	Size
R_1	100 $k\Omega$
R_2	100 $k\Omega$
C_1	12 pF
C_2	900 fF

Figure 3.32: First Order RC Filter with High-Pass Input

As part of the channel selection function (two complex conjugate poles) is already provided by the TIA, the remaining real pole can be realized by a RC active filter as shown in Fig. 3.32.

The filter provides a gain of R_2/R_1, and a real pole of $1/R_2C_2$. C_2 is also implemented as a 4-bit capacitor bank (with 80fF unit capacitor size) for cut-off frequency reconfiguration. The capacitor bank shares the same control signals with the capacitor banks in the TIA. R_1 and C_1 create a first order high pass filter which is responsible for filtering out the DC offset and flicker noise. The Op-Amp is implemented in the same way as that in Fig. 3.29 but scaled down by a factor of 4. The filter consumes 75uA current.

3.6 Simulation of Proposed Receiver Front-End

Simulation results of the proposed receiver front-end is summarized in Fig. 3.33-3.37. Fig. 3.33 shows the simulated transfer function of the receiver front-end. The receiver front-end achieves a 52.6dB in-band gain and a -60dB/dec stop-band attenuation. The -1dB cut-off frequency can be reconfigured between 1MHz and 2.1MHz.

Fig. 3.34 shows the simulated noise figure of the receiver front-end. The integrated double-side-band noise figure over the signal bandwidth (200KHz-1.4MHz) is 2.1dB.

Fig. 3.35 shows the out-of-band IIP3 simulation with two tones placed at [LO+50MHz, LO+99MHz]. Fig. 3.36 shows the out-of-band IIP3 simulation with two tones placed at [LO+10MHz, LO+19MHz]. The two tones in both cases create a third-order intermodulation product folding into the signal band at 1MHz. Since the tones are attenuated by the filter when measuring at the output, a normalization factor needs to be taken into account when evaluating IIP3, as described in the equation below:

$$IIP_3 = P_{IN} + \frac{P_O - P_{O3}}{2} + \frac{\Delta A}{2} \tag{3.17}$$

Where ΔA is the difference between the in-band gain and the gain at tone location

After the normalization, an OB-IIP3 of 2dBm and -4dBm is obtained respectively for the two cases.

Fig. 3.37 shows the compression of in-band signal due to an out-of-band blocker. The blocker is placed at 50MHz offset. The in-band gain drops by 1dB as the blocker power increases above -13.5dBm.

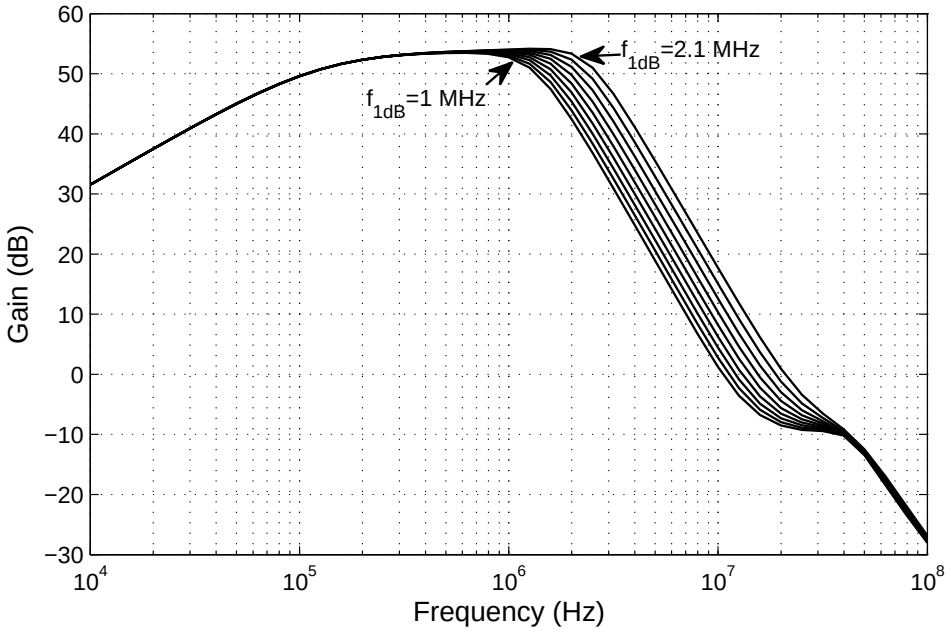


Figure 3.33: Proposed Front-End: Transfer Function

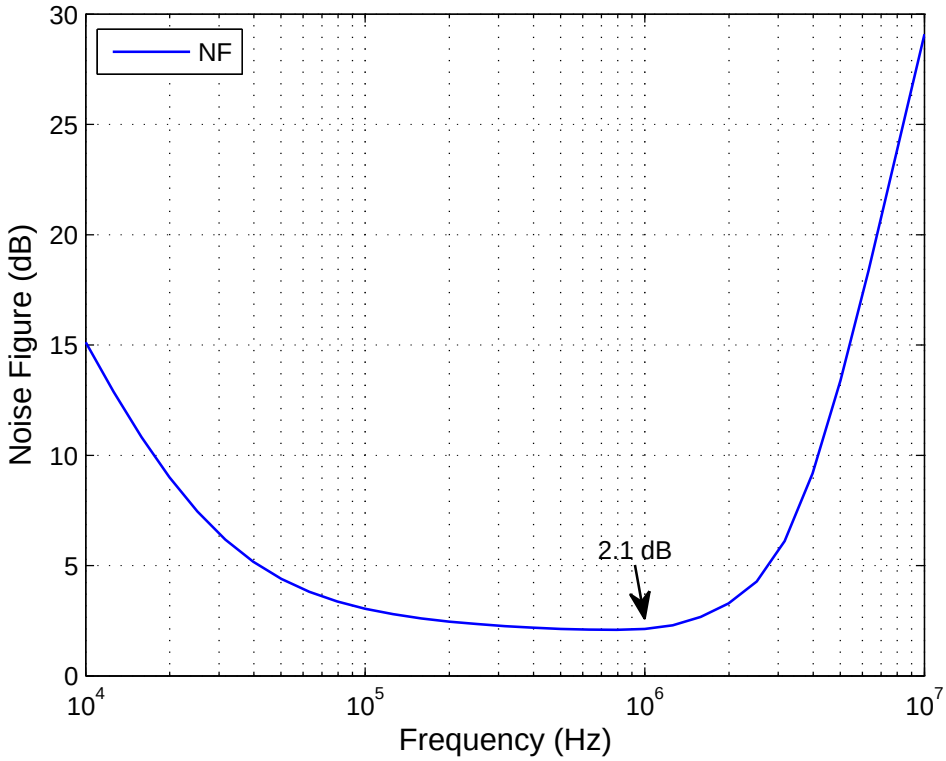


Figure 3.34: Proposed Front-End: Noise Figure

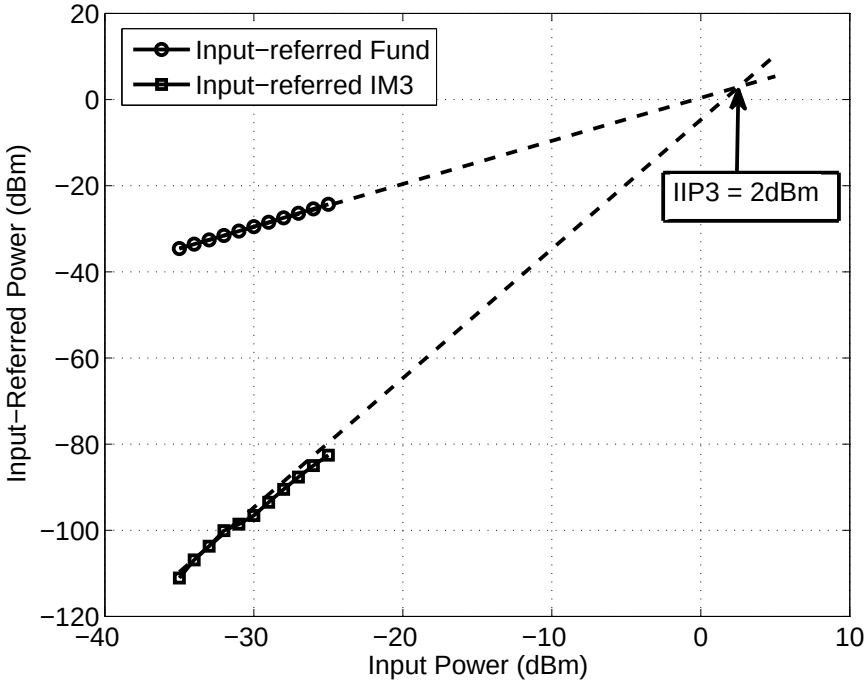


Figure 3.35: Proposed Front-End: OB-IIP3 with Two tones @[LO+50MHz, LO+99MHz]

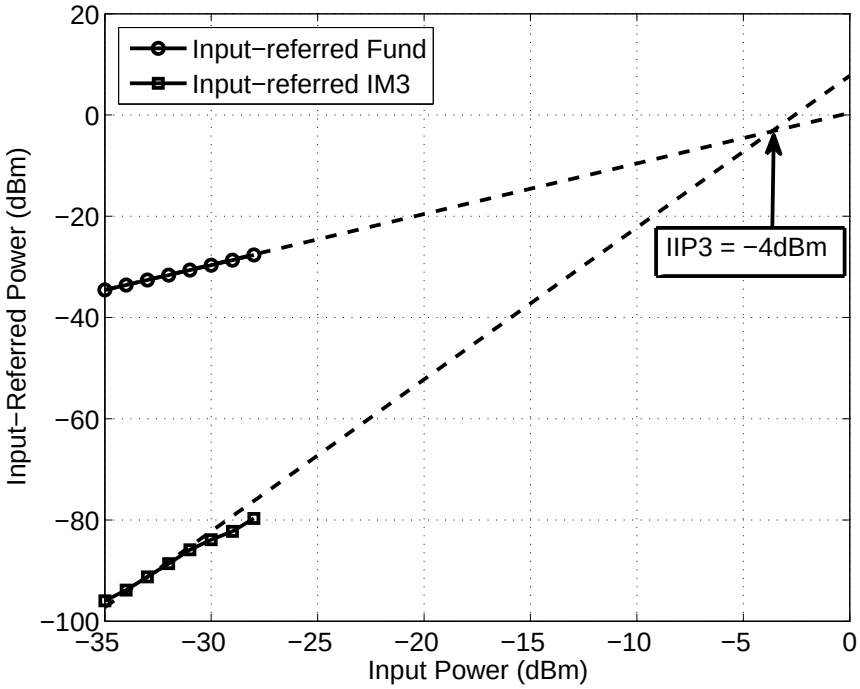


Figure 3.36: Proposed Front-End: OB-IIP3 with Two tones @[LO+10MHz, LO+19MHz]

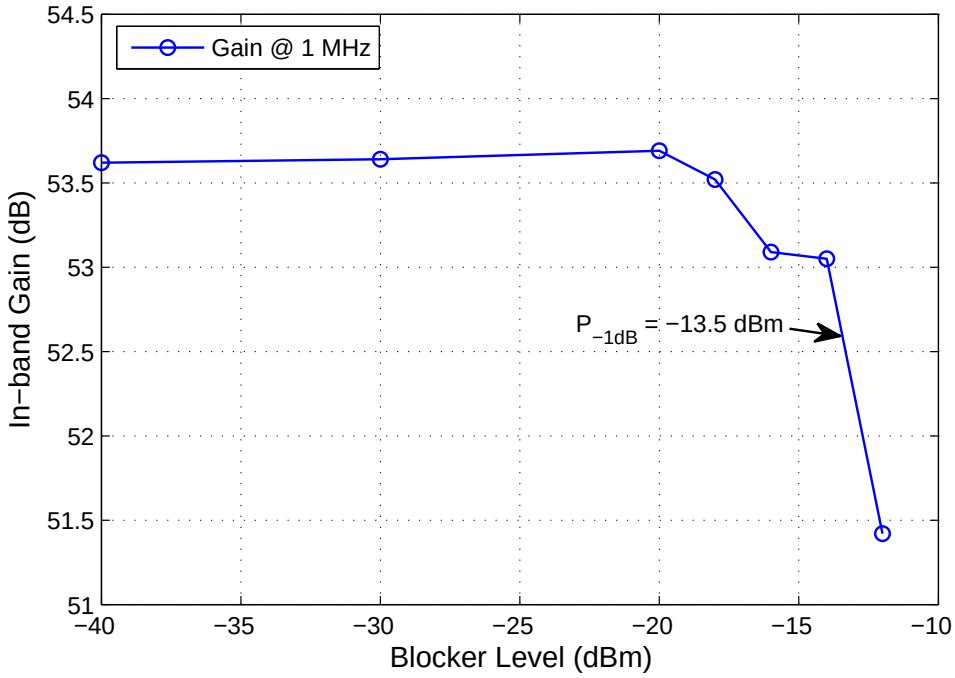


Figure 3.37: Proposed Front-End: OB-P1dB

The Spurious-Free-Dynamic-Range (SFDR) of the receiver can be calculated from the equation:

$$SFDR = \frac{2}{3}(IIP3 - Noise\ floor - NF) - SNR_{min} \tag{3.18}$$

The noise floor at the input of the receiver is the integrated 50Ω noise over the signal band (1.2MHz) and has a value of -113dBm. The minimum required SNR according to the IEEE 802.15.4 standard is 6dB. Plug these parameters along with the simulated IIP3 (2dBm/-4dBm) and NF (2.1dB) into eqn. 3.18, the SFDR of the receiver front-end is 69/65dB.

Table 3.3 summarizes the simulated performance of the proposed receiver front-end.

Table 3.3: Simulated Receiver Front-End Performance

Operation Band (MHz)	868/915
Baseband Cut-off Frequency (MHz)	1-2.1
Gain (dB)	52.6
NF (dB)	2.1
OB-IIP3 (dBm)	+2/-4
OB-P1dB (dBm)	-13.5
SFDR (dB)	69/65
Current (mA) @V_{DD}	2.1 @1.2V

Chapter 4

Measurement Results

4.1 Test Setup

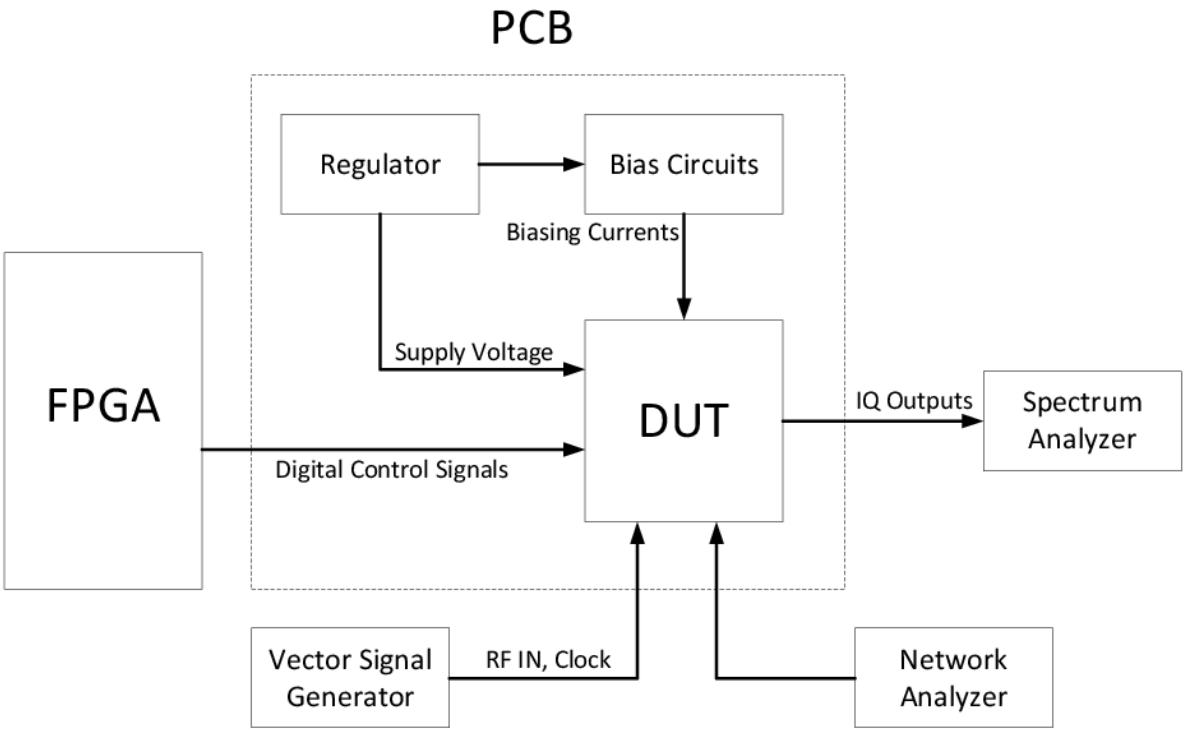


Figure 4.1: Testing Block Diagram

Fig. 4.1 shows the block diagram for lab measurement setup. The FPGA tester (National Instruments RIO USB-7856R) connects the PCB through a D-type socket and provides digital

control signals for the DUT (chip prototype). The PCB provides the regulated power supplies and biasing currents for the DUT. The Network Analyzer (R&S ZVH8) measures the input impedance matching for the LNA. The Vector Signal Generator (R&S SMW200A) feeds the RF input and LO signal to the PCB through SMA connectors. Finally the Spectrum Analyzer (R&S FSW) is used for baseband signal measurements including noise figure, linearity and signal transfer function.

4.1.1 Chip Prototype

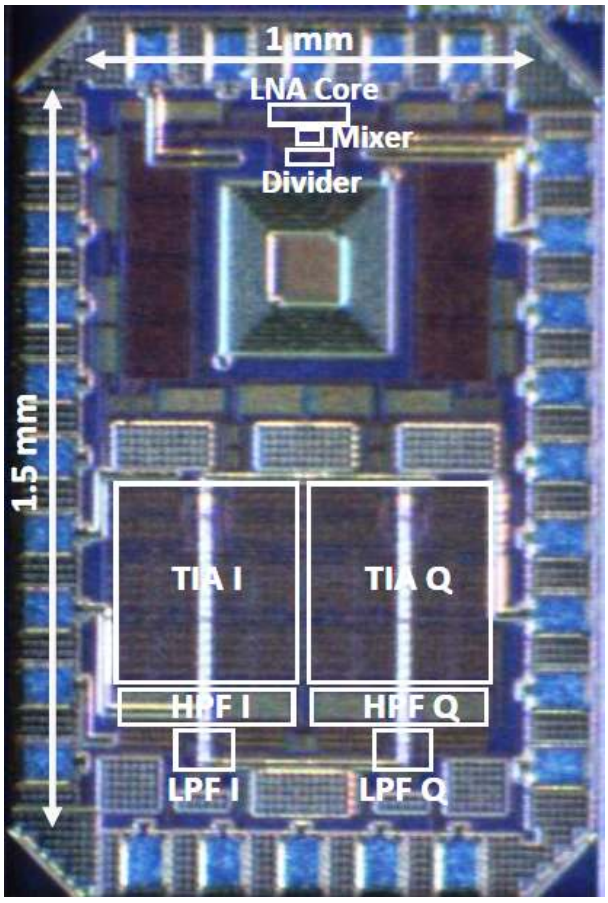


Figure 4.2: Proposed Receiver Front-End Die Photo

The proposed receiver front-end chip is fabricated in CMOS 0.13um technology. It occupies $1mm \times 1.5mm$ with an active area of $0.5mm^2$ (Fig. 4.2). The chip has 28 pins and is packaged through MOSIS using the open cavity plastic package with a cavity of $5mm \times 5mm$ (OCP_QFN_5x5_28A). The packaged chip prototype is manually soldered on the PCB for testing.

4.1.2 Printed Circuit Board

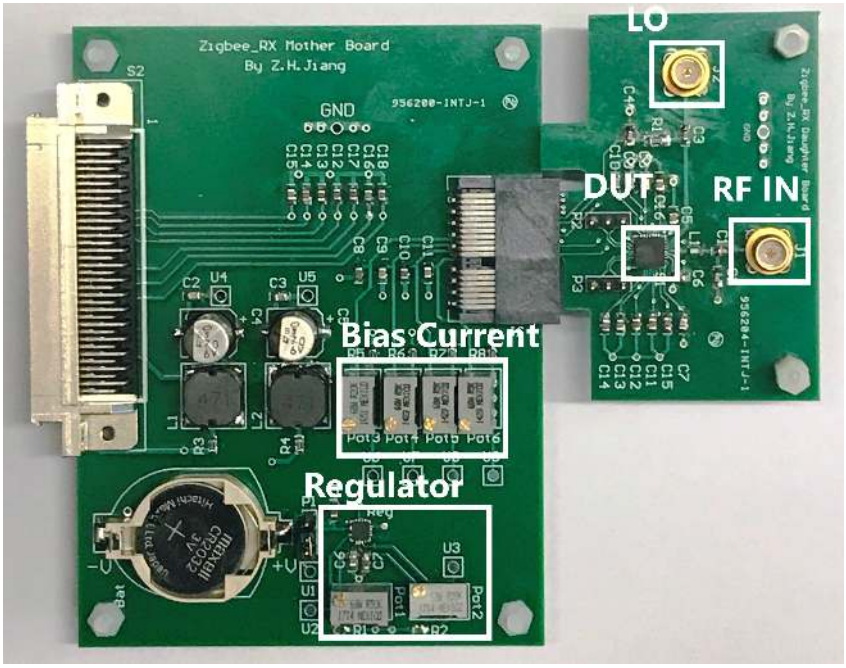


Figure 4.3: PCB Test Boards Photo

Two 4-layer PCBs (Fig. 4.3) are designed using Altium Designer and fabricated to facilitate chip prototype testing. The top and bottom layers are used for signal routing, and the two internal layers are used for power and ground planes. The two boards are connected through a PCIE interface.

The motherboard contains low frequency DC signals such as regulated power supplies, digital control signals and biasing currents. Digital control signals (capacitor bank control) as well as voltage references are provided by the FPGA tester and can be controlled by a LabView GUI on the PC. The regulator provides two adjustable outputs (DVDD and AVDD) for the digital and analog circuits in the chip respectively. Potentiometers are used to generate adjustable biasing currents for the chip prototype. Small resistors are inserted in the power and biasing current lines and the voltage drop across them are fed back to the FPGA for current measurements.

The daughterboard contains the chip prototype, baseband outputs, and high frequency signals such as clock and RF input. The high frequency signal routes are designed as transmission lines with 50Ω characteristic impedance. Low frequency baseband outputs are connected to the spectrum analyzer through a differential active probe.

4.2 Chip Measurements

4.2.1 Input Impedance Matching

The actual input impedance of the LNA is affected by the parasitic capacitance and inductance introduced by the package and PCB routing. Therefore, external components are used to optimize the input matching for the receiver. A low-pass hi-low matching network is used in this case, as shown in Fig. 4.4. The S11 measurement (Fig. 4.5) performed on the R&S ZVH8 Network Analyzer shows that good matching (S11<-10dB) is obtained over the desired bandwidth (868MHz-924MHz).

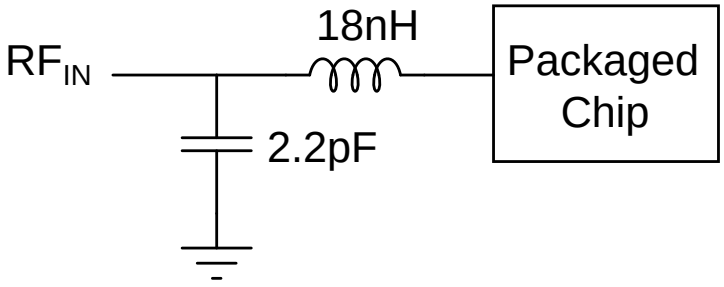


Figure 4.4: Off-chip Matching Network

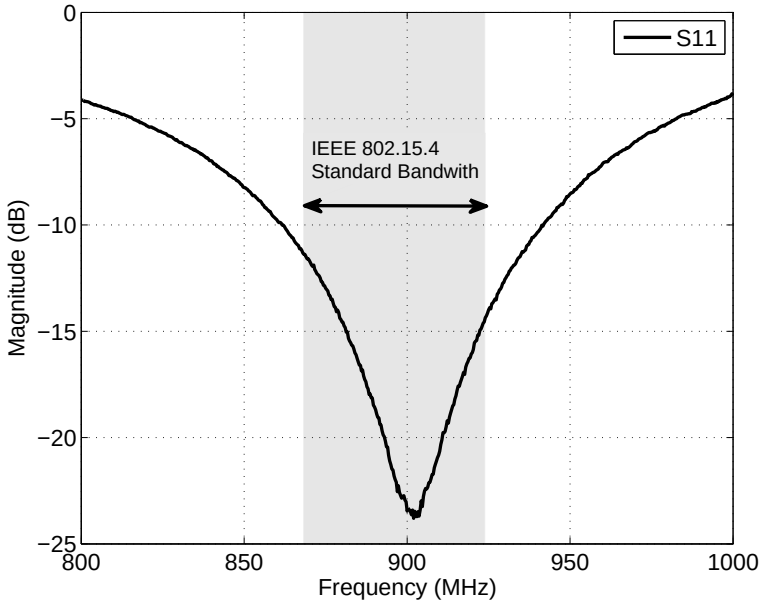


Figure 4.5: Measurement: S11

4.2.2 Transfer Function

The transfer function is measured by placing a fixed LO at 1.83GHz (the on-chip divider will then divide it to 915MHz) and sweeping the RF input frequency from LO+10KHz to LO+100MHz. With such setup, the down-converted signal at the I(Q) baseband output will span between 10KHz and 100MHz, and is displayed on the R&S FSW Spectrum Analyzer for gain measurements.

Fig. 4.6 shows the measured transfer function. The receiver front-end achieves a 50dB in-band gain. The 1^{st} order high-pass shape at low frequency is due to the passive high-pass filter between the TIA and channel selection filter (Fig. 3.1). The stop band achieves a 3^{rd} order Butterworth filtering profile.

Fig. 4.7 shows the measured transfer function with reconfigurable bandwidth. By setting the control code of capacitor banks in the TIA (Fig. 3.26) and Channel Selection Filter (Fig. 3.32), the 1dB cut-off frequency of the receiver can be tuned between 1MHz and 2MHz.

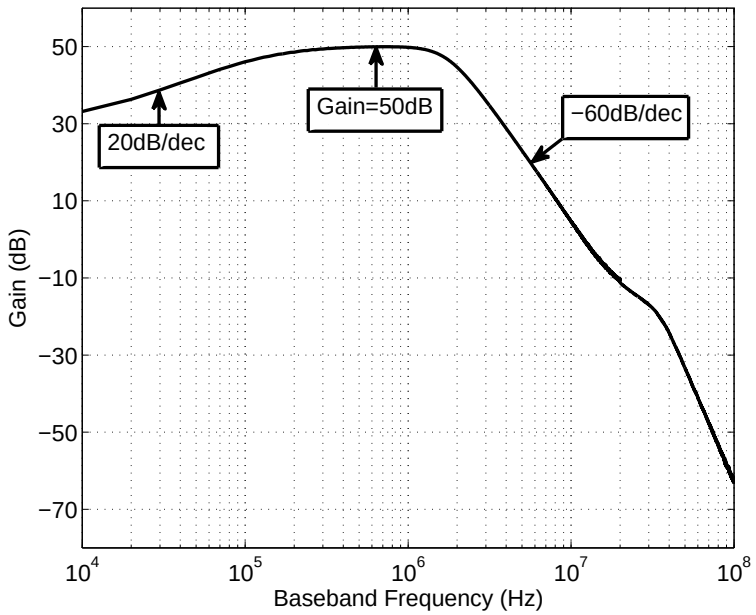


Figure 4.6: Measurement: Transfer Function

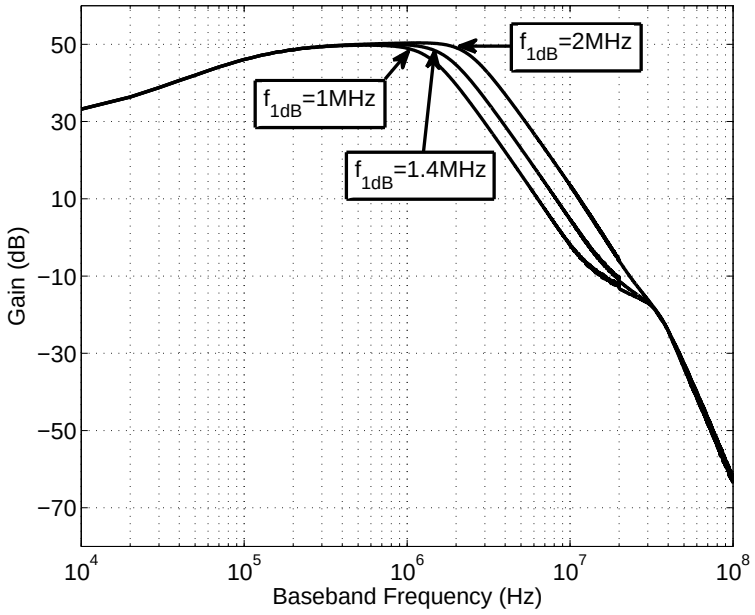


Figure 4.7: Measurement: Reconfigurable Bandwidth

4.2.3 Noise Figure

The noise figure is measured with the gain method. Recall from (2.2) that $NF = SNR_{in} - SNR_{out}$. By rewriting this equation, an equivalent NF as a function of the input noise, output noise, and gain of the system can be obtained as follows:

$$NF = Output\ Noise - Input\ Noise - Gain \text{ (in dB)} \tag{4.1}$$

The output noise can be found by terminating the RF input with a 50Ω source, powering up the receiver, and measuring the output noise density at the frequency of interest on the spectrum analyzer. The input noise is the noise generated from the 50Ω source and has a noise density of -174dBm/Hz. The gain of the receiver can be obtained from the transfer function which has already been measured in the previous section. The NF measurement is repeated at different frequencies and a relationship of NF vs baseband frequency is shown in Fig. 4.8. The integrated NF over the signal band (0.2-1.4MHz) is 2.7dB. This is obtained by integrating the output noise over the signal band, referring it back to the input of the receiver, and subtracting it from the integrated input noise.

To test the NF in the presence of a blocker, the NF was measured with an out-of-band blocker at [LO+50MHz] and its power swept from -50dBm to -10dBm (Fig. 4.9). The NF is almost

unchanged for blocker <-30dBm, and the NF is below the specification's maximum allowable value (<15dB) for blocker <-11dBm.

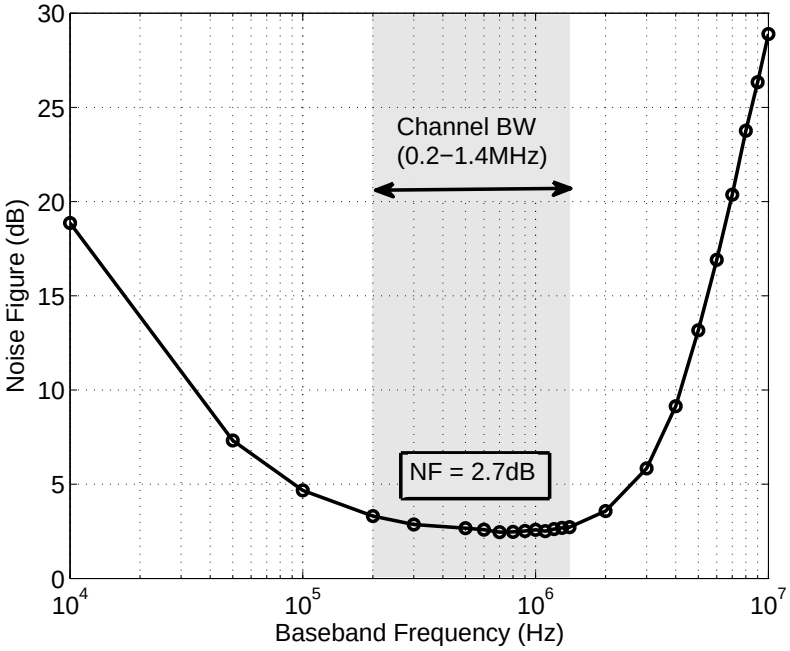


Figure 4.8: Measurement: Noise Figure

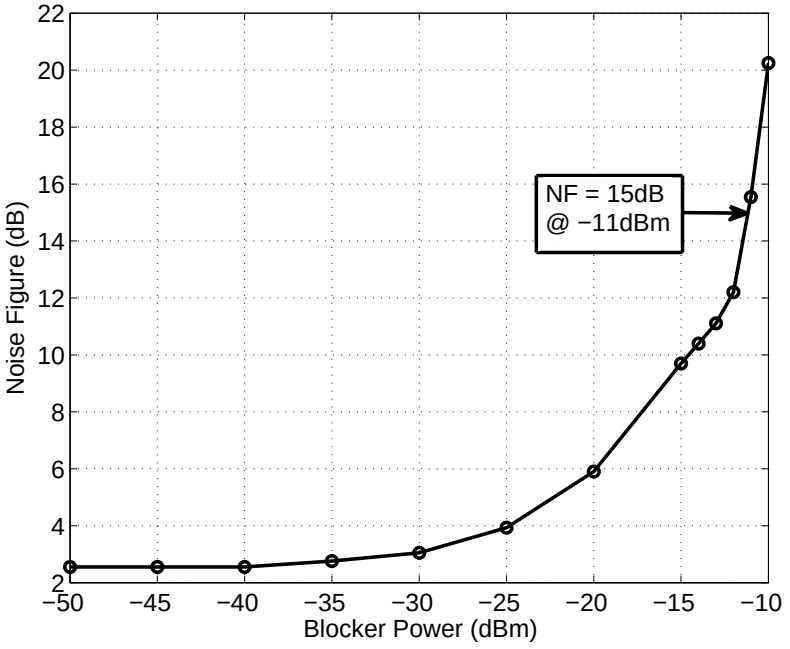


Figure 4.9: Measurement: Noise Figure with Blocker

4.2.4 Linearity

Linearity tests measure the out-of-band IIP3, IIP2 and P1dB, and are performed at the maximum gain. To test the OB-IIP3 of the receiver, two tones are placed at [LO+50MHz, LO+99MHz] and input to the receiver. These two tones create an intermodulation product IM3 which falls into the signal band at LO+1MHz. By recording the power of the down-converted fundamental tones and their intermodulation product in the baseband, and then referring them back to the input, the OB-IIP3 plot is constructed and shown in Fig. 4.10. The measurement is repeated by placing two near-band tones at [LO+10MHz, LO+19MHz] and the results is shown in Fig. 4.11. The measured OB-IIP3 shows +2dBm and -2dBm respectively for these two cases.

For completeness, non-linearity effects due to the second-order distortion is also measured with out-of-band IIP2 (OB-IIP2) test. The OB-IIP2 test is performed for two scenarios. The first test is the beat frequency leakage due to the mismatch in the quadrature mixers (low frequency beat leaks from the RF to BB without frequency translation). To test such effect, two closely-spaced tones at [LO+10MHz, LO+11MHz] are input to the receiver and an IM2 at 1MHz is measured in the baseband. The OB-IIP2 in this case is +37dBm (Fig. 4.12). The second test measures the IM2 product falling into the signal band due to two farther-spaced tones at [LO+10MHz, 2LO+11MHz] (which create an IM2 at LO+1MHz), and an OB-IIP2 of +35dBm is obtained in this case (Fig. 4.13). According to the specification, the near band interferer at LO+10MHz is -62dBm. If a 10dB in-band SNR degradation due to IM2 is allowed, the measured IIP2 value allows the receiver to handle a -6dBm out-of-band blocker (which is above the compression point of the system).

The out-of-band P1dB (OB-P1dB) is measured by sweeping the power of an out-of-band blocker until the in-band gain was compressed by 1dB. This test is repeated by placing the blocker at different offset frequencies from the LO and the result is shown in Fig. 4.14. The receiver front-end exhibits a high blocker tolerance. The P1dB is as high as -18dBm even at a near-band offset frequency (10MHz), and it further increases to -10.5dBm as the blocker offset frequency increases to 100MHz.

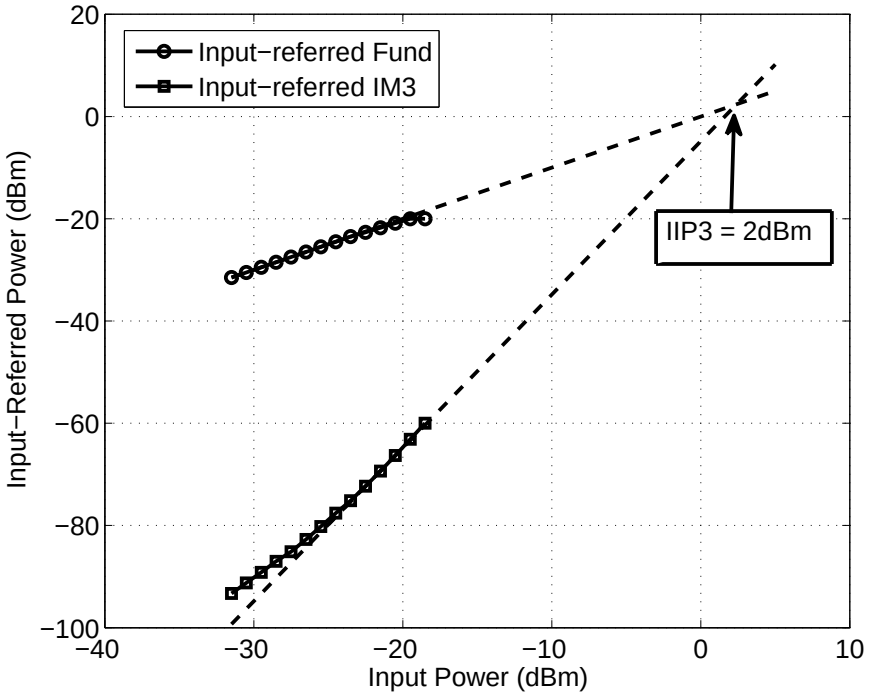


Figure 4.10: Measurement: OB-IIP3 with Two tones @[LO+50MHz, LO+99MHz]

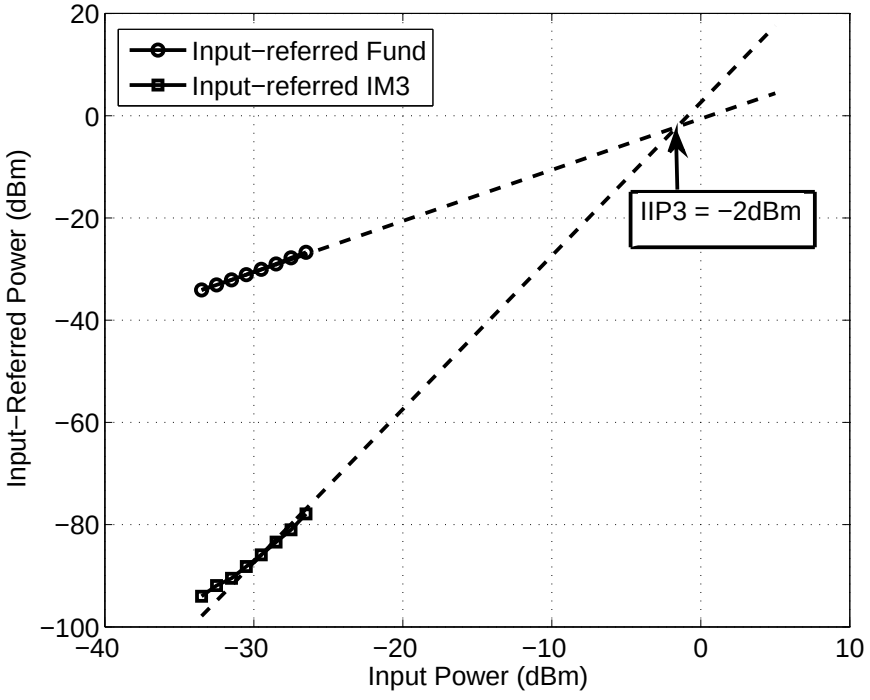


Figure 4.11: Measurement: OB-IIP3 with Two tones @[LO+10MHz, LO+19MHz]

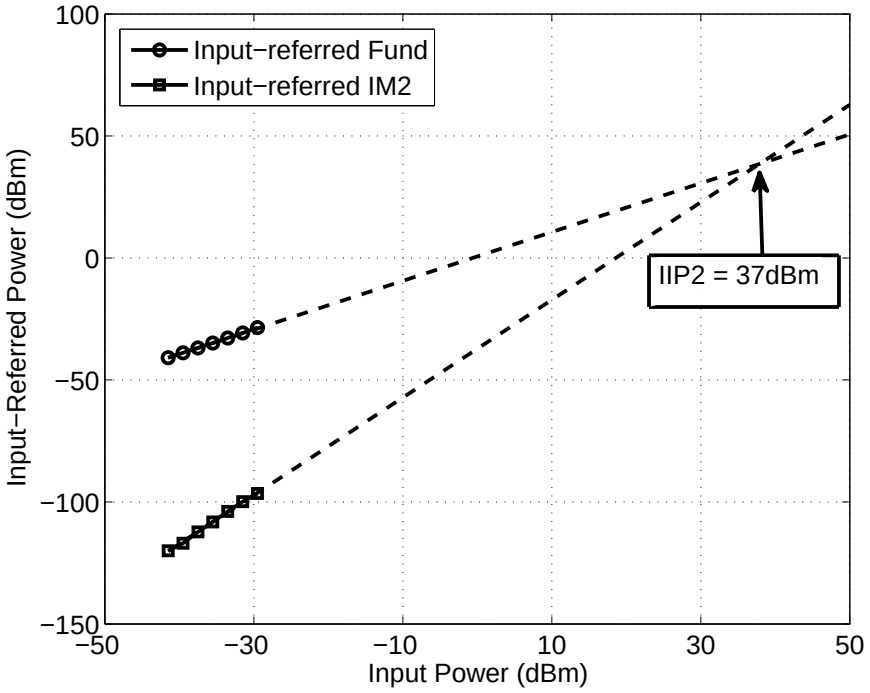


Figure 4.12: Measurement: OB-IIP2 with Two tones @[LO+10MHz, LO+11MHz]

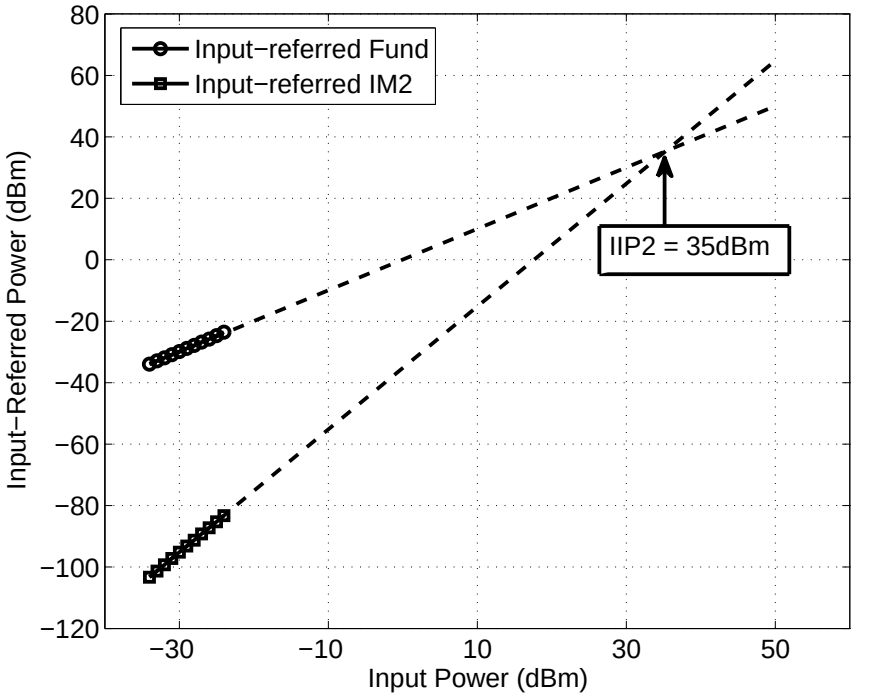


Figure 4.13: Measurement: OB-IIP2 with Two tones @[LO+10MHz, 2LO+11MHz]

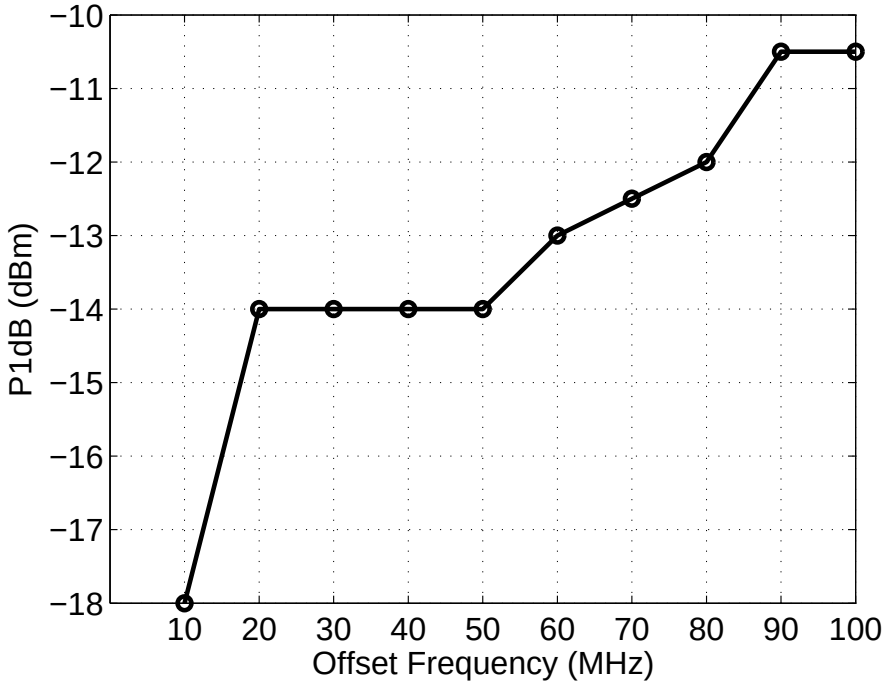


Figure 4.14: Measurement: OB-P1dB

4.2.5 Performance Summary and Comparison

Table 4.1: Performance Comparison with the State-of-the-art Works

	This Work	JSSC 2014[5]	MTT 2006[27]	CICC 2012[28]	RFIC 2014[29]
Technology (nm)	130	65	180	180	130
Active Area (mm^2)	Low-IF Single-ended LNA	Low-IF Single-ended LNA	DCR Single-ended LNA	DCR/Low-IF Differential LNA	Low-IF Differential LNA
Frequency (MHz)	868/915[1]	433/860/915/960[1]	915[1]	170/433/868/915/950	960
BW (MHz)	1.2	1.2	1.2	0.001	1.2[4]
Gain (dB)	50	50	30	39	59.6
NF (dB)	2.7	8.1	3	6.5	8.2
OB-IIP3 (dBm)	+2/-2	-20.5	-5[2]	-8[2]	-19
OB-IIP2 (dBm)	+37/+35	-	+45[2]	-	-
OB-P1dB (dBm)	-10.5	-23	-15[2]	-	-
SFDR (dB)[3]	69/66	50	64[2]	74[2]	51[4]
Supply (V)	1.2	0.5	1.8	1.8	1.2
Current (mA)	2.1[5]	1[5]	2	2.3	2.6[5]

[1] IEEE 801.15.4 standard
[2] In-band linearity test with minimum gain setting
[3] $SFDR = 2/3(IIP3 - Noise\ Floor - NF) - SNR_{min}$
[4] Standard unspecified, number derived based on IEEE 801.15.4 standard
[5] Including a clock divider

Due to the limited number of existing works in sub-GHz receiver design and the lack of description in their measurement setups (especially for linearity tests), it is challenging to present a comprehensive comparison of this work with the state-of-the-art. To the best of the author's knowledge, previous works with the most comprehensive measurement results are reported in Table 4.1. Compared to [5], this work consumes more power but achieves a much better performance in both noise and linearity. A similar noise figure was reported in [27], however, its out-of-band linearity tests were not provided, and its in-band linearity tests were performed with minimum gain setting. In [28], comparable power consumption leads to a much higher noise figure in a channel bandwidth 100 times smaller. Such small bandwidth significantly enhances the sensitivity resulting in a high SFDR. Finally the solution presented in [29] did not provide the information regarding the specification, therefore its SFDR was derived based on the IEEE 802.15.4 specification for a fair comparison. Overall, the benefits of the proposed class-AB receiver show the best noise figure and a much higher blocker tolerance compared to the state-of-the-art with a competitive power dissipation.

Chapter 5

Conclusion

5.1 Summary

This thesis presents the design of a low power high SFDR sub-GHz RF receiver front-end. The design exploited the class-AB biasing in both the RF and baseband sections, resulting in a very low sensitivity and an excellent blocker tolerance. The receiver front-end is fully compliant with the IEEE 802.15.4 standard, and its excellent sensitivity performance also makes it suitable for the emerging long-range applications. The test-chip was fabricated in 0.13um CMOS technology to validate the performance of the proposed receiver front-end design. The receiver front-end operates at the 868/915MHz ISM band and consumes 2.1mA from a 1.2V supply. Measurement results show that the design achieves a 50dB in-band gain, 2.7dB in-band Noise Figure, +2dBm OB-IIP3, +35dBm OB-IIP2, and -10.5dB OB-P1dB. Compared with previous IEEE 802.15.4-compliant state-of-the-art works, this work achieves the lowest noise figure, highest blocker tolerance, and highest dynamic range with competitive power consumption.

5.2 Future Work

The RF receiver front-end presented in this thesis is only part of the whole receiver system. To complete the receiver chain, the Variable Gain Amplifier (VGA) with automatic gain control, and the ADC after the front-end blocks should also be included. In addition, an on-chip voltage-controlled oscillator (VCO) should be designed to generate the LO for quadrature mix-

ers. No special care was taken to optimize the 25% duty-cycle divider and the clock buffers. Therefore, the power dissipation in these circuits can be further reduced. Finally, the scope of the project can be extended to the digital domain to investigate the design of IQ recombination circuits and digital filters.

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