A Low-Power, Variable-Resolution Analog-to-Digital Converter

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(Abstract)

Analog-to-digital converters (ADCs) are used to convert analog signals to the digital domain in digital communications systems. An ADC used in wireless communications should meet the necessary requirements for the worst-case channel condition. However, the worst-case scenario rarely occurs. As a consequence, a high-resolution and subsequently high power ADC designed for the worst case is not required for most operating conditions. A solution to reduce the power dissipation of ADCs in wireless digital communications systems is to detect the current channel condition and to dynamically vary the resolution of the ADC according to the given channel condition. In this thesis, we investigated an ADC that can change its resolution dynamically and, consequently, its power dissipation. Our ADC is a switched-current, redundant signed-digit (RSD) cyclic implementation that easily incorporates variable resolution. Furthermore, the RSD cyclic algorithm is insensitive to offsets, allowing simple, low-power comparators. Our ADC is implemented in a 0.35 μm CMOS technology with a single-ended 3.3 V power supply. Our ADC has a maximum power dissipation of 6.35 mW for a 12-bit resolution and dissipates an average of 10 percent less power when the resolution is decreased by two bits. Simulation results indicate our ADC achieves a bit rate of 1.7 MHz and has a SNR of 84 dB for the maximum input frequency of 8.3 kHz.

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Chapter 1

Introduction

Analog-to-digital converters (ADCs) are a major component in digital communications systems where signals transmitted over radio frequencies are received and subsequently converted to digital signals for digital signal processing. Digital signal processing is preferable to its analog counterpart since digital circuits are often more scalable, more reliable in noisy environments, faster, and cheaper to design than analog circuits. Additionally, most fabrication facilities are limited to cheaper CMOS digital processes where accurate analog components are unavailable. As a result, analog designs requiring accurate analog components are seldom used in modern communications systems.

Recently, portable wireless applications have made power dissipation a major concern in wireless applications. Applications such as cellular phones, pagers, and camcorders require small power dissipation to reduce the size and weight of batteries and to extend the lifetime of the battery. Also, increased complexity in signal processing for wireless video and wireless web in cellular phones has increased the necessity of low power dissipation.

An ADC used in wireless communications should meet the necessary requirements for the worst-case channel condition. However, the worst-case scenario rarely occurs. As a consequence, a high-resolution and subsequently high-power ADC designed for the worst case is not required for most operating conditions. A solution to reduce the wasted power is to detect the current channel condition and change the resolution of the ADC dynamically such that an ADC with an appropriate resolution is used.

In this thesis, a low-power, variable-resolution ADC suitable for CMOS digital processes is investigated. Variable-resolution is investigated with the goal of reducing power dissipation when the resolution of the ADC is lowered. We have implemented an ADC whose resolution is dynamically adjustable according to the given channel condition. The ADC has a maximum power dissipation of 6.35 mW for a 12-bit resolution for a single-ended 3.3 V power supply voltage in a 0.35 μm technology. Also, when the resolution of our ADC is lower by two bits, our ADC has an average power savings of ten percent. Simulation results indicate our ADC achieves a bit rate of 1.7 MHz and has a signal-to-noise ratio (SNR) of 84 dB for the maximum input frequency of 16.7 kHz. The core size of our ADC is 1.26 mm^2.

The organization of this thesis is as follows. Chapter 2 introduces important concepts of ADCs and reviews contemporary ADCs suitable for low-power applications. Feasibility of variable resolution is also investigated. Chapter 3 gives an overview of the proposed ADC architecture. The advantages of the proposed algorithm adopted by our ADC are also shown. Chapter 4 discusses the implementation of the algorithm and its components in detail. Chapter 5 presents the simulation results of our ADC, including accuracy, speed, and power dissipation for various resolutions. Chapter 6 concludes the thesis and presents future improvements.

Chapter 2

Background

2.1 Introduction

In this chapter, we review fundamentals of analog-to-digital converters (ADCs) and several types of ADC architectures. We also review low-power approaches to ADCs and contemporary high-performance ADC architectures. Finally, we investigate the feasibility of two ADC architectures for implementation of variable-resolution.

2.2 Fundamentals of Analog-to-Digital Converters

In this section we review the function of an ideal ADC and the major parameters of analog-to-digital converter (ADC) performance, which include the resolution, the effective number of bits, the integral nonlinearity error, the differential nonlinearity error, the conversion time, the sampling rate, and the power dissipation of ADCs.

The transfer characteristic of an ideal 2-bit ADC is given in Figure 2.1.

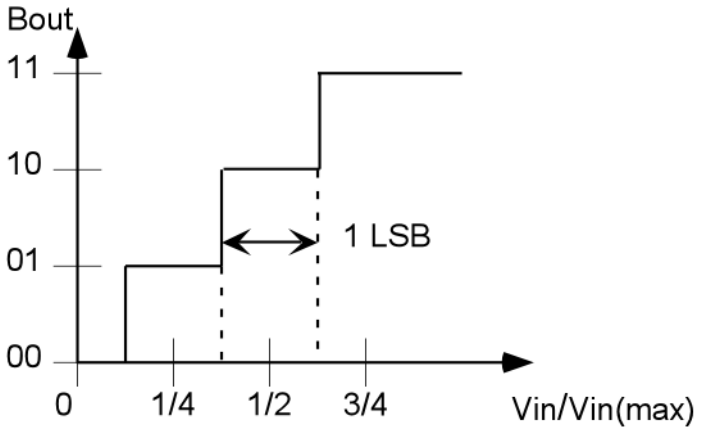


Figure 2.1 Transfer Characteristic of an Ideal 2-bit ADC

Figure 2.1 shows an ideal 2-bit ADC that produces a 2-bit digital word B_{out} for an analog input V_{in}. The input voltage has been normalized with respect its upper bound $V_{in}(max)$. The bounds of the input voltage and the resolution N of an ADC determine the range of the input voltage that corresponds to the same output word. The range denoted as V_{LSB} is given by

$$V_{LSB} = \frac{L_u - L_l}{2^N},$$

where N is the number of bits of the ADC, L_u is the upper bound of the input of the ADC, and L_l is the lower bound of the input of the ADC. Specifically, V_{LSB} is the change of the input necessary to cause the least-significant bit of the output word to change. When V_{LSB} is divided by the dynamic range (the difference of the upper bound and the lower bound) of the input, the resulting quantity is denoted as 1 LSB. As shown in the figure, 1 LSB is ¼ for a 2-bit ADC [12].

The transfer characteristic of an ideal ADC is defined mathematically by

$$(L_u - L_l)\left(b_1 2^{-1} + b_2 2^{-2} + b^3 2^{-3} + \cdots + b_N 2^{-N}\right) = V_{in} \pm V_x,$$

where V_x is the quantization error. Since a range of input voltage corresponds to a single output word, a quantization error is unavoidable. The quantization error for an ideal ADC is bound by the condition

$$-\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB}.$$

Since V_{LSB} is inversely proportional to 2^N, the quantization error becomes smaller as the resolution grows larger, resulting in a more accurate digital representation of the input voltage [12].

The performance parameters used to characterize an ADC are the resolution, the effective number of bits, the integral nonlinearity (INL) error, the differential nonlinearity (DNL) error, the conversion time, the sampling rate, and power dissipation of the ADC. The resolution of an ADC is defined as the number of analog levels that correspond to unique binary words. Specifically, an N-bit ADC has 2^N output words. If this definition is strictly followed, the resolution of a converter does not necessarily mean that the ADC is accurate to N bits. The accuracy of an ADC is determined by its effective number of bits, as will be shown next.

The signal-to-noise ratio (SNR) of an ADC gives the effective number of bits N_e. The SNR in decibels (dB) for an ADC with an effective number of bits, N_e, is given as

$$SNR = 6.02N_e + 1.76\ dB$$

for a sinusoid that spans the entire input range of the ADC. The SNR is given by the ratio of the root-mean-square (rms) value of the input voltage and the rms value of the quantization noise [12]. The SNR maintains this value when the difference of the upper bound of the quantization noise and the lower bound of the quantization noise is V_{LSB} (i.e. $V_x(max)-V_x(min) = V_{LSB}$).

The effective number of bits of an ADC is the number of bits the ADC accurately computes. For example, assume that an ADC computes ten bits. However, an error causes the signal-to-noise ratio to be 50 dB. In such a case, the effective number of bits, N_e, is eight, as computed by the SNR equation. Thus, the effective number of bits can be less than or greater than the resolution of an ADC.

The INL error of an ADC is the deviation of the line through the endpoints of the transfer characteristic from the line through the endpoints of the ideal transfer characteristic of the ADC. The INL error is depicted in Figure 2.2.

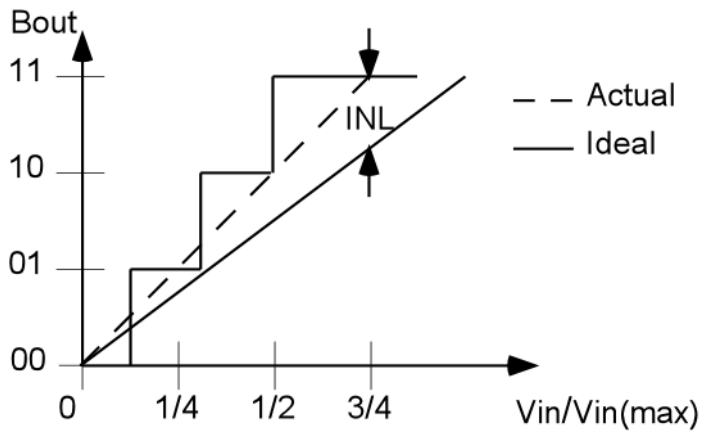


Figure 2.2 INL Error for a 2-bit ADC

The INL error is defined for each digital output word. Most literature reports the maximum INL error, which is an indication of the accuracy of the ADC. An ADC is guaranteed to be N-bit accurate if the INL error is less than ½ LSB [12].

The DNL error of an ADC is the deviation of the analog step sizes from 1 LSB. Figure 2.3 shows the DNL errors for output words "01" and "00" for a 2-bit ADC.

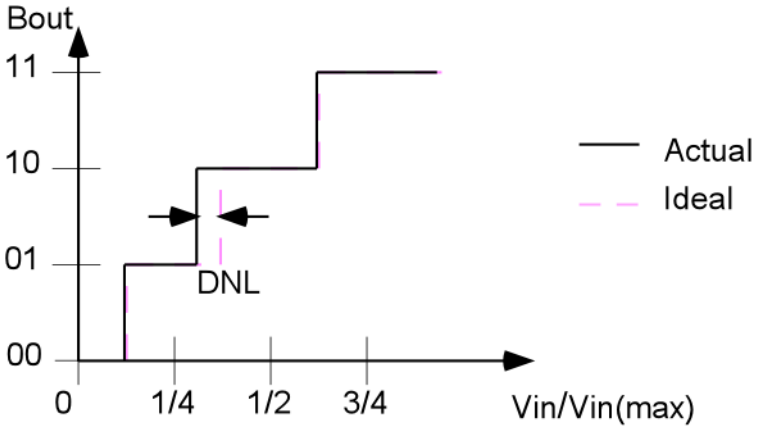


Figure 2.3 DNL Error for a 2-bit ADC

The DNL error of an ADC is also defined for each digital output word and is a measure of the accuracy of the ADC. When the DNL error of an ADC is less than 1 LSB, the ADC is guaranteed to be N-bit accurate [12].

The conversion time of an ADC is the amount of time taken to complete one digital word. The sampling rate is the speed that an ADC can continuously convert analog samples to digital words. The sampling rate is often the inverse of the conversion time, but some converters require latency between conversions [12]. If latency is

required between words, then the sampling rate includes the conversion time and the additional latency. The sampling rate is most often reported in samples per second (or Hertz) in literature.

The power dissipation of an ADC often reported is the amount of power required to complete a digital word. The power dissipation varies greatly with the conversion speed and the chosen ADC architecture. Also, power dissipation increases with increased accuracy since high-performance components, which typically have high power dissipation, are necessary for accurate ADCs. Power dissipation also increases for architectures that utilize parallelism.

The performance parameters of an ADC mentioned in this section are greatly dependent on the type of architecture chosen to implement the ADC. Common types of ADC architectures and their limitations are reviewed in the next section.

2.3 Various Types of Analog-to-Digital Converter Architectures

In this section, we briefly review several types of analog-to-digital converters, the general operation, and the characteristics of each ADC presented. The types of ADCs discussed here are the flash, the successive-approximation, the cyclic, the pipelined, and the sigma-delta architectures.

Generally, the fastest analog-to-digital converters are flash converters. A flash ADC determines the digital output word by performing 2^N parallel comparisons for an N-bit conversion. Since the hardware complexity of a flash ADC increases exponentially with resolution, power dissipation increases accordingly. Thus, flash ADCs are often limited to four to six bits. Interpolating or folding techniques use analog pre-processing blocks to reduce the amount of parallel comparisons, allowing greater resolution for less hardware complexity without decreasing the conversion rate of the ADC [12]. However, the analog pre-processing blocks grow increasingly complex as the number of parallel comparisons decreases. As a result, high-resolution interpolating and folding ADCs are seldom implemented.

Cyclic and successive-approximation ADCs compute the digital output using an iterative algorithm, where one bit is computed per conversion cycle. Generally, one

digital word is completed in N conversion cycles for an N-bit cyclic (or an N-bit successive-approximation) ADC. Due to the iterative approach, these ADCs utilize a small amount of hardware when compared with other types of converters. The reduction in circuit complexity is gained at the cost of conversion speed since N conversion cycles are required to complete the conversion. To maintain a constant conversion rate, cyclic and successive-approximation ADCs must operate with linearly increasing speed as the resolution increases. Cyclic and successive-approximation converters are one of the most popular approaches for analog-to-digital converter implementations due to the reasonably fast conversion speed and moderate circuit complexity [12].

A pipelined analog-to-digital converter is broken into stages of small-resolution (typically 1.5 bits) ADCs where each stage computes one bit per conversion cycle. When the first stage of a pipeline finishes computing the most-significant bit of the digital output for the current analog sample, the next stage starts to compute the next most-significant bit for the same analog sample. At the same time the first stage computes the most-significant bit for the next analog sample. In this manner, no stage of the pipeline is ever idle, and the analog-to-digital converter is continually working on new data in each conversion cycle. Thus, a pipelined analog-to-digital converter has a throughput comparable to a flash converter [12]. Due to the parallel architecture, power dissipation grows with increased resolution.

The ADC architectures discussed above are called Nyquist-rate ADCs. Nyquist-rate ADCs produce one N-bit digital output for each analog input at the Nyquist rate. A different approach is called an oversampling ADC, which utilizes oversampling techniques. An oversampling ADC includes a sigma-delta modulator that produces a low-resolution digital output (typically one to two bits) for every analog sample at a much faster speed than the Nyquist rate (typically 20 to 512 times the Nyquist rate). The quantization noise of the digital output of the modulator is digitally filtered to produce a higher-resolution digital output. As the oversampling rate increases, the accuracy of the ADC increases. Oversampling techniques provide a trade-off between analog and digital circuit complexity [12]. This trade-off is advantageous in digital processes where precision analog components are not available. However, since high-resolution sigma-

delta converters use a high oversampling rate, these converters generally have moderate conversion times.

2.4 Low-Power Analog-to-Digital Converter Design Approaches

Since low-power ADC designs are necessary for many applications, such as portable devices, most types of ADC architectures have been designed with low power dissipation as an objective. Most approaches for low-power analog designs are specific to the application at hand. Some general techniques for lowering power dissipation have been used in many ADC designs and are described in this section.

A technique often employed in low-power analog designs is lowering the supply voltage. Since power dissipation is quadratically related to the supply voltage, this approach reduces power dissipation. However, MOSFETs are often cascaded in analog designs. Since cascaded devices require a larger voltage drop across the cascade, lowering the supply voltage may not be feasible.

Many classic analog designs use resistors in their implementation. However, resistors have large quiescent power dissipation. As a result, resistive circuits are not good candidates for low-power designs. In architectures that employ resistor ratios, resistors can be replaced with capacitors. Since capacitors do not dissipate steady-state power, this technique reduces power dissipation.

A common component for ADCs is a comparator that produces the digital output of the ADC. For high-accuracy ADCs, high-gain comparators that use offset-cancellation techniques are often required. Such comparators have large power dissipation. One approach to reduce the necessary comparator power dissipation is to reduce or eliminate the need for high-gain components with offset-cancellation. This objective is accomplished by implementing digital error correction or by adopting algorithms immune to offsets. This approach is important for pipelined or flash converters since parallel comparators are used in these architectures. We employ this approach in our ADC design.

2.5 Review of Contemporary Analog-to-Digital Converters

In this section, we review state-of-the-art analog-to-digital converters. Since we wish to implement our analog-to-digital converter in a standard digital CMOS process, we will not consider ADC architectures implemented in other technologies, such as BiCMOS or gallium-arsenide. Also, in order to make a fair comparison between architectures, we propose the following figure of merit (FOM)

$$FOM = \frac{S * R}{P},$$

where S is the conversion rate or speed of the ADC in kiloHertz (kHz), R is the resolution of the ADC in bits, and P is the power dissipation in milliWatts (mW). A larger FOM implies a more efficient ADC design. The figure of merit does not take into account the power supply voltage or the CMOS technology used, but it is helpful for a general comparison.

Low-power ADCs designed in CMOS technologies were investigated extensively in the past decade [1], [3], [4], [5], [7], [9], [11], [13], [15], [19], [20], [21], [22], [23], [24], [25], [26], [29], [30], [31], [32]. Venes and Plassche reported an 8-bit, folding analog-to-digital converter with a sampling frequency of 80 MHz and a power dissipation of 80 mW. Folding techniques are used to reduce the number of comparators in a flash converter. Venes and Plassche partitioned their ADC into a 3-bit coarse ADC and a 5-bit fine ADC using a folding rate of 32 as a tradeoff between the number of required comparators and the complexity of the analog preprocessing block. The reported SNR of the ADC is 44 dB or 7.5 effective bits of resolution. The reported maximum INL of the ADC is 0.8 LSB, and the maximum DNL is 0.45 LSB [29]. Venes and Plassche's architecture has a FOM value of 8000.

Baird and Fiez developed a 14-bit, 500 kHz, sigma-delta ADC with a power dissipation of 58 mW. Baird and Fiez reduced the oversampling rate by utilizing a 4-bit sigma-delta modulator in their converter. Since the accuracy of the digital output is greater than the typical 1-bit resolution, the oversampling rate and power dissipation were

reduced. This architecture has a SNR of 86 dB or 14.3 effective bits [3]. Their architecture has a FOM value of 120.

Cho and Gray reported a 10-bit, 20 MHz, 35 mW, pipelined ADC. Cho and Gray applied several techniques to reduce the power dissipation of the pipelined ADC. They lowered the supply voltage from 5 V to 3.3 V, and capacitors were reduced to the minimal size necessary to overcome thermal noise. However, the reduction in capacitor sizes did require some additional circuitry. Digital-error correction was implemented to reduce the comparator requirements. The components in the latter stages of the pipeline were scaled down with respect to speed and accuracy since requirements of the latter stages of the pipeline are less rigorous than the first stages of the pipeline. The reported SNR is 62 dB or 10.3 effective bits. The reported maximum INL is 0.6 LSB, and the maximum DNL is 0.5 LSB [7]. Cho and Gray's ADC has a FOM value of 5714.

A 12-bit, 0.83 MHz, 2 mW, switched-current, redundant signed-digit cyclic converter was reported by Wang and Wey. Their ADC is based on the redundant signed-digit (RSD) cyclic algorithm. The RSD cyclic algorithm is immune to loop and comparator offsets, consequently reducing the comparator requirements of the ADC. Wang and Wey also lowered the power supply voltage from 5 V to 3.3 V. Wang and Wey reported a SNR of 74 dB or 12.3 effective bits, an INL of 0.45 LSB, and a DNL of 0.6 LSB [30]. Wang and Wey's ADC has a FOM value of 5000.

The figure of merits for the converters discussed above indicate that the flash converter proposed by Venes and Plassche is the best approach. However, low-power, high-resolution flash converters are not feasible due to the high degree of parallelism and large power dissipation. Thus, the best candidates for a high-resolution, low-power analog-to-digital converter are pipelined and cyclic converters. Since we wish to implement a variable-resolution analog-to-digital converter, we will discuss the feasibility of a variable-resolution approach for the pipelined ADC proposed by Cho and Gray and the cyclic ADC proposed by Wang and Wey in the following section.

2.6 Feasibility of Variable-Resolution Analog-to-Digital Converters

While each type of converter mentioned in Section 2.3 has its own merit for some applications, we are investigating a low-power analog-to-digital converter with variable resolution in this thesis. Good candidates for a variable-resolution ADC are the pipelined and cyclic implementations described in Section 2.5.

The 10-bit, pipelined ADC presented by Cho and Gray is a switched-capacitor approach [7]. Specifically, each of the ten stages of the pipeline consists of a high-speed, high-gain op-amp and capacitors. To implement variable resolution, the most obvious approach would be to dynamically disable the latter stages of the pipeline. However, operational amplifiers dissipate a large amount of steady-state power even when they are not performing a useful function. Consequently, disabling the latter stages of the pipeline would not save a large amount of power. While Cho and Gray's implementation exhibits low-power dissipation, the switched-capacitor implementation does not easily lend itself to a variable-resolution approach.

The 12-bit, redundant signed-digit cyclic ADC presented by Wang and Wey is based on a switched-current approach [30]. In Wang and Wey's architecture, the main components of the ADC are four MOSFET-capacitor pairs, four current sources, and one moderate-gain op-amp. An approach to variable resolution for a cyclic converter is limiting the number of conversion cycles for a lower-resolution conversion. Opening all the switches in the architecture effectively disables the switched-current converter. In Wang and Wey's architecture, no steady-state power is dissipated when its switches are open with the exception of the power dissipation of the moderate-gain op-amp. As a result, steady-state power would be small when the converter is disabled. Furthermore, the redundant signed-digit cyclic algorithm allows for low-power comparators that do not dissipate steady-state power. Also, since their architecture is based on switched-current techniques, it is appropriate for digital processes where precision analog components are not required. This advantage will be discussed further in the next chapter. Thus, Wang and Wey's cyclic converter is a good approach for a variable-resolution ADC, which aims to reduce power dissipation.

In this chapter we showed that a switched-current, redundant signed-digit cyclic ADC is a good approach for a variable-resolution, low-power, analog-to-digital converter. In the following chapter, we discuss the major components of the ADC in detail.

Chapter 3

Features of the Analog-to-Digital Converter Architecture

3.1 Introduction

In this chapter, we provide an overview of switched-current, redundant signed-digit (RSD) cyclic analog-to-digital converters (ADCs) related to the implementation of our ADC. First, we review cyclic analog-to-digital converters and then briefly describe the RSD cyclic algorithm and its advantages. We also describe an appropriate comparator for our ADC and then the common architectures of current copiers. Finally, we present an approach for achieving variable resolution, which is implemented in our ADC to reduce power dissipation.

3.2 Conventional Cyclic Analog-to-Digital Converters

A conventional cyclic ADC applies an iterative algorithm to determine the digital output of the ADC, where the input of the ADC can be a current or a voltage. Specifically, a cyclic ADC calculates one bit per conversion cycle beginning with the most significant bit (MSB). Unlike flash or pipelined ADCs, parallel hardware is not required for cyclic ADCs to result in a hardware efficient implementation. However, hardware efficiency is gained at the cost of conversion speed since cyclic ADCs require N conversion cycles for an N-bit conversion.

3.2.1 Conventional cyclic conversion algorithm

The cyclic algorithm is based on the conventional restoring division principle [9]. A flow-graph describing the cyclic conversion algorithm for an unsigned, N-bit, current-mode, cyclic ADC is shown in Figure 3.1.

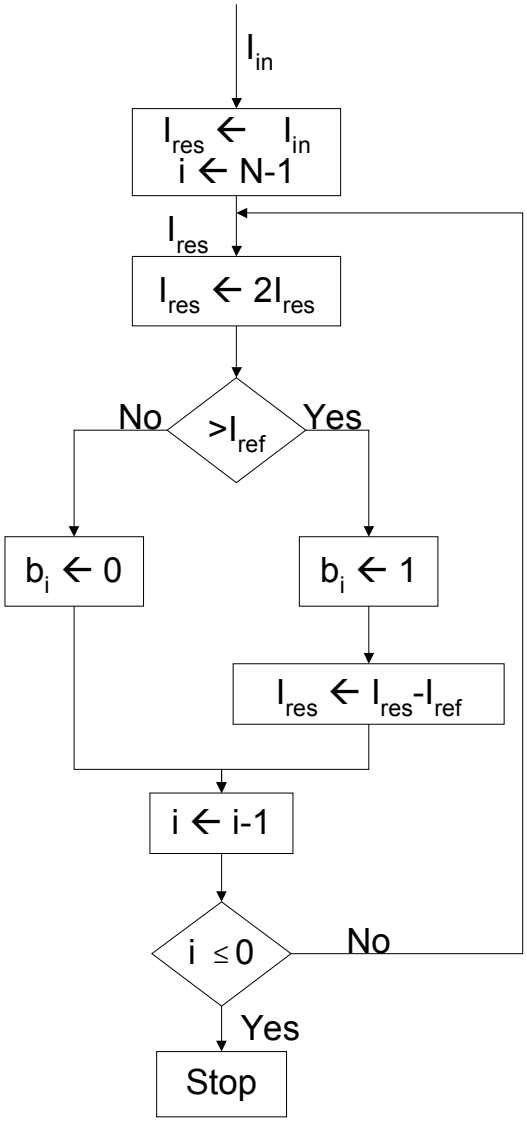


Figure 3.1 Flow Graph for a Conventional Cyclic Conversion Algorithm [12]

The residue current I_{res} in Figure 3.1 is initially the sampled input current I_{in}, and the loop variable i is set to the resolution N of the ADC. The initial residue current I_{res} is then multiplied by two and compared to the reference current I_{ref}. The reference current is set to the dynamic range of the ADC, which is the difference of the maximum input current and the minimum input current (i.e. $[I_{max}-I_{min}]$). If $2I_{res}$ is greater than the reference current, the current bit b_i is set to a digital '1', and the residue current is reduced by I_{ref}. Otherwise, the current bit is set to a digital '0', and the residue current remains the same. The loop variable is decremented by one, and the process repeats N times. The loop transfer characteristic can be expressed as

$$I_{res}* = \begin{cases} 2I_{res} - I_{ref} & if\ 2I_{res} > I_{ref} \\ 2I_{res} & if\ 2I_{res} \le I_{ref} \end{cases}$$

$$b_i = \begin{cases} 1 & if\ 2I_{res} > I_{ref} \\ 0 & if\ 2I_{res} \le I_{ref} \end{cases},$$

where $I_{res}*$ is the updated residue current used in the next conversion cycle and I_{res} is the initial residue current.

The conversion process of a cyclic ADC is illustrated for a 4-bit ADC, where the dynamic range of the ADC extends from 0 mA to 1 mA and the reference current is 1 mA. The residue current and the bit generated for each conversion cycle are given in Table 3.1 for a sampled input current of 0.35 mA.

Table 3.1 Illustration of a 4-bit Cyclic ADC

cycle n	**3**	**2**	**1**	**0**
$\mathbf{I_{res}}$	0.35 mA	0.7 mA	0.4 mA	0.8 mA
$\mathbf{2I_{res}}$	0.7 mA	1.4 mA	0.8 mA	1.6 mA
$\mathbf{b_n}$	0	1	0	1
$\mathbf{I_{res}}$*	0.7 mA	0.4 mA	0.8 mA	0.6 mA

3.2.2 Offset requirements

A limitation of a conventional cyclic ADC is its offset requirements. A Robertson diagram represents the loop transfer function of a cyclic ADC and is useful for illustrating the offset limitations. The horizontal axis of the Robertson diagram shown in Figure 3.2 is twice the initial residue current, which is the quantity used for comparison with the reference current in the current conversion cycle. The vertical axis is the updated residue current, I_{res}*.

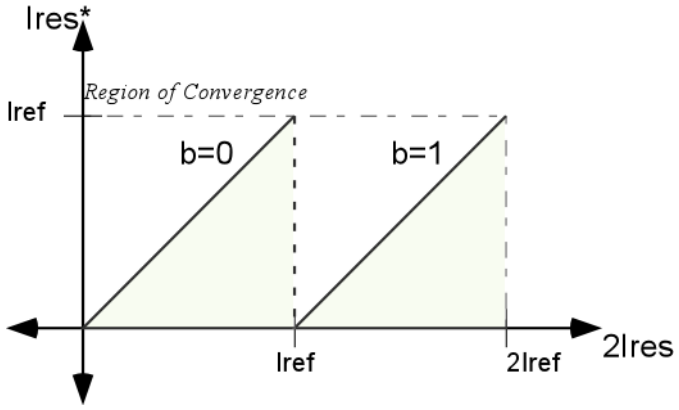


Figure 3.2 Robertson Diagram of a Conventional Cyclic ADC [9]

The region of convergence shown in Figure 3.2 is the range of the initial residue current and the updated residue current for which the cyclic algorithm converges. If the updated reside current, I_{res}*, exceeds the bounds of the region of convergence, the cyclic algorithm diverges since the residue current grows further from the bounds of the region of convergence with each iteration. Thus, after a cyclic ADC leaves the region of convergence, the ADC is effectively overloaded. Figure 3.2 shows that the region of convergence of a conventional cyclic ADC is [0, I_{ref}] for I_{res}* and [0, $2I_{ref}$] for $2I_{res}$. The requirement to stay in the region of convergence determines the offset limitations of a cyclic ADC.

In Figure 3.2, the line designated as b=1 is the one defined by $I_{res}^* = 2I_{res}-I_{ref}$ in the interval $[I_{ref}, 2I_{ref}]$, and the line designated as b=0 is the one defined by $I_{res}^* = 2I_{res}$ in the interval $[0, I_{ref}]$. The diagram shows that the current bit is set to '0' if $2I_{res}$ is less than I_{ref}, and $I_{res}^* = 2I_{res}$; otherwise, the current bit is set to '1', and $I_{res}^* = 2I_{res}-I_{ref}$.

Figure 3.2 indicates the only appropriate comparison level is I_{ref}. If the actual comparison level of a conventional cyclic ADC is $\hat{I}_{ref}$ instead of I_{ref} due to an offset, the ADC leaves its region of convergence under certain conditions, as demonstrated next. If $\hat{I}_{ref}$ is greater than I_{ref}, the residue current used in the next conversion cycle, I_{res}^*, exceeds I_{ref} for $\hat{I}_{ref} > 2I_{res} > I_{ref}$. When $2I_{res}$ is less than $\hat{I}_{ref}$, the reference current is not subtracted from $2I_{res}$. However, $2I_{res}$ exceeds I_{ref}. I_{res}^* then becomes $2I_{res}$, which is greater than I_{ref}. Consequently, the ADC leaves the region of convergence.

If the actual comparison level is greater than I_{ref} and the residue current is less than I_{ref} for a particular conversion cycle, the ADC does not leave the region of convergence. However, the ADC leaves the region of convergence when $\hat{I}_{ref} > 2I_{res} > I_{ref}$. Thus, under this condition, the ADC only converts analog inputs that map to the output word consisting of all zeros (i.e. "00...0") correctly.

Furthermore, if $\hat{I}_{ref}$ is less than I_{ref}, the residue current used in the next conversion cycle is less than zero for $I_{ref} > 2I_{res} > \hat{I}_{ref}$. When $2I_{res}$ is greater than $\hat{I}_{ref}$, the reference current is subtracted from $2I_{res}$, which is less than I_{ref}. The updated residue current, I_{res}^*, becomes $2I_{res}-I_{ref}$, which is less than zero. Consequently, the ADC leaves the region of convergence.

If the actual comparison level is less than I_{ref} and the residue current is greater than I_{ref} for a particular conversion cycle, the ADC does not leave the region of convergence. However, the ADC leaves the region of convergence when $I_{ref} > 2I_{res} > \hat{I}_{ref}$. However, the ADC only converts analog inputs that map to the output word "11...1" correctly.

The Robertson diagram of the cyclic ADC with a positive comparator offset Δ_c (i.e. $\hat{I}_{ref} > I_{ref}$) is shown in Figure 3.3. Figure 3.3 shows that if $2I_{res}$ is in the range $[I_{ref}, I_{ref}+\Delta_c]$, the ADC leaves the region of convergence.

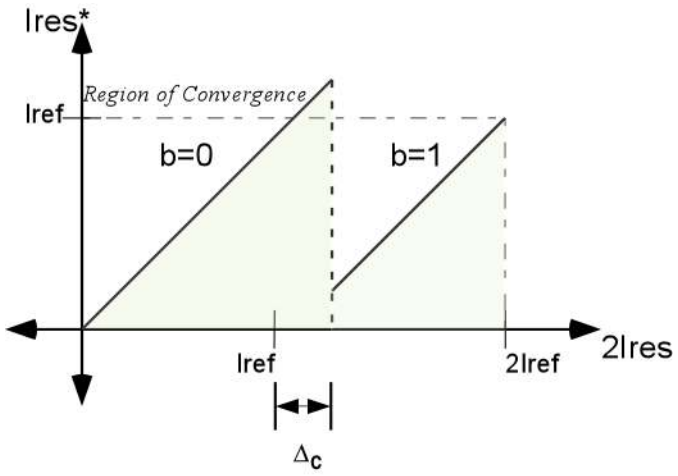


Figure 3.3 Robertson Diagram of a Conventional Cyclic ADC with a Comparator Offset $+\Delta_c$ [9]

The actual comparison level, $\hat{I}_{ref}$, of a conventional cyclic ADC must be within ½ I_{LSB} of I_{ref} to maintain an N-bit accuracy. (Note I_{LSB} is defined as $(I_{max} - I_{min})/2^N$.) For any loop offset less than or equal to ½ I_{LSB}, the difference of the bounds of the quantization error remains less than I_{LSB}; thus, the digital output of the ADC has N effective bits as given by the SNR equation. However, if a loop offset is greater than ½ I_{LSB}, a conventional cyclic ADC leaves its region of convergence, resulting in less than N-bit accuracy. Since constant loop offsets are often present in the hardware implementation of an ADC and cyclic ADCs are sensitive to offsets, a high-resolution cyclic ADC needs offset-cancellation techniques. Note that the offset may be due to a comparator offset or a constant offset elsewhere in the loop.

The ADC transfer characteristic for a signed, 4-bit ADC with a constant loop offset of I_{LSB} is shown in Figure 3.4.

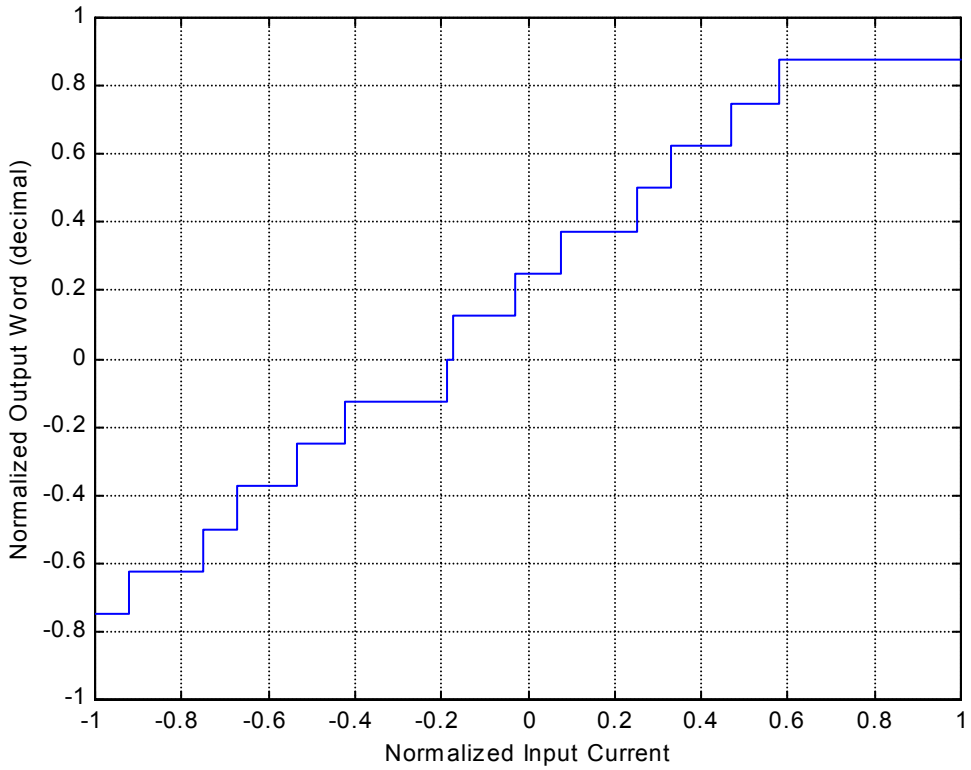


Figure 3.4 Transfer Characteristic of a Conventional Cyclic ADC with a Loop Offset of $+I_{LSB}$

The horizontal axis of Figure 3.4 is the normalized input current, which ranges from -1 to 1, and the vertical axis is the normalized output word in decimal, which is found by dividing the decimal equivalent of the output by 2^N. Figure 3.4 shows that the analog step sizes are neither uniform nor 1 I_{LSB} in step size when an offset of I_{LSB} is present. In fact, the difference of the bounds of the quantization error exceeds I_{LSB}, giving a SNR less than that required for eight effective bits. Thus, the ADC does not have 8-bit accuracy. Figure 3.3 and Figure 3.4 show a loop offset due to a comparator offset or a constant loop offset reduces the accuracy of a conventional cyclic ADC.

3.3 Redundant Signed-Digit Cyclic Analog-to-Digital Converters

In this section, we describe redundant signed-digit (RSD) cyclic ADCs and their advantages over conventional cyclic ADCs. An ADC based on the RSD algorithm is a

cyclic ADC with a ternary alphabet {-1, 0, 1} rather than a binary alphabet {0, 1}. However, the actual representation of the output bits of a RSD cyclic ADC is binary by necessity, and the binary representation is specific to the underlying hardware implementation (to be discussed in Chapter 4). Like a conventional cyclic ADC, a RSD cyclic ADC calculates one bit per conversion cycle beginning with the most significant bit. However, use of a ternary alphabet for a RSD cyclic ADC makes it tolerant of loop offsets and comparator inaccuracy.

3.3.1 RSD cyclic conversion algorithm

The RSD cyclic conversion algorithm is based on the Sweeney-Robertson-Tocher division principle [9]. A flow-graph illustrating the signed RSD cyclic conversion algorithm is shown in Figure 3.5.

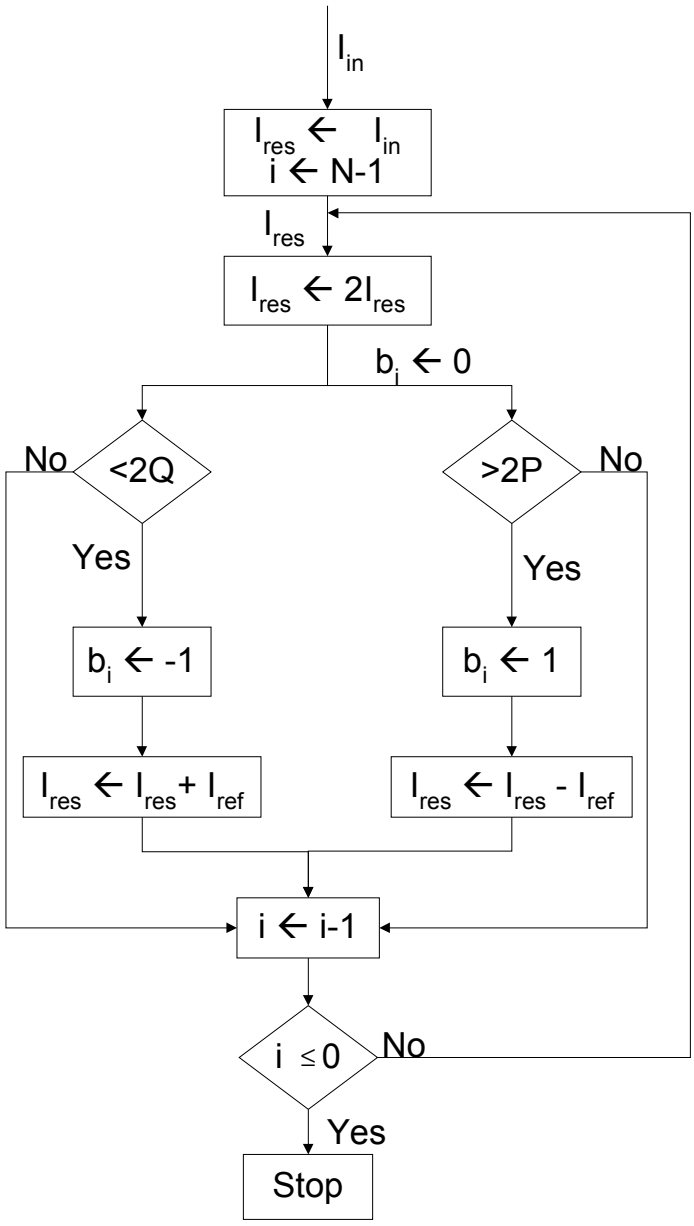


Figure 3.5 Flow Graph for the RSD Cyclic Conversion Algorithm [9]

As shown in Figure 3.5, the residue current I_{res} is initially the sampled input current, and the loop variable i is set to the resolution N of the ADC. The residue current is then multiplied by two, and two parallel comparisons are performed between $2I_{res}$ and the two constant comparison levels 2Q and 2P. 2Q is in the range of $[-I_{ref}, 0]$, and 2P is in the range of $[0, I_{ref}]$. The reference current, I_{ref}, is the difference of the maximum input current and the minimum input current divided by two (i.e. $(I_{max} - I_{min})/2$). If $2I_{res}$ is less than 2Q, the current bit b_i is '–1', and the reference current, I_{ref}, is added to $2I_{res}$. If $2I_{res}$ is

greater than 2P, the current bit is '1', and the reference current is subtracted from $2I_{res}$. If I_{res} is greater than 2Q but less than 2P, then the residue current remains the same, and the current bit is '0'. The loop variable is decremented by one, and the process repeats N times. The loop transfer characteristic can be expressed by

$$I_{res}* = \begin{cases} 2I_{res} + I_{ref} & if\ 2I_{res} < 2Q \\ 2I_{res} & if\ 2Q \le 2I_{res} \le 2P \\ 2I_{res} - I_{ref} & if\ 2I_{res} > 2P \end{cases}$$

$$b_i = \begin{cases} -1 & if\ 2I_{res} < 2Q \\ 0 & if\ 2Q \le 2I_{res} \le 2P \\ 1 & if\ 2I_{res} > 2P \end{cases}$$

The conversion process of a RSD cyclic ADC is illustrated for a 4-bit ADC, where the dynamic range of the ADC extends from -1 mA to 1 mA and the reference current is 1 mA, which is the dynamic range of the ADC divided by two. The comparison levels 2P and 2Q are chosen to be 0.5 mA and –0.5 mA, respectively. The residue current and the bit generated for each conversion cycle are given in Table 3.2 for the sampled input current of 0.35 mA.

Table 3.2 Illustration of a 4-bit RSD Cyclic ADC

cycle n	**3**	**2**	**1**	**0**
$\mathbf{I_{res}}$	0.35 mA	-0.3 mA	0.4 mA	-0.2 mA
$\mathbf{2I_{res}}$	0.7 mA	-0.6 mA	0.8 mA	-0.4 mA
$\mathbf{b_n}$	1	-1	1	0
$\mathbf{I_{res}}$*	-0.3 mA	0.4 mA	-0.2 mA	-0.4 mA

3.3.2 Offset requirements

While a RSD cyclic ADC is similar to a conventional cyclic ADC, it does not have the same offset requirements under certain conditions. The requirements on the ranges of 2Q and 2P are examined to identify the conditions. As mentioned previously, 2Q should be in the range [$-I_{ref}$, 0], and 2P is should be in the range [0, I_{ref}]. The range requirements of 2Q and 2P are illustrated with the three Robertson diagrams in Figure 3.6.

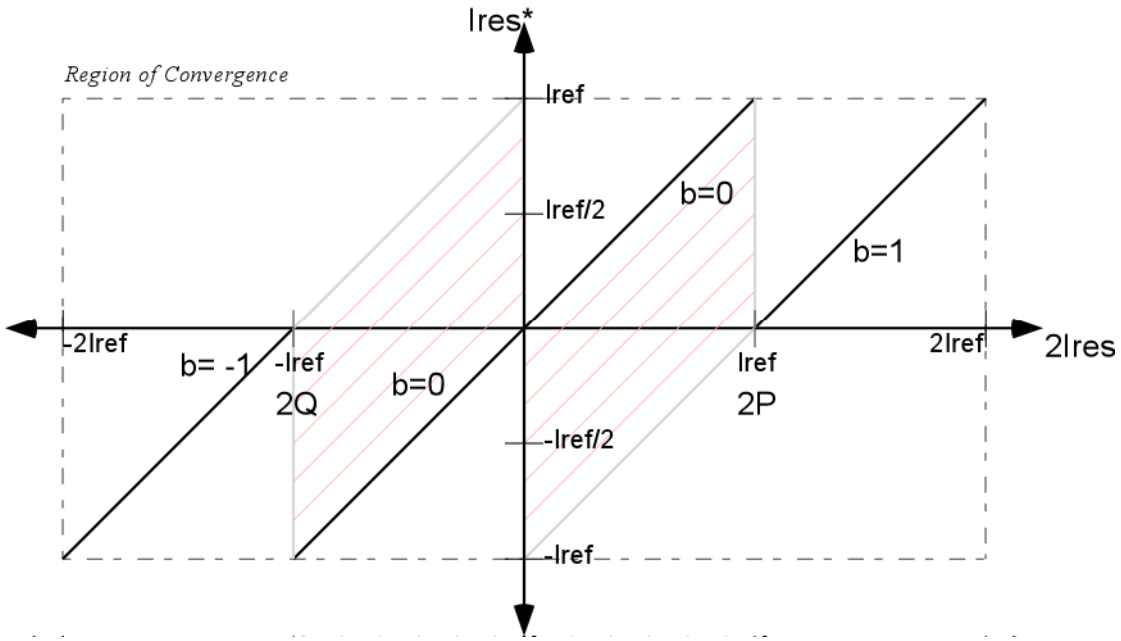


Figure 3.6 (a) Robertson Diagram of a RSD Cyclic ADC for 2P = -2Q = I_{ref}

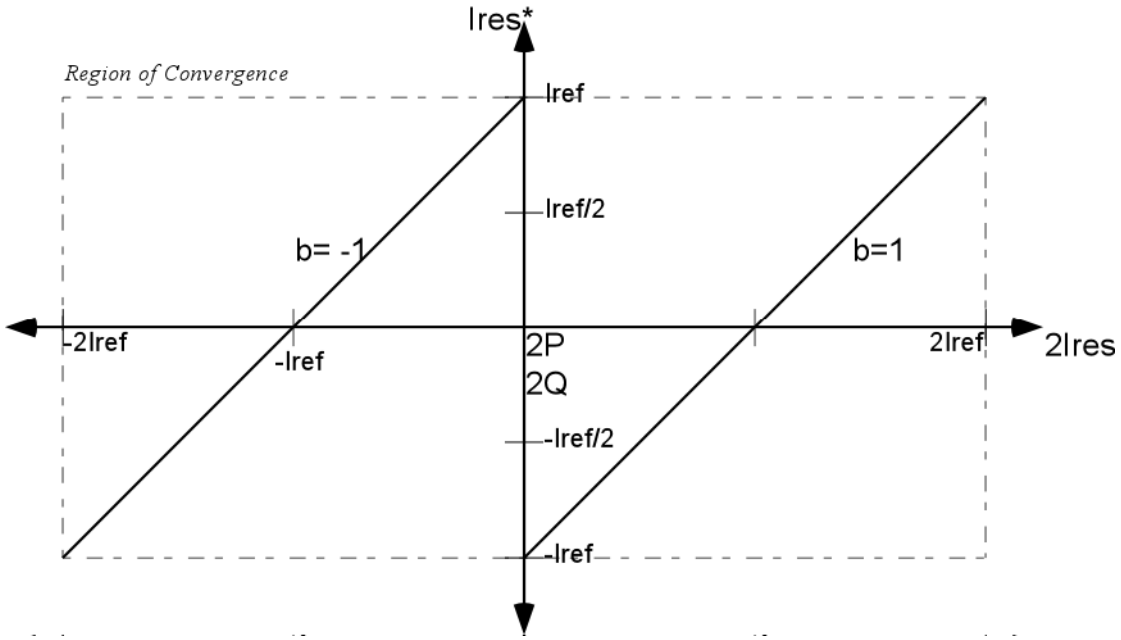


Figure 3.6 (b) Robertson Diagram of a RSD Cyclic ADC for 2P = -2Q = 0

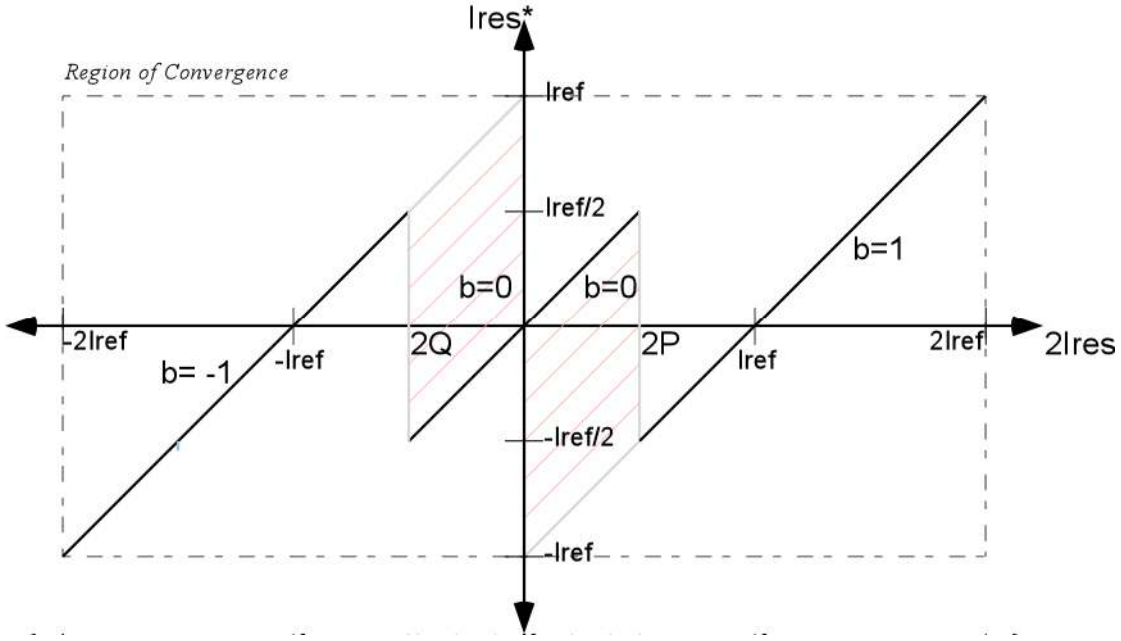


Figure 3.6 (c) Robertson Diagram of a RSD Cyclic ADC for 2P = -2Q = $I_{ref}/2$ [9]

The region of convergence shown in the three diagrams is [$-2I_{ref}$, $2I_{ref}$] for $2I_{res}$ and is [$-I_{ref}$, I_{ref}] for I_{res}*. The diagram shows that if $2I_{res}$ is less than 2Q, the current bit is set to '-1', and $I_{res}^* = 2I_{res}+I_{ref}$. If $2I_{res}$ is greater than 2P, the current bit is set to '1', and $I_{res}^* = 2I_{res}-I_{ref}$. Otherwise, the current bit is set to '0', and $I_{res}^* = 2I_{res}$. Figure 3.6 (a)

shows the case of $2P = I_{ref}$ and $2Q = -I_{ref}$. It will be shown that I_{res} remains in the region of convergence if $2P = -2Q = I_{ref}$. I_{res} also remains in the region of convergence for the case shown in Figure 3.6 (b), where $2P = 2Q = 0$. Figure 3.6 (c) shows the general case where $0 < 2P < I_{ref}$ and $-I_{ref} < 2Q < 0$. We show that I_{res} remains within the region of convergence for $0 \leq 2P \leq I_{ref}$ and $-I_{ref} \leq 2Q \leq 0$ next.

Suppose that $2P > 2I_{res} > I_{ref} > 2Q$. As $2I_{res}$ is less than 2P and greater than 2Q, I_{res}* is $2I_{res}$. However, $2I_{res}$ exceeds I_{ref}; thus, I_{res}* is greater than I_{ref}, which causes the ADC to leave the region of convergence. Now, suppose that $0 > 2I_{res} > 2P > 2Q$. As $2I_{res}$ is greater than 2P, $I_{res}* = 2I_{res}-I_{ref}$. However, $2I_{res}$ is less than zero; thus, I_{res}* is less than $-I_{ref}$. Consequently, the ADC leaves the region of convergence. Thus, 2P should be in the range $[0, I_{ref}]$. Similar arguments can be made for the range requirement of 2Q.

If the comparison levels 2P and 2Q are set to the limits of their required ranges (i.e. $2P = -2Q = I_{ref}$ or $2P = 2Q = 0$), the comparator offset of a RSD cyclic converter cannot exceed ½ I_{LSB}. In this case, the tolerable offset is the same as a conventional cyclic ADC. However, if 2P and 2Q are within their required ranges, the comparator offset can exceed ½ I_{LSB}. The Robertson diagram of Figure 3.6 (c) illustrates such a case.

Setting 2P and 2Q to $I_{ref}/2$ and $-I_{ref}/2$, respectively, gives the maximum comparison level tolerance $I_{ref}/2$ [9]. Given that 2P is $I_{ref}/2$ and $I_{res} = 0$, suppose the comparator makes the wrong decision by setting b_i = '1' (rather than b_i = '0') due to a comparator offset. The updated residue current is $I_{res}* = 2I_{res}-I_{ref} = -I_{ref}$, which is in the region of convergence of the ADC. Likewise, given that 2P is $I_{ref}/2$ and $I_{res} = I_{ref}/2$, suppose that the comparator makes the wrong decision by setting b_i = '0' (rather than b_i = '1') due to a comparator offset. The updated residue current is then $I_{res}* = 2I_{res} = I_{ref}$, which is in the region of convergence. The Robertson diagram for a RSD cyclic ADC resulting from a comparator offset Δ_c of $I_{ref}/2$ with $2P = -2Q = I_{ref}/2$ is shown in Figure 3.7. The figure shows that a RSD cyclic ADC remains in its region of convergence for this comparator offset.

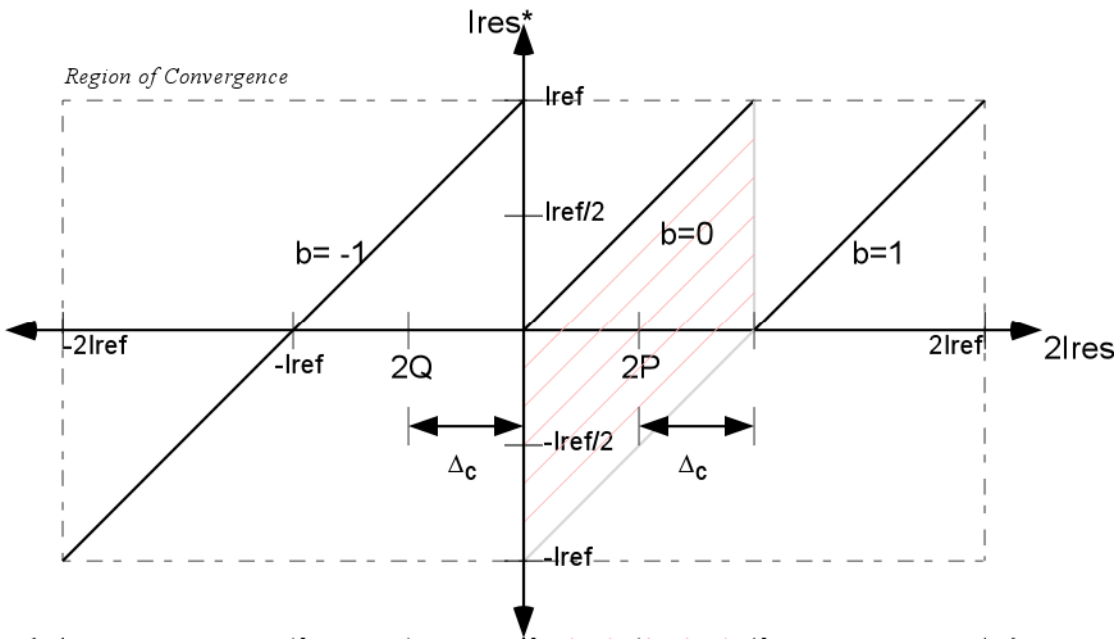


Figure 3.7 Robertson Diagram of a RSD Cyclic ADC with a Comparator Offset $+I_{ref}/2$

In the above, we showed that setting $2P = -2Q = I_{ref}/2$ provides the maximum tolerance for comparator offsets. Setting $2P = -2Q = I_{ref}/2$ also provides the maximum tolerance for constant loop offsets. If a constant loop offset is added after the multiplication by two, an RSD cyclic ADC can withstand loop offsets less than or equal to $I_{ref}/2$ for $2P = -2Q = I_{ref}/2$. In this case, the quantization error of an N-bit RSD cyclic converter is less than $^1/_2\, I_{LSB}$, assuming no other errors are present. As a result, offset-cancellation techniques are rarely required for RSD cyclic ADCs.

Figure 3.8 shows the transfer characteristic of a RSD cyclic ADC with a loop offset of $I_{ref}/2$, where $2P = -2Q = I_{ref}/2$ and the input range is [-1, 1].

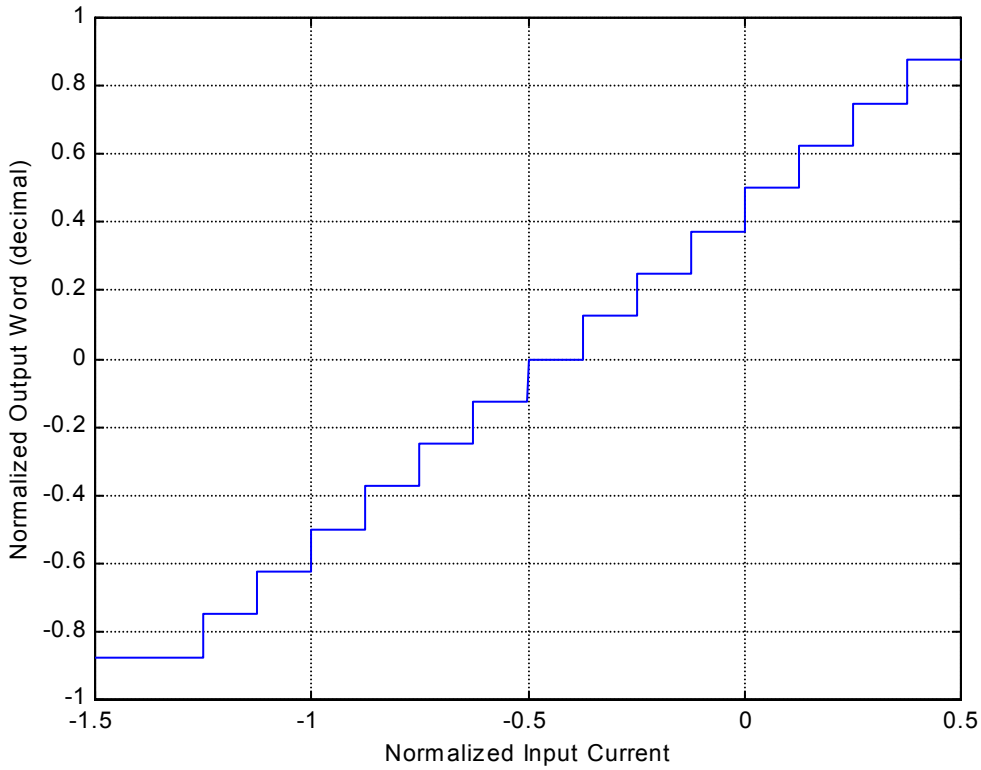


Figure 3.8 Transfer Characteristic of the RSD Cyclic ADC with a Loop Offset of $+I_{ref}/2$

Figure 3.8 shows the input dynamic range experiences a vertical shift of $I_{ref}/2$, which is the loop offset. However, the linearity of the RSD cyclic ADC is not affected by the loop offset. Thus, setting $2P = -2Q = I_{ref}/2$ is the optimum choice for 2P and 2Q to provide tolerance for any offsets present in a RSD cyclic ADC.

While an N-bit conventional cyclic ADC requires a loop offset less than or equal to ½ I_{LSB} for N-bit accuracy, an N-bit RSD cyclic ADC maintains N-bit accuracy for offsets less than or equal to $I_{ref}/2$ for $2P = -2Q = I_{ref}/2$. Since I_{LSB} is proportional to $1/2^N$, I_{LSB} is much smaller than $I_{ref}/2$ for high-resolution converters. Thus, RSD cyclic converters have a substantial advantage over conventional cyclic ADCs.

3.3.3 Advantages of the RSD cyclic conversion algorithm

The RSD cyclic conversion algorithm is superior to the conventional cyclic conversion algorithm with respect to loop offsets and required comparator accuracy. A conventional cyclic ADC with high resolution requires a precise comparison against the reference current in order to remain within its region of convergence. A precise comparison demands high gain components with offset cancellation. In contrast, the RSD algorithm allows relatively large comparator offsets.

Another advantage of the RSD cyclic conversion algorithm is its immunity to loop offset errors. As mentioned in Section 3.2, the loop offset of a conventional ADC does not exceed ½ I_{LSB} for an ADC with N-bit accuracy. As a result, a high-accuracy cyclic ADC frequently requires offset-cancellation techniques since constant loop offsets are often present in the hardware implementation of an ADC and cyclic ADCs are sensitive to offsets. However, as long as the loop offset does not exceed the tolerance set by the comparison levels 2P and 2Q, a RSD cyclic ADC remains in its convergence region. If an offset is present in a RSD cyclic ADC, the input dynamic range simply experiences a vertical shift.

While a RSD cyclic ADC is superior to a conventional cyclic ADC with respect to offsets, the cost of superiority is an additional comparator. However, comparators of a RSD cyclic ADC need not be accurate due to the comparator-offset insensitivity of a RSD cyclic ADC. A simple comparator suitable for a RSD cyclic ADC is explored in the next section.

3.4 Comparator

In this research, the RSD cyclic conversion algorithm is employed due to its superiority over the conventional cyclic conversion algorithm. The RSD cyclic conversion algorithm greatly relieves the constraints on the comparators used in an ADC architecture. Specifically, if the comparison levels 2P and 2Q are chosen to be $I_{ref}/2$ and -

$I_{ref}/2$, respectively, the required offset of the comparators of a RSD cyclic ADC is $I_{ref}/2$. Thus, a simple comparator architecture can be used for RSD cyclic ADCs.

A comparator often used in ADCs based on the RSD algorithm consists of two strobed and cross-coupled inverters. The circuit diagram for such a comparator is given in Figure 3.9.

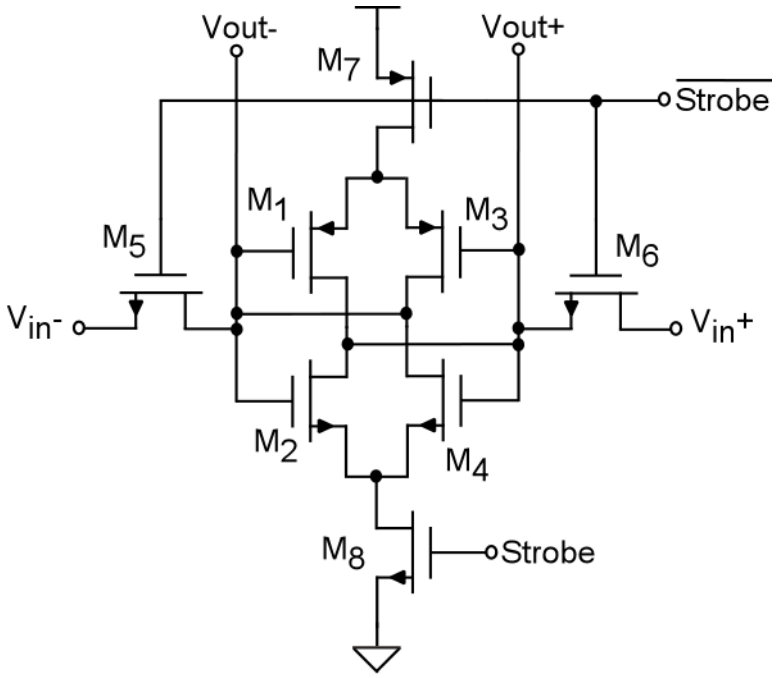


Figure 3.9 Circuit Diagram of a Strobed, Cross-Coupled Inverter Comparator [9]

The transistor pair M_1 and M_2 form one inverter, and the transistor pair M_3 and M_4 form another inverter. The inverters are cross-coupled, as shown in the figure. Vin+ and Vin- are the input voltages, where one input voltage is chosen to be the comparison level for the comparator. The outputs of the two inverters, Vout+ and Vout-, are the outputs of the comparator.

When strobe is low, Vin+ and Vin- charge the parasitic gate capacitances of the inverters. However, no path exists from the supply rails (i.e. Vdd and ground) since the transistors M_7 and M_8 are off. Consequently, Vout- follows Vin-, and Vout+ follows Vin+. When the strobe signal transitions from low to high, M_5 and M_6 are turned off and the input voltages are sampled at the gates of the inverters. When the strobe signal is high, the circuit of Figure 3.9 simplifies to two cross-coupled inverters. The cross-

coupled inverters amplify the difference between the two input voltages, forcing the output voltages to the appropriate digital values for the given comparison level and input voltage. For example, suppose that the comparison level is chosen to be Vin- = Vdd/2 = 1.65 V and the input voltage is Vin+ = 0.5 V. Vout+ settles to ground, and Vout- settles to Vdd. The output voltages indicate that Vin+ is less than Vin-.

Since a strobed, cross-coupled inverter comparator consists of fully complementary logic, it consumes a negligible amount of steady-state power. The comparator dissipates power only during the period when the inverters are amplifying the difference between the input voltages. Thus, a strobed, cross-coupled inverter comparator is suited to low-power applications.

3.5 Current Copiers

The analog-to-digital converter that we investigated in this thesis employs a switched-current architecture. In switched-current architectures, all the variables of interest are currents rather than voltages. A major building block of switched-current architectures is a current copier. A current copier acts as a current memory, which stores current. We review several current copiers in this section. The descriptions of the current copiers are given in [27].

3.5.1 Simple current copier

A simple current copier consists of a single transistor and a capacitor. The circuit diagram is shown in Figure 3.10.

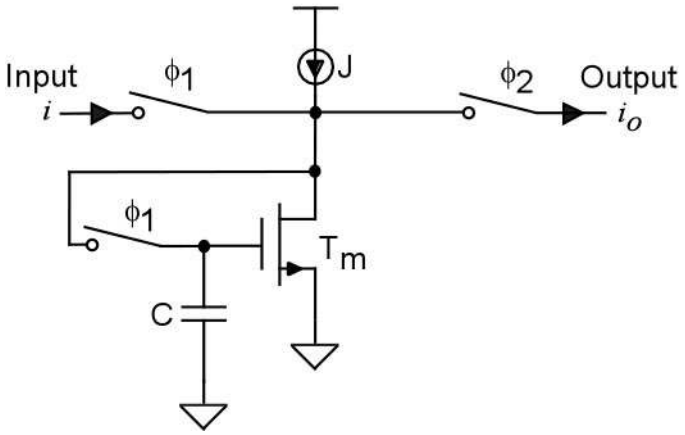


Figure 3.10 A Simple Current Copier [28]

During phase ϕ_1, the drain and gate of the transistor are connected, and the signal current i plus the bias current J is sourced to the copier cell. The total current, J+i, initially charges the gate capacitance C. Eventually, the gate capacitance is charged to the voltage that causes the memory transistor T_m to conduct current J+i. At this point, the current copier cell has memorized the signal current i.

During phase ϕ_2, the switch connecting the gate and drain of the transistor is opened, disconnecting the memory transistor from the input current. Also, the drain of the memory transistor is connected to the output of the current copier cell. Since the gate capacitance is charged to the voltage that causes the transistor to have a drain current of J+i, the output current is –i, assuming that the memory transistor operates in the saturation region. Hence, the current copier is acting as a current source with current value i [28]. Note that if the memory transistor is not in the saturation region, the drain current is dependent on the drain voltage as well as the gate voltage of the transistor, greatly diminishing the accuracy of the current copier.

The current copier is suitable for digital processes since the value of the capacitor of the regulated-cascode current copier is not critical. Specifically, since the capacitor of the current copier is only used to store a voltage, the value of the stored current is not dependent on the value of the capacitor. Thus, the current copier does not require precise analog components, which are not available in digital processes.

While this architecture is simple, it is not accurate. The accuracy of the simple current copier is limited by two main factors. First, the current memorized during phase ϕ_1 is not equal to the current sourced in phase ϕ_2 due to the secondary channel-length modulation effect. The channel-length modulation effect is the phenomenon where the effective channel length of a MOSFET is reduced as the drain-source voltage V_{ds} increases, producing higher drain currents for higher drain-source voltages. The channel-length modulation effect results in a drain-source conductance g_{ds} that is given by

$$g_{ds} = \lambda I_{ds},$$

where λ is the channel-length modulation coefficient and I_{ds} is the drain-source current of the memory transistor. Since the drain current of a transistor is dependent on its drain and gate voltage, the current copier does not source an output current of -i if the drain-source voltage differs from phase ϕ_1 to phase ϕ_2.

Secondly, when the switch at the gate of the memory transistor is open during phase ϕ_2, changes in the drain voltage cause current to flow from the gate-drain overlap capacitance C_{dg} into the memory capacitance C. This current causes the gate-source voltage of the memory transistor to change during phase ϕ_2, producing an error in the stored current.

Channel-length modulation and the change in the gate-source voltage of the memory transistor due to C_{dg} produce an error current δI_{ds}, which results from the change in the drain-source voltage δV_{ds} of the memory transistor. The error current is given by

$$\delta I_{ds} = \delta V_{ds}\left(g_{ds} + \frac{C_{dg}}{C_{dg} + C} g_m \right),$$

where g_m is the small-signal input conductance of the memory transistor. The memory transistor can be modeled as an ideal transistor with an output conductance g_o connected from its drain to its source, which is defined by

$$g_o = g_{ds} + \frac{C_{dg}}{C_{dg} + C} g_m .$$

Consider two identical, cascaded current copiers as shown in Figure 3.11, where one current copier is sourcing current to a second current copier.

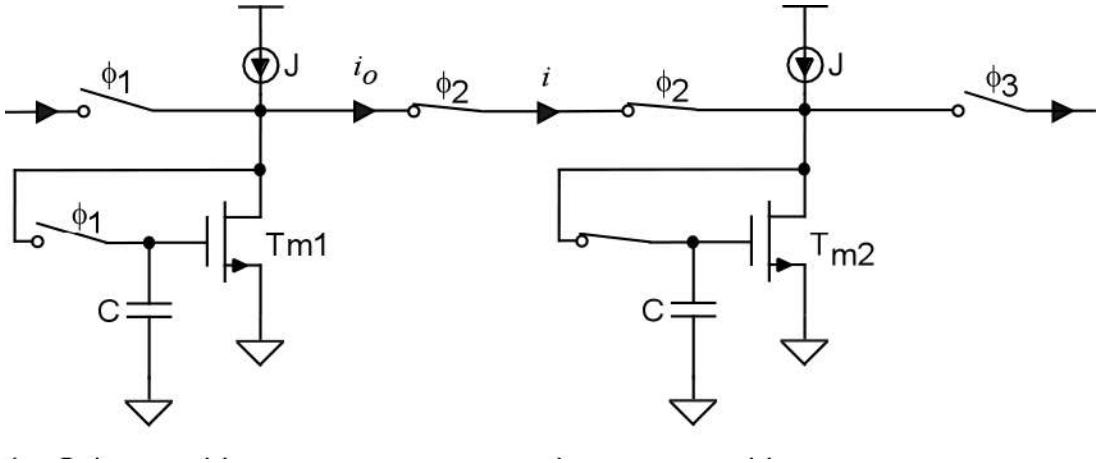


Figure 3.11 Two Identical, Cascaded Simple Current Copiers [27]

Each current copier is modeled as an ideal transistor with an output conductance g_o. When the first current copier is sourcing its stored current to the second current copier, the z-transform of the transfer function H(z) obtained as

$$H(z)=\frac{i_o(z)}{i(z)}=\frac{-z^{1/2}}{1+\frac{2g_o}{g_m}}=\frac{H_i(z)}{1+\frac{2g_o}{g_m}},$$

where $i_o(z)$ is the output current of the first current copier in the z domain, i(z) is the input current of the second current copier in the z domain, and $H_i(z) = -z^{-1/2}$ is the ideal transfer function of the two cascaded current copiers. For physical frequencies $z=e^{j\omega T}$, the transfer function H(z) becomes

$$H(e^{j\omega T})=\frac{H_i(e^{j\omega T})}{1+\frac{2g_o}{g_m}},$$

where T is the period of the clock signals ϕ_1 and ϕ_2. An approximation to relate the actual frequency response to the ideal frequency response for small errors is given by

$$H(e^{j\omega T})=\frac{H_i(e^{j\omega T})}{1-m(\omega)-j\theta(\omega)},$$

where m(ω) is the magnitude difference from the ideal frequency response, and θ(ω) is the phase difference from the ideal frequency response. The magnitude error and phase error for the simple current copier are given by

$$m(\omega) = -\frac{2g_o}{g_m} = \varepsilon_G,$$
$$\theta(\omega) = 0$$

where the transmission error ε_G is the magnitude difference between the current memorized during phase ϕ_1 and the current sourced by the memory transistor during phase ϕ_2. The transmission error is given by

$$\varepsilon_G = -2\left(\frac{g_{ds}}{g_m} + \frac{C_{dg}}{C_{dg} + C}\right).$$

Thus, to decrease the transmission error, the output conductance of the current copier cell must be decreased, and/or the small-signal conductance must be increased. Long-channel devices reduce the output conductance, g_o, but larger devices result in reduced bandwidth due to larger parasitic capacitances [27]. Several alternative architectures have been proposed to stabilize the drain voltage of the current copier cell. Among these are the op-amp active current copier and the regulated-cascode current copier, which are described in the next section.

3.5.2 Op-amp active current copier

An op-amp active current copier consists of a simple current copier with a feedback amplifier. The circuit diagram of an op-amp active current copier is given in Figure 3.12.

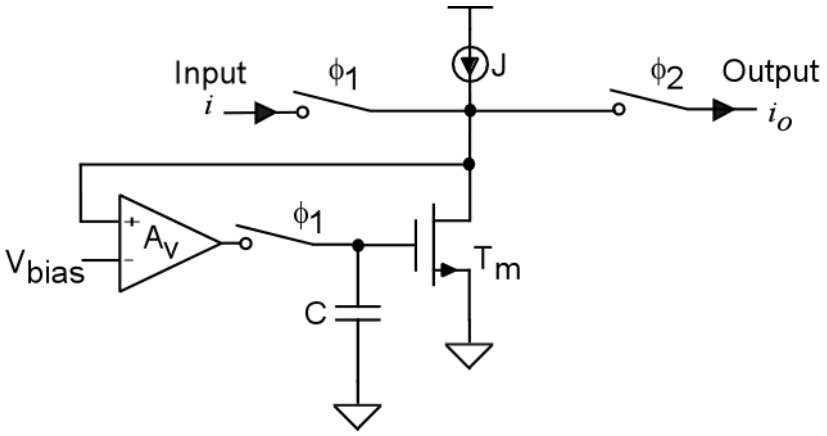


Figure 3.12 An Op-Amp Active Current Copier [28]

During phase ϕ_1, the drain of the memory transistor T_m is connected to one of the differential inputs of the op-amp, the bias current J, and the input signal current i. The gate of the transistor is connected to the single-ended output of the op-amp. Initially, the input current i acts to disturb the voltage at the input terminal of the op-amp. Consequently, the op-amp sources a current to the gate capacitance of the memory transistor. This feedback loop reaches equilibrium when the memory transistor sources the total current, J+i. Upon this condition, the memory transistor has memorized the signal current i. The op-amp suppresses any change in the drain voltage of the memory transistor since a high-gain op-amp creates a virtual short between its differential inputs.

During phase ϕ_2, the switch at the gate of the memory transistor is open, and the drain of the memory transistor is connected to the output of the current copier cell. Since the gate capacitance is charged to the voltage that causes the transistor to have a drain current of J+i, the output current is –i. Hence, the current copier acts as a current source with value i [28]. During this phase, the op-amp maintains an approximately constant voltage at the drain of the memory transistor, T_m.

An op-amp active current copier combats the transmission error by maintaining a nearly constant drain voltage. If the op-amp has a high voltage gain, then the drain voltage is close to V_{bias}. For an op-amp active current copier, the transmission error is given by

$$\varepsilon_G = \frac{-2g_o}{A_v g_m},$$

where A_v is the voltage gain of the op-amp, g_o is the output conductance of the memory transistor, and g_m is the small-signal input conductance of the memory transistor. The reduction in the transmission error is due to an increase of the small-signal conductance g_m by a factor of the voltage gain of the op-amp due to the feedback loop [27].

While the transmission error is greatly reduced for a moderate-gain op-amp, low-power, high-speed op-amps are difficult to implement in practice. For example, if a settling time of 5 ns with an accuracy of 72 dB is to be achieved, the op-amp would need a bandwidth of approximately 2 GHz. Such amplifiers are power hungry, and thus inappropriate for low-power designs.

3.5.3 Regulated-cascode current copier

A regulated-cascode current copier consists of a simple current copier with a cascode transistor and a regulating transistor, as shown in Figure 3.13.

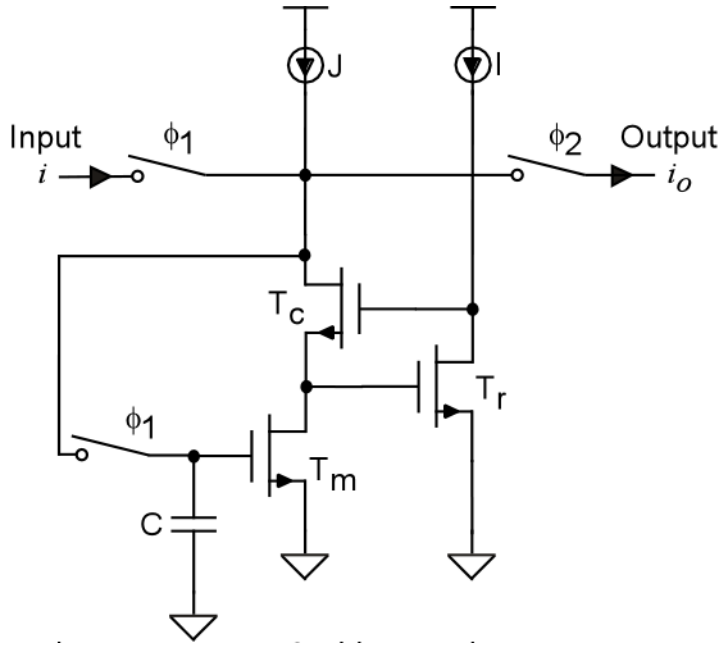


Figure 3.13 A Regulated-Cascode Current Copier [28]

During phase ϕ_1, the drain of the cascode transistor T_c is connected to the bias current J, and the signal current i is connected to the drain of T_c and the gate of T_m. The total current, J+i, charges the gate capacitance of the transistor T_m until the transistor

maintains a current J+i. Since the regulating transistor T_r is biased with a constant current, it suppresses any change in the drain voltage of the memory transistor. Specifically, the negative feedback loop created by the two transistors T_r and T_c suppresses any variance at the drain of the memory transistor, T_m.

During phase ϕ_2, the switch connecting the gate of the memory transistor and signal current i is opened. The drain of the cascode transistor is connected to the output of the current copier cell. Since the gate capacitance C is charged to the voltage that causes the transistor to have a drain current of J+i, the output current is –i. Hence, the current copier acts as a current source with value i. The regulating transistor still suppresses any variance at the drain of the memory transistor during this phase.

The transmission error of the regulated-cascode current copier cell is greatly reduced due to the decrease of the output conductance of the current copier cell. Consider the circuit of Figure 3.13 with the regulating transistor removed. In this case, the output conductance of the current copier cell at the drain of the cascode transistor can be shown to be

$$g_{oc} = g_o \left[\frac{g_{dsc}}{g_{ds} + g_{dsc} + g_{mc}} \right],$$

where g_{mc} is the small-signal input conductance of the cascode transistor, g_{dsc} is the drain-source conductance of the cascode transistor, g_o is the output conductance of the memory transistor when the switch at its gate is open, and g_m is the small-signal input conductance of the memory transistor. Given $g_{ds} << g_{mc}$, and $g_{dsc} << g_{mc}$,

$$g_{oc} \approx g_o \frac{g_{dsc}}{g_{mc}}.$$

Thus, the cascode transistor decreases the output conductance of the regulated-cascode current copier cell by a factor of g_{dsc}/g_{mc}. This reduction is typically on the order of 100.

The addition of the regulating transistor decreases the output conductance of the regulated-cascode current copier cell by an additional factor of g_{dsr}/g_{mr}, where g_{mr} is the small-signal input conductance of the regulating transistor, and g_{dsr} is the output conductance of the regulating transistor. Hence, the output conductance of the regulated-cascode current copier is

$$g_{or} \approx g_o\left(g_{dsc}/g_{mc}\right)\left(g_{dsr}/g_{mr}\right).$$

The transmission error is given by

$$\varepsilon_G = \left(-2g_o/g_m\right)\left(g_{dsc}/g_{mc}\right)\left(g_{dsr}/g_{mr}\right).$$

The transmission error is typically lowered by a factor of 10,000. Thus, accuracy on the order of 0.01 percent is feasible for the regulated-cascode current copier [27]. In addition, the power consumption of the regulated-cascode current copier is small due to its moderate circuit complexity. Furthermore, the regulated-cascode current copier is suitable for digital processes since the value of the capacitor of the regulated-cascode current copier is not critical. Due to its potential for high accuracy, relatively small power dissipation, and suitability for digital processes, we adopt this current copier for our ADC design.

3.6 Variable Resolution

The ADC investigated in this research has variable resolution and is based on the RSD cyclic algorithm. The purpose of implementing a variable-resolution ADC is to reduce power consumption. Unlike complementary MOS circuits, conventional analog circuits consume steady-state power due to biasing of analog components. However, when compared to customary analog components, switched-current copiers dissipate little steady-state power when the circuit is neither storing nor sourcing current. Also, the regulated-cascode current copiers can be disabled when the circuit is not storing or sourcing current. Thus, an ADC based on switched-current copiers is an appropriate architecture for a variable-resolution approach.

As indicated in Section 3.1, a cyclic ADC computes one bit per conversion cycle. After a cyclic ADC has computed N bits, the ADC computes the next digital output word for the next sampled input. In order to implement variable resolution, the number of conversion cycles is simply limited to n clock cycles for an n-bit digital output word, where n is dynamically set in the range of 1 to N. Furthermore, the current copiers can be disabled during the period when no output bits are being computed.

The architecture of the ADC studied in this research utilizes switched-current copiers as the main computational unit. Referring to Figure 3.13, if the switches ϕ_1 and

ϕ_2 are open, the current copier is not performing a computation, and the current copier is in standby mode. A finite-state machine can be used to open these switches when the ADC has reached the desired n-bit resolution.

Additionally, high-accuracy comparators often consume much power due to the need for high-gain components. However, a simple comparator can be used for a RSD cyclic ADC due to the characteristics of the RSD cyclic algorithm. In addition, since the comparator given in Figure 3.9 is a fully complementary MOS circuit, the comparator does not dissipate power when it is not performing a useful function. Consequently, the comparator shown in Figure 3.9 is suitable for a variable-resolution ADC with low power dissipation.

In summary, a current-mode, RSD cyclic ADC is suitable for low-power applications. Moreover, a RSD cyclic ADC can easily accommodate a variable-resolution approach, further reducing the power dissipation when a lower-resolution ADC is sufficient for certain periods during its operation.

Chapter 4

Implementation

4.1 Introduction

The ADC that we have implemented is a switched-current, variable-resolution analog-to-digital converter based on the RSD cyclic algorithm. Our ADC has a maximum resolution of 12 bits and a dynamic range of 0 μA to 90 μA. In this chapter, we review the implementation of our ADC architecture and its operation.

The major units of computation of our ADC are regulated-cascode current copiers, which are used to double the residue current as required by the RSD cyclic algorithm. Regulated-cascode current sources are used to add and subtract the reference current and create an offset in the residue current, while strobed, cross-coupled inverter comparators are used to compare the residue current to the comparison levels P and Q. Variable resolution is implemented through digital techniques by limiting the number of bit cycles the ADC executes. We discuss the architecture of our proposed ADC, the implementation of the RSD cyclic algorithm, and the implementation of each component of our ADC. We also present the method used to implement variable resolution, discuss layout considerations, and present our test chip.

4.2 Architecture of the Analog-to-Digital Converter

In this section we describe the ADC architecture and its components. We also review the implementation of the RSD algorithm. The ADC architecture that we have

implemented is based on Wang and Wey's current-mode, RSD cyclic ADC architecture [30]. The ADC architecture is shown in Figure 4.1.

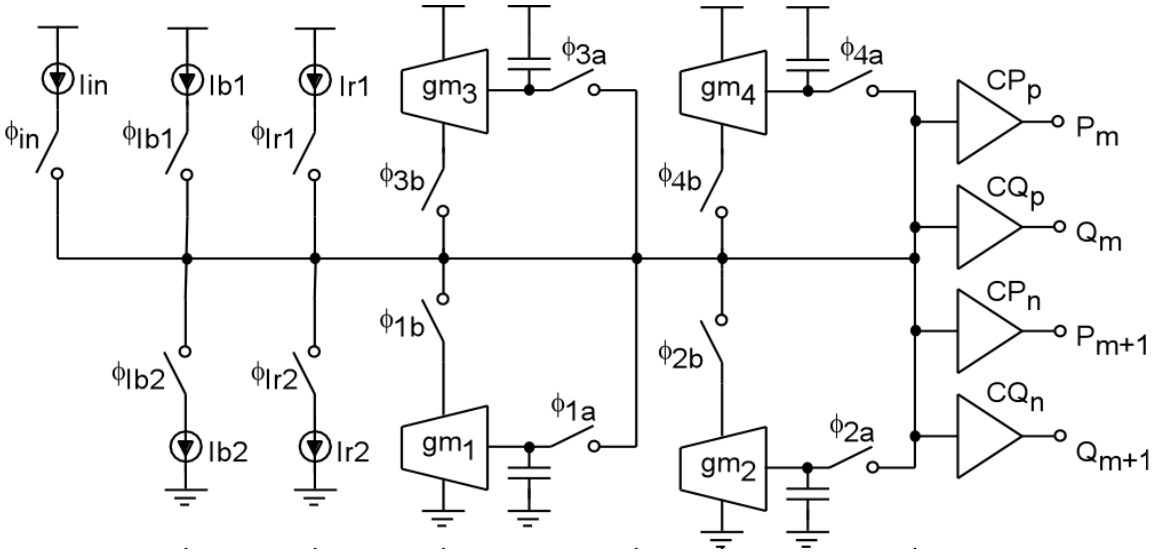


Figure 4.1 Analog-to-Digital Converter Architecture

The current source I_{in} is the input current of the ADC. The g_m blocks are regulated-cascode current copiers used to double the residue current. Blocks g_{m1} and g_{m2} are NMOS regulated-cascode current copiers, and blocks g_{m3} and g_{m4} are PMOS regulated-cascode current copiers. The four comparator blocks produce the digital outputs of the ADC, P_m, Q_m, P_{m+1}, and Q_{m+1}. The comparators are strobed, cross-coupled inverter comparators as discussed in Section 3.4. The reference currents I_{r1} and I_{r2} are equally-valued constant current sources used to add and subtract the reference current as required by the RSD cyclic algorithm. The equally-valued constant bias currents I_{b1} and I_{b2} are used to create an offset in the residue current. Note that the switches associated with the PMOS regulated-cascode current copiers and the PMOS regulated-cascode current sources are P-type switches, and the switches associated with the NMOS regulated-cascode current copiers and the NMOS regulated-cascode current sources are N-type switches. The implementation of the RSD cyclic algorithm using the architecture of Figure 4.1 is described in the next section

4.3 Implementation of the RSD Algorithm

The implementation of the RSD algorithm in our ADC is a slightly altered version of the flow graph of Figure 3.5. The flow graph for the typical bit cycle employed in our ADC is given in Figure 4.2.

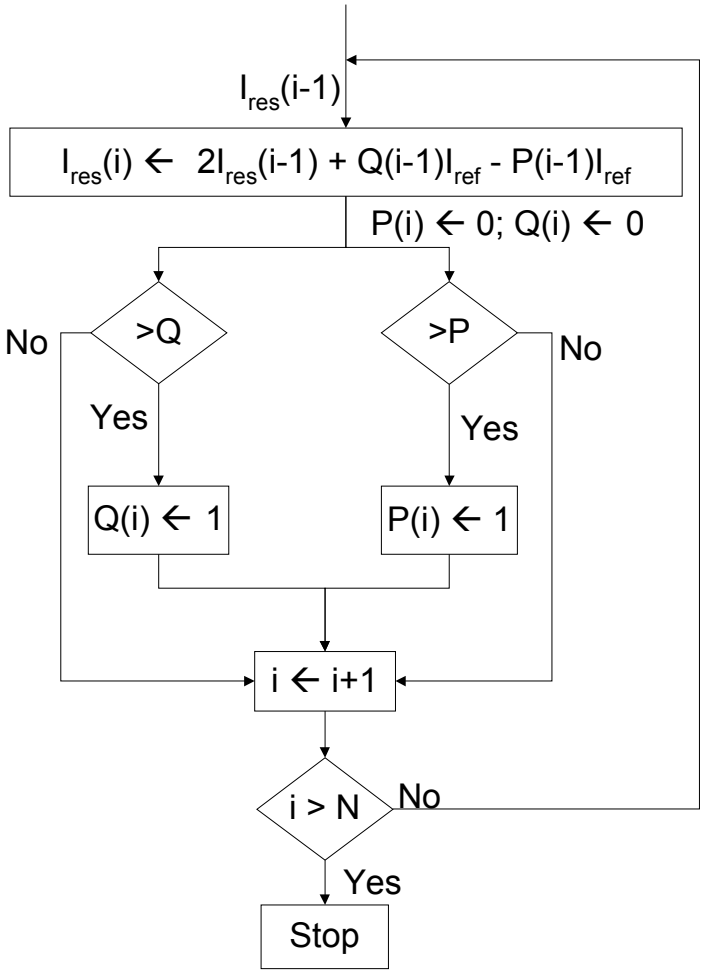


Figure 4.2 Flow Graph for a Typical Bit Cycle

Figure 4.2 shows that the computation of the updated residue current of a particular bit cycle is delayed by one bit cycle. Specifically, the updated residue of bit cycle i-1 (which is $I_{res}*(i-1) = I_{res}(i)$) is not computed until the i^{th} bit cycle. Also, *the comparisons of the RSD algorithm are made before the residue current is multiplied by two*. As a result, the comparisons are made with Q and P rather than 2Q and 2P. The purpose of these alterations is to avoid unnecessary latency in the conversion process. As will be shown

later, two clock cycles are required to double the residue current. Thus, if a direct implementation of the RSD algorithm illustrated by Figure 3.5 were used, the conversion process would require a latency of two clock cycles. The implementation of the RSD algorithm shown in Figure 4.2 is given below.

Our ADC operates in four different phases that implement the RSD algorithm given in Figure 4.2. The first two phases make up the m^{th} bit cycle, and the second two phases make up the $(m+1)^{th}$ bit cycle. In the first phase of the m^{th} bit cycle, the residue current of the m^{th} bit cycle $I_{res}(m)$ is computed. $I_{res}(m)$ is found by doubling the residue current of the previous bit cycle, subtracting a bias current, and adding or subtracting the reference current if the residue current of the previous bit cycle is less than the comparison level Q (Q_{m-1} = '0') or greater than the comparison level P (P_{m-1} = '1'), respectively. The newly computed residue current, $I_{res}(m)$, is stored in the PMOS current copier g_{m3}, and the output bits P_m and Q_m are found. P_m is set to 1 (0) if $I_{res}(m)$ is greater than (less than) the comparison level P. Q_m is set to 1 (0) if $I_{res}(m)$ is greater than (less than) the comparison level Q. In the second phase of the m^{th} bit cycle, $I_{res}(m)$ is stored in the PMOS regulated-cascode current copier g_{m4}.

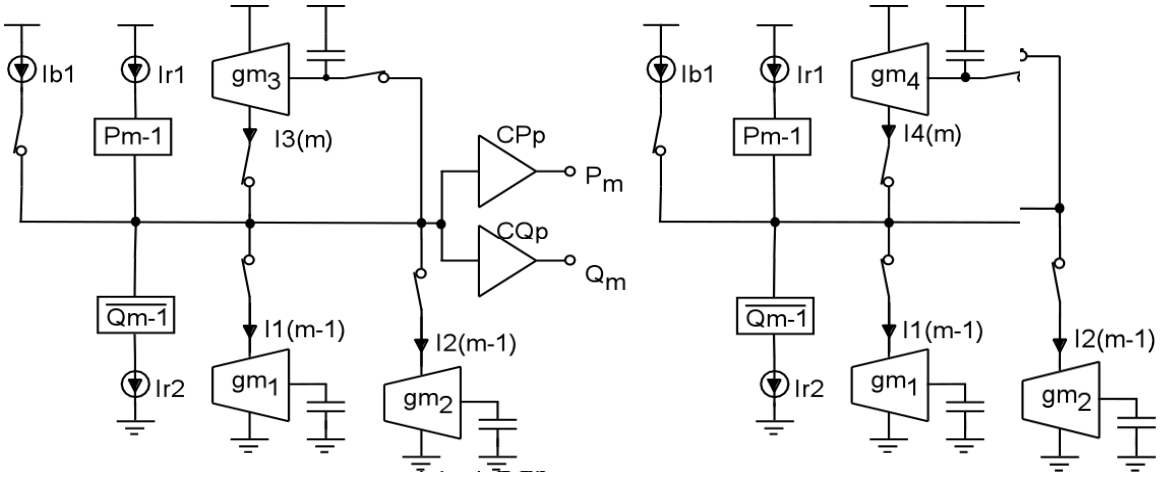
In the first phase of the $(m+1)^{th}$ bit cycle, the residue current of the $(m+1)^{th}$ bit cycle $I_{res}(m+1)$ is computed. $I_{res}(m+1)$ is also found by doubling the residue current of the previous bit cycle, subtracting a bias current, and adding or subtracting the reference current if Q_m = '0' or P_m = '1', respectively. $I_{res}(m+1)$ is stored in the NMOS current copier g_{m1}, and the output bits P_{m+1} and Q_{m+1} are set accordingly. In the second phase of the $(m+1)^{th}$ bit cycle, $I_{res}(m+1)$ is stored in the NMOS regulated-cascode current copier g_{m2}. The phases of operation are now described in detail.

4.3.1 First phase of the m^{th} bit cycle

In the first phase of the m^{th} bit cycle, $I_{res}(m)$ is computed and stored in current copier g_{m3}. Both copiers g_{m1} and g_{m2}, each storing $I_{res}(m-1)$, source their stored current to produce $2I_{res}(m-1)$. Also, the updated residue current of the previous bit cycle is obtained by subtracting the bias current I_{b1} and adding or subtracting the reference current from $2I_{res}(m-1)$. The output bits of the previous bit cycle determine if the reference currents I_{r1} and I_{r2} are to be subtracted or added, respectively. Specifically, if the residue current stored in the previous bit cycle was greater than the comparison level P, I_{r1} is subtracted from the current sourced by g_{m1} and g_{m2}; if the residue current of the previous bit cycle was less than the comparison level Q, I_{r2} is added to the current sourced by g_{m1} and g_{m2}. The operation performed in the m^{th} bit cycle can be expressed as

$$\begin{aligned} I_{res}(m) = I_3(m) &= I_1(m-1) + I_2(m-1) - I_{b1} - P_{m-1} I_{r1} + \overline{Q_{m-1}} I_{r2} \\ &= 2I_{res}(m-1) - I_{b1} - P_{m-1} I_{r1} + \overline{Q_{m-1}} I_{r2} \end{aligned},$$

where $I_1(m-1)$ and $I_2(m-1)$ are the currents sourced by g_{m1} and g_{m2}, respectively, and $I_3(m)$ is the current stored in g_{m3} in the m^{th} bit cycle. After $I_{res}(m)$ has been computed, P_m is set to 1 (0) if $I_{res}(m) > P$ ($I_{res}(m) \leq P$). Similarly, Q_m is set to 1 (0) if $I_{res}(m) > Q$ ($I_{res}(m) \leq Q$). The circuit diagram corresponding to the first phase of the m^{th} bit cycle is found in Figure 4.3 (a).



(a) **(b)**

Figure 4.3 (a) Phase One of the m[th] Bit Cycle **(b)** Phase Two of the m[th] Bit Cycle

4.3.2 Second phase of the m[th] bit cycle

In this phase, $I_{res}(m)$ is stored in g_{m4}. The phase is identical to the first phase of the m[th] bit cycle with the exceptions that $I_{res}(m)$ is stored in g_{m4} rather than g_{m3} and that the output bits P_m and Q_m are not computed. Note that the output bits have been computed in the previous phase. The circuit diagram of the second phase of the m[th] bit cycle is shown in Figure 4.3 (b).

4.3.3 First phase of the (m+1)[th] bit cycle

In first phase of the (m+1)[th] bit cycle, $I_{res}(m+1)$ is computed and stored in g_{m1}. Now, the current copiers g_{m3} and g_{m4} each source $I_{res}(m)$. The residue current of the (m+1)[th] bit cycle $I_{res}(m+1)$ is obtained as

$$\begin{aligned} I_{res}(m+1) = I_1(m+1) &= I_3(m) + I_4(m) - I_{b2} - P_m I_{r2} + \overline{Q_m} I_{r1} \\ &= 2I_{res}(m) - I_{b2} - P_m I_{r2} + \overline{Q_m} I_{r1} \end{aligned},$$

where $I_1(m+1)$ is the current stored in g_{m1} in the (m+1)[th] bit cycle. $I_3(m)$ and $I_4(m)$ are the currents sourced by g_{m3} and g_{m4}, respectively, and are equal to $I_{res}(m)$. The two outputs

P_{m+1} and Q_{m+1} are computed with respect to $I_{res}(m+1)$. The circuit configuration for the first phase of the $(m+1)^{th}$ bit cycle is given in Figure 4.4 (a).

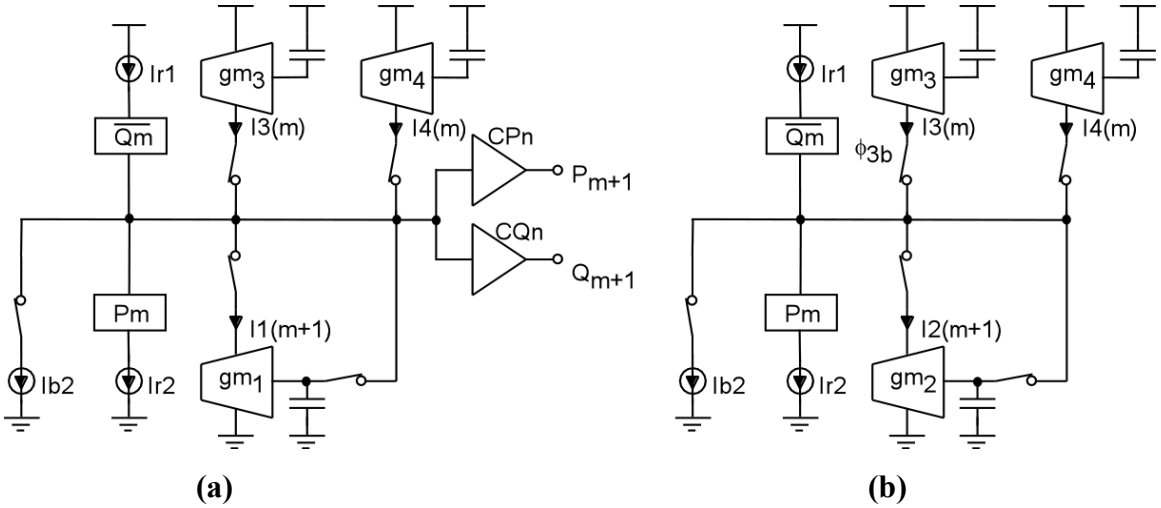


Figure 4.4 (a) Phase One of the $(m+1)^{th}$ Bit Cycle **(b)** Phase Two of the $(m+1)^{th}$ Bit Cycle

4.3.4 Second phase of the $(m+1)^{th}$ bit cycle

This phase is identical to the first phase of the $(m+1)^{th}$ bit cycle with the exception that $I_{res}(m+1)$ is stored by g_{m2} rather than g_{m1} and that the output bits are not computed. The circuit diagram of the second phase of the $(m+1)^{th}$ bit cycle is shown in Figure 4.4 (b).

The operations described for the m^{th} and $(m+1)^{th}$ bit cycles are alternately repeated to generate an n-bit resolution. The procedure for the $(m+2i)^{th}$ bit cycle is identical to the m^{th} bit cycle, and the procedure for the $(m+1+2i)^{th}$ bit cycle is identical to the $(m+1)^{th}$ bit cycle. Further details of the operation of the ADC of Figure 4.1 are given in the next section.

4.3.5 Details of operation

In the first bit cycle, a positive input current I_{in} is stored in current copier g_{m1} and then stored in current copier g_{m2} in two consecutive clock cycles. Additionally, the two

output bits P_1 and Q_1 are set during the first phase of the first bit cycle. P_1 is set to 1 (0) if $I_{in} > P$ ($I_{in} \leq P$), and Q_1 is set to 1 (0) if $I_{in} > Q$ ($I_{in} \leq Q$). Note that the MSB and the next MSB of the output word are generated from P_1 and Q_1. The circuit configurations of the first bit cycle are given in Figure 4.5

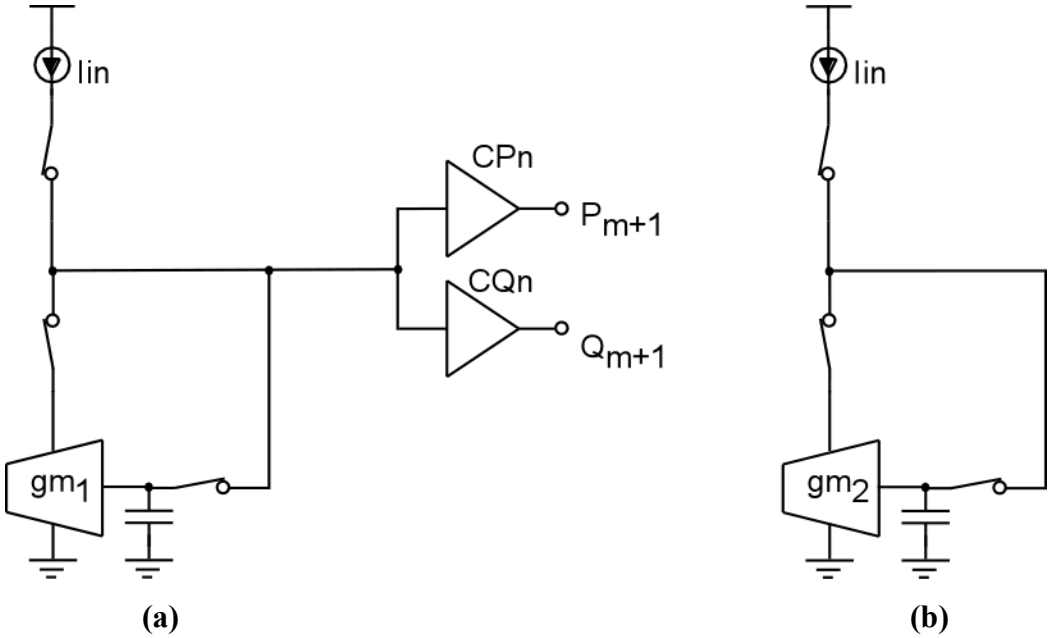


Figure 4.5 **(a)** Phase One of the First Bit Cycle **(b)** Phase Two of the First Bit Cycle

The second bit cycle is identical to the m^{th} bit cycle for m = 2, where the residue current $I_{res}(1)$ is stored in g_{m1} and g_{m2}. The third bit cycle is identical to the $(m+1)^{th}$ bit cycle. The m^{th} and $(m+1)^{th}$ bit cycles alternately repeat to generate an n-bit word. Details of operations involved in this procedure are explained below.

Multiplying the residue current, I_{res}, by two is accomplished by storing the residue current in two NMOS (PMOS) current copiers and then simultaneously sourcing the stored currents to a PMOS (NMOS) current copier. Since one clock cycle is required to copy a current, two clock cycles are required to store the residue current in two current copiers.

The parallel comparisons required by the RSD algorithm are performed in the first phase of every bit cycle. As noted in Section 4.3, the comparisons are made with P and Q rather than 2P and 2Q. If the residue current is greater than the reference current P, the

output bit P is set to a logic '1'; otherwise, it is set to '0'. The output bit Q is determined in the same manner. These logic values indicate if the reference current is added or subtracted in the next bit cycle.

The comparison levels P and Q are set to $^5/_4\ I_{ref}$ and $^3/_4\ I_{ref}$, respectively. The comparison levels are $+I_{ref}/4$ and $-I_{ref}/4$ offset by the reference current, I_{ref}. The comparison levels are offset since only positive residue currents are used in the ADC. These comparison levels allow large offsets to exist in the residue current as shown in Section 3.3.2.

The dynamic range of the ADC determines the values of the reference and bias currents. The RSD algorithm causes the dynamic range to be twice the reference current, I_{ref}. The dynamic range of our ADC is 0 μA to 90 μA due to bias conditions of the regulated-cascode current copiers. Thus, the reference currents I_{r1} and I_{r2} are set to 45μA.

The parallel comparisons are made between the gate-source voltage of the memory transistor of a current copier and reference voltages corresponding the comparison levels P and Q. The gate-source voltage of a current copier in Figure 3.13 is the capacitor voltage. A first-approximation of the reference voltage can be determined by the drain-source current equation

$$I_{ds} = \mu C_{ox} \frac{W}{L}\left(\left(V_{gs} - V_t\right)V_{ds} - \frac{V_{ds}^{\ 2}}{2} \right),$$

where I_{ds} is J+i. Note that the memory transistor operates in triode mode. In practice the reference voltages are determined through HSPICE simulation to circumvent the inaccuracy of the drain-source current equation. Also, note that the gate-source voltage of the PMOS current copiers differs from the gate-source voltage of the NMOS current copiers since the source voltages and threshold voltages of the two types of current copiers differ. Thus, four reference voltages and comparators are necessary. The estimated bias voltages computed by the drain-source current equation and the voltages found using HSPICE are given in Table 4.1. P_n and Q_n refer to the reference voltages for the NMOS current copiers, and P_p and Q_p refer to the reference voltages for the PMOS current copiers. For the NMOS reference voltages, $\mu_n C_{ox} W/L = 1185\ \mu A/V^2$, $V_{ds} = 0.61$ V, $V_s = 0$, and $V_t = 0.58$ V; for the PMOS reference voltages, $\mu_p C_{ox} W/L = 750\ \mu A/V^2$, $V_{ds} = -0.8$ V, $V_s = 3.3$ V, and $V_t = -0.76$ V.

Table 4.1 Reference Voltages for Comparators

Reference Voltage	J+i (μA)	Estimate (V)	As Calculated with HSPICE (V)
$\mathbf{P_n}$	256.25	0.93	1.26
$\mathbf{Q_n}$	233.75	0.90	1.21
$\mathbf{P_p}$	256.25	2.11	1.56
$\mathbf{Q_p}$	233.75	2.15	1.61

Furthermore, the input node of the comparator chosen as the reference voltage for the comparison of the PMOS gate-source voltage differs from the input node chosen as the reference voltage for the comparison of the NMOS gate-source voltage (refer to Figure 3.9). The difference is necessary since the gate-source voltage of an NMOS transistor increases as the drain-source current increases, while the gate-source voltage of a PMOS transistor decreases as the drain-source current increases. As a result, the reference voltage of the comparators used for the NMOS current copiers is applied to the Vin+ node, and the reference voltage of the comparators used for the PMOS current copiers is applied to the Vin- node. The implementation of the reference voltage generator is described in Section 4.6.

Subtracting and adding the reference currents, I_{r1} and I_{r2}, is accomplished by sourcing the reference current in the appropriate direction. The switches ϕ_{Ir1} and ϕ_{Ir2} controlled by the logic values P and Q determine whether the reference currents are added or subtracted.

A bias current is subtracted every bit cycle with the exception of the first bit cycle. The bias current, I_b, is subtracted to create an offset in the residue current. The bias current necessary to create a current range of –45 μA to 45 μA from the input range of 0 μA to 90 μA is 45 μA. Hence, both bias currents, I_{b1} and I_{b2}, are set to 45 μA. A summary of the comparison levels P and Q, the reference currents, and the bias currents are given in Table 4.2.

Table 4.2 Summary of the Currents of the ADC

	Current (μA)	Corresponding Voltage (V)
I_{b1}, I_{b2}	45	
I_{r1}, I_{r2}	45	
P_n	56.25	1.26
Q_n	33.75	1.21
P_p	56.25	1.56
Q_p	33.75	1.61
Input Range	0 - 90	

This section discusses the proposed ADC architecture and the methods used to execute the RSD algorithm. The implementation of the components shown in Figure 4.1 is described next.

4.4 Regulated-Cascode Current Copier

In this section, we review the design considerations of the regulated-cascode current copier. The regulated-cascode current copier is the major computational unit of our ADC architecture and limits the accuracy and speed of our ADC. The design of the regulated-cascode current copier is considered in detail in this section. The design considerations of the regulated-cascode current copier include the sizes of the transistors of the current copier, the operating point, and charge injection. We describe the implementation of the NMOS regulated-cascode current copiers first and then briefly mention the PMOS regulated-cascode current copiers later.

4.4.1 Transistor size considerations

The sizes of the transistors of the regulated-cascode current copier are important in the determining the speed and accuracy of the current copier. The memory transistor, its gate capacitance, and the size of the regulating transistor determine the speed of the

current copier, while accuracy is largely determined by charge injection considerations. The sizes of the regulating and cascode transistors also affect the output resistance of the regulated-cascode current copier and, consequently, its accuracy. The circuit diagram of the regulated-cascode current copier is duplicated in Figure 4.6 and is discussed in the following.

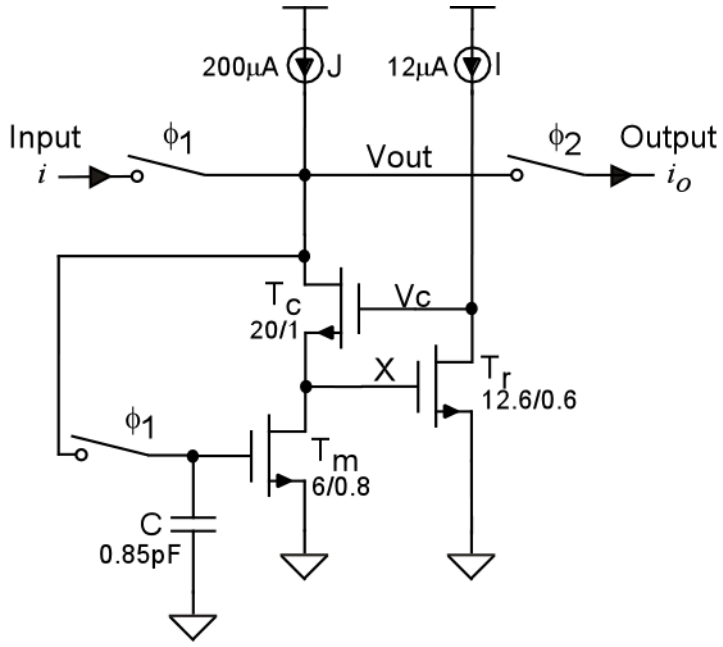


Figure 4.6 NMOS Regulated-Cascode Current Copier

The time constant of the regulated-cascode current copier when storing current can be shown to be

$$\tau \approx \frac{C}{g_m},$$

where C is the size of the capacitor of the current copier and g_m is the small-signal input conductance of the memory transistor [27]. The small-signal input conductance is given by

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ds}$$

for triode operation of the memory transistor, T_m. Thus, the speed of the regulated-cascode current copier increases as the W/L ratio of the memory transistor increases and

the capacitor size decreases. However, the error introduced by charge injection also increases in proportion to the size of the memory transistor and is inversely proportional to the size of the capacitor. Thus, the W/L ratio and the size of the gate capacitance of the memory transistor is a tradeoff between the speed and accuracy of the regulated-cascode current copier.

The time constant τ of the regulated-cascode current copier is chosen to be 1.2 ns where the gate capacitance of the memory transistor is 0.85 pF and g_m is 728 μA/V. The capacitor was implemented using double-poly layers where the unit size capacitance is $8.9\text{x}10^{-4}$ pF/μm^2. The capacitance of 0.85 pF is obtained with a WL = 30.9 μm x 30.9 μm capacitor area. The value for g_m is obtained with $\mu_n C_{ox}$=158 μA/V^2, W = 6 μm, L = 0.8 μm, and V_{ds} = 0.6 V. Discussion of the choice of V_{ds} is given in Section 4.4.2. The size of the memory transistor and the gate capacitance of the memory transistor were fine tuned using HSPICE to minimize the settling time of the current copier while maintaining accuracy. This time constant gives a reasonable settling time of the regulated-cascode current copier while maintaining a practical accuracy.

The size of the regulating transistor, T_r, is determined by the settling characteristics of the regulated-cascode current copier when sourcing current. When the regulated-cascode current copier is sourcing current, it acts as a regulated-cascode current source. Lima showed that a regulated-cascode current source is a dominant-pole system under the condition that

$$\frac{g_{mc}}{g_{mr}} >> \frac{C_{gsr}}{\alpha^2 C_{gsc}},$$

where g_{mc} and g_{mr} are the small-signal input conductances of the cascode and regulating transistors, respectively, and C_{gsr} and C_{gsc} are the gate-source capacitances of the regulating and cascode transistors, respectively. The parameter α is given as

$$\alpha \approx \frac{1}{g_{mc} r_{dsc}} + \frac{1}{g_{mc} r_{dsm}} + 1,$$

where r_{dsc}, and r_{dsm} are the output resistances of the cascode transistor and the memory transistor, respectively [16]. Since the gate-source capacitance of a transistor is proportional to the gate area and the small-signal input conductance is proportional to the drain-source current, the requirement for a dominant-pole system can be met by using a

regulating transistor whose size is on the order of the cascode transistor size. The size meets the requirement since the drain-source current and, consequently, the small-signal input conductance of the regulating transistor is much smaller than that of the cascode transistor.

HSPICE was used to fine tune the settling behavior of the regulating-cascode current copier since the output resistance of a transistor is difficult to accurately define. Also, note that the equations are estimates. The regulating transistor is chosen to have approximately the same W/L ratio (12 μm /0.6 μm) as the cascode transistor, but a smaller channel length (which is 0.6 μm) is used to minimize the settling time of the current copier when sourcing current. The channel length of the regulating transistor is still relatively long in order to increase its output resistance and reduce the transmission error of the regulated-cascode current copier. The parameters related to the regulating transistor were found using HSPICE and are as follows:

$$
\begin{aligned}
W &= 12.6\ \mu m \\
L &= 0.6\ \mu m \\
g_{mc} &= 1.19\ mA/V \\
g_{mr} &= 166\ \mu A/V \\
r_{dsc} &= 63\ k\Omega \\
r_{dsm} &= 11\ k\Omega \\
\alpha &= 1.09 \\
C_{gsr} &= 21\ fF \\
C_{gsc} &= 70\ fF
\end{aligned}
\qquad .
$$

Note that the condition for a dominant-pole system has been met.

It is shown in the next section that the W/L ratio of the cascode transistor is set to maximize the dynamic range of the current copier under the given bias conditions. Furthermore, to increase the output resistance of the cascode transistor, a long-channel cascode transistor is used to reduce the transmission error.

4.4.2 Operating point

The operating point of the regulated-cascode current copier is largely determined by the conditions on the operating modes of its transistors and the size of the memory

transistor. These aspects of the bias point of the regulated-cascode current copier are discussed in this section.

The operating regions of the transistors of the regulated-cascode current copier chiefly set the operating point. To sustain the small transmission error of the regulated-cascode current copier as given in Section 3.5.3, *the cascode and regulating transistors must maintain saturation operation*. Furthermore, *the effects of charge injection are minimized when the memory transistor operates in triode mode*. The justification of triode operation of the memory transistor is discussed later.

For an NMOS transistor, the channel of the transistor is inverted and is conducting current if

$$V_{gs} \geq V_t ,$$

where V_{gs} is the gate-source voltage and V_t is the threshold voltage. For strong inversion, the gate-source voltage of the transistor must exceed the threshold voltage by approximately 0.2 V [30]. If a transistor is not in strong inversion, the first-order current equations are fairly inaccurate [12]. Saturation operation is assured if

$$V_{ds} \geq V_{gs} - V_t ,$$

where V_{ds} is the drain-source voltage of the transistor. If the saturation condition is not met, then an NMOS transistor is in triode mode. Also, the first-order drain-source current equations for saturation and triode operation, respectively, are

$$I_{ds} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_t\right)^2 ,$$

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left(\left(V_{gs} - V_t\right)V_{ds} - \frac{{V_{ds}}^2}{2}\right).$$

Momentarily ignoring the strong inversion requirement, the limits on the node voltages as imposed by the cascode transistor, T_c, the regulating transistor, T_r, and the memory transistor, T_m, are as follows:

$$
\begin{aligned}
T_c \text{ Saturation Condition}: &\quad V_{out} \geq V_c - V_t \\
T_c \text{ On Condition}: &\quad V_c \geq X + V_t \\
T_r \text{ Saturation Condition}: &\quad V_c \geq X - V_t \\
T_r \text{ On Condition}: &\quad X \geq V_t \\
T_m \text{ Triode Condition}: &\quad V_{out} \geq X + V_t \\
T_m \text{ On Condition}: &\quad V_{out} \geq V_t
\end{aligned}
$$

In order to maintain saturation operation of the regulating transistor, its gate voltage must be less than the gate voltage of the cascode transistor by at least one threshold voltage. In order to ensure the maximum dynamic range of the regulating transistor and to minimize power dissipation, the gate voltage of the regulating transistor should be set to nearly the threshold voltage, V_t. Under this condition, the regulating transistor is in weak inversion but is guaranteed to be in saturation mode, regardless of the gate voltage of the cascode transistor. Weak inversion operation is acceptable since the sole purpose of the regulating transistor is to maintain a constant gate voltage. The bias point also assures the minimum power dissipation for the regulating transistor since the bias current I need only be the minimum current for saturation operation as governed by the size of the transistor. Due to the advantages of this bias point, the bias current I is set to the minimum current needed for saturation operation of the regulating transistor. For our ADC the bias current I is set to 12 μA, producing a gate-source voltage, X, of 0.61 V (refer to Figure 4.6).

Under the condition that the gate voltage of the regulating transistor is the threshold voltage, the limiting conditions on the node voltages of the regulated-cascode current copier are

$$
\begin{aligned}
T_c \text{ Saturation Condition}: &\quad V_{out} \geq V_t + 0.2\,V \\
T_c \text{ On Condition}: &\quad V_c \geq 2V_t + 0.2\,V \\
T_m \text{ Triode Condition}: &\quad V_{out} \geq 2V_t
\end{aligned}
$$

Given the size of the memory transistor, the condition that the voltage at the gate of the memory transistor exceeds twice the threshold voltage determines the minimum bias current J. The condition determines the lower bound of the dynamic range of the current copier. Since the copier should be able to store a 0 μA signal current and the memory transistor operates in triode mode, the first-order approximation of the minimum bias current J is given by

$$J = \mu_n C_{ox}\left(\frac{W}{L}\right)_m\left(V_t^{\,2} - \frac{V_t^{\,2}}{2}\right),$$

where $(W/L)_m$ is the W/L ratio of the memory transistor. A higher bias current could be used but would offer no advantage. To the contrary, a larger bias current J would cause the minimum gate voltage of the memory transistor to be larger than necessary. As a result, the lower bound of the dynamic range would be limited since the acceptable voltage at the output node of the regulated-cascode current copier would be increased. Thus, the minimum bias current J is used to minimize power dissipation and maximize the dynamic range. As governed by the chosen size of the memory transistor, the bias current J of the current copier is 200 μA for $\mu_n C_{ox}$ = 158 μA/V^2, W = 6 μm, L = 0.8 μm, and V_t = 0.58 V.

To ensure the maximum dynamic range of the regulated-cascode current copier, the circuit is designed to meet the minimum conditions on the voltage at its output node. The W/L ratio of the cascode transistor is chosen such that saturation operation is maintained for the smallest possible gate voltage for the given minimum bias current. Choosing this W/L ratio allows the smallest possible voltage at the output node of the regulated-cascode current copier. Consequently, the W/L ratio of the cascode transistor can be determined by the bias current J and the condition that its gate voltage exceeds twice the threshold voltage by 0.2 V. The size of the cascode transistor is determined as follows:

$$J = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_c (Vc - X - Vt)^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_c (0.2V)^2$$
$$\Rightarrow \left(\frac{W}{L}\right)_c = \frac{2J}{(0.2V)^2 \mu_n C_{ox}},$$

where $(W/L)_c$ is the W/L ratio of the cascode transistor. When the cascode transistor is chosen to have this size, the voltage at the output of the current copier can be as low as 0.2 V above the threshold voltage when the regulated-cascode current copier is sourcing current. Consequently, this size gives the maximum dynamic range of the regulated-cascode current copier.

While this equation does allow for the maximum dynamic range of the regulated-cascode current copier, a slightly smaller value is used to prevent the cascode transistor

from entering weak inversion under process variation. Since both the mobility and gate-source voltage varies with process, we can assume that the gate-source voltage can be smaller than 0.2 V for different processes. For instance, if the mobility of the cascode transistor is larger than that assumed for our calculations, the gate-source voltage is smaller than 0.2 V for a constant drain-source current and transistor size. Consequently, to eliminate the possibility of the cascode transistor entering weak inversion, the size of the cascode transistor is chosen to correspond to a gate voltage of approximately $2V_t$ + 0.36 V rather than $2V_t$ + 0.2 V.

Using the $(W/L)_c$ equation where the effective gate-source voltage ($V_c - X - V_t$) is 0.36 V rather than 0.2 V, the size of the cascode transistor is 20 μm/1 μm under J = 200 μA and $\mu_n C_{ox}$ = 158 μA/V^2. A fairly long-channel device is used to increase the output impedance of the transistor, reducing the transmission error of the regulated-cascode current copier (refer to Section 3.5.3).

4.4.3 Charge injection considerations

Charge injection is the major source of error in switched-current designs. Charge injection occurs when the switch at the gate of the memory transistor is turned off. Charge injection creates an error in the stored gate voltage of the memory transistor, which in turn creates an error current when the memorized current is sourced. In our ADC architecture, charge injection is alleviated by using dummy switches and by operating the memory transistor in triode mode.

When transistors turn off, charge is injected into the connected circuit. Most of the charge injected is due to the channel charge of the MOSFET, while a smaller portion is due to the overlap capacitance of the transistor. The charge injection creates errors when switched capacitors are used to store voltage. Since a MOSFET switch operates in triode mode when it is turned on, no voltage drop exists across the switch. As a result, the channel charge due to the gate capacitance of the switch is given by

$$Q_s = C_s(V_{gs} - V_t),$$

where C_s is the gate capacitance of the switch. Since the gate voltage of a switch is a digital signal, the gate voltage is Vdd for an NMOS switch that is turned on, giving

$$Q_s = C_s(Vdd - V_c - V_t),$$

where V_c is the voltage stored on the storage capacitor. If the digital signal controlling the gate voltage of the switch has a steep slope, approximately half of the channel charge of the switch is discharged into the storage capacitor C (refer to Figure 4.6). For an NMOS switch, the charge injected is negative. Consequently, the charge on the storage capacitor is decreased by approximately $Q_s/2$ [12].

Dummy switches alleviate charge injection by discharging a positive charge approximately equal to the injected charge of the primary switch. As a consequence, the channel charges of the primary switch and the dummy switch cancel. Specifically, the dummy switch injects a charge $+Q_s/2$ while the primary switch injects a charge $-Q_s/2$. Thus, the injected charge is ideally zero. To accomplish charge cancellation, the dummy switch is half the size of the primary switch, and the clock signal of the dummy switch is the inverted form of the clock signal of the primary switch. The circuit configuration used to implement a dummy switch is shown in Figure 4.7.

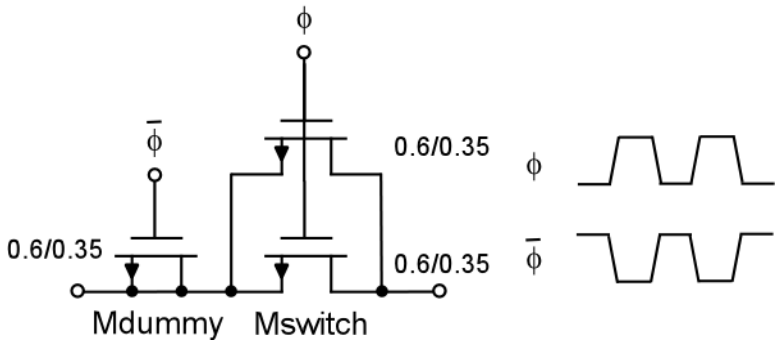


Figure 4.7 Dummy Switch Circuit Configuration

In the figure, Mswitch consists of two parallel MOSFETs that have equal W/L ratios. Also, Mdummy is a MOSFET with the same W/L ratio. Thus, Mdummy is half the size of Mswitch.

While the dummy switch ideally eliminates charge injection, some charge injection is still present. Charge injection is not completely eliminated since the clock waveforms are usually not fast enough to produce a charge injection of exactly $Q_s/2$ [12]. Furthermore, the charge injection due to overlap capacitance is not alleviated. However,

dummy switches greatly reduce the amount of charge injection. Consequently, dummy switches are used in the regulated-cascode current copier at the gate capacitor of the memory transistor.

Another method used to reduce the effect of charge injection is operating the memory transistor of the regulated-cascode current copier in the triode mode. This approach renders a portion of the charge injected into the gate capacitor of the memory transistor a constant. The error in the stored current of the memory transistor is given by

$$\begin{aligned} i_{error} &= \frac{\alpha C_s \left(Vdd - V_{gs} - V_t\right)}{C} \frac{\Delta I_{ds}}{\Delta V_{gs}} \\ &= \frac{\alpha C_s \left(Vdd - V_{gs} - V_t\right)}{C} g_m \end{aligned},$$

where α is the portion of the channel charge of the switch injected into the gate capacitor, V_{gs} is the gate-source voltage stored on the gate capacitance, I_{ds} is the drain-source current of the memory transistor, and g_m is the small-signal input conductance of the memory transistor. The equation indicates that the error current is directly proportional to the small-signal input conductance g_m of the memory transistor and is inversely proportional to the gate capacitance. The small-signal input conductance is given by

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ds}$$

for triode operation of the memory transistor. Since the regulating transistor of the current copier (refer to Figure 4.6) forces V_{ds} of the memory transistor to be constant, g_m is constant. As a result, the error current can be separated into constant and signal-dependent portions and is given by

$$\begin{aligned} i_{error} &= \frac{\alpha C_s Vdd g_m}{C} - \frac{\alpha C_s V_t g_m}{C} - \frac{\alpha C_s V_{gs} g_m}{C} \\ &= K - \frac{\alpha C_s V_{gs} g_m}{C} \end{aligned},$$

where K is a constant. Since the RSD algorithm is tolerant of constant offsets, operating the memory transistor in the triode mode reduces the detrimental effects of charge injection in our ADC architecture. Thus, the memory transistor of the regulated-cascode current copier is biased to operate in the triode region of operation to alleviate charge injection errors.

4.4.4 Current Sources

The remaining issue of the regulated-cascode current copier is the implementation of the bias current sources I and J. The bias current I is implemented with a single PMOS transistor whose gate is connected to a bias voltage. This transistor is a very long-channel device so that it maintains an approximately constant drain-source current, regardless of its drain voltage. Since this transistor is not in the feedback loop of the cascode and regulating transistors, the large parasitics associated with it are acceptable. The bias current I is implemented with a simple transistor since the bias current I is used only to force the gate voltage of the regulating transistor to be an approximately constant voltage. Since the gain of the regulating transistor ($\mu_n C_{ox}(W/L)_r$) is large, a small change in the bias current I causes a much smaller change in its gate-source voltage. Specifically, if the bias current I changes by ΔI, the gate-source voltage of the regulating transistor changes by

$$\sqrt{\frac{\Delta I}{\mu_n C_{ox}\left(W/L\right)_r}},$$

as governed by the drain-source current equation. The current source I is shown in Figure 4.8. The voltage Vbp is an external voltage for our ADC.

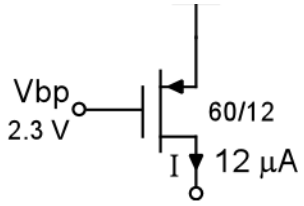


Figure 4.8 Current Source I of the NMOS Regulated-Cascode Current Copier

While the current source I is implemented with a very long-channel device, the bias current J is implemented with a regulated-cascode current source. The bias current J is required to be accurate since the value has a direct consequence on the current stored and sourced by the current copier.

Assume that J_s is the value of the current source J when the current copier is sourcing current and J_c is the value of the current source J when the current copier is storing current. The stored current is J_c+i (refer to Section 3.5.3). Also, the sourced current is J_s-(J_c+i), which is ideally –i. However, if the value of J changes when the current copier sources current, the sourced current is no longer –i but is –i+ΔJ, where ΔJ is J_s-J_c. Thus, if the value of the current source J changes, an error is introduced into the signal current i. To avoid errors, the bias current J is implemented as a PMOS regulated-cascode current source. The implementation of the regulated-cascode current source is discussed in Section 4.5.

4.4.5 Layout and verification of operation

An NMOS regulated-cascode current copier is laid out in a triple-metal, double-poly, 0.35 μm CMOS technology. As noted earlier, the capacitor is implemented using double-poly layers. The layout of the current copier is shown in Figure 4.9. The area of the current copier is 82 x 137 μm^2.

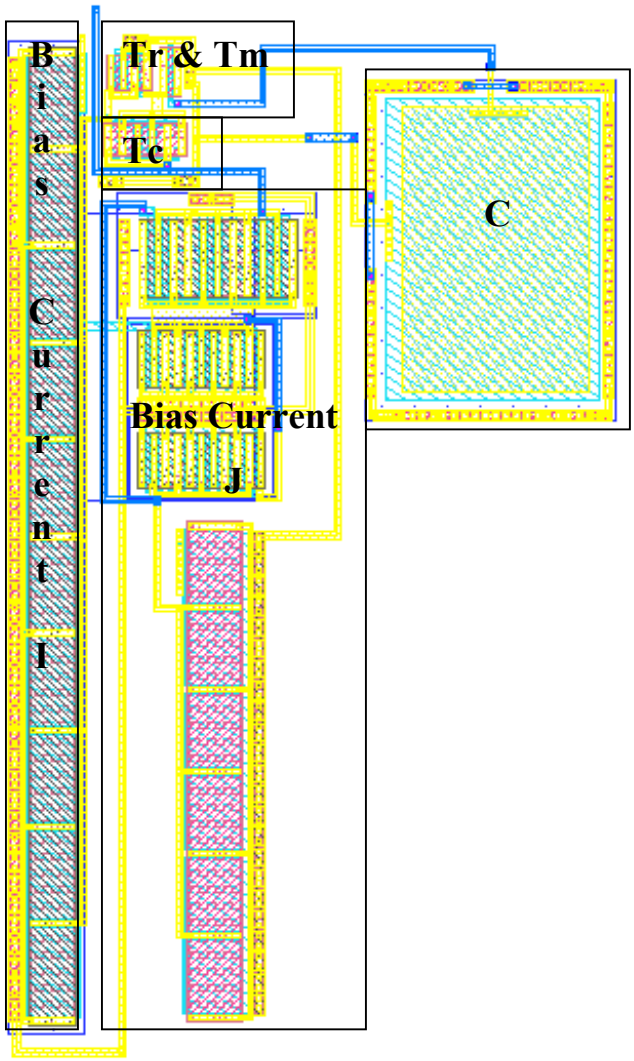


Figure 4.9 Layout of the NMOS Regulated-Cascode Current Copier

The operation of the current copier was verified by simulating the ADC architecture of Figure 4.1 with Avant! HSPICE using ideal reference and bias currents and no comparators. Thus, any errors present are due solely to the current copiers. The simulation results are shown in Figure 4.10.

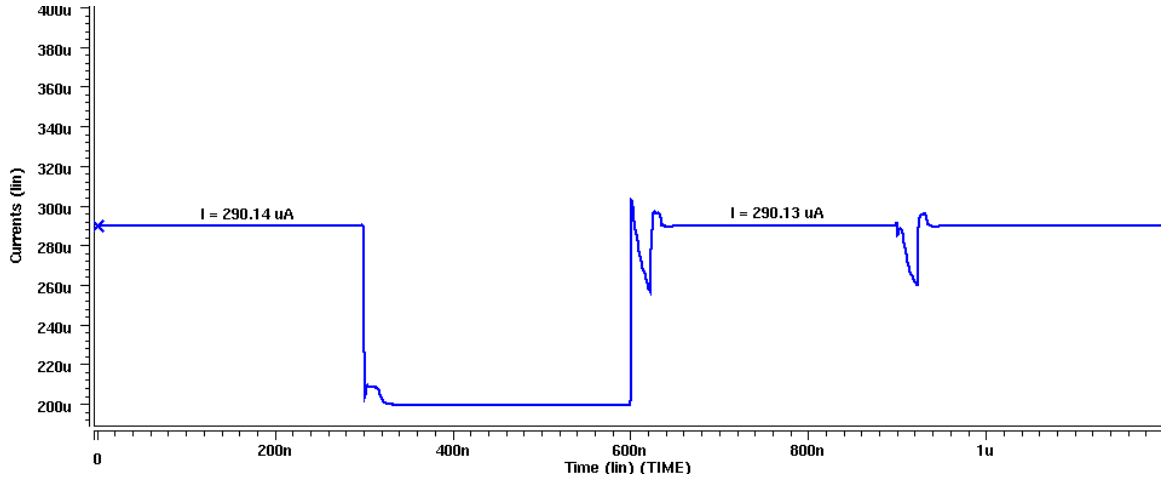


Figure 4.10 Simulation Results for the NMOS Regulated-Cascode Current Copier

The vertical axis of the figure is the current being sourced by the memory transistor. The y-axis is time in nanoseconds (ns). The signal current is stored in the NMOS current copier until 300 ns. The signal current is sourced at 600 ns. Between 300 ns and 600 ns, the switch at the drain of the current copier is open. Thus, at this time the memory transistor is sourcing the 200 µA bias current J. The current stored is 290.14 µA, and the current sourced is 290.13 µA. The simulation results indicate the current copier is 12-bit accurate since the difference between the stored and sourced currents is less than ½ I_{LSB} (90 µA/2^{12}).

4.4.6 Implementation of PMOS current copiers

A PMOS current copier is the dual of an NMOS current copier. The sizes of the transistors are adjusted according to the bias point of the PMOS current copier and the mobility of holes, μ_p. The PMOS current copier used in our ADC is shown in Figure 4.11.

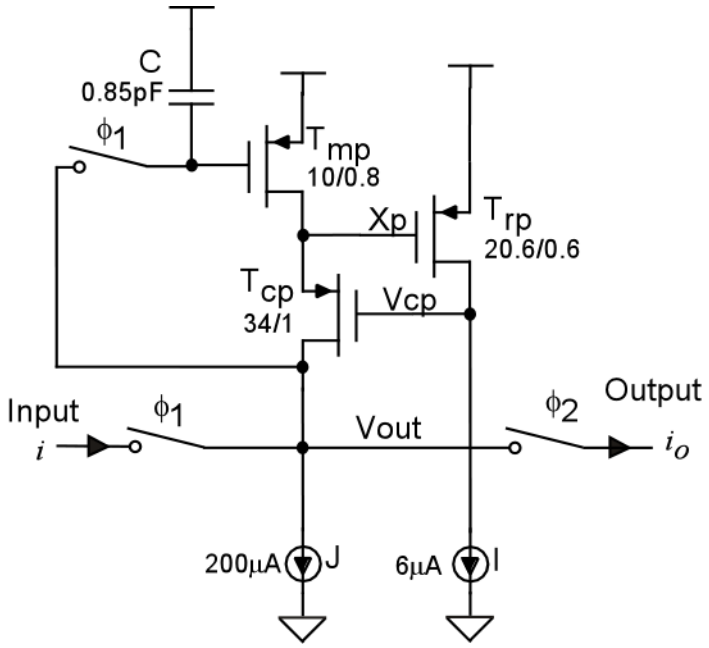


Figure 4.11 PMOS Regulated-Cascode Current Copier

The bias point of the PMOS current copier differs from that of the NMOS current copier since the source voltage of the memory transistor, T_{mp}, and the regulating transistor, T_{rp}, is the supply voltage, Vdd, rather than ground. Furthermore, the threshold voltage of P-type MOSFET is not equal to the threshold voltage of an N-type MOSFET. However, the bias point was determined in a similar manner. Using the methods discussed for determining the operating conditions of the NMOS regulated-cascode current copiers, the limiting conditions for the PMOS current copier are

$$\begin{aligned} T_{cp}\ Saturation\ Condition: &\quad V_{out} \le Vdd + V_{tp} - 0.2V \\ T_{cp}\ On\ Condition: &\quad V_{cp} \le Vdd + 2V_{tp} - 0.2V\ . \\ T_{mp}\ Triode\ Condition: &\quad V_{out} \le Vdd + 2V_{tp} \end{aligned}$$

The bias current J and the bias current I are found according to these conditions. The parameters of the PMOS regulated-cascode current copier are given in Table 4.3.

Table 4.3 Parameters of the PMOS Regulated-Cascode Current Copier

Memory Transistor	
$\mu_p C_{ox}$	60 μA/V^2
g_m	600 μA/V
$V_{ds} \approx V_t$	-0.8 V
C	0.85 pF
τ	1.4 ns
$(W/L)_m$	10 μm/0.8 μm
J	200 μA
Regulating Transistor	
$(W/L)_r$	20.6 μm/0.6 μm
g_{mc}	770 μA/V
g_{mr}	104 μA/V
r_{dsc}	80 kΩ
r_{dsm}	26 kΩ
α	1.07
C_{gsr}	33 fF
C_{gsc}	120 fF
I	6 μA
Cascode Transistor	
$(W/L)_c$	34 μm/1 μm

The switches for the memory transistor are implemented in the same manner as that of the NMOS current copier using PMOS switches rather than NMOS switches. The switch is shown in Figure 4.12.

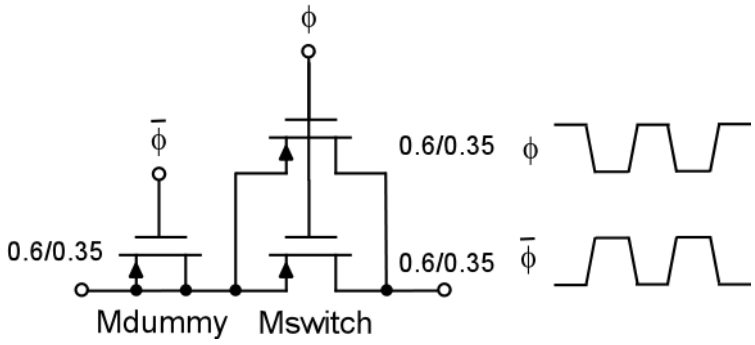


Figure 4.12 PMOS Dummy Switch Circuit Configuration

The switch sizes are minimum in order to alleviate charge injection.

The current sources of the PMOS current copier are implemented in the same manner as the current sources of the NMOS current copier. The current source I is a single, very long-channel NMOS transistor, and the current source J is an NMOS regulated-cascode current source. The implementation of the current source I is shown in Figure 4.13. The implementation of the regulated-cascode current source is discussed in Section 4.5. The voltage Vb is an external voltage for our ADC.

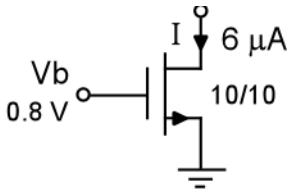


Figure 4.13 Current Source I of the PMOS Regulated-Cascode Current Copier

Finally, we discuss the layout and verification of the PMOS current copier. The layout of the PMOS current copier is given in Figure 4.14. The area of the current copier is 60 x 133 μm^2. The PMOS current copier was also verified by simulating the ADC architecture of Figure 4.1 using ideal reference and bias currents and no comparators. The simulation results are shown in Figure 4.15.

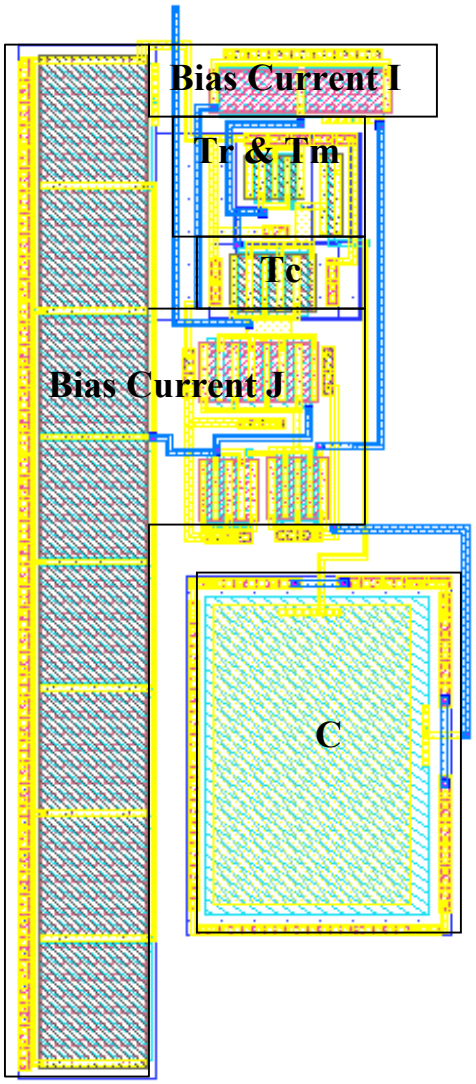


Figure 4.14 Layout of the PMOS Regulated-Cascode Current Copier

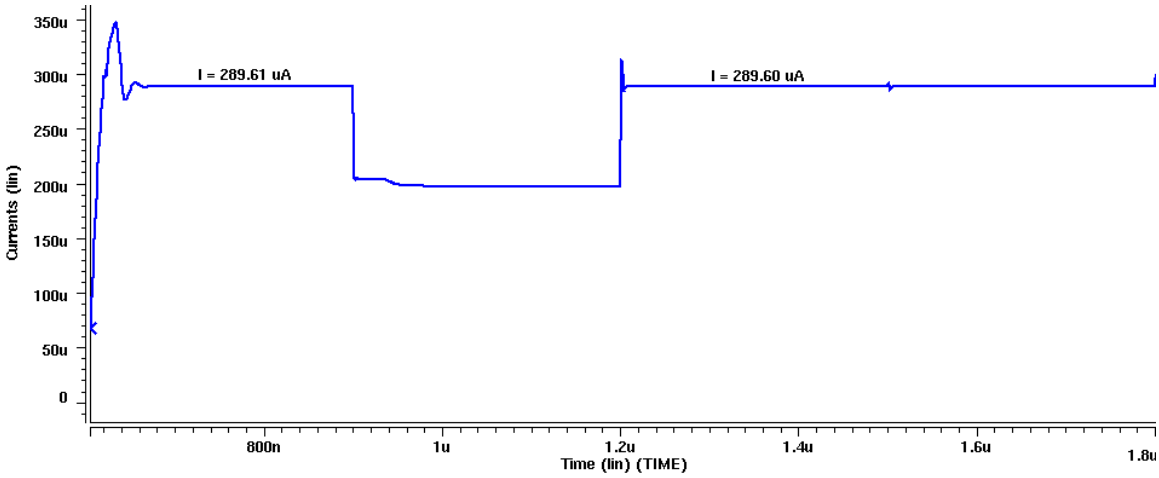


Figure 4.15 Simulation Results for the PMOS Regulated-Cascode Current Copier

The vertical axis of the figure is the current being sourced by the memory transistor. The horizontal axis is time in nanoseconds. The signal current is stored in the PMOS current copier until 900 ns. The signal current is sourced at 1.2 µs. Between 900 ns and 1.2 µs, the switch at the drain of the current copier is open. Thus, at this time the memory transistor is sourcing the 200 µA bias current J. The current stored is 289.61 µA, and the current sourced is 289.60 µA. The simulation results indicate the PMOS current copier is 12-bit accurate since the difference between the stored and sourced currents is less than ½ I_{LSB}.

4.4.7 Dynamic range of the current copiers

As mentioned in Section 4.4.2, the lower limit of the dynamic range of the current copiers is bound by the triode operation of the memory transistor. However, the upper limit of the dynamic range is imposed by the conditions for saturation operation of the cascode transistors of the PMOS and NMOS current copiers.

The upper limit of the dynamic range is limited by the conditions

$$T_c \ \textit{Saturation Condition}: \quad V_{out} \geq V_c - V_t$$
$$T_{cp} \ \textit{Saturation Condition}: \quad V_{out} \leq V_{cp} - V_{tp}.$$

As the residue current increases, V_c increases, and V_{cp} decreases. Consequently, an upper bound of the residue current is reached. A mathematical solution for the dynamic range is difficult to produce; therefore, the dynamic range of the current copiers was found through HSPICE simulations. The upper bound of the dynamic range was found to be 90 μA for our ADC. Hence, the total dynamic range of the ADC is 0 μA to 90 μA.

4.5 Regulated-Cascode Current Sources

Regulated-cascode current sources are used to implement the current sources of the ADC architecture of Figure 4.1 and the bias current J of the regulated-cascode current copiers. As expected, several design considerations of the regulated-cascode current sources are similar to those of the regulated-cascode current copiers. Consequently, only the aspects that differ from the regulated-cascode current copiers are presented in this section. These aspects include the operating point and the dynamic range of the regulated-cascode current source.

We discuss the implementation of the NMOS regulated-cascode current source first. NMOS regulated-cascode current sources are used to implement the reference current I_{r2} and the bias current I_{b2} of the ADC architecture of Figure 4.1. Also, an NMOS regulated-cascode current source is used to implement the bias current J of the PMOS regulated-cascode current copier and a bias current in the input circuit of our ADC, which will be discussed later. The circuit diagram of the NMOS regulated-cascode current source is given in Figure 4.16. The voltage Vb is an external voltage for our ADC.

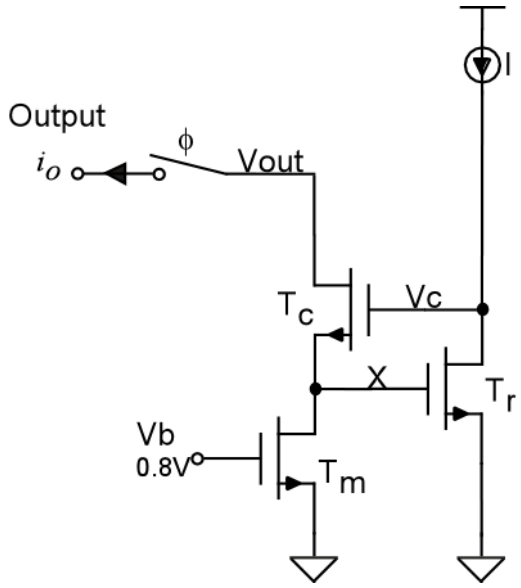


Figure 4.16 NMOS Regulated-Cascode Current Source

The bias point of the regulated-cascode current source is established by the value of the bias voltage V_b and the bias current I. Note that the bias voltage is generated off-chip. Since charge injection is not a factor in the accuracy of the current source, the transistor T_m operates in the saturation mode, increasing the accuracy of the regulated-cascode current source. Operating T_m in the saturation mode rather than the triode mode increases the accuracy since the output resistance of the current source is increased. Specifically, the transistor T_m is less sensitive to changes in its drain voltage when operating in saturation mode.

To minimize power dissipation, the bias current I is set such that the gate voltage of the regulating transistor is approximately the threshold voltage. Thus, according to the condition for saturation operation of a transistor, the bias voltage of T_m must be less than twice the threshold voltage. Furthermore, for strong inversion, the bias voltage must be greater than the threshold voltage by 0.2 V. To meet these conditions, the bias voltage is set to approximately 0.2 V above the threshold voltage. The sizes of the transistors are determined by the value of the current source and the chosen bias voltage.

The bias point also allows for saturation operation of the regulated-cascode current source under all circuit conditions. The cascode transistor T_c should maintain saturation operation for as wide a range as possible to ensure high output impedance.

Saturation operation of the NMOS cascode transistor of the NMOS regulated-cascode current source is assured if

$$\begin{aligned} T_c \text{ Saturation Condition}: &\quad V_{out} \geq V_c - V_t \\ T_c \text{ On Condition}: &\quad V_c \geq 2V_t + 0.2\,V \\ &\Rightarrow\ V_{out} \geq V_t + 0.2\,V \end{aligned} .$$

Due to the bias points of the regulated-cascode current sources, the lowest allowable voltage at the output node of the current source is approximately 0.2 V above the threshold voltage. Thus, setting the gate voltage of the regulating transistor to approximately the threshold voltage allows saturation operation of the cascode transistor of the NMOS regulated-cascode current source under all circuit conditions, assuring the accuracy of the NMOS current sources of the ADC. The transistor sizes and relevant parameters of the NMOS current sources are given in Table 4.4. Note that HSPICE was used to tune the sizes of the transistors to ensure the value of the current sources.

Table 4.4 Parameters of the NMOS Regulated-Cascode Current Sources

	Value=45 μA	**Value=200 μA**
T_m: W/L	6.5 μm/0.6 μm	29.2 μm/0.6 μm
T_c: W/L	11 μm/1 μm	49 μm/1 μm
T_r: W/L	11 μm/1 μm	49 μm/1 μm
T_b: W/L	38.7 μm/ 15 μm	102.4 μm/ 15 μm
Vbias	0.8 V	0.8 V
I	6 μA	17 μA

The layouts of the NMOS regulated-cascode current sources are given in Figures 4.17 – 4.18. Note that the layout of Figure 4.17 includes both the 45 μA reference current source I_{r2} and the 45 μA bias current source I_{b2}. The layouts of these two current sources are combined in order to match the current sources across process variations. Layout considerations will be discussed later in this chapter. The transistors labeled as T*i*b of Figure 4.17 are those of the 45 μA bias current I_{b2}, and the transistors labeled as T*i*r are those of the 45 μA reference current I_{r2}. The transistors labeled Tr*i* are the regulating transistors of the current sources, the transistors labeled Tc*i* are the cascode transistors of the current sources, and the transistors labeled Tb*i* are the bias transistors, which implement the bias current I. The area of the two current sources with value 45 μA is 58 x 158 μm^2, and the area of the current source with value 200 μA is 32 x 132 μm^2.

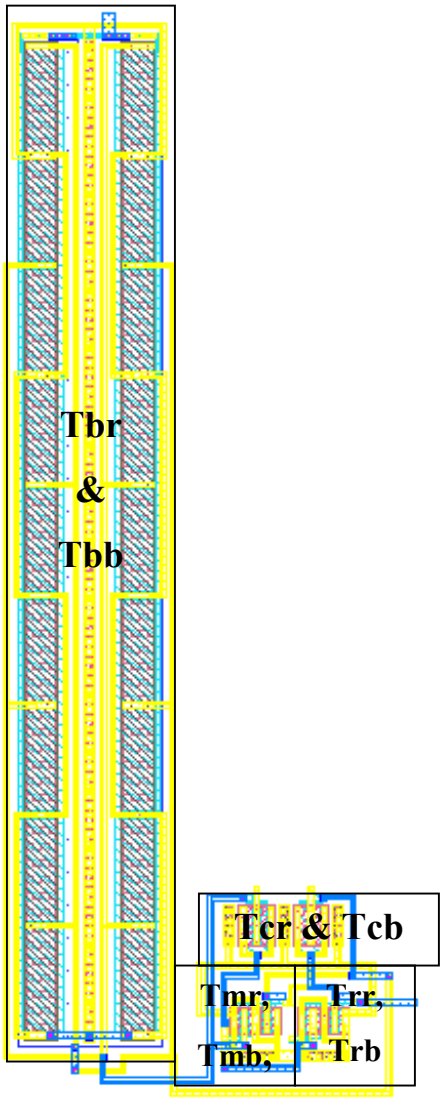


Figure 4.17 Layout of the 45 µA NMOS Regulated-Cascode Current Sources

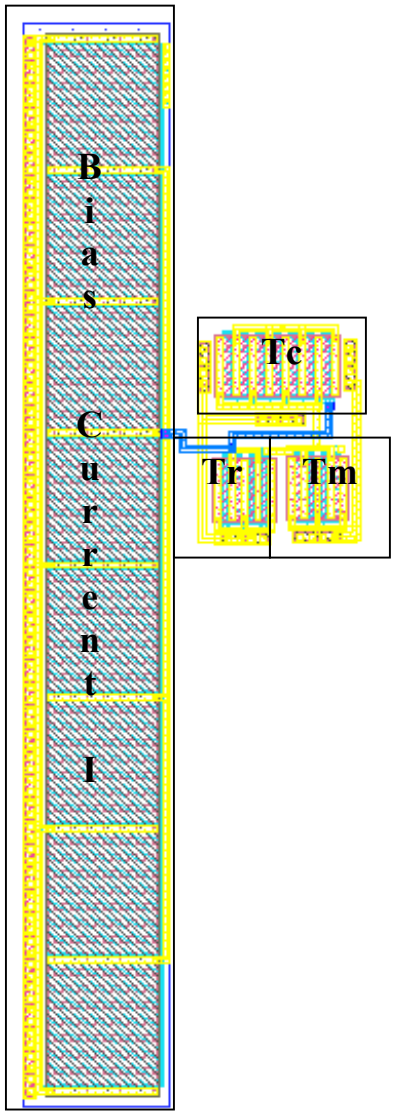


Figure 4.18 Layout of the 200 µA NMOS Regulated-Cascode Current Source

Each NMOS current source was verified by simulating the current source to ensure the value of the current source did not vary with the output node V_{out}. The voltage at the node V_{out} used in the simulation has a signal swing that is approximately the same as the voltage swing present during normal operation of the ADC, which is 1.2 V to 1.6 V. The simulation results are shown in Figures 4.19 – 4.20.

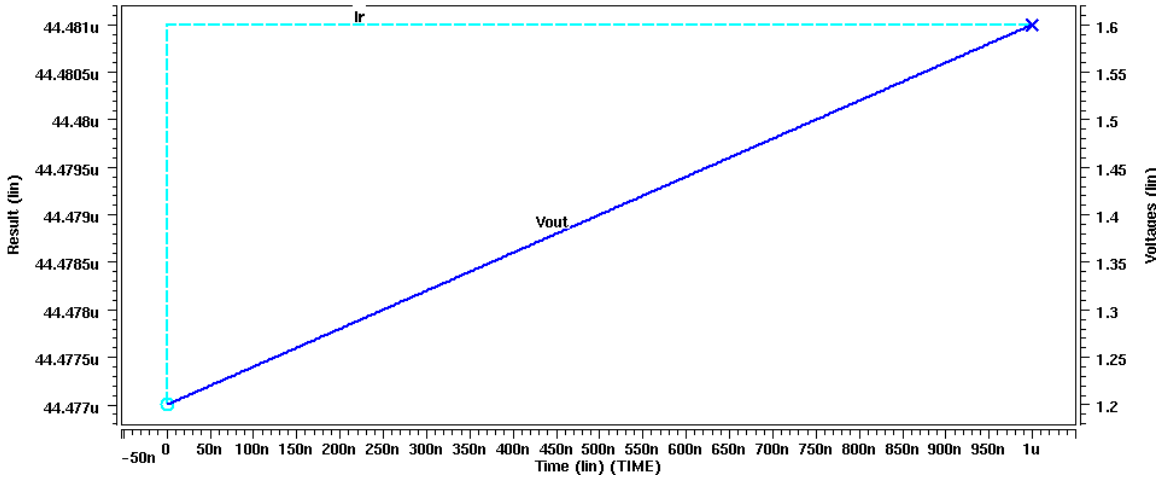


Figure 4.19 Simulation Results of the 45 µA NMOS Regulated-Cascode Current Sources

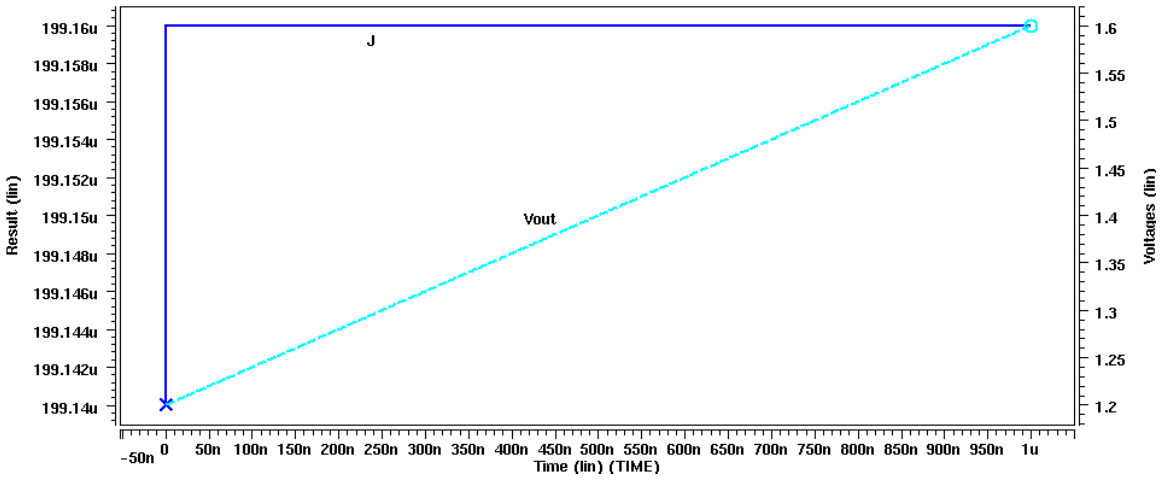


Figure 4.20 Simulation Results of the 200 µA NMOS Regulated-Cascode Current Source

The right vertical axes of the graphs shown in the figures are the output voltage, and the left vertical axes are the output current. The output node is varied from 1.2 V to 1.6 V, which is approximately the signal swing on the output node of the current source when used in the ADC architecture of Figure 4.1. The simulation results indicate that the NMOS regulated-cascode current sources have an effectively constant output current when the voltage at the output node is varied. Thus, the current sources are accurate.

The 45 µA NMOS regulated-cascode current source dissipates 0.19 mW, and the 200 µA NMOS regulated-cascode current source dissipates 0.38 mW.

The recovery time of the NMOS current sources was also found. The recovery time of the current sources was found by applying a constant voltage to the output nodes of the current sources. Also, the bias voltage Vb was set to ground at 0 ns and set to 0.8 V after 20 ns. The simulation results for the recovery time of the NMOS regulated-cascode current sources are found in Figure 4.21.

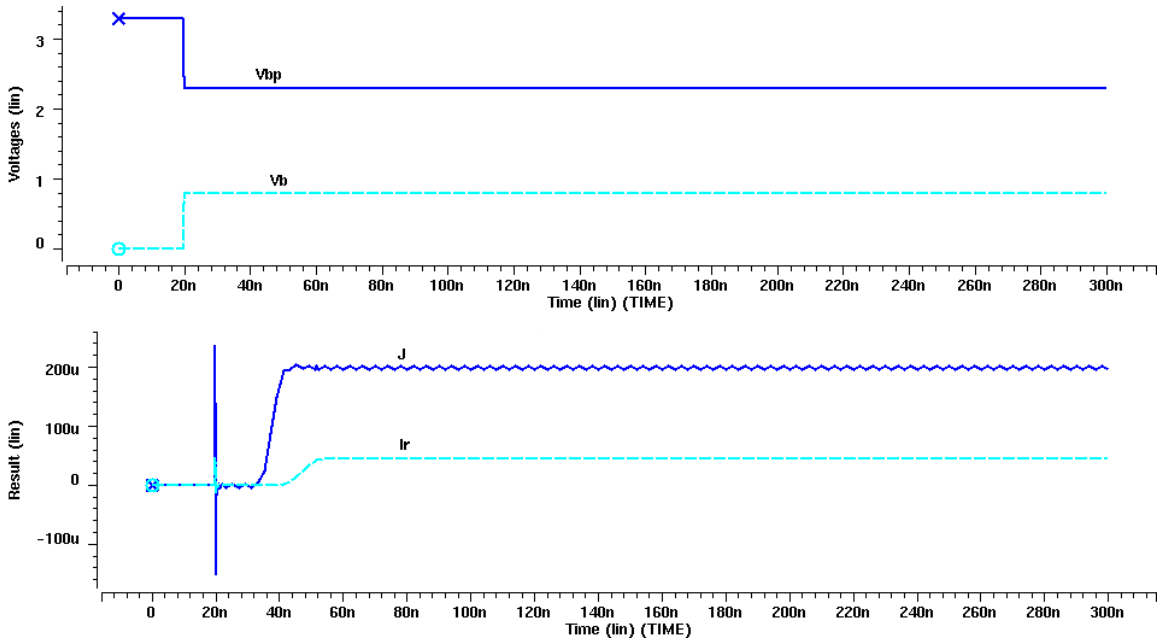


Figure 4.21 Recovery Time of the NMOS Regulated-Cascode Current Sources

The upper waveform of Figure 4.21 is the value of the external bias voltages of our ADC, Vb and Vbp. The lower waveform is the current sourced by the NMOS regulated-cascode current copiers for the given bias voltages. The simulation results indicate that the 45 µA NMOS regulated-cascode current source and the 200 µA NMOS regulated-cascode current source recover in less than 50 ns.

PMOS regulated-cascode current sources are used to implement the reference current I_{r1} and the bias current I_{b1} of the ADC architecture. Also, a PMOS regulated-cascode current source is used to implement the bias current J of the NMOS regulated-cascode current copier and a bias current in the input circuit of our ADC.

The PMOS regulated-cascode current source is implemented in the same manner as the NMOS regulated-cascode current source. The differing aspects are the operating point and the mobility of the charge carriers of the PMOS transistors of the current source. The circuit diagram of the PMOS regulated-cascode current source is given in Figure 4.22. The voltage Vbp is an external voltage for our ADC.

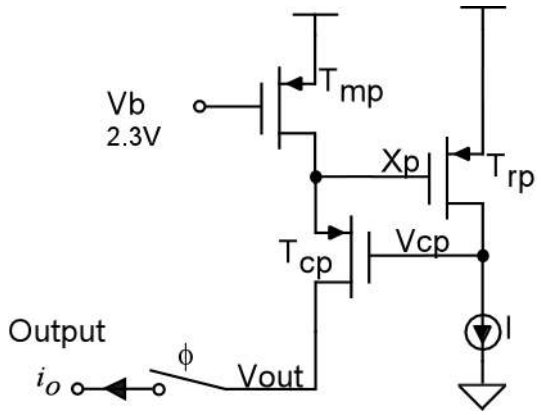


Figure 4.22 PMOS Regulated-Cascode Current Source

Saturation operation of the PMOS cascode transistor of the PMOS regulated-cascode current source is assured if

$$T_{cp}\ Saturation\ Condition: \quad V_{out} \le V_{cp} - V_{tp}$$
$$T_{cp}\ On\ Condition: \quad V_{cp} \le Vdd + 2V_{tp} - 0.2\,V\,.$$
$$\Rightarrow \quad V_{out} \le Vdd + V_{tp} - 0.2\,V$$

The highest allowable voltage is approximately Vdd less the threshold voltage. As a result, setting the gate voltage of the regulating transistor to approximately the threshold voltage allows saturation operation of the cascode transistor of the PMOS regulated-cascode current source under all circuit conditions, assuring the accuracy of the PMOS current sources of the ADC. The transistor sizes and bias currents are chosen in the same manner as the transistors of the NMOS regulated-cascode current source. The corresponding transistor sizes and relevant parameters of the PMOS current sources are given in Table 4.5.

Table 4.5 Parameters of the PMOS Regulated-Cascode Current Sources

	Value=45 μA	**Value=200 μA**
T_{mp}: W/L	16.6 μm/0.6 μm	70 μm/0.6 μm
T_{cp}: W/L	24.6 μm/1 μm	100 μm/1 μm
T_{rp}: W/L	24.6 μm/1 μm	100 μm/1 μm
T_{bp}: W/L	12.6 μm/ 10.05 μm	36 μm/ 10 μm
I	8 μA	27 μA
Vbias	0.8 V	0.8 V

The layouts of the PMOS regulated-cascode current sources are given in Figures 4.23 – 4.24. The layout of Figure 4.23 includes both the 45 μA reference current source I_{r1} and the 45 μA bias current source I_{b1}. The transistors labeled T*i*r of Figure 4.23 are the transistors of the reference current, I_{r1}, and the transistors labeled T*i*b are the transistors of the bias current, I_{b1}. The transistors labeled Tr*i* are the regulating transistors of the current sources, the transistors labeled Tc*i* are the cascode transistors of the current sources, and the transistors labeled Tb*i* are the bias transistors, which implement the bias current I of the current sources. The area of the 45 μA current sources is 39 x 84 μm^2, and the area of the current source with value 200 μA is 29 x 110 μm^2.

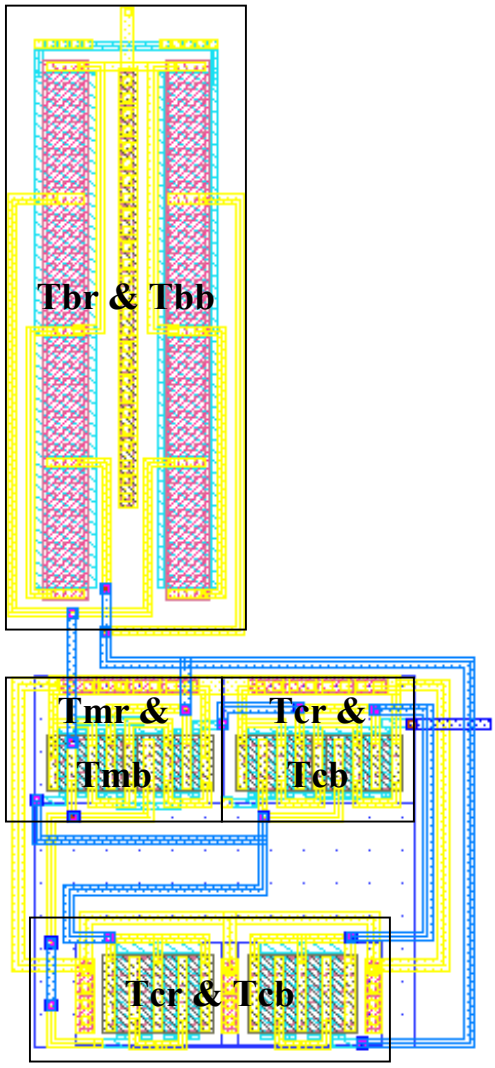


Figure 4.23 Layout of the 45 µA PMOS Regulated-Cascode Current Sources

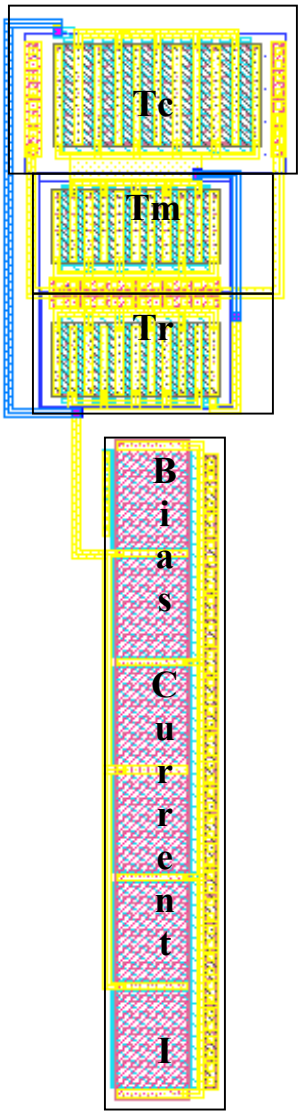


Figure 4.24 Layout of the 200 µA PMOS Regulated-Cascode Current Source

Each PMOS current source was also verified by simulating the current source and varying the voltage of the output node, V_{out}, to ensure the value of the current source did not vary with V_{out}. The voltage at the output node of the current sources varies from 1.2 V to 1.6 V. The simulation results are shown in Figures 4.25 – 4.26.

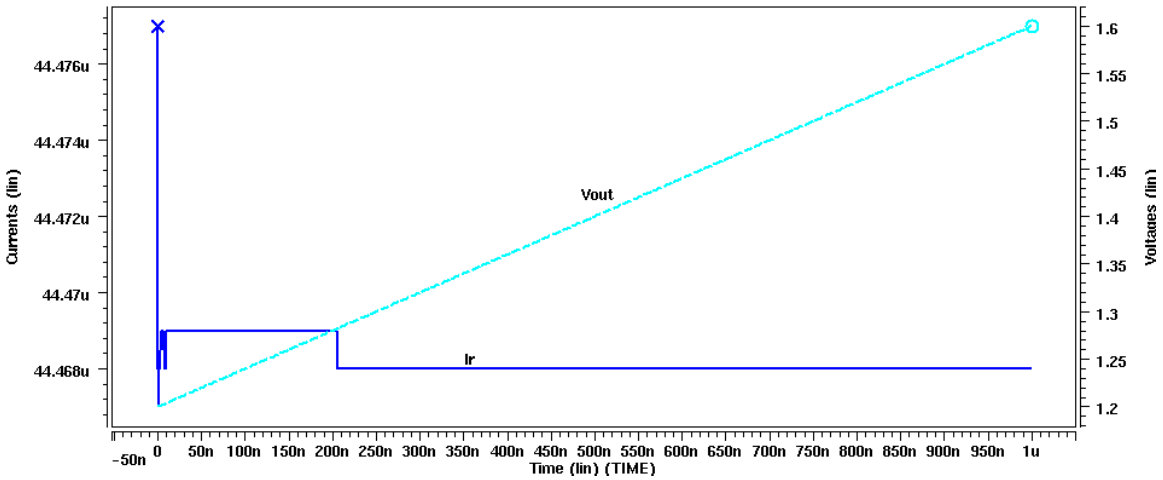


Figure 4.25 Simulation Results of the 45 µA PMOS Regulated-Cascode Current Source

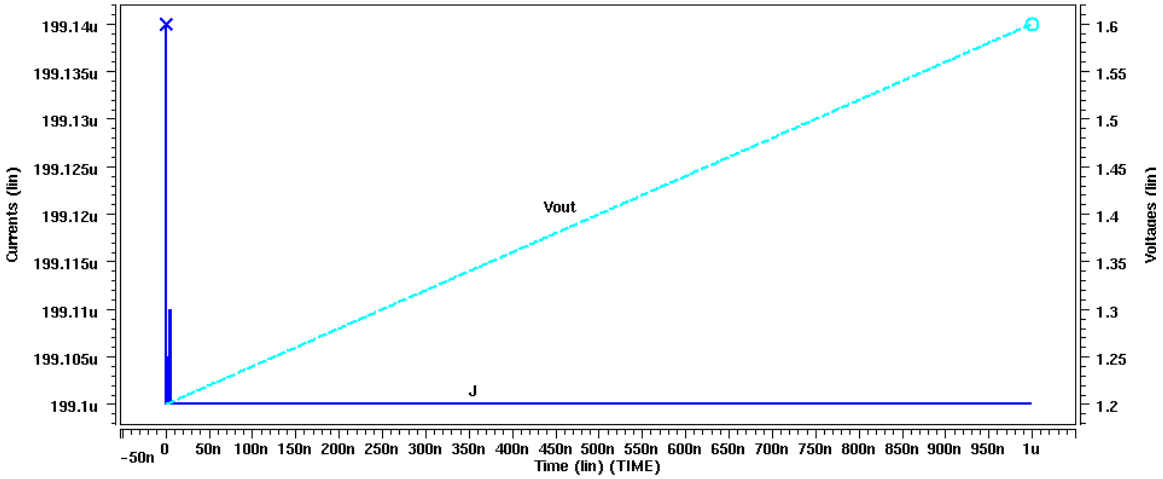


Figure 4.26 Simulation Results of the 200 µA PMOS Regulated-Cascode Current Source

In Figures 4.25 – 4.26, the left vertical axes are the output current, and the right vertical axes are the voltage at the output node of the current source. The simulation results indicate that the PMOS regulated-cascode current sources source an effectively constant current when the voltage at its output node is varied and, hence, are accurate. The 45 µA PMOS regulated-cascode current source dissipates 0.21 mW, and the 200 µA PMOS regulated-cascode current source dissipates 0.45 mW.

The recovery time of the PMOS current sources was also found. The recovery time of the current sources was found by applying a constant voltage to the output nodes

of the current sources. Also, the bias voltage Vbp was set to Vdd at 0 ns and set to 2.3 V after 20 ns. The simulation results for the recovery time of the PMOS regulated-cascode current sources are found in Figure 4.27.

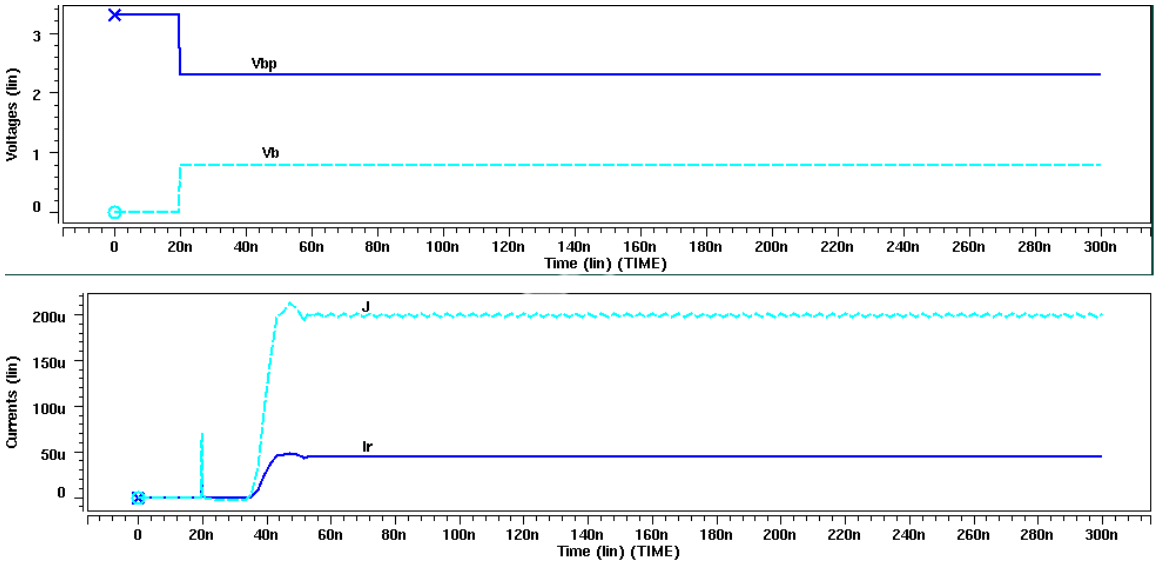


Figure 4.27 Recovery Time of the PMOS Regulated-Cascode Current Sources

The upper waveforms of Figure 4.27 are the values of the external bias voltages of our ADC, Vb and Vbp. The lower waveform is the current sourced by the PMOS regulated-cascode current sources for the given bias voltages. The simulation results indicate that the 45 µA PMOS regulated-cascode current source and the 200 µA PMOS regulated-cascode current source recover in less than 50 ns.

4.6 Comparators

Strobed, cross-coupled inverter comparators are used to determine the output bits of the ADC each bit cycle. These simple comparators can be used since the RSD algorithm tolerates large offsets in the comparison levels. The design considerations for the strobed, cross-coupled inverter comparator and its reference voltage are considered in this section.

The strobed, cross-coupled inverter comparators of Figure 4.1 were implemented using small inverters. The transistors of the comparator need not be large since the

settling time of the analog components of the ADC is much greater than that of the comparators. Thus, the dynamic power dissipation of the comparators is minimized. The circuit diagram of the strobed, cross-coupled inverter comparator is given in Figure 4.28, and the sizes of the transistors are given in Table 4.6. The layout of the comparator is shown in Figure 4.29 and has an area of 26 x 24 μm^2.

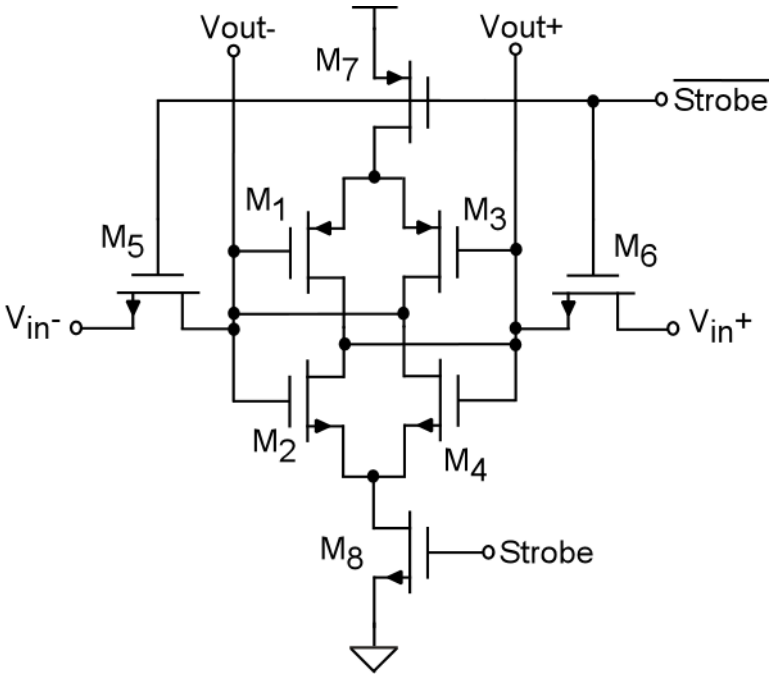


Figure 4.28 Strobed, Cross-Coupled Inverter Comparator

Table 4.6 Transistor Sizes of the Comparator

	W/L
M_1, M_3, M_7	8 μm/0.6 μm
M_2, M_4, M_8	0.7 μm/1 μm
M_5, M_6	10 μm/1 μm

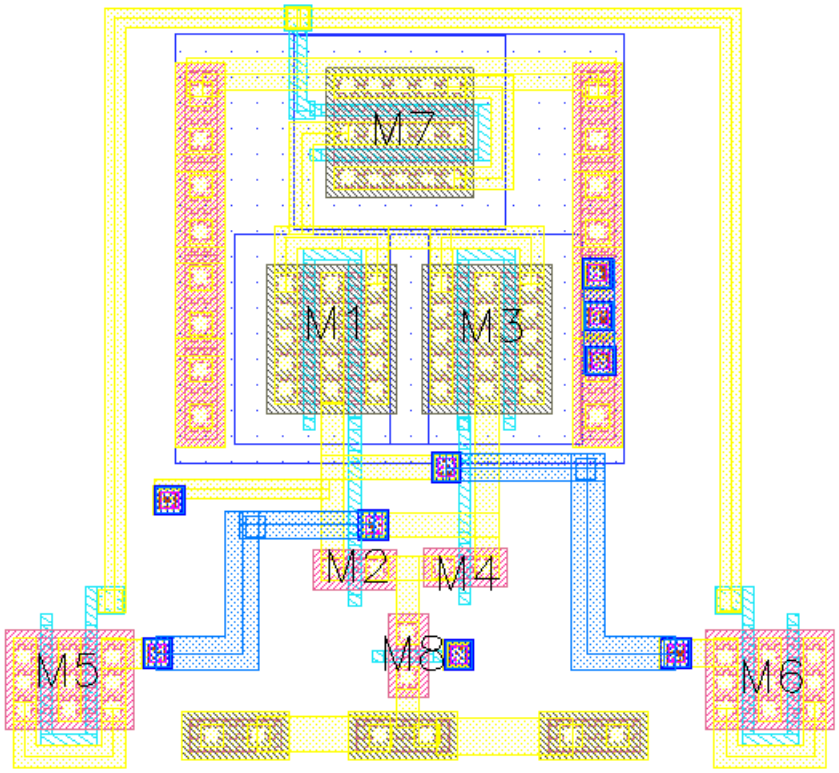


Figure 4.29 Layout of the Strobed, Cross-Coupled Inverter Comparator

The comparator was verified by comparing a voltage at the Vin+ node to a reference voltage at the Vin- node. As mentioned in Section 3.4, the voltage at the output node Vout+ should rise to Vdd for voltages at the node Vin+ greater than the voltage at the node Vin-. The reference voltage is set to 1.65 V for this simulation. The simulation results are shown in Figure 4.30.

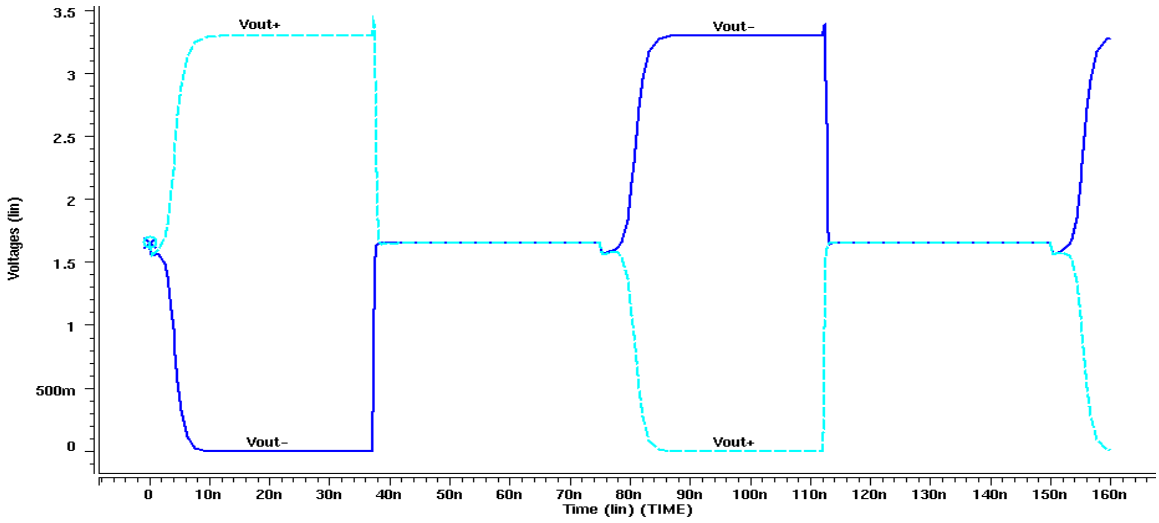


Figure 4.30 Strobed, Cross-Coupled Inverter Comparator Simulation Results

The comparator first samples the input voltage at time zero. The comparator samples the input again at 75 ns. The input voltage (Vin+) is 1.66 V at time zero and is 1.64 V at 75 ns. The reference voltage (Vin-) is set to 1.65 V. The simulation results indicate that the comparator correctly evaluates a voltage of 1.66 V as being greater than 1.65 V since Vout+ is Vdd after the 1.66 V input voltage is sampled. Also, the comparator correctly evaluates a voltage of 1.64 V as being less than 1.65 V since Vout+ is ground after the 1.64 V input voltage is sampled. The power dissipation of the strobed, cross-coupled inverter comparator is 2.3 μW.

Four references voltages are required for the four comparators of the ADC architecture of Figure 4.1. The reference voltage of each comparator is implemented using capacitor voltage dividers followed by a voltage buffer. The capacitors of the reference voltage circuits are implemented in double poly and are implemented using arrays of unit-sized capacitors and non-unit sized capacitors to minimize mismatches across process variation. The implementation of the capacitors of the reference voltage circuit is discussed further in Section 4.11.1.

The reference voltage circuit is shown in Figure 4.31. The capacitor sizes corresponding to each reference voltage are given in Table 4.7. The layouts of the four voltage reference voltage circuits are given in Figures 4.32-4.33. The voltage references of the two comparators CP_n and CQ_n are incorporated into one block in Figure 4.32, and

the voltage references of the comparators CP_n and CQ_n are incorporated into a block in Figure 4.33 to minimize area. The layout of Figure 4.32 has an area of 134 x 196 μm^2, and the layout of Figure 4.33 has an area of 134 x 174 μm^2.

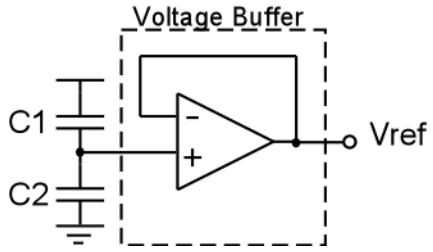


Figure 4.31 Reference Voltage Circuit

Table 4.7 Capacitor Sizes for Comparator Reference Voltages

Comparator	V_{ref} (V)	C1 (pF)	C2 (pF)
CP_p	1.56	0.456	0.5
CQ_p	1.61	0.514	0.5
CP_n	1.26	0.315	0.5
CQ_n	1.21	0.268	0.5

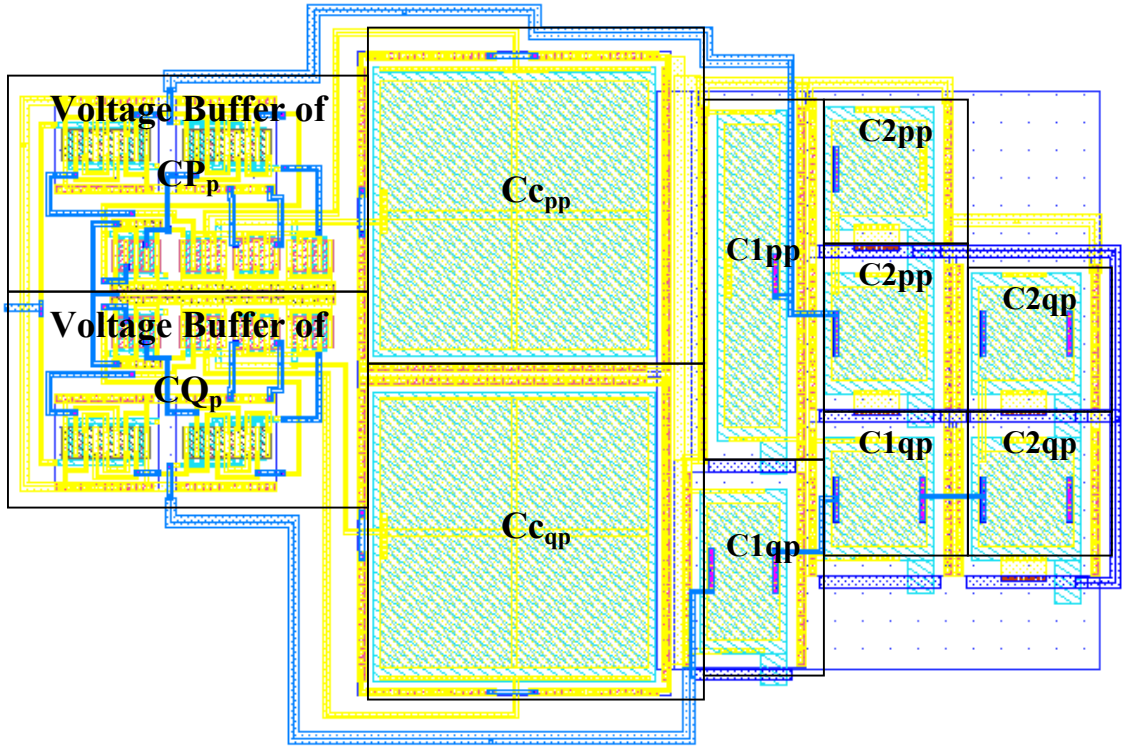


Figure 4.32 Layout of the CP_p and CQ_p Reference Voltages

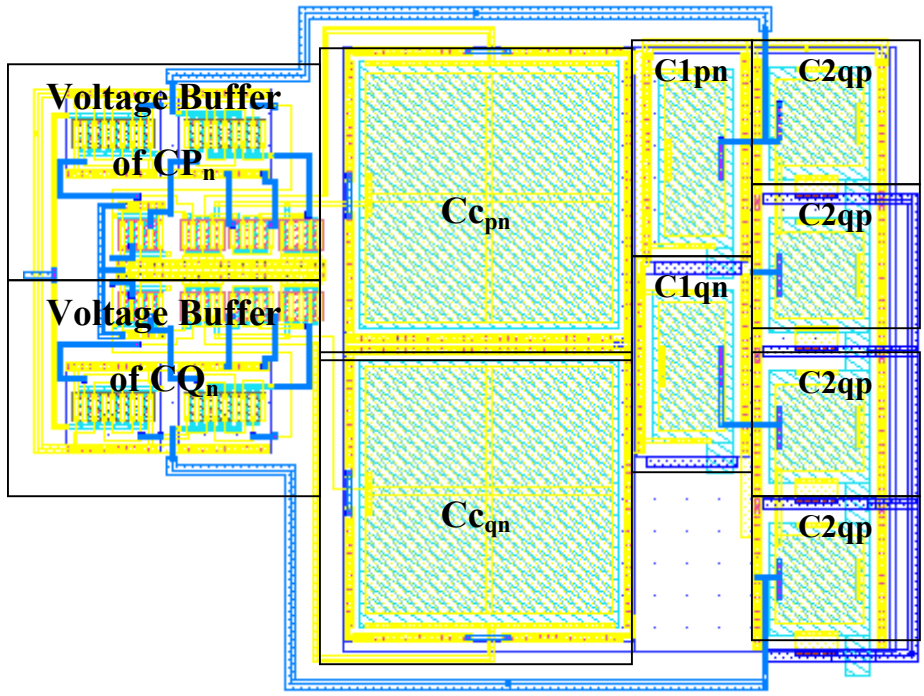


Figure 4.33 Layout of the CP_n and CQ_n Reference Voltages

Table 4.7 indicates that the ideal value of the capacitor divider circuit is not produced. Specifically, an approximately 15 mV offset is present in the reference voltages for the comparators CP_p and CP_n, and an approximately 60 mV offset is present in the reference voltages for the comparators CQ_p and CQ_n. These offsets are a product of parasitic capacitances associated with the capacitor arrays of the capacitor divider circuits. However, these offsets are constant and are compensated for by adjusting the sizes of the capacitors appropriately. Specifically, if the output voltage of a voltage buffer is not the ideal output voltage, the size of the capacitor C1 of Figure 4.31 is adjusted such that the output voltage is the required output voltage.

In Figures 4.32-4.33, the boxes labeled Cipp are capacitors associated with the voltage reference for the comparator CP_p of the ADC of Figure 4.1; the boxes labeled Ciqp are capacitors associated with the voltage reference for the comparator CQ_p; the boxes labeled Cipn are capacitors associated with the voltage reference for the comparator CP_n; the boxes labeled Ciqn are capacitors associated with the voltage reference for the comparator CQ_n. Capacitors labeled C1*i* correspond to the capacitor C1 in Figure 4.31, and capacitors labeled C2*i* correspond to the capacitor C2 in Figure 4.31. The capacitors labeled Cc are the compensation capacitors of the op-amps of the voltage buffers (refer to Figure 4.35). The simulation results of each reference voltage circuit are shown in Figure 4.34. The simulation results indicate each voltage reference circuit maintains a constant output voltage.

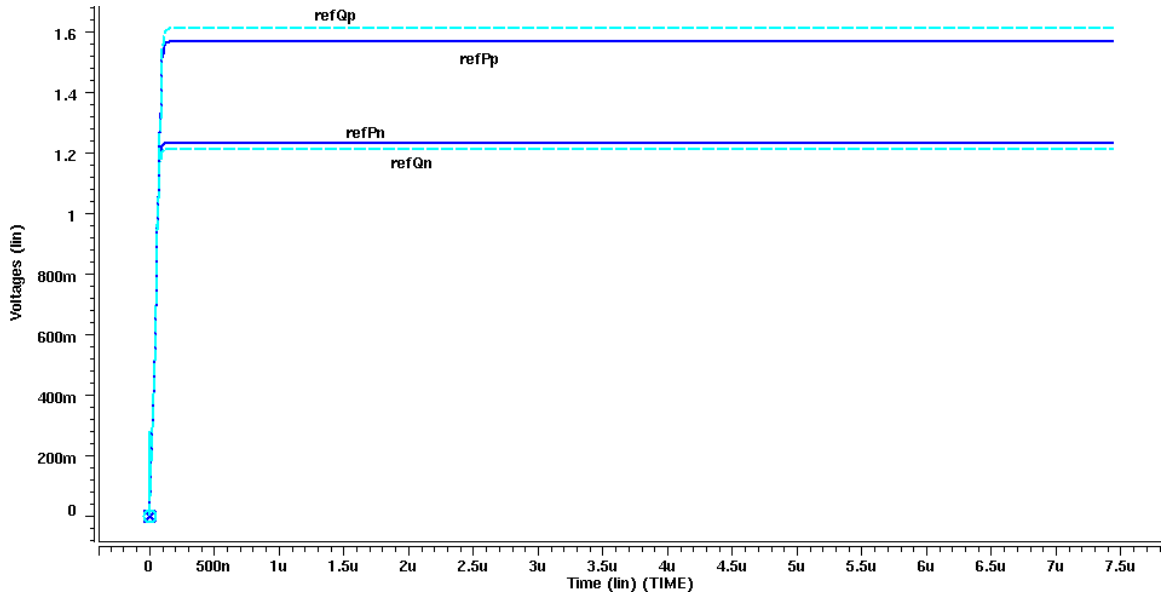


Figure 4.34 Simulation Results for the Voltage Reference Circuits

The reference voltage of the comparators CP_p (CP_n) corresponds to the gate-voltage of the memory transistor of the PMOS (NMOS) current copier when the current P = $^5/_4$ I_{ref} is being stored, and the reference voltages of the comparators CQ_p (CQ_n) corresponds to the gate-voltage of the memory transistor of the PMOS (NMOS) current copier when the current Q = $^3/_4$ I_{ref} is being stored. Note that the reference voltages were found through HSPICE simulation due to the inaccuracy of the drain-source current equations given in Section 4.4.2.

The only source of power dissipation in the reference voltage circuit is the op-amp. Since only a constant voltage output is needed, the gain of the op-amp is moderate. As a consequence, the size of the op-amps transistors and bias currents are small, dissipating little power in comparison to higher performance op-amps.

The op-amp is a two-stage CMOS op-amp with a differential input and a single-ended output. The op-amp implementation given by Johns is used [12]. The op-amp circuit diagram is given in Figure 4.35, and the layout is given in Figure 4.36. The voltage buffer layout has an area of 61 x 110 μm^2.

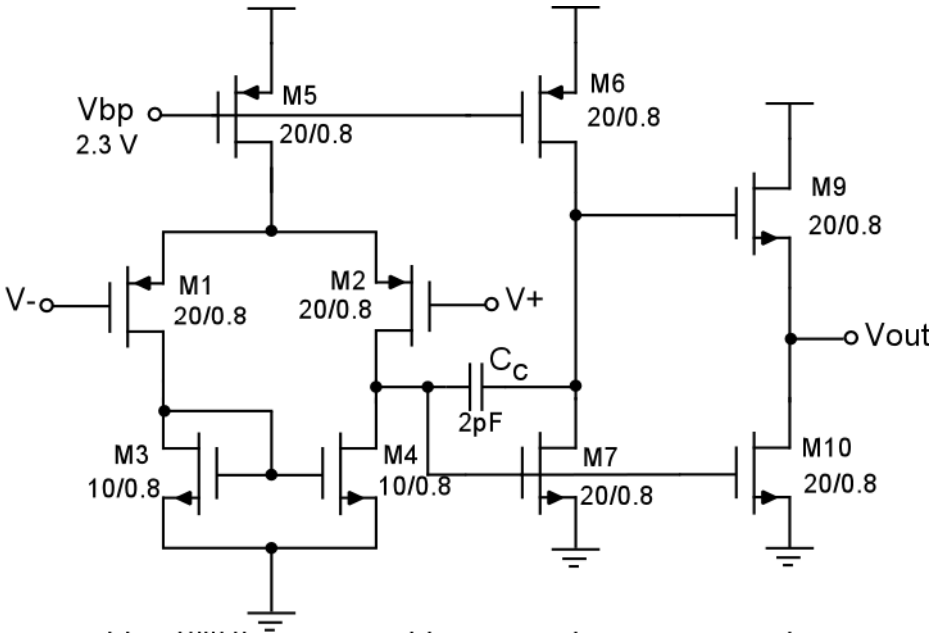


Figure 4.35 Op-Amp of the Voltage Reference Circuit [12]

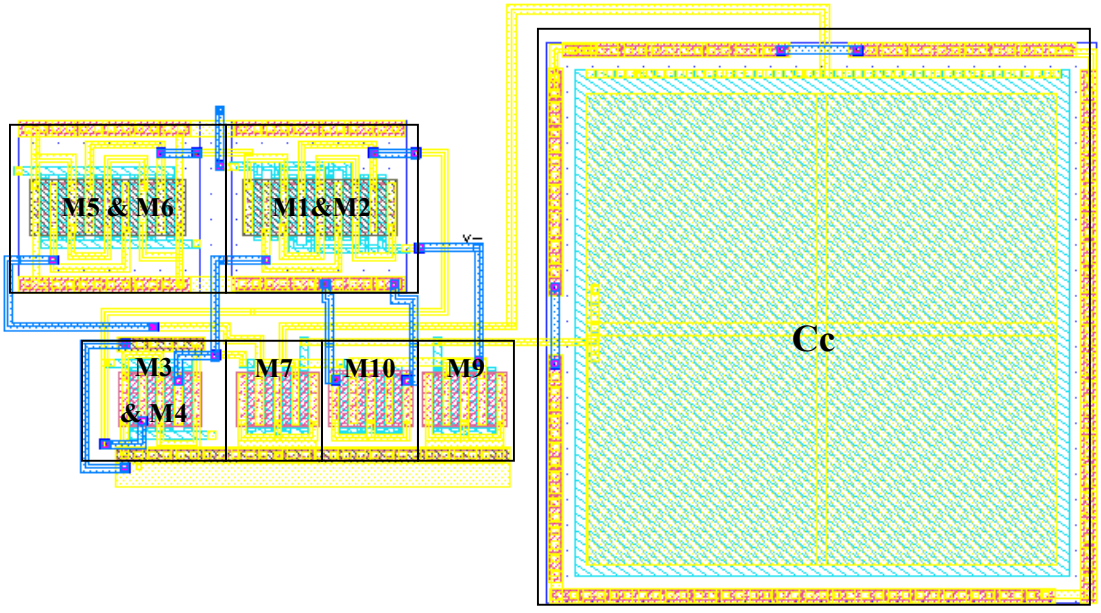


Figure 4.36 Layout of the Voltage Buffer

The operation of the op-amp was verified by placing it in the voltage buffer configuration shown in Figure 4.31 and applying a triangular voltage input that varied

from 0 V to 3.3 V with a frequency of 100 kHz. The simulation results of the voltage buffer are given in Figure 4.37.

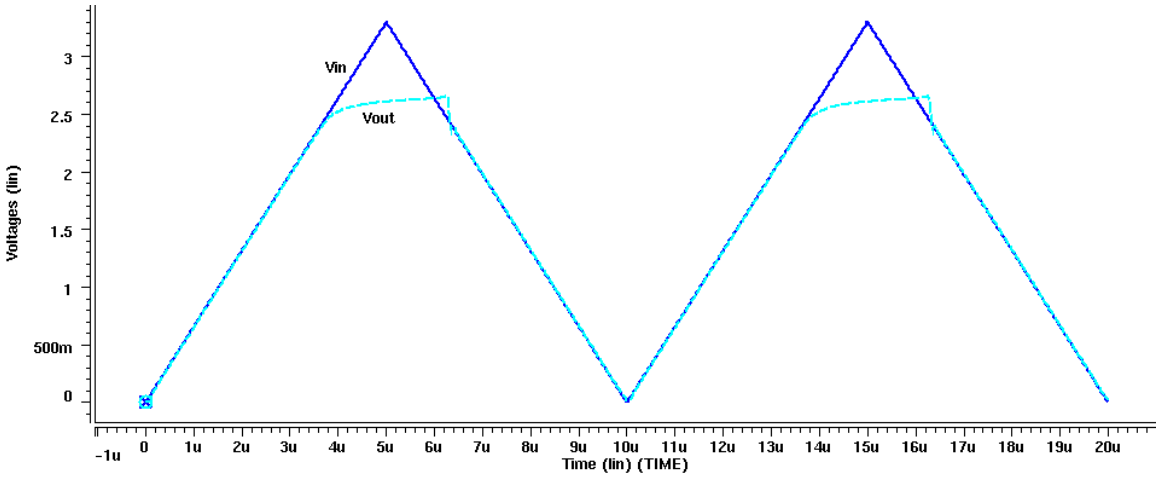


Figure 4.37 Simulation Results of the Voltage Buffer

Figure 4.37 shows that output of the voltage buffer does not swing from ground to Vdd. The cause is the source-follower voltage buffer used at the output of the op-amp. The largest possible voltage that an N-type MOSFET passes from Vdd is Vdd-V_t, which is approximately 2.5 V for our op-amp implementation. However, since the required reference voltages do not exceed 2 V, this limitation is not a concern. The dc gain of the op-amp and bandwidth as computed by HSPICE is 71 dB and 4 kHz, respectively. The power dissipation is approximately 0.4 mW for a constant input voltage.

4.7 Input Circuit

The input of our ADC is current rather than voltage. However, since voltage is traditionally used as the signal variable, current signals are seldom available as input. Consequently, a voltage-to-current converter is used to provide the input to our ADC.

An off-chip voltage input with a series resistance is used to source current to the ADC. However, a voltage-resistor circuit cannot be directly applied to the input node of the ADC. If a voltage-resistor circuit were applied to the input node, a large error would be created since the input impedance of our ADC is a function of the input current. An

input circuit with low input impedance is utilized to ensure a large input signal bandwidth. A large RC time constant would be introduced if the input circuit had high input impedance due to the large capacitance associated with the input pad. The input circuit presented by Wang is given in Figure 4.38.

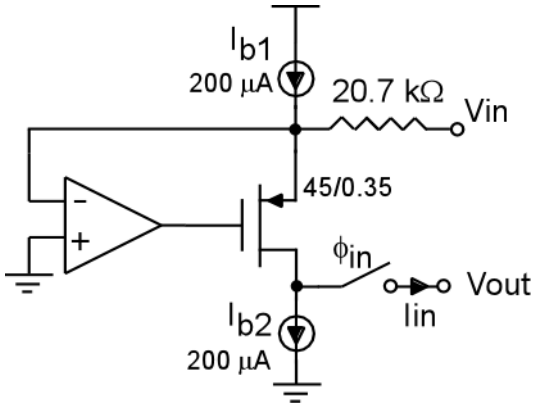


Figure 4.38 Input Circuit [30]

The input circuit uses a common-gate PMOS amplifier to provide low input impedance. In order to minimize the input impedance, an op-amp is used in a feedback configuration that increases the small-signal input conductance of the common-gate amplifier by a factor of the gain of the op-amp. Equivalently, the op-amp decreases the input impedance by the gain factor of the op-amp. Furthermore, to allow an input current of 0 μA and to further minimize the input impedance of the input circuit, the common-gate amplifier is biased with two 200 μA current sources. The layout of the input circuit is given in Figure 4.39, and the area is 100 x 132 μm^2.

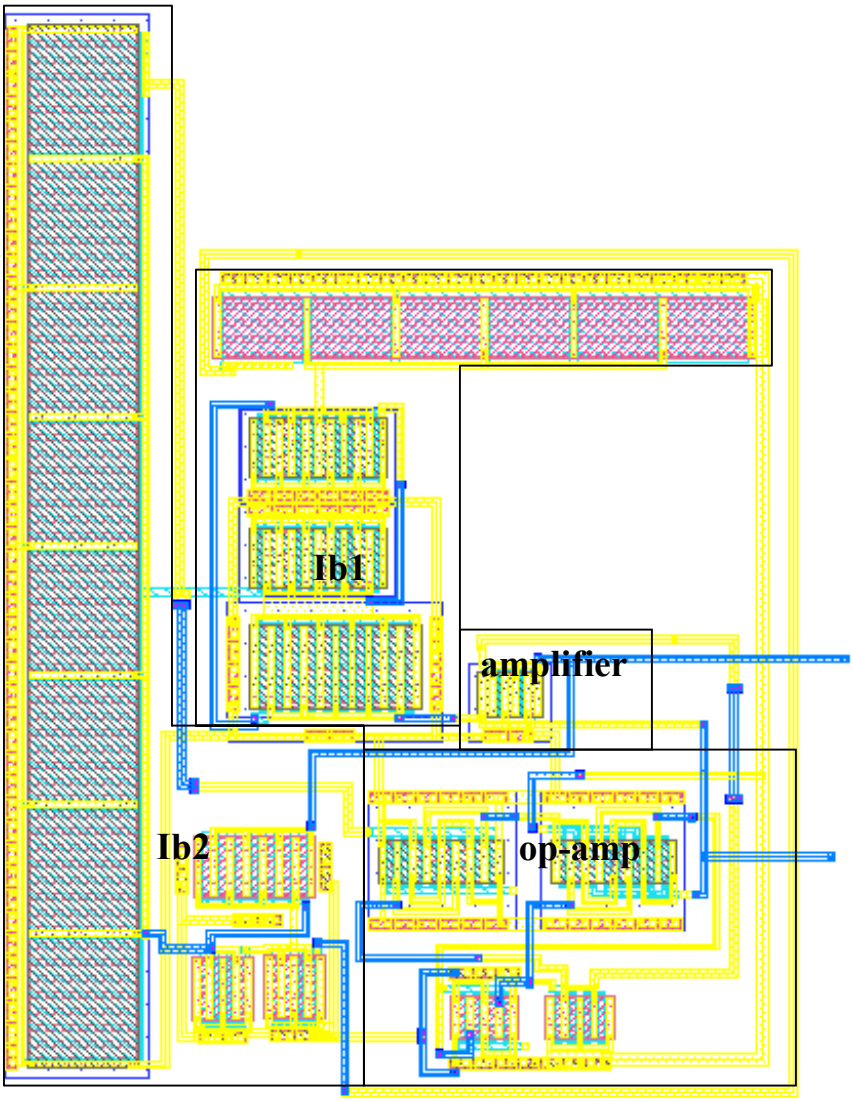


Figure 4.39 Layout of the Input Circuit

The operation of the input circuit was verified by applying a triangular voltage input that varied from 1.3 V to 3.3 V with a frequency of 62.5 kHz. The input voltage swing corresponds to an input current range of 0 µA to 90 µA. The difference between the input current (flowing through the Vin node in Figure 4.38) and the current sourced by the input circuit (flowing through the Vout node) was measured. The simulation results are given in Figure 4.40.

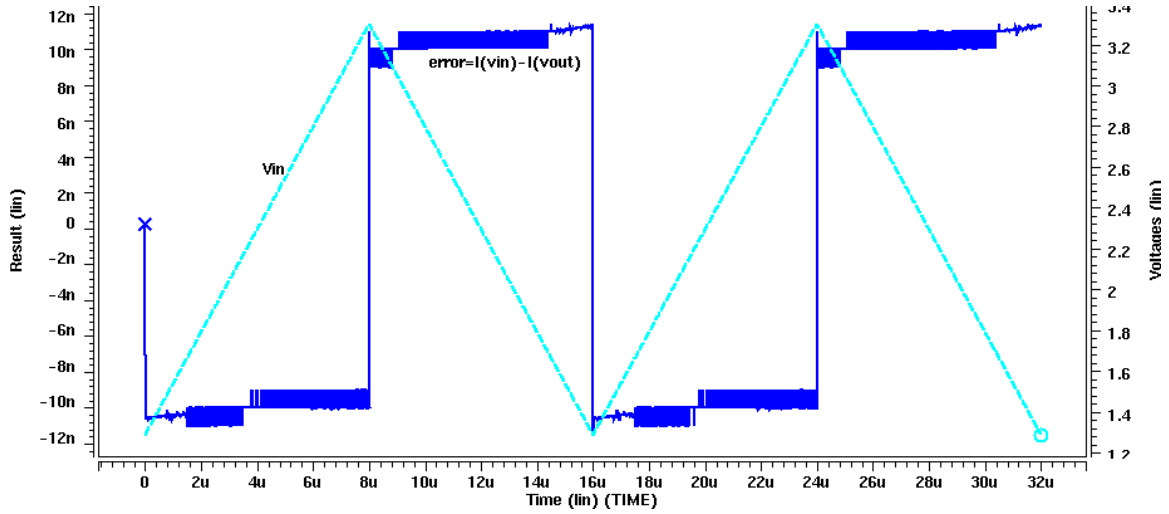


Figure 4.40 Simulation Results of the Input Circuit

The left vertical axis of Figure 4.40 is the error of the input circuit. The right vertical axis is the input voltage of the input circuit. Figure 4.40 shows that the error of the input circuit is less than 11 nA for an input frequency of 62.5 kHz. This error corresponds to approximately ½ I_{LSB} (90 µA/2^{12}). As the input signal frequency decreases, the error also decreases. For instance, for an input signal frequency of 50 kHz, the error is less than 8 nA. Thus, 12-bit accuracy is maintained for input signal frequencies less than 62.5 kHz. The power dissipation for the maximum input current of 90 µA is 1.3 mW measured over a period of 7.2 µs.

At-speed testing of our ADC is not possible due to the limited bandwidth of the input circuit. This is true since the Nyquist rate of our ADC is 70 kHz but the bandwidth of the input circuit is 62.5 kHz. If our ADC were incorporated into a larger system, the input circuit utilized would not be necessary. Recall that the input circuit of our ADC is used in order to minimize the band-limiting effects associated with the I/O pads. Thus, when the ADC is incorporated into a larger system, a more appropriate input circuit, such as a transconductor, can be used. For example, a transconductor with a bandwidth of 40 MHz has been reported recently [8].

The recovery time of the input circuit was also found. The recovery time of the input circuit was found by applying a constant voltage to the input node of the ADC. Also, the bias voltage Vbp of the op-amp and of the PMOS regulated-cascode current source (refer to Figure 4.22), I_{b1}, was set to Vdd at 0 ns and set to 2.3 V after 20 ns. The

bias voltage Vb of the NMOS regulated-cascode current source (refer to Figure 4.16), I_{b2}, was set to ground at 0 ns and set to 0.8 V after 20 ns. The simulation results for the recovery time of the input circuit are found in Figure 4.41.

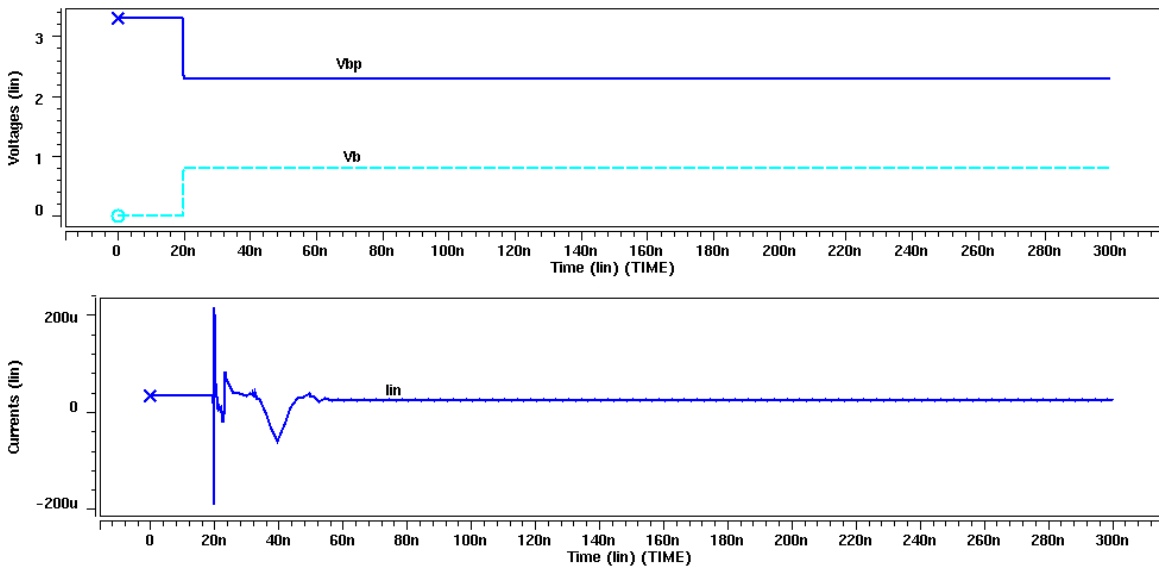


Figure 4.41 Recovery Time of the Input Circuit

The upper waveforms of Figure 4.41 correspond to the external bias voltages of the ADC, Vb and Vbp. The lower waveforms correspond to the current sourced by the input circuit for the given bias voltages. The simulation results indicate that the input circuit recovers in less than 60 ns.

The op-amp used in the input circuit is very similar to the op-amp used in the voltage reference circuit shown in Figure 4.35. For the input circuit, the op-amp does not include a source-follower output buffer or a compensation capacitor C_c. An output buffer is not required since the op-amp of the input circuit has a purely capacitive load. A compensation capacitor is not used to ensure a large bandwidth. The circuit diagram of the op-amp is given in Figure 4.42, and the layout is given in Figure 4.43. The layout has an area of 35 x 45 μm^2.

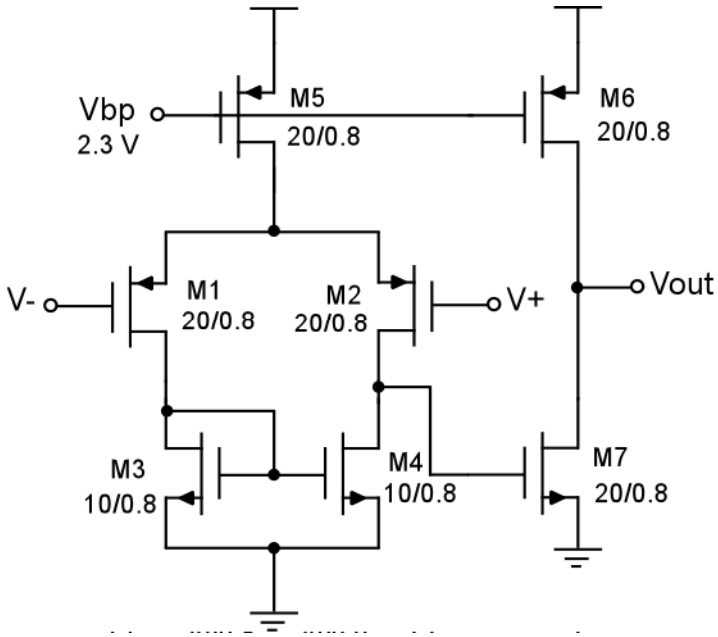


Figure 4.42 Op-Amp of the Input Circuit

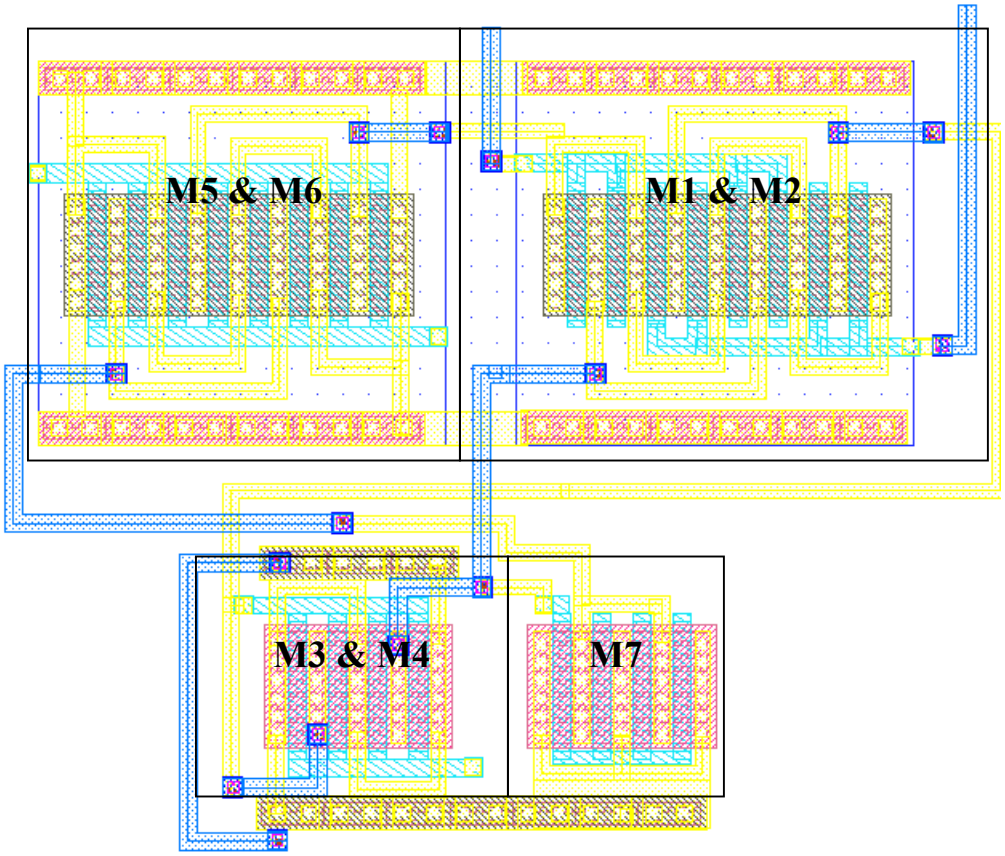


Figure 4.43 Layout of the Op-Amp

The operation of the op-amp was verified by placing it in the inverting configuration and applying a triangular input voltage that varied from 0 V to 3.3 V with a frequency of 62.5 kHz. The closed-loop gain of the inverting configuration is one-half. Alternatively, the signal output voltage is ideally half the input voltage of the circuit. The signal error was measured as the difference between the signal input voltage less twice the signal output voltage. The simulation results of the op-amp are given in Figure 4.44.

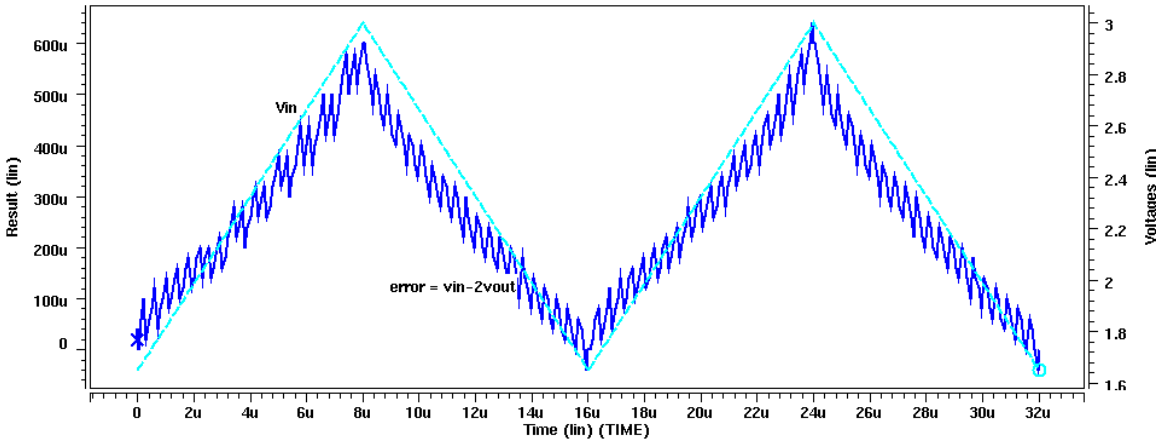


Figure 4.44 Simulation Results of the Op-Amp of the Input Circuit

Figure 4.44 shows the signal error is less than 0.7 mV. However, the voltage at the output of the op-amp in the input circuit has an error less than 0.1 mV for an input frequency of 62.5 kHz. Furthermore, when the input circuit of Figure 4.38 is simulated with an ideal op-amp, the accuracy of the input circuit is not improved. Thus, the op-amp does not cause errors in the input circuit. The dc gain and the bandwidth of the op-amp as computed by HSPICE is 73 dB and 900 kHz, respectively. The power dissipation of the op-amp for a constant input voltage of 1.6 V is 0.3 mW measured over a period of 7.2 μs.

The current sources of the input circuit are implemented with regulated-cascode current sources to ensure constant bias currents. The bias current I_{b1} was implemented using a 200 μA PMOS regulated-cascode current source, and the bias current I_{b2} was implemented using a 200 μA NMOS regulated-cascode current source. The current

sources are identical to those used as the bias current J of the regulated-cascode current copiers. The parameters of the current sources were given previously in Section 4.5.

4.8 Floor Plan of the ADC

The layout of the analog portion of our ADC is given in Figure 4.45.

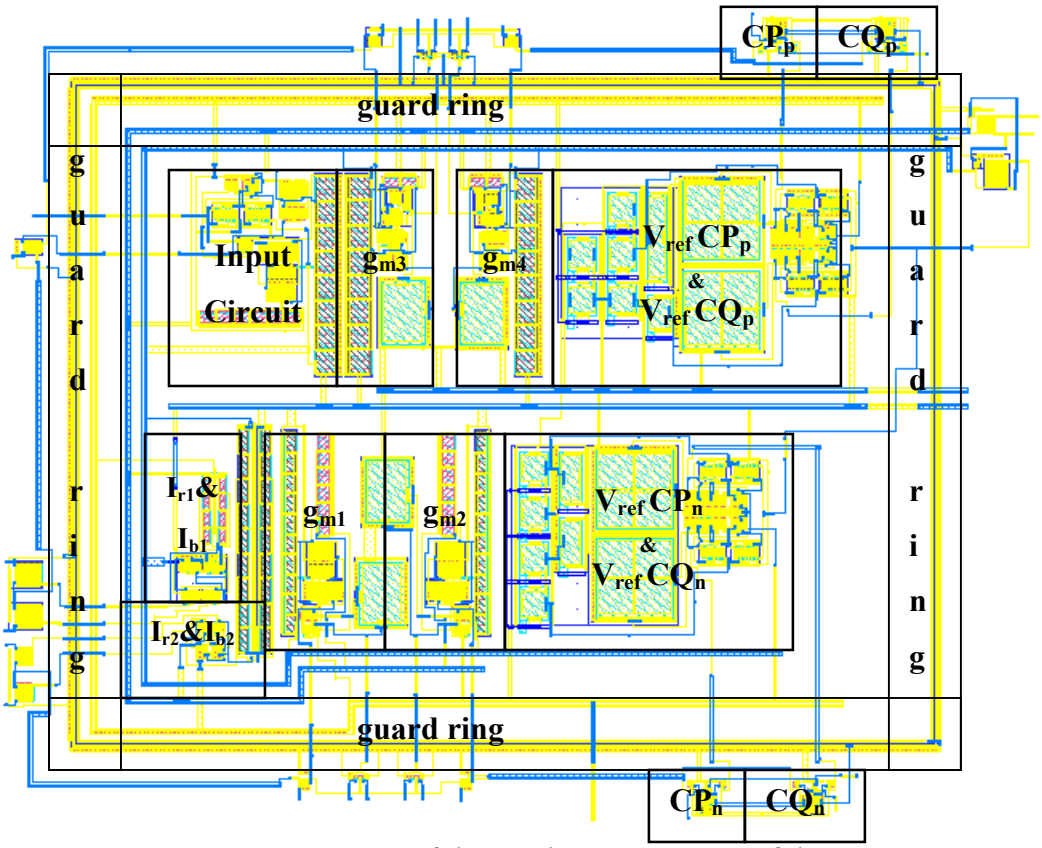


Figure 4.45 Layout of the Analog Component of the ADC

The major components of Figure 4.1 are labeled. The analog components are inside a guard ring to minimize digital noise. The switches of Figure 4.1 are outside the guard ring since they are controlled by digital clock signals and, hence, are coupled to noisy digital signals. The switches are not labeled in the figure but can be found outside the guard ring of the ADC. The area of the analog component of our ADC is 514 x 663 μm^2.

4.9 Digital Components of the Analog-to-Digital Converter

Digital logic controls the switches of the ADC and decodes the P and Q outputs of the ADC to generate binary output words. The digital logic also controls the variable resolution of the ADC. The finite-state machine used to control the switches of the ADC, the variable resolution technique, and the RSD decoder are discussed in this section. The author of this thesis developed the digital logic design. However, the hardware implementation of the digital logic described here was developed by Nate August and Steven Richmond of Virginia Tech [2].

4.9.1 Input/output signals

We discuss the input and output signals of the digital component of our ADC in this section. The digital component of the ADC is controlled by a clock signal, a load signal, a start signal, and an 11-bit word resolution. The output of the ADC is a 12-bit word. All synchronous elements of the digital component of the ADC are rising-edge active. The block diagram of the digital component of our ADC is given in Figure 4.46.

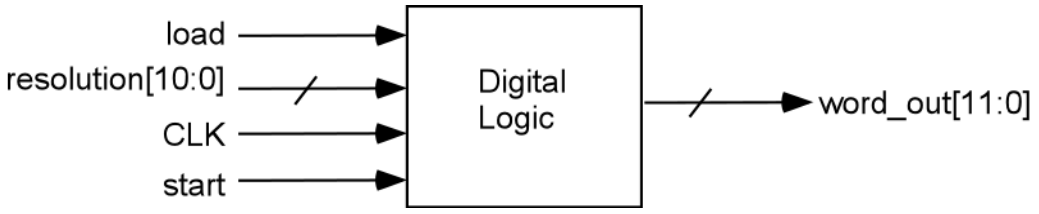


Figure 4.46 Block Diagram of the Digital Component of the ADC

The input signals of the ADC are resolution, load, start, and clock. The output of the digital component is the 12-bit word_out. Resolution is an 11-bit input that specifies the chosen resolution of the ADC. The resolution input has the form "00...011...1" where the first p bits are '0' and the remaining q bits are '1'. The resolution of the ADC is set to (q+1) bits. For instance, if resolution is "000 1111 1111", the resolution of the ADC is

nine bits. If resolution is "00...0", then the resolution is one bit, which is the minimum resolution of our ADC.

The load signal causes the ADC to load the new resolution. The load signal is synchronous with the operation of the ADC. When load is high, the resolution of the ADC is dynamically changed to that indicated by the 11-bit resolution input.

The system clock CLK is a 1.7 MHz square wave with a 25% duty cycle. The purpose of a 25% duty cycle is discussed in Section 4.9.3. The start signal is used to synchronize an internal clock signal slow_clk with the system clock and is synchronous with the system clock. When the start signal changes to '0', the system starts.
The ADC produces a 12-bit output word word_out, which is the signed, two's complement equivalent of the redundant signed-digit (RSD) output word of the analog component of the ADC. The ADC is designed to have an input voltage range corresponding to a specific word_out shown in Table 4.8 when the resolution of the ADC is set to 12 bits. The corresponding input voltage range is found by assuming the total impedance of the input circuit and the off-chip resistance is 22.75 kΩ. Hence, a current step of I_{LSB} corresponds to the voltage step of I_{LSB}*22.75 kΩ. The output word is in two's complement form.

Table 4.8 The Input Voltage Range and the Corresponding 12-bit Output Word

Input Voltage Range	**Corresponding Input Current Range (μA)**	**word_out**
<1.4505	< 0.0220	1000 0000 0001
1.4505 - 1.4510	0.0220 - 0.0439	1000 0000 0001
⋮	⋮	⋮
2.4737 - 2.4742	45 - 45.0220	0000 0000 0000
2.4742 - 2.4747	45.0220 - 45.0439	0000 0000 0001
⋮	⋮	⋮
3.4963 - 3.4968	89.9561 - 89.9780	0111 1111 1110
>3.4968	> 89.9780	0111 1111 1111

The lower bound of the input current range corresponds to $(2^i-1)*I_{LSB}$ (which is $(2^i-1)*90\ \mu A/2^{12}$) for the i^{th} output word. The upper bound of the input current range corresponds to 2^i*I_{LSB}. Note that the output word of the ADC is symmetric about zero and ranges from the most negative number represented by an n-bit number plus one to the most positive number represented by an n-bit number.

The most significant bit (MSB) of word_out is the sign bit of the output word. The remaining 11 bits correspond to the magnitude of the output word when the resolution of the ADC is set to 12 bits. If the resolution of the ADC is less than 12 bits, the output word is signed-extended. When the resolution of the ADC is set to n bits, the first 13-n bits are sign-extended bits, and the remaining n-1 bits represent the magnitude of the output word. For example, if the resolution is set to eight bits and the input current is 0 μA, the output word is "1111 1000 0001". The output word is the two's complement equivalent of –127. Furthermore, if the resolution is set to eight bits and the input current is 90 μA, the output word is "0000 0111 1111", which is equivalent to 127. Only the underlined bits are significant.

The sign bit and the next MSB are produced first, and then the remaining bits are sequentially generated. For instance, if the resolution is set to nine bits and the input current is 90 μA, word_out is generated as follows:

"0000 0000 0001"
"0000 0000 0011"
"0000 0000 0111"
⋮
"0000 0111 1111"
"0000 1111 1111".

If the resolution is set to nine bits and the input current is 0 μA, word_out is generated as follows:

"1111 1111 1110"
"1111 1111 1101"
"1111 1111 1001"
⋮
"1111 1000 0001"
"1111 0000 0001".

4.9.2 Overview of operation

In this section, we discuss the overall operation of the digital component of our ADC. The relationships between the different components of our ADC are described. The digital component of the ADC can be broken into four blocks, which include the switch controller, the resolution controller, the RSD decoder, and a clock divider. The block diagram of the overall system is shown in Figure 4.47.

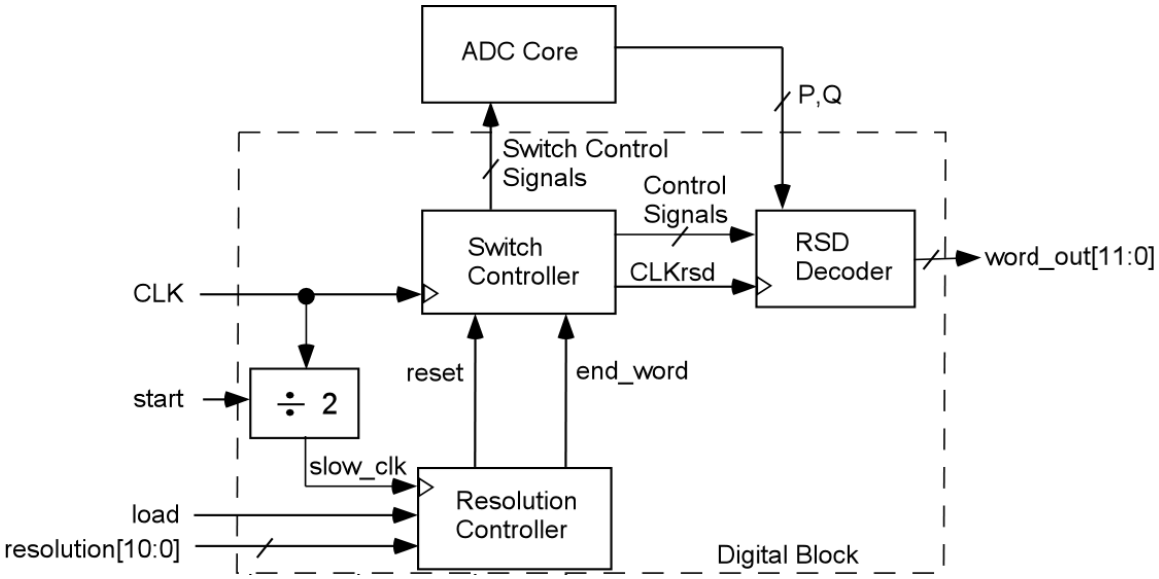


Figure 4.47 Block Diagram of the ADC

The switch controller controls the switches of the ADC architecture and the four comparators of Figure 4.1. The switch controller also controls the decoding process of the P and Q output bits of the ADC. The switch control signals are those necessary to implement the initial bit cycle, the m^{th} bit cycle, and the $(m+1)^{th}$ bit cycle described in Section 4.3. The output signals of the switch controller are described in more detail in the next section.

The resolution controller controls the resolution of the ADC. Specifically, the reset and end_word output signals of the resolution controller control when the ADC is placed in standby mode. The 11-bit resolution input of the resolution controller

determines the resolution of the ADC. When the load signal is asserted, the new resolution is loaded into the resolution controller, and the resolution controller asserts the end_word and reset signals. When end_word goes high, 12 bit cycles have been completed. When resolution goes high, n bit cycles have been completed for an n-bit resolution. When reset and end_word are '1' and '0', respectively, the ADC is placed in standby mode by the switch controller. The clock signal of the resolution controller is half the frequency of the clock signal used by the switch controller. In fact, the resolution controller operates at the rate bits are produced by the ADC.

The divide-by-two frequency divider generates the clock of the resolution controller. The frequency divider divides the clock frequency of the switch controller by two, generating the slow_clk signal. The start signal is used to reset the frequency divider to ensure the CLK signal and the slow_clk signal are in phase. The start signal is synchronous with the CLK signal.

The RSD decoder decodes the P and Q output bits of the ADC to produce the two's complement equivalent of the RSD output. The clock signal CLKrsd and the control signals of the RSD decoder are synchronized with the switch controller. The CLKrsd signal occurs one bit cycle after the ADC produces the P and Q bits. As a consequence, the P and Q bits are decoded one bit cycle after the ADC produces them. The output of the ADC, word_out, is completed 2n-1 CLK cycles after load is asserted for an n-bit resolution.

The timing diagram of the ADC for a 4-bit resolution is shown in Figure 4.48, and the timing diagram for a 12-bit resolution is given in Figure 4.49. Note the start signal is not included since it is used only for initialization purposes at system startup.

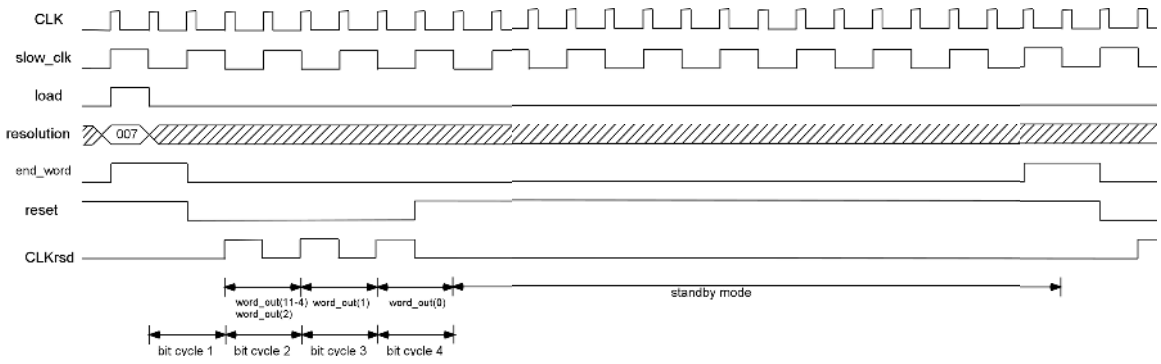


Figure 4.48 Timing Diagram of the ADC for a 4-bit Resolution

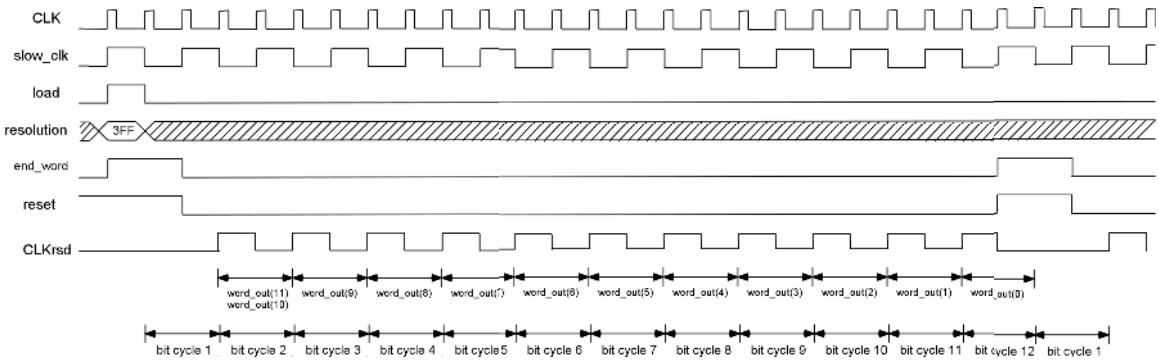


Figure 4.49 Timing Diagram of the ADC for a 12-bit Resolution

Figure 4.48 shows the ADC is placed in standby mode after four bits have been produced for a 4-bit resolution. Figure 4.49 shows 12 bits are produced by the digital component every 12 bit cycles and the ADC begins conversion on the next analog sample immediately after 12 bit cycles have been completed. Thus, no latency is required between output words. Also, the timing diagrams show that the sign bit and the next MSB are produced during the second bit cycle. Bits are produced sequentially thereafter. The output word is completed seven clock cycles after load is asserted for a 4-bit resolution, and the output word is completed 23 clock cycles after load is asserted for a 12-bit resolution.

4.9.3 Implementation of the switch controller

The switch controller consists of a finite-state machine (FSM) and additional logic to control the RSD decoder and to control the comparators of the ADC. The logic used to control the RSD decoder is discussed in Section 4.9.6. The implementation of the FSM and the logic used to generate the strobe signals of the comparators are discussed in this section.

A Mealy-type FSM is used to generate the control signals of the switches of our ADC that are necessary to implement the RSD algorithm described in Section 4.3. The state transition table of the FSM is given in Table 4.9.

Table 4.9 State Transition Table of the FSM

Present State	**Next State**			**Output**		
Inputs	NS0	NS1	NS2	P(m-1) = 1	Q(m-1) = 1	P(m-1) = Q(m-1) = 0
S0	S0	S1	S1			
S1	X	X	S2	$\boldsymbol{\phi_{in}}$, ϕ_{1a}, ϕ_{1b}	$\boldsymbol{\phi_{in}}$, ϕ_{1a}, ϕ_{1b}	$\boldsymbol{\phi_{in}}$, ϕ_{1a}, ϕ_{1b}
S2	X	X	S3	$\boldsymbol{\phi_{in}}$, ϕ_{2a}, ϕ_{2b}	$\boldsymbol{\phi_{in}}$, ϕ_{2a}, ϕ_{2b}	$\boldsymbol{\phi_{in}}$, ϕ_{2a}, ϕ_{2b}
S3	X	X	S4	$\boldsymbol{\phi_{Ib1}}$, $\boldsymbol{\phi_{3a}}$, $\boldsymbol{\phi_{3b}}$, ϕ_{1b}, ϕ_{2b}, $\boldsymbol{\phi_{Ir1}}$	$\boldsymbol{\phi_{Ib1}}$, $\boldsymbol{\phi_{3a}}$, $\boldsymbol{\phi_{3b}}$, ϕ_{1b}, ϕ_{2b}, ϕ_{Ir2}	$\boldsymbol{\phi_{Ib1}}$, $\boldsymbol{\phi_{3a}}$, $\boldsymbol{\phi_{3b}}$, ϕ_{1b}, ϕ_{2b}
S4	S0	S1	S5	$\boldsymbol{\phi_{Ib1}}$, $\boldsymbol{\phi_{4a}}$, $\boldsymbol{\phi_{4b}}$, ϕ_{1b}, ϕ_{2b}, $\boldsymbol{\phi_{Ir1}}$	$\boldsymbol{\phi_{Ib1}}$, $\boldsymbol{\phi_{4a}}$, $\boldsymbol{\phi_{4b}}$, ϕ_{1b}, ϕ_{2b}, ϕ_{Ir2}	$\boldsymbol{\phi_{Ib1}}$, $\boldsymbol{\phi_{4a}}$, $\boldsymbol{\phi_{4b}}$, ϕ_{1b}, ϕ_{2b}
S5	X	X	S6	ϕ_{Ib2}, ϕ_{1a}, ϕ_{1b}, $\boldsymbol{\phi_{3b}}$, $\boldsymbol{\phi_{4b}}$, ϕ_{Ir2}	ϕ_{Ib2}, ϕ_{1a}, ϕ_{1b}, $\boldsymbol{\phi_{3b}}$, $\boldsymbol{\phi_{4b}}$, $\boldsymbol{\phi_{Ir1}}$	ϕ_{Ib2}, ϕ_{1a}, ϕ_{1b}, $\boldsymbol{\phi_{3b}}$, $\boldsymbol{\phi_{4b}}$
S6	S0	S1	S3	ϕ_{Ib2}, ϕ_{2a}, ϕ_{2b}, $\boldsymbol{\phi_{3b}}$, $\boldsymbol{\phi_{4b}}$, ϕ_{Ir2}	ϕ_{Ib2}, ϕ_{2a}, ϕ_{2b}, $\boldsymbol{\phi_{3b}}$, $\boldsymbol{\phi_{4b}}$, $\boldsymbol{\phi_{Ir1}}$	ϕ_{Ib2}, ϕ_{2a}, ϕ_{2b}, $\boldsymbol{\phi_{3b}}$, $\boldsymbol{\phi_{4b}}$

X denotes a "don't care".
NS0 denotes Reset End_word = 10.
NS1 denotes End_word = 1.
NS2 denotes Reset = 0.
Bold signals ($\boldsymbol{\phi_{in}}$, $\boldsymbol{\phi_{Ib1}}$, $\boldsymbol{\phi_{Ir1}}$, $\boldsymbol{\phi_{3a}}$, $\boldsymbol{\phi_{3b}}$, $\boldsymbol{\phi_{4a}}$, $\boldsymbol{\phi_{4b}}$) are active-low.

State S0 of the FSM is a special state called the *standby state*, where all the control signals of the switches of the ADC are inactive. In other words, the control voltages of the NMOS switches of Figure 4.1 are '0', and the control voltages of the PMOS switches are '1'. All switches of the ADC are open, and the ADC is in standby mode, which dissipates the least amount of power. The ADC remains in standby mode when reset = '1' and end_word = '0'. The standby state is described in detail in Section 4.11.

States S1 and S2 in the table correspond to the initial bit cycle of the ADC described in Section 4.3.5. The active outputs of the FSM are ϕ_{in}, ϕ_{1a}, and ϕ_{1b} in state S1, and the active outputs are ϕ_{in}, ϕ_{2a}, and ϕ_{2b} in state S2. The next two states, S3 and S4, correspond to the m^{th} bit cycle, which are described in Section 4.3.1 and Section 4.3.2. The last two states, S5 and S6, correspond to the $(m+1)^{th}$ bit cycle, which are described in Section 4.3.3 and Section 4.3.4. The ϕ_{Ir1} and ϕ_{Ir2} signals are activated depending on the values of the P and Q bits produced in the previous bit cycle, denoted P(m-1) and Q(m-1)

in the state transition table. The denotation is used for the purpose of brevity. The inputs corresponding to P(m-1) and Q(m-1) are actually four different input signals. In states S3 and S4, P(m-1) corresponds to the latched P(m+1) output of the ADC, and Q(m-1) corresponds to the latched Q(m+1) output of the ADC. In states S5 and S6, P(m-1) corresponds to the latched P(m) output of the ADC, and Q(m-1) corresponds to the latched Q(m) output of the ADC. Note that the FSM can enter S0 or S1 after leaving the S4 or S6 state.

When the load signal is applied to the digital component of the ADC, the FSM enters the state S1 since end_word is set to '1'. Thus, the conversion process for a new output word begins after load is applied, regardless of the present state of the FSM. This characteristic allows the word-rate of the ADC to be changed dynamically. If an n-bit ADC is desired, the ADC can be forced to produce an output word every n bit cycles by loading a new resolution every n slow_clk cycles. However, this characteristic was not employed for our simulations.

We used a Gray code shown in Table 4.10 for the state encoding for the seven states.

Table 4.10 State Encoding of the FSM

State	**Code ($Q_2Q_1Q_0$)**
S0	000
S1	001
S2	011
S3	111
S4	110
S5	100
S6	101

The logic equations developed for the output signals of the FSM are as follows [2]:

$\phi_{in} = (Q_2' Q_0)'$
$\phi_{Ib1} = (Q_2Q_1)'$
$\phi_{Ib2} = Q_2Q_1'$

$\phi_{1a} = (Q_2 \oplus Q_0)\, Q_1'$
$\phi_{1b} = Q_2'Q_1'Q_0 + Q_2(Q_1 + Q_0')$
$\phi_{2a} = (Q_2 \oplus Q_1)Q_0$
$\phi_{2b} = Q_2Q_1 + Q_2Q_0 + Q_1Q_0$
$\boldsymbol{\phi_{3a}} = (Q_2Q_1Q_0)'$
$\boldsymbol{\phi_{3b}} = Q_2' + Q_1Q_0'$
$\boldsymbol{\phi_{4a}} = (Q_2Q_1Q_0')'$
$\boldsymbol{\phi_{4b}} = Q_2' + Q_1Q_0$
$\boldsymbol{\phi_{Ir1}} = (\, P(\hat{m+1})\,(Q_2Q_1 + Q(\hat{m})\, Q_2Q_1')'$
$\phi_{Ir2} = Q(\hat{m+1})\, Q_2Q_1 + P(\hat{m})\, Q_2Q_1'.$

In the logic equations the tick mark, ', denotes the logical NOT function. For convenience, we use $\hat{X}$ to denote the latched outputs as shown in Figure 4.64. Note $\hat{X}$ is a label and not a logic function.

The three flip-flops of the FSM are implemented as positive-edge triggered true single-phase clocked (TSPC) flip-flops. The circuit diagram is given in Figure 4.50. Andrew Gouldey of Virginia Tech sized the transistors of the flip-flop [10].

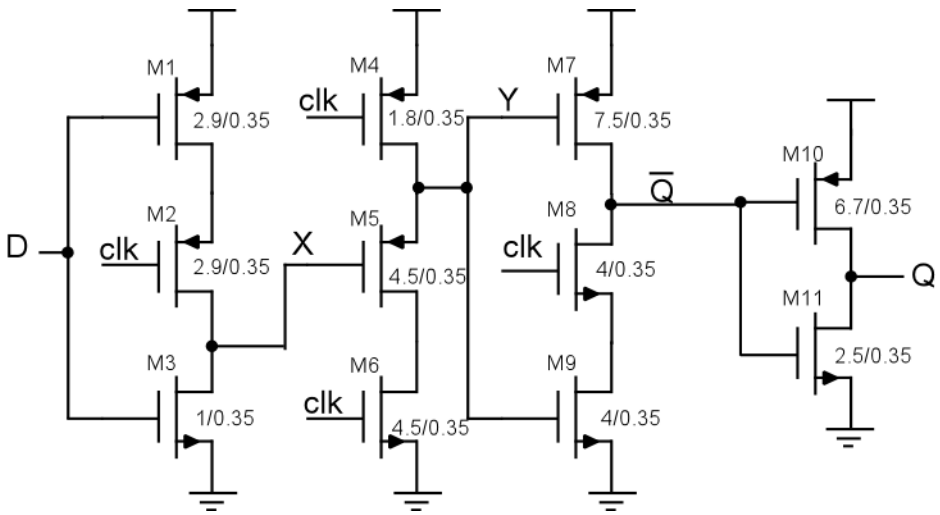


Figure 4.50 TSPC Flip-Flop

The TSPC flip-flop is a dynamic flip-flop where internal gate capacitances are used to hold the state of the flip-flop between positive transitions of the clock. The node X is set to D' and the node Y is set to Vdd when the clk signal is low. The signal Q' is left floating and has the value set in the previous clock cycle. When clk is high, X is the

value set when the clk signal was low, and the node Y is conditionally discharged according to the value of X. If X is Vdd, Y is set to ground. Otherwise, Y remains Vdd. Thus, the output Q is set to the value of D on the rising edge of the clock.

The layout of the FSM is given in Figure 4.51. The FSM layout has an area of 137 x 164 μm^2. The FSM was verified through HSPICE simulations. However, the simulation results are not given here due to the large number of outputs, which are difficult to illustrate concisely.

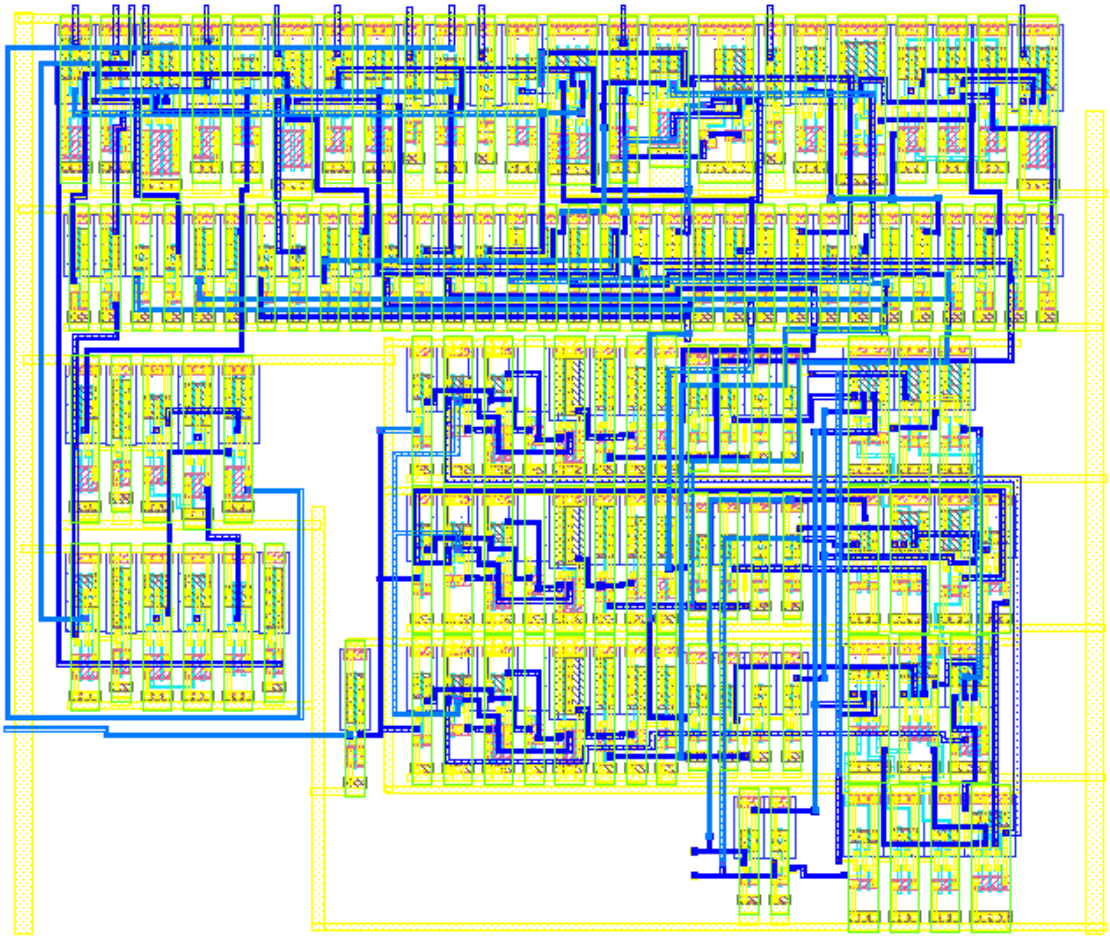


Figure 4.51 Layout of the FSM

The logic used to control the comparators is shown in Figure 4.52.

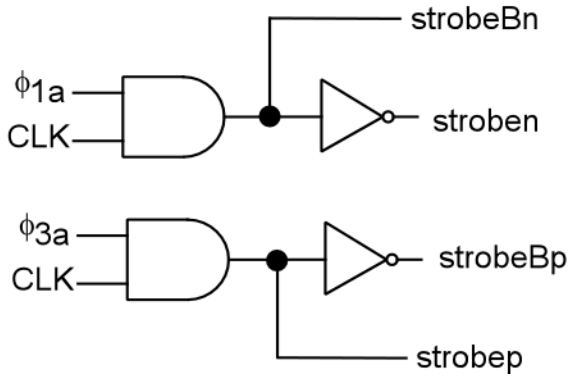


Figure 4.52 Signal Generator of the Strobe Signals

The stroben and strobeBn signals are used to control the comparators that generate the P(m+1) and Q(m+1) bits, and the strobep and strobeBp signals are used to control the comparators that generate P(m) and Q(m). The stroben (strobep) signals are the logical NOT of the strobeBn (strobeBp) signals. The timing diagram of the comparator control signals is given in Figure 4.53. The PS waveform in the timing diagram denotes the present state of the FSM.

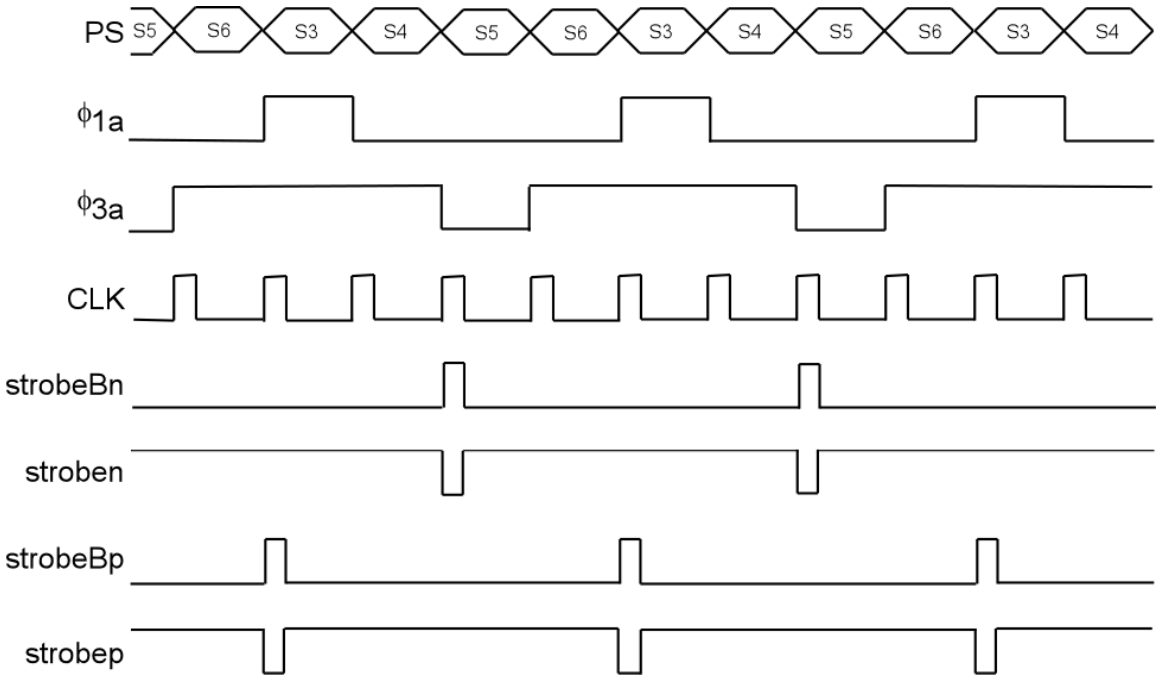


Figure 4.53 Timing Diagram of Control Signals of the Comparators

The strobeB*i* signals are high when the signals controlling the gate switches of the current copiers g_{m1} and g_{m3} are active and the 25% duty cycle clock signal is high. Specifically, the current copiers are storing current when the strobeB*i* signals are high. The strobeB*i* signals transition low after one quarter of the time allowed for the current copiers to settle has elapsed. The gate voltages of the current copiers have settled sufficiently during this period of time to make a comparison. When the strobeB*i* signals transition from high to low, the gate voltages of the current copiers are sampled by the comparators (refer to Section 3.4).

4.9.4 Implementation of the resolution controller

A 12-bit shift register, where the output of the register is fed back to the input of the register, is used to control the resolution of the ADC. The resolution controller is shown in Figure 4.54.

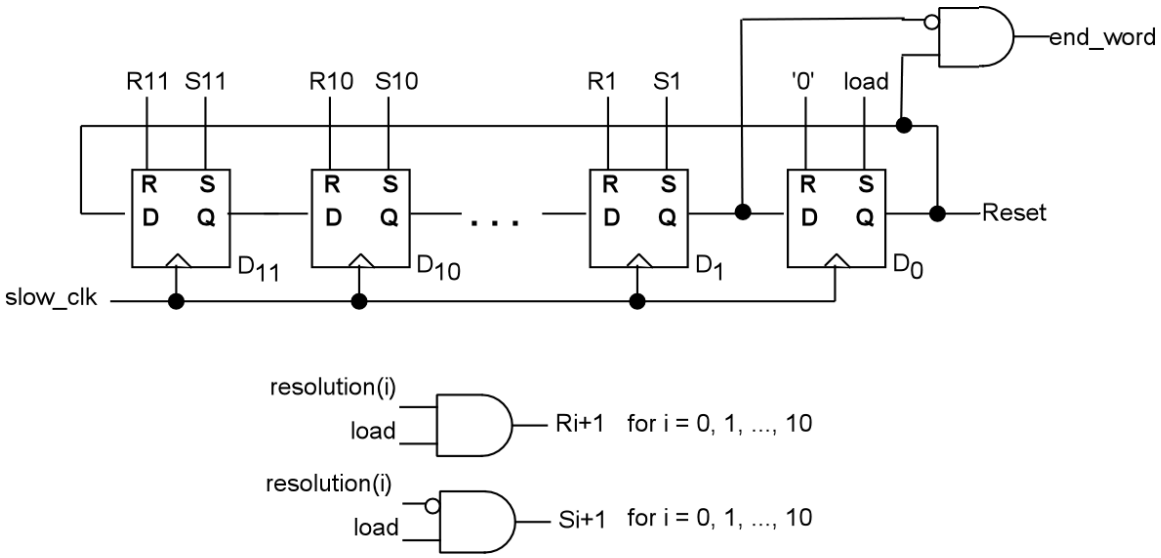


Figure 4.54 Resolution Controller

Each D-type flip-flop of the resolution controller is positive-edge triggered with an *asynchronous* reset and set signal. When the load signal is high, the shift register loads the inverted values of the signal resolution[10:0]. When the load operation is performed, a flip-flop D_{i+1} is set to the complement of resolution(i). Flip-flop D_0 is always set when

load is applied. The load signal is applied the first half of a slow_clk cycle and is synchronous with the CLK signal of the switch controller. The operation of the resolution controller is illustrated for the case of a 4-bit resolution below.

Assume that the signal resolution[10:0] is set to "000 0000 0111" for a 4-bit resolution. When the load signal is applied for the first half of a slow_clk cycle, the contents of the shift register are $D_{11}D_{10}D_9D_8D_7D_6D_5D_4D_3D_2D_1D_0$ = "1111 1111 0001". Both reset and end_word are set to '1'. Since end_word is '1', the FSM described in the previous section enters state S1 upon the rising edge of the CLK signal. During state S1, the sign bit of the output word and the next MSB is generated. On the rising edge of slow_clk, the contents of the resolution controller become "1111 1111 1000", and both end_word and reset are set to '0'. For three slow_clk cycles, end_word and reset are set to '0'. During this time, the FSM goes through the states corresponding to the m^{th}, the $(m+1)^{th}$, and the $(m+2)^{th}$ bit cycles since reset is '0'. The RSD decoder generates four bits during this period. Note that an extra bit cycle is executed by the ADC. The extra bit cycle is required to generate the control signals of the RSD decoder, which will be discussed in Section 4.9.6. Also, end_word is set to '1' after 11 slow_clk cycles. As a consequence, after four bit cycles have occurred, the FSM enters the standby state and remains in the state until either eight slow_clk cycles have occurred or a new resolution is loaded.

The 12 flip-flops of the RSD decoder are implemented as a positive-edge triggered, true single-phase clocked (TSPC) flip-flops with *asynchronous* set and reset. The circuit diagram is given in Figure 4.55.

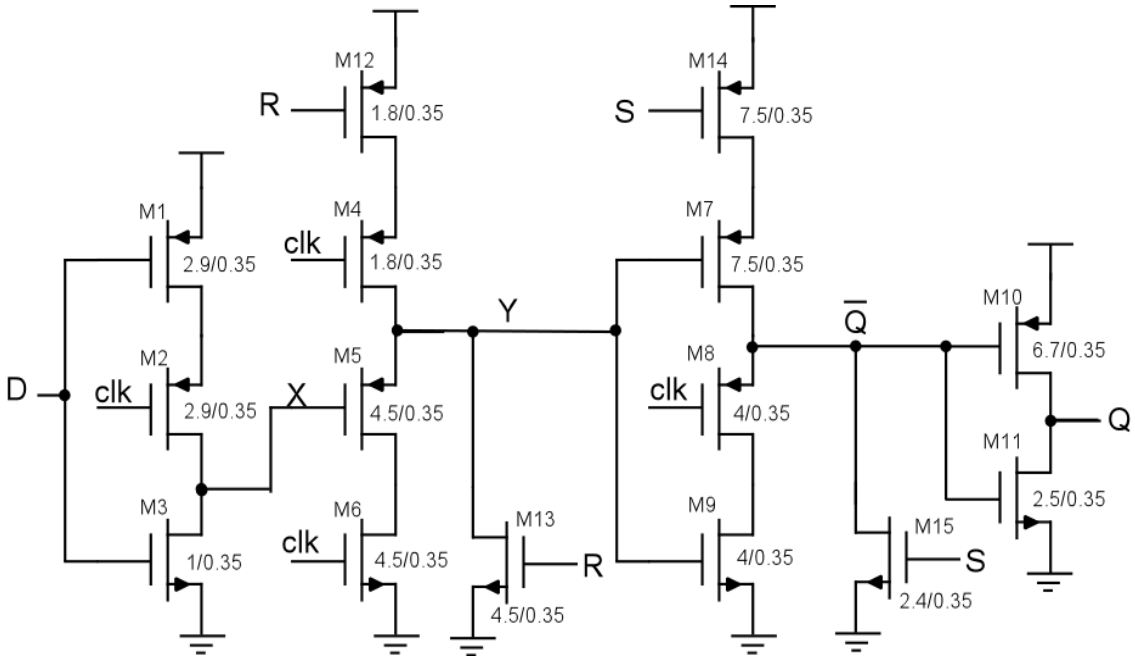


Figure 4.55 TSPC Flip-Flop with Set and Reset

The TSPC flip-flop operates identically to the TSPC flip-flop of Figure 4.50 when set and reset are not active. When the reset signal (R) is high, the node Y is set to ground by the transistor M13, and X is set to NOT(D). The transistor M12 prevents a path from Vdd to ground through the transistors M4 and M13. Thus, Q is set to ground.

If the set signal (S) is '1', Q is set to Vdd regardless of the value of the clk signal. If the clk signal is high and the set signal is high, the node X is the value set when the clock was low, and Q' is set to ground by the transistor M15. The node Y is conditionally discharged according to the value of X. If the clk signal is low, Y is set to Vdd, and Q' is the value set when the clock signal was high. Thus, if the set signal becomes active when clk is high and remains active until the clock transitions low, Q remains at Vdd for the entire clock period. However, a problem occurs if the set signal becomes active when clk is low and becomes inactive after the clk signal transitions high. Under this condition, the value of Q is the value of D sampled at the rising edge of the clock since the node voltages X and Y are not changed when the set signal is asserted. Thus, *the set signal can only be applied on the rising edge of the clk signal and must last less than an entire clk cycle*.

The problem is avoided when the load signal occurs on the rising edge of the slow_clk signal and is high for one cycle of the CLK signal. The limitation is acceptable

since latency is introduced into the output word if the reset and set signals of the resolution controller are active the latter half of a slow_clk cycle. If the load signal were active the latter half of a slow_clk cycle, the reset and end_word signals would be delayed one bit cycle. The reset and end_word signals would be delayed since the setup time of the flip-flops of the resolution controller would not be met until one slow_clk cycle after load was unasserted. The delay of the reset and end_word signals would introduce latency into the ADC. Since latency is not desirable, the limitation of the TSPC flip-flop of Figure 4.55 is acceptable.

The circuit to generate an appropriate load signal is found in Figure 4.56. The circuit of Figure 4.56 is not implemented in the digital component of our ADC and can be implemented off-chip. The $\hat{load}$ signal is the asynchronous version of the load signal.

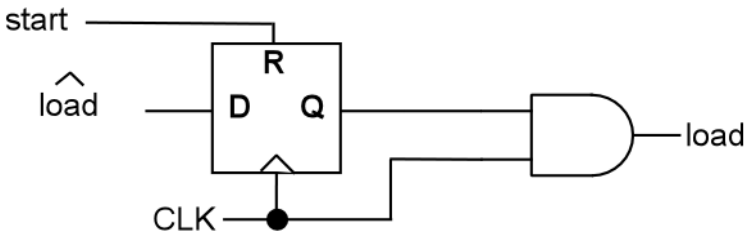


Figure 4.56 Circuit to Generate the Signal load

The layout of the resolution controller is given in Figure 4.57. The area of the layout is 78 x 437 μm^2.

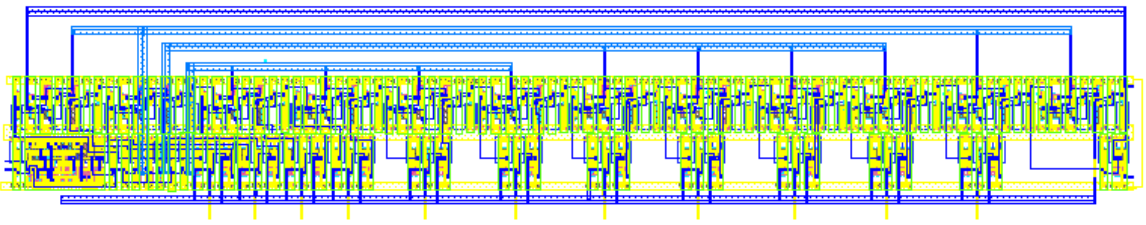


Figure 4.57 Layout of the Resolution Controller

The resolution controller was verified using HSPICE. The simulation results for a 4-bit resolution (resolution = "000 0000 0111") are given in Figure 4.58. The end_word, reset, load, and slow_clk signals are shown in the figure.

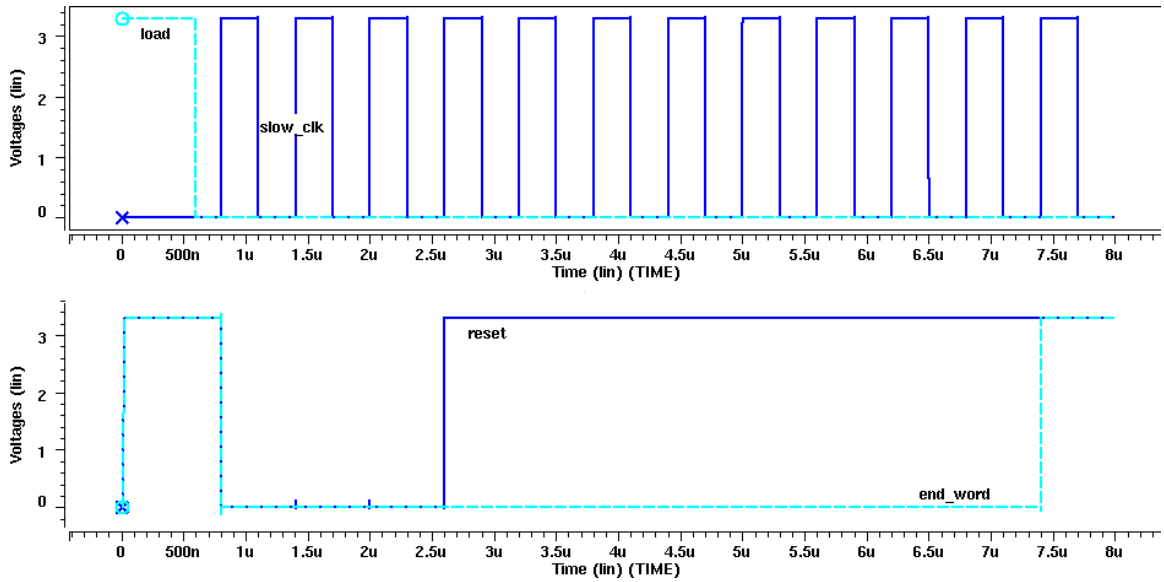


Figure 4.58 Simulation Results of the Resolution Controller

The simulation results show the reset signal goes high after three slow_clk cycles and the end_word signal goes high 11 slow_clk cycles after load is unasserted. Hence, the resolution controller behaves as expected.

4.9.5 Frequency divider

The frequency divider generates the slow_clk signal. The frequency divider is implemented with a static D-type flip-flop. The flip-flop is a standard cell (cell wdrp_4) in the CMC standard cell library for the TSMC 0.35 µm technology. A standard cell is used since it has higher drive strength than the TSPC D-type flip-flop of Figure 4.55. Higher drive strength is required since the slow_clk signal drives the 12 flip-flops of the resolution controller. The logic diagram of the frequency divider is given in Figure 4.59.

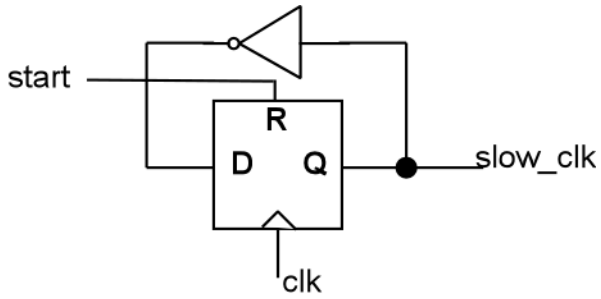


Figure 4.59 Frequency Divider

The start signal is used to initialize the frequency divider and synchronize the slow_clk signal with the system clock. Also, the start signal ensures the slow_clk signal is in phase with the system clock. The start signal is active high and is synchronous with the system clock. The timing diagram for the frequency divider is given in Figure 4.60.

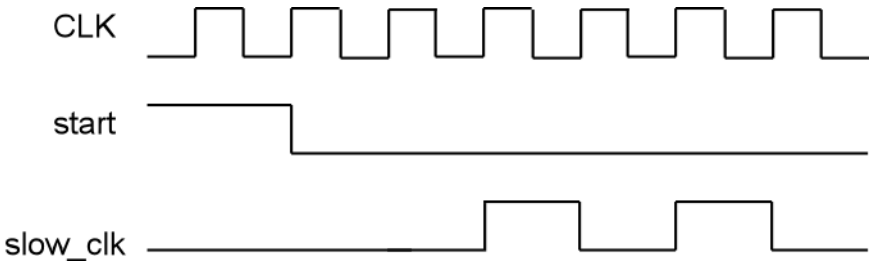


Figure 4.60 Timing Diagram for the Frequency Divider

4.9.6 Implementation of the RSD decoder

The P and Q outputs of our n-bit ADC are 2(n-1) bits in total. Recall b_i = '1' is represented by P_iQ_i' = "10", b_i = '0' is represented by P_iQ_i' = "00", and b_i = '-1' is represented by P_iQ_i' = "01". The decimal equivalent of a number represented in the RSD format can be found by performing

$$word\_out_{10} = \sum_{i=0}^{n-2} 2^i b_i \,,$$

where n is the resolution of the ADC, b_i = {-1,0,1}, and $word\_out_{10}$ is the base ten form of the RSD number.

Ginetti proposed a decoder circuit that decodes a serial RSD word to a two's complement binary number [9]. A 12-bit decoder suited for our ADC is shown in Figure 4.61.

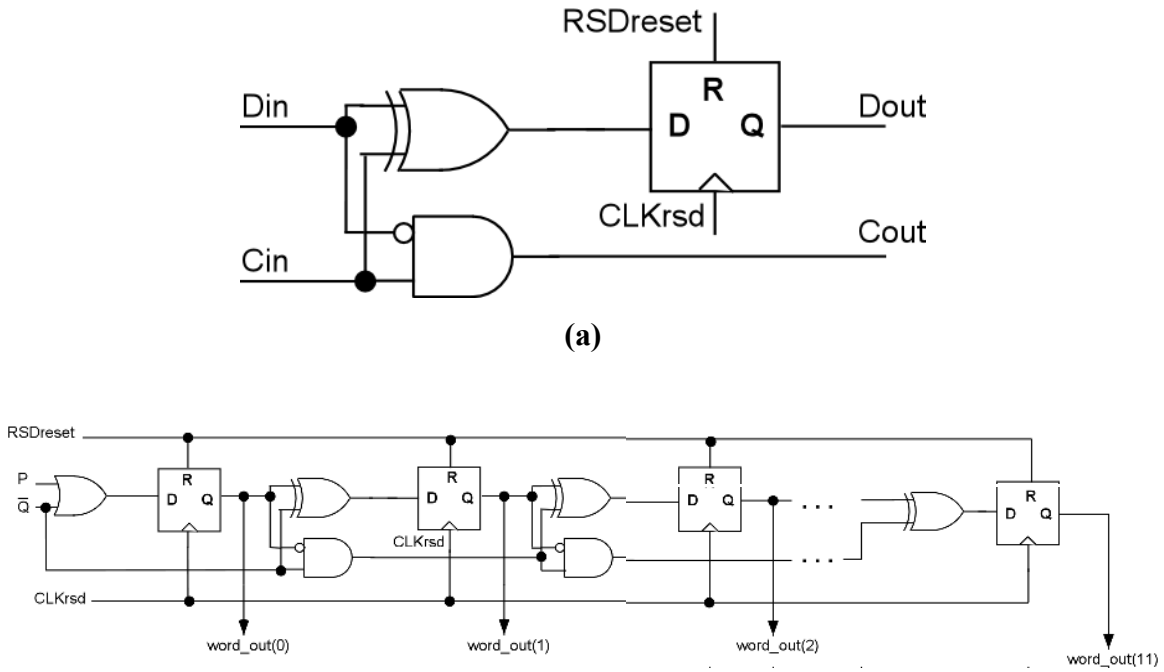


Figure 4.61 **(a)** RSD Decoder Cell **(b)** Serial RSD to Two's Complement Decoder [9]

The RSD decoder cell in Figure 4.61 (a) performs 1-bit subtraction as shown in Table 4.11. Dout is the resultant bit, and Cout is the carry out bit, which corresponds to the sign of the result.

Table 4.11 Operation for a 1-bit Subtraction

Din	Cout	Dout	Cout
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

The 12-bit RSD decoder is a cascade of 12 RSD decoder cells. Note that the first and last cells of the decoder are degenerated. The RSDreset signal and CLKrsd signals are generated by the switch controller and are synchronous with the FSM. When P_iQ_i' = "10" (b_i = '1'), the decoder holds the value 2N+1 (which is 2N+b_i) after a positive clock edge, where N is the binary number stored in the decoder before the clock edge. When P_iQ_i' = "01", the decoder holds 2(N-1)+1 = 2N-1 (which is 2N-b_i) after the clock edge. Finally, when P_iQ_i' = "00", the decoder holds 2N. Therefore, the decoder performs the necessary conversion

$$word\_out_{10} = \sum_{i=0}^{n-2} 2^i b_i \ .$$

The RSDreset signal and CLKrsd signals are generated by the switch controller and are synchronous with the FSM. The RSDreset signal is used to reset the RSD decoder before the output bits of the ADC are decoded, and the CLKrsd signal is used as the clock signal of the decoder. Both signals are synchronous with the state of the FSM.

The logic used to generate the RSDreset signal is given in Figure 4.62.

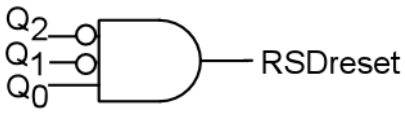


Figure 4.62 RSDreset Signal Generator

The RSDreset signal is active high when the FSM is in state S1. We chose not to reset the decoder in state S0 since the FSM does not enter the standby state for a 12-bit resolution. Since the RSD decoder is reset in state S1, the RSD decoder cannot latch the first P and Q bits generated by the ADC in state S2. The RSD decoder cannot latch the outputs bits P and Q in state S2 since the setup time of the flip-flops would not be met. Thus, the first output bits of the ADC cannot be decoded until the FSM enters state S3, which is one bit cycle after the first bit cycle of the ADC. Thus, the RSD decoder decodes the output bits of the ADC one bit cycle after they are produced. An extra bit cycle must be executed by the FSM in order to decode n-1 P and Q output bits for an n-bit resolution. If an extra bit cycle were not executed, the RSD decoder would fail to decode the bit produced in the $(n-1)^{th}$ bit cycle for an n-bit resolution.

The decoding process begins on the first rising edge of the CLKrsd signal. The CLKrsd signal is generated by the switch controller and is a function of the state of the FSM. The logic diagram for the CLKrsd signal is given in Figure 4.63.

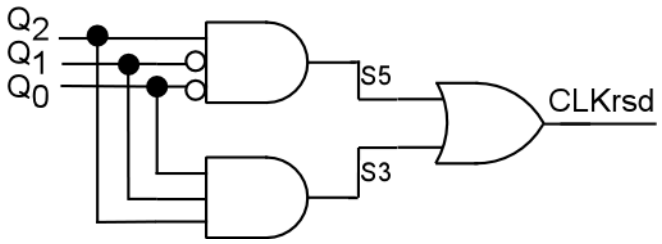


Figure 4.63 Clock Generator of the RSD Decoder

The RSD decoder is triggered when the FSM enters states S3 or S5.

The input of the RSD decoder is the latched, multiplexed version of the P and Q output bits of the ADC. The logic diagram for the input circuit of the RSD decoder is given in Figure 4.64. We use $\hat{X}$ to denote the latched outputs of the ADC.

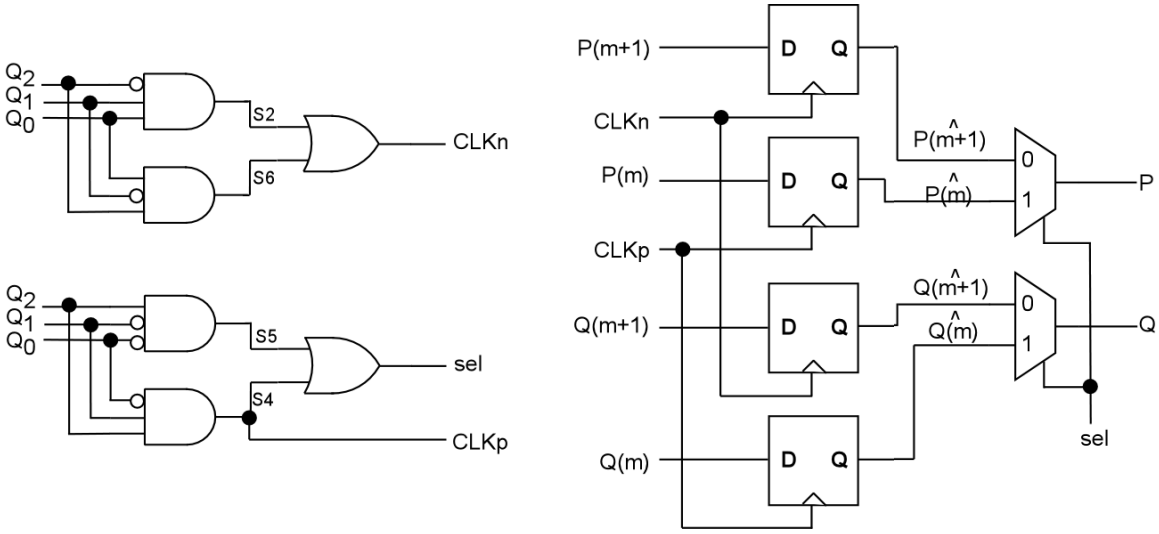


Figure 4.64 Input Circuit of the RSD Decoder

The outputs of the ADC are latched by the input circuit of the RSD decoder in states S2, S4, and S6, which are the states after the P and Q output bits of the ADC are generated. The P(m) and Q(m) bits are latched in the states S2 and S6, and the P(m+1) and Q(m+1) bits are latched in state S4. When the FSM is in the S4 or S5 states, the

inputs of the RSD decoder are selected as the latched P(m) and Q(m) bits, which are denoted $P(\hat{m})$ and $Q(\hat{m})$, respectively. When the FSM is not in the S4 or S5 states, the inputs of the RSD decoder are selected as the latched P(m+1) and Q(m+1) bits, which are denoted $P(\hat{m+1})$ and $Q(\hat{m+1})$, respectively. Note that the latched P and Q bits are those used by the FSM machine.

The timing diagram of the control signals of the RSD decoder is shown in Figure 4.65. The signal PS denotes the present state of the FSM.

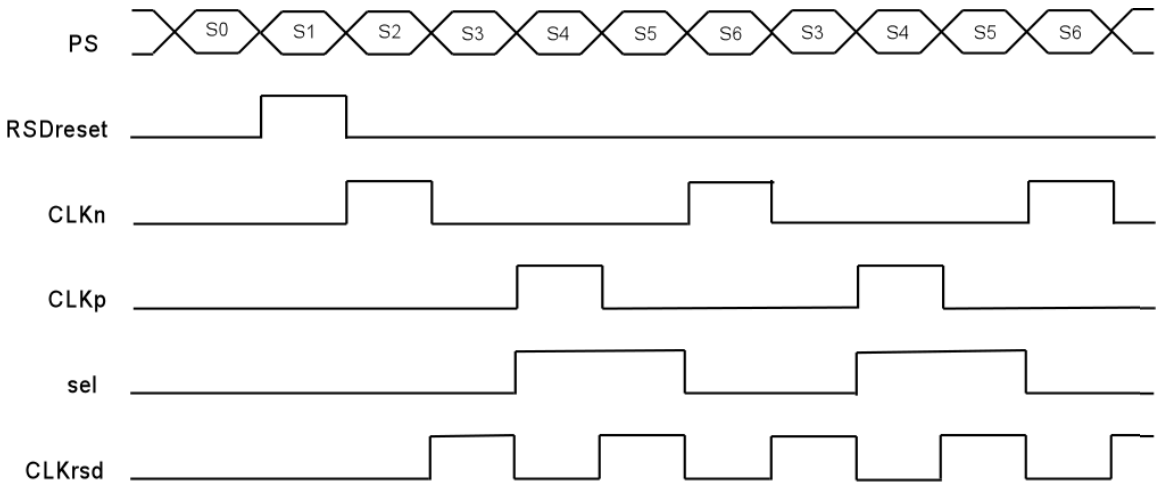


Figure 4.65 Timing Diagram of the RSD Decoder Control Signals

The flip-flops of the RSD decoder are TSPC flip-flops with an asynchronous reset. The circuit of Figure 4.55 is used where transistors M14 and M15 are removed. The circuit diagram of the exclusive-or gate used for the RSD decoder is given in Figure 4.66. Andrew Gouldey of Virginia Tech sized the transistors of the XOR gate [10].

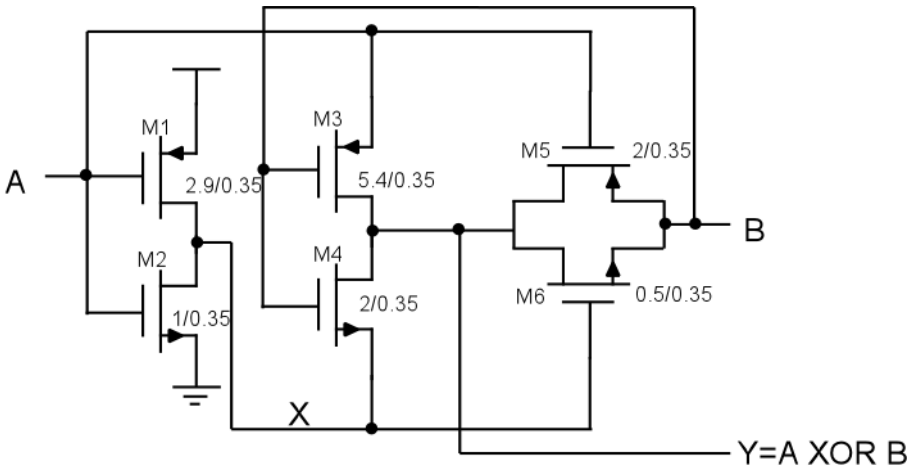


Figure 4.66 Exclusive-OR Gate of the RSD Decoder

The exclusive-or gate is a pass-gate structure. When the input signal A is logic '1', the node X is set to ground. The transistors M3 and M4 act as an inverter that passes Vdd and ground faithfully. The inverter produces the logical not of the input signal B. Thus, for A = '1', the output Y is the logical NOT of the input signal B.

When the input signal A is logic '0', the node X is set to Vdd. The transistors M3 and M4 act as a weak inverter that passes Vdd-V_t for a logic '1' and passes V_t for logic '0', where V_t is the threshold voltage of the transistors M3 and M4. Also, the pass-gate consisting of the transistors of M5 and M6 is turned on. Thus, the input signal B is passed to the output node, assuming that the input signal is stronger than the output of the weak inverter. Thus, the structure of Figure 4.66 implements the function $Y = A\overline{B} + \overline{A}B$.

The layout of the RSD decoder is given in Figure 4.67. Note that the logic used to generate the control signals of the RSD decoder is included in the layout. The area of the layout is 88 x 555 μm^2.

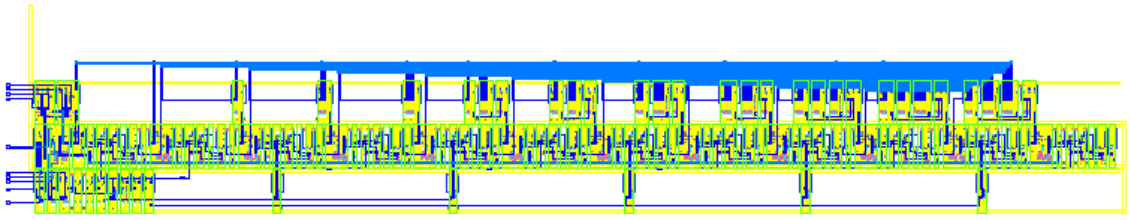


Figure 4.67 Layout of the RSD Decoder

The RSD decoder was verified using HSPICE. The simulation results are given in Figure 4.68.

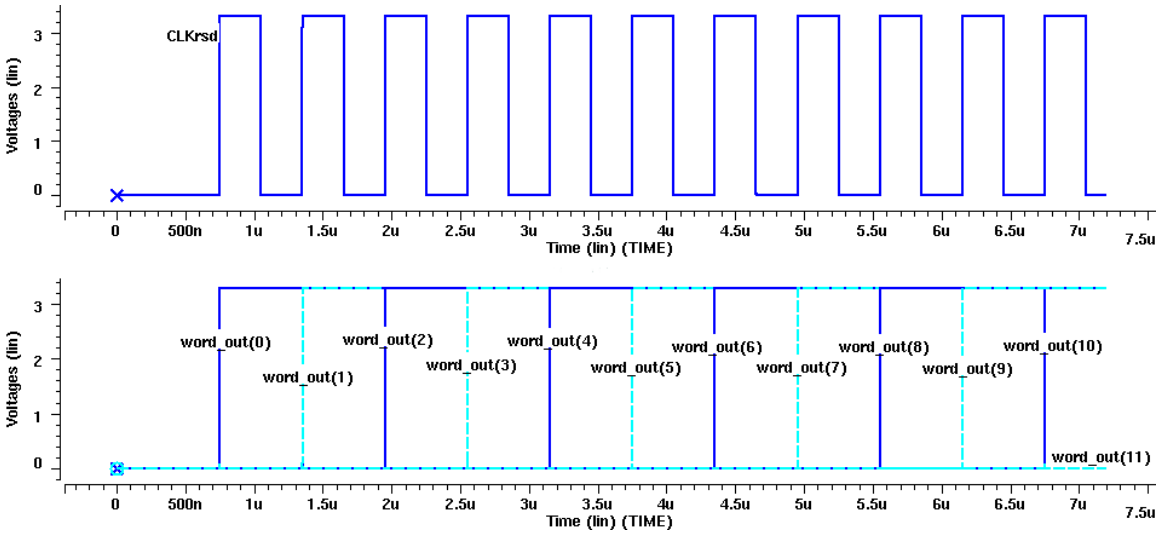


Figure 4.68 Simulation Results of the RSD Decoder

For the simulation P and Q' are set to '1' and '0', respectively. (b_i = '1'). The RSD decoder correctly decodes 11 RSD bits to the output word "0111 1111 1111" after 11 CLKrsd cycles.

4.9.7 Floor plan of digital components

The layout of the digital component of our ADC is shown in Figure 4.69. The major components are labeled. The area of the digital component of the ADC is 433 x 694 μm^2. In the system layout, the large amount of white space was filled with substrate contacts to reduce digital noise in the substrate.

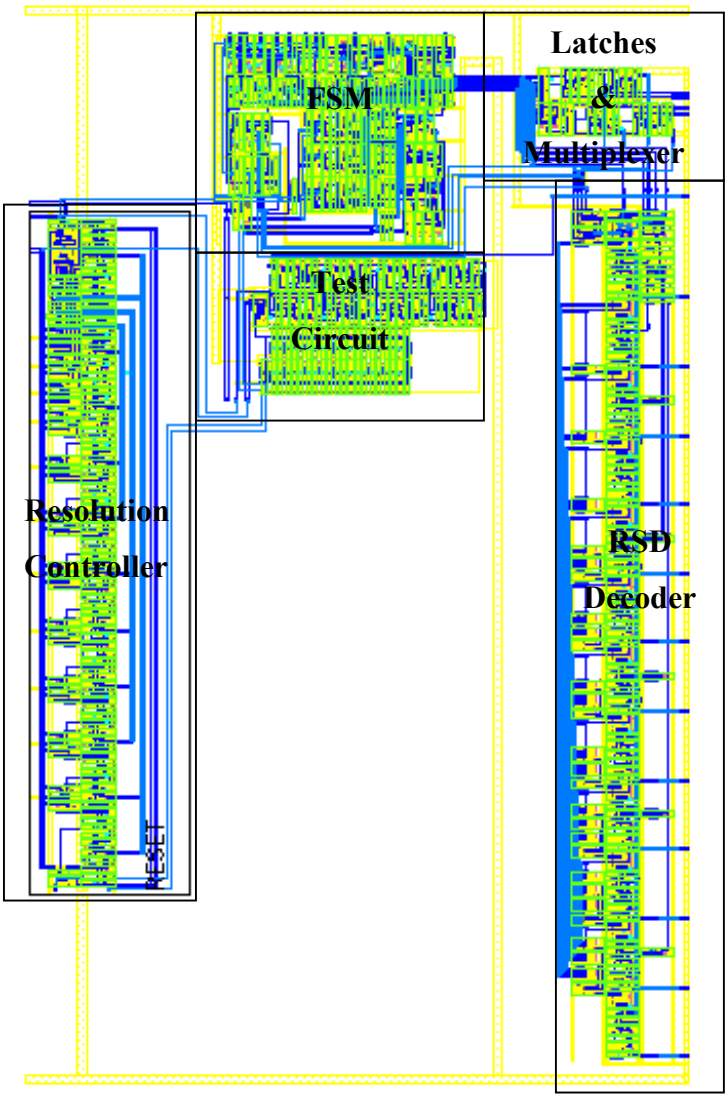


Figure 4.69 Layout of the Digital Component of the ADC [2]

The power dissipation of the digital component of our ADC measured over 12 bit cycles is 0.27 mW for a 12-bit resolution.

4.10 Standby State

Whenever the ADC is not in the process of generating an output, it enters the standby state (which is S0 in Table 4.9). In the standby state, all the switches of the ADC architecture of Figure 4.1 are open. Furthermore, the regulated-cascode current sources

and the input circuit are disabled. Consequently, the power dissipation of the analog core is greatly reduced in the standby state.

In the standby state, all the switches of the ADC architecture in Figure 4.1 are open, and the bias voltages of the NMOS regulated-cascode current sources (refer to Figure 4.16) are set to ground. Since applying ground to the gate of an NMOS transistor turns the transistor off, the regulated-cascode current sources source no current during the standby state. The NMOS regulated-cascode current sources include the current sources I_{r2} and I_{b2} in Figure 4.1, the current source I_{b2} of the input circuit in Figure 4.38, and the bias current J of g_{m3} and g_{m4}, the PMOS regulated-cascode current copiers (refer to Figure 4.11). Thus, these current sources and current copiers dissipate no power during the standby state.

Furthermore, the bias voltage of the PMOS regulated-cascode current sources of the ADC is set to Vdd during the standby state. The PMOS regulated-cascode current sources (refer to Figure 4.22) include the current sources I_{r1} and I_{b1} in Figure 4.1, the bias current I_{b1} of the input circuit, and the bias current J of g_{m1} and g_{m2}, the NMOS regulated-cascode current copiers (refer to Figure 4.6). Since applying Vdd to the gate of a PMOS transistor turns the transistor off, the PMOS current sources source no current during the standby state.

Finally, the bias voltage of the op-amp of the input circuit in Figure 4.38 is set to Vdd. Thus, the op-amp of the input circuit dissipates no power during the standby state. The only analog components dissipating power in the standby state are the reference voltage circuits used by the comparators of the ADC. These components are not disabled since the output voltages of the voltage buffers do not settle within a period of the system clock (which is the signal CLK in Figure 4.46). When the bias voltages of these components are disabled, the ADC core dissipates a total of 1.78 mW over the period necessary to complete 12 bit cycles. The power dissipation is approximately the power dissipation of the four voltage reference circuits of the ADC, which is 1.62 mW.

The circuits given in Figure 4.70 produce the bias voltages used by the regulated-cascode current sources and the input circuit of the ADC.

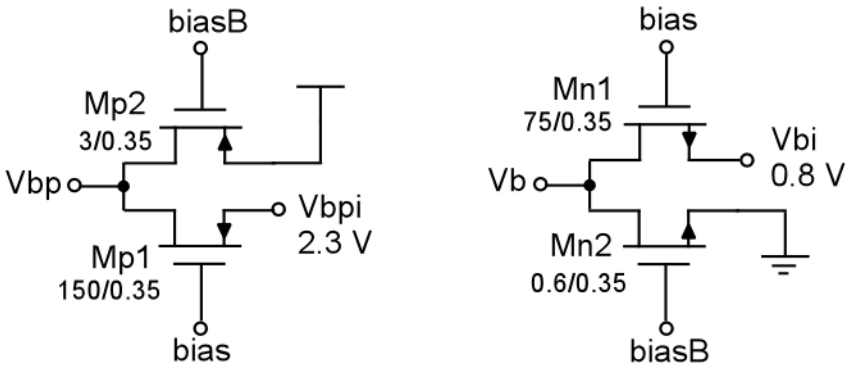


Figure 4.70 (a) Circuit to Generate the Bias Voltage Vbp **(b)** Circuit to Generate the Bias Voltage Vb

The voltage at node V_{bp} in Figure 4.70 (a) is used to bias the PMOS regulated-cascode current sources and the op-amp of the input circuit. The voltage V_{bpi} in Figure 4.70 (a) is passed through M_{p1} when the ADC is not in standby mode, and the voltage at node V_{bp} is set to Vdd through M_{p2} during the standby state. The voltage at node V_b in Figure 4.70 (b) is used to bias the NMOS regulated-cascode current sources. The voltage V_{bi} in Figure 4.70 (b) is passed through the switch M_{n1} when the ADC is not in standby mode. When the ADC is in the standby state, V_b is set to ground through the transistor M_{n2}. The transistors M_{n1} and M_{p1} are large so the impedance of the switch is minimized, reducing the voltage drop across the switches. The transistors M_{n2} and M_{p2} are small to reduce the parasitic capacitance at the nodes V_{bi} and V_{bpi}, respectively. Note that V_{bi} and ground are passed through NMOS transistors since NMOS transistors faithfully pass voltages below Vdd-V_{tn}, where V_{tn} is the threshold voltage of the NMOS transistors. Also, V_{bpi} and Vdd are passed through PMOS transistors since PMOS transistors faithfully pass voltages above V_{tp}, where V_{tp} is the threshold voltage of the PMOS transistors. The description of the control signals bias and biasB are given below.

The logic diagram for the circuit that produces the control signals bias and biasB is shown in Figure 4.71.

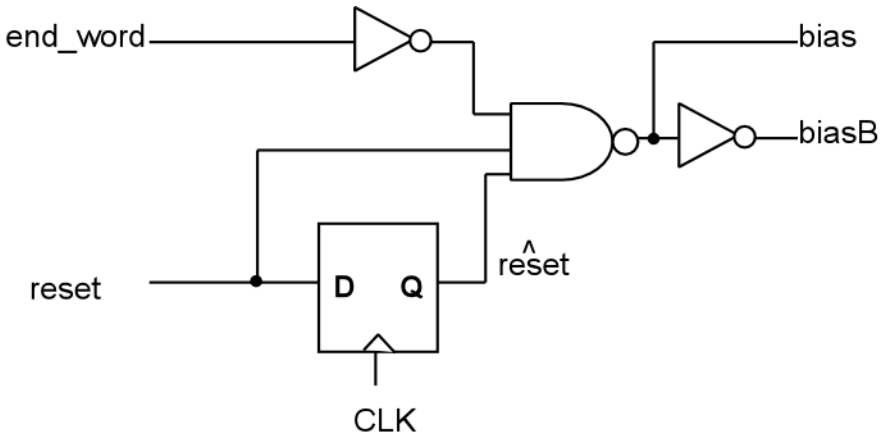


Figure 4.71 Control Voltage Generator of the Bias Voltage Generators

The circuit of Figure 4.71 generates the control voltages of the circuit of Figure 4.70. The timing diagram for the control voltage generator is shown in Figure 4.72.

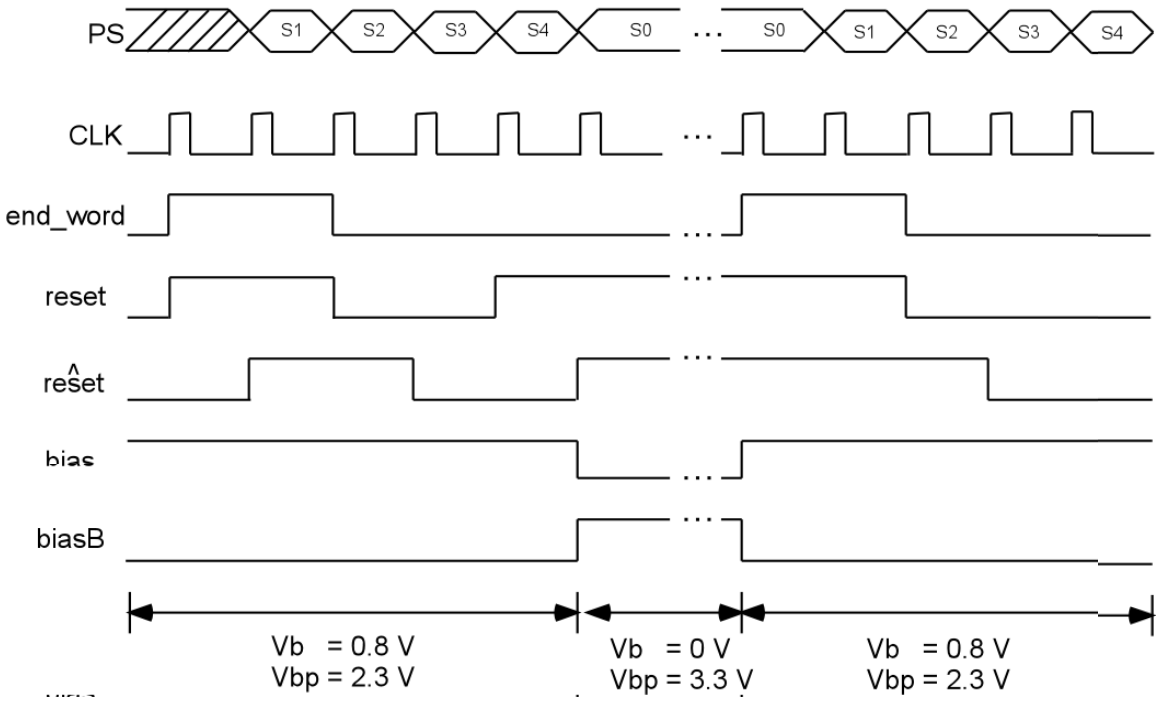


Figure 4.72 Timing Diagram for the Control Voltage Generator of the Bias Voltage Generators

The timing diagram corresponds to a 2-bit resolution, where the ADC completes two bit cycles. The bias voltages, Vb and Vbp, are disabled at the end of the second phase of the

n^{th} bit cycle (state S4 in the timing diagram) for an n-bit resolution. The signal $\hat{reset}$ of Figure 4.71 allows the ADC to complete the second phase of the n^{th} bit cycle for an n-bit resolution. However, the ADC is not required to complete the n^{th} bit cycle for an n-bit output word. The inclusion of the $\hat{reset}$ signal in the control voltage generator of Figure 4.71 is an oversight of the designer and can actually be eliminated. Figure 4.72 shows the bias voltages are enabled one CLK cycle before the ADC begins conversion of the next analog input sample. Note that the input is sampled during state S1 in the timing diagram.

Since the control voltages are active one clock period before the ADC begins the conversion process, the regulated-cascode current sources and the op-amp of the input circuit are allowed one period of the system clock to reestablish their bias points. The recovery time of the disabled circuits was found to be less than one period of the system clock. Simulation results indicate the disabled circuits recover in less than 60 ns (refer to Section 4.5 and Section 4.7). The recovery times are acceptable since the period of the system clock is 300 ns.

4.11 Layout Considerations

One should consider process variations and digital noise in the layout of an ADC. While process variations are a concern for all analog circuits, digital noise is a concern solely for mixed-signal circuits, which include both analog and digital components on the same chip.

4.11.1 Process variation issues

Process variation is a major concern for analog circuit designers. Process variation causes the gain and sizes of transistors and other components to vary across wafers, chips, and even different portions of a chip. Thus, the adverse effects of process variation must be compensated for in layout as much as possible.

Variations in gain and sizes of transistors are problematic in differential circuits, such as differential op-amps. In order to reduce process variations effects in the op-amps

of our ADC, the differential pairs of the op-amps are formed in a common-centroid layout. The goal of common-centroid layout is to match process variations across the transistors. Thus, each transistor has the same size and gain across process variations. Multiple fingers of one transistor are interdigitated with the multiple fingers of the other transistor to be matched in a common-centroid layout. Furthermore, the boundary conditions of the two differential transistors should also be matched. The transistor pairs (M1, M2), (M3, M4), and (M5, M6) of the op-amps in Figure 4.35 and Figure 4.42 are implemented using a common-centroid layout. The transistor pair (M1, M2) layout of the op-amps is given in Figure 4.73.

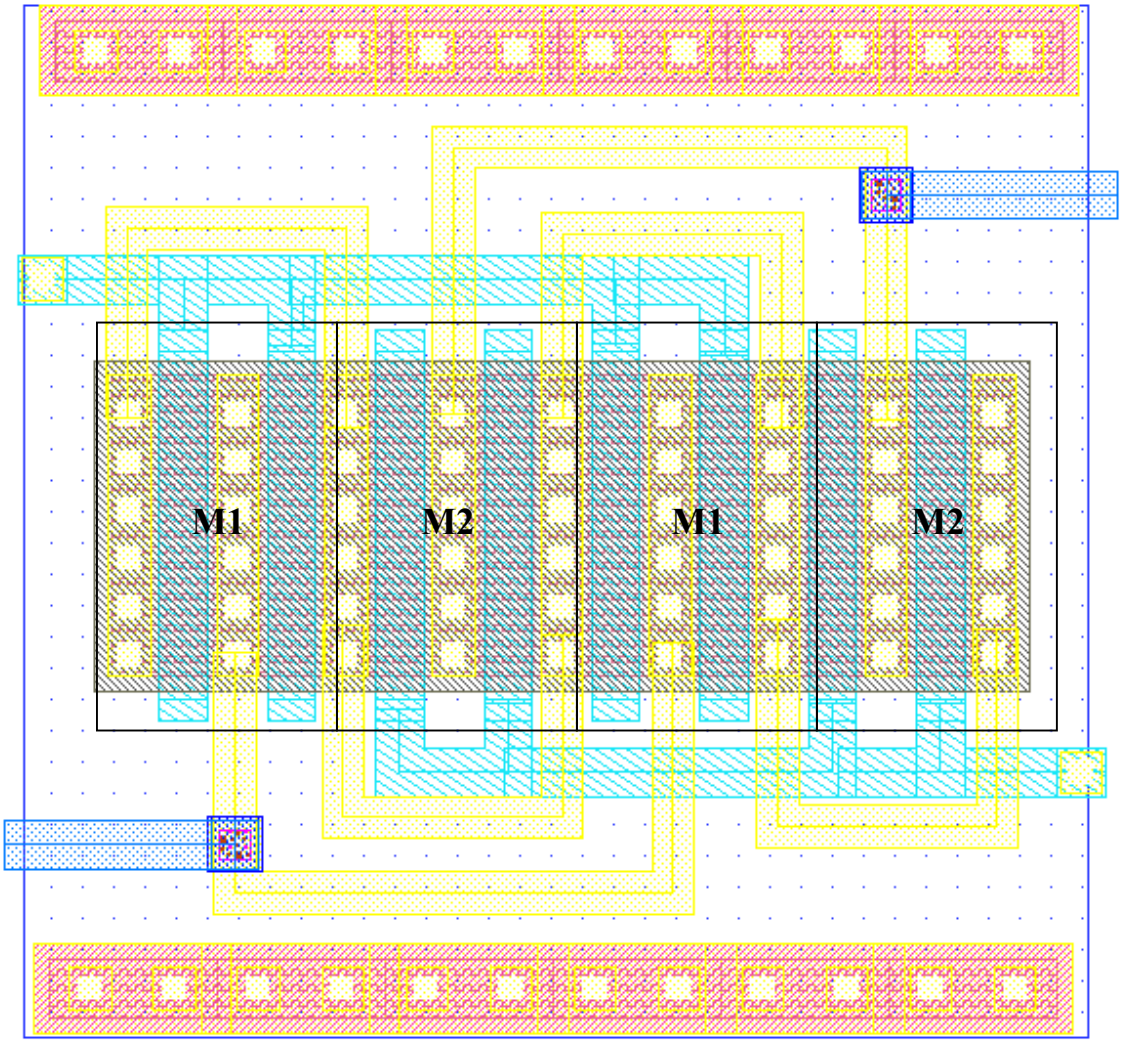


Figure 4.73 Common-Centroid Layout of the Differential Pair (M1, M2)

Mismatches in the current sources of the ADC also present a problem. The reference currents and bias currents of the ADC should match to increase the accuracy of the ADC. However, matching transistors of the NMOS regulated-cascode current sources and the PMOS regulated-cascode current sources is not possible since the gains of P-type and N-type MOSFETS vary across process independently. The bias voltages of the NMOS and PMOS regulated-cascode current sources for our ADC are off-chip inputs for the purposes of testing. Thus, the NMOS and PMOS regulated-cascode current sources can be matched externally by tuning the bias voltages.

While the reference current sources I_{r1} and I_{r2} of Figure 4.1 should match, and the bias current sources I_{b1} and I_{b2} should match, it is not necessary that the bias currents match the reference currents. If the bias currents do not match the reference currents, an offset exists. Although offsets are not a major concern for our ADC owing to the RSD algorithm, the offset is easily remedied through transistor matching. The transistors of the NMOS regulated-cascode current sources I_{r2} and I_{b2} and the transistors of the PMOS regulated-cascode current sources I_{r1} and I_{b1} are matched by using the common-centroid layout for the T_m transistors and the T_r transistors in Figures 4.17 and 4.23. Thus, the offset tolerance granted by the RSD algorithm is not unnecessarily employed for mismatches between the reference and bias current sources.

Capacitor matching was also employed for the voltage reference circuit of Figure 4.31. Since the reference voltage is only dependent on the ratio of the capacitors, matching the relative sizes of the capacitors across process variations maintains the same reference voltage. The capacitors of Figure 4.32 and Figure 4.33 are realized with arrays of unit-sized (16.75 μm x 16.75 μm) capacitors and non-unit sized capacitors. To minimize the effects of process variation, the non-unit sized capacitors have the same perimeter-to-area ratio (67 μm/ 280.56 μm^2) as the unit-sized capacitors. When the same perimeter-to-area ratio is used for both unit-sized and non-unit-sized capacitors, the changes in the capacitor values due to overetching will have the same relative errors for both types of capacitors [12]. As a result, the ratio of the unit-sized and non-unit-sized capacitors is maintained across process variations.

4.11.2 Digital noise issues

Layout of mixed-signal circuits requires minimizing the digital noise propagating to analog components. Prevention of digital noise in analog components requires separate analog and digital power supplies, guard rings, and shielding.

Digital components often create significant noise in the power supplies at the transitions of clock signals. The switching noise can propagate along the power rails to sensitive analog components. Thus, to prevent large spikes of current being injected into the analog portion of the ADC, separate analog and digital power supplies are used.

An additional source of digital noise is the P-type substrate since digital switching noise is coupled into the substrate of the chip. The use of substrate contacts and guard rings minimizes the substrate noise. Substrate contacts prevent current in the substrate from propagating by providing a low-impedance path from the substrate to ground. Substrate contacts are liberally distributed across both digital and analog ground.

Guard rings surround the analog portion of the ADC. The guard rings consist of an n-type well connected to Vdd between two substrate contact rings connected to ground. The n-type well connected to Vdd increases the resistance of the substrate between the two substrate contact rings since the substrate doping is much lower below the N-type well than at the surface of the substrate [12]. Thus, digital noise is minimized in the substrate of the analog components of the ADC. The guard rings can be seen around the ADC core layout of Figure 4.45.

Finally, shielding is used to guard the gate capacitors of the regulated-cascode current copiers from digital noise in the substrate. The capacitors are shielded from the substrate using an N-well so their stored voltages are not corrupted by the noisy substrate. The shield prevents digital noise from being coupled into the bottom plate of the capacitor.

4.12 Design of the Test Chip

The final layout of the ADC test chip is given in Figure 4.74.

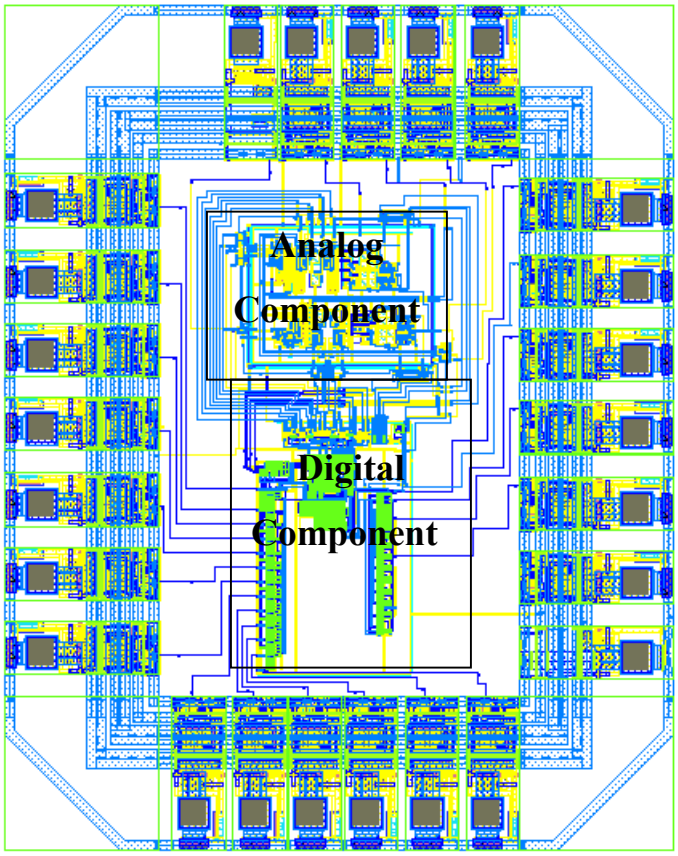


Figure 4.74 Test Chip Layout

The upper portion of the layout is the analog component of the ADC, while the lower portion is the digital portion of the ADC. The digital and analog components were separated to prohibit digital noise from propagating to the analog component. Excluding the pad ring, the area is approximately 1.26 mm^2.

As can be seen in Figure 4.74, a large amount of the chip area is not utilized. This is due to the fact that our ADC requires a large number of pins to make the chip pad bound. The input and output pins are quite large, producing a chip area larger than necessary. However, if the ADC is embedded in a larger system, the unused space can be utilized by other circuitry. Furthermore, the hardware implementation of the digital component of our ADC is not area efficient. The area of the digital component could be

reduced by a more compact layout. The extra space is filled with substrate contacts in the final test chip to reduce substrate noise.

The pin diagram of the test chip is given in Figure 4.75

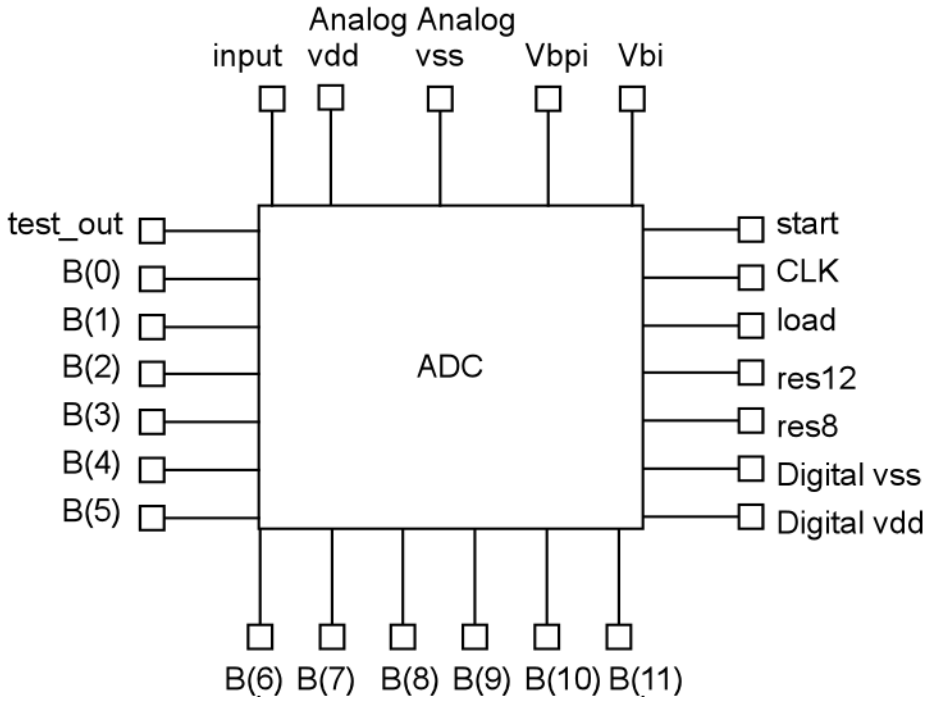


Figure 4.75 Pin Diagram of the Test Chip

In order to test our ADC, a 50 kHz voltage sine wave varying from 1.4 V to 3.6 V is applied to a 20.7 kΩ resistor that is connected to the input pin of the chip. The clock input (CLK) is a 1.7 MHz square wave with a 25% duty cycle. The start and load inputs are applied for two clock cycles at system startup for initialization purposes, and the load input is applied for one clock cycle whenever a new resolution is loaded. The circuit of Figure 4.56 can be used to generate the load signal. The 12-bit word B[11:0] is the 12-bit output word of the ADC and is in binary two's complement form. The output of the test chip B[11:0] is completed 2n-1 CLK cycles after load is asserted for an n-bit resolution. The test_out signal is used to find the maximum speed of the flip-flops used in the digital portion of the ADC. The test_out output is active when the ADC is inactive, which is when start is high. All digital inputs are active high for the test circuit.

Since we did not wish to use 11 pins to apply the resolution input of Figure 4.46, we limited the number of resolutions that can be set for the test chip. On the test chip the most significant four bits of the resolution input are shorted together (i.e. resolution[10:7] in Figure 4.46), the next two bits of the resolution input (i.e. resolution[6:5]) are shorted together, and the last five bits of the resolution input (i.e. resolution[4:0]) are shorted together. The node for the most significant four bits of the resolution input is denoted res12 and the node for the next two bits of the resolution input is denoted res8. The last five bits of the resolution input are set to Vdd. The res12 and res8 inputs are used to indicate 12- and 8-bit resolutions, respectively. When res12 is high and res8 is high, the resolution of the ADC is 12 bits. If res12 is low and res8 is high, the resolution of the ADC is eight bits. If both res8 and res12 are low, the resolution of the ADC is six bits.

The V_{bi} and V_{bpi} inputs are nominally 0.8 V and 2.3 V, respectively. These voltages are the bias voltages of the analog component of our ADC and can be used to match the PMOS regulated-cascode current sources to the NMOS regulated-cascode current sources. The matching process involves setting one bias voltage to a constant while varying the other in order to determine which bias voltages produce the expected accuracy of the ADC.

In order to find the accuracy of the ADC, the transfer characteristic should be found. Several methods have been proposed to measure the transition points and linearity of an ADC [6, 18, 14]. The measures of accuracy are the integral nonlinearity (INL) error and the differential nonlinearity (DNL) error. If the normalized INL and DNL errors are less than I_{LSB} ($[I_{max}-I_{min}]/2^N$), the ADC is N-bit accurate for a RSD cyclic ADC [30].

An additional measure of accuracy is the dynamic range of the ADC. The dynamic range is the rms value of the maximum amplitude sinusoidal input divided by the rms output noise plus the distortion measured when the same sinusoid is present in the output [12]. This measure is used to find the effective number of bits as given by the SNR equation in Section 2.2.

A test circuit is included in our chip that indicates the maximum clock speed of the TSPC flip-flops with asynchronous reset can operate and the propagation delay of a

minimum-size inverter. The circuit diagram of the minimum-size inverter is given in Figure 4.76.

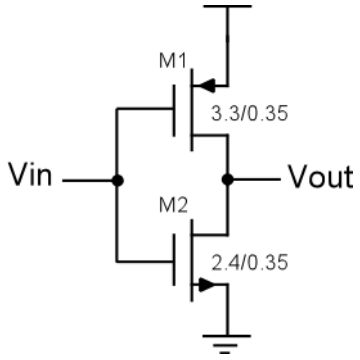


Figure 4.76 Minimum-Size Inverter

The test_out signal is produced by the circuit of Figure 4.77.

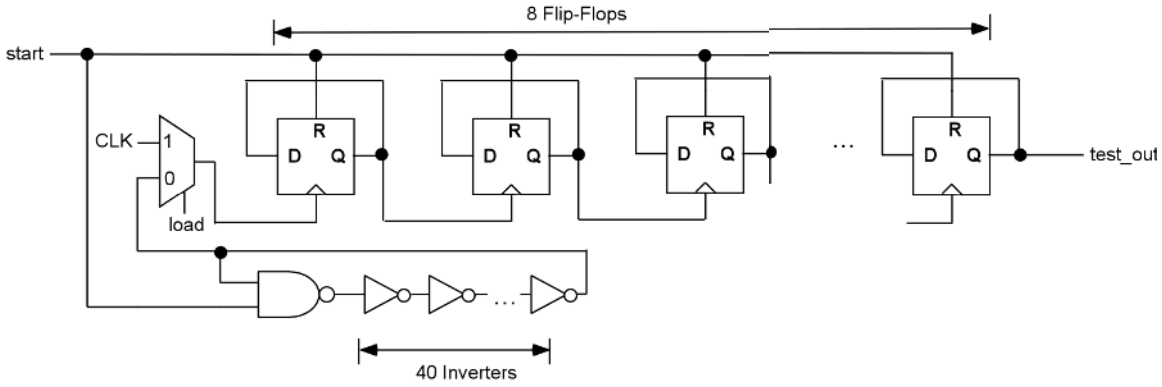


Figure 4.77 Generator of the test_out Signal

The test circuit consists of a ripple counter and a ring oscillator. The ring oscillator of our test circuit is made of one NAND gate, which reduces to an inverter when the start signal is high, and forty inverters. The test circuit is activated when start is '1'. The system clock, CLK, is the clock signal of the counter when load is '1', and the output of the ring oscillator is the clock signal of the counter when load is '0'. The output of the test circuit is the MSB of the 8-bit counter. Thus, the frequency of the output of the test circuit is $^{1}/_{256}$ the frequency of the clock signal that is driving the counter.

The propagation delay of an inverter can be determined by observing the frequency of the test_out signal. The inverse of the oscillation frequency multiplied by a factor of 41 is the propagation delay of the minimum-size inverter. The propagation delay of the minimum-size inverter can be calculated as

$$propagation\ delay = \frac{1}{256 * 41 * f_{out}},$$

where f_{out} is the frequency of the test_out signal when load is '0'. Also, the frequency of the signal test_out is the frequency of the clock signal of the 8-bit counter divided by 2^8 or 256. The maximum clock speed of the flip-flops is determined by increasing the frequency of the CLK signal until the frequency of the test_out signal is less than $^1/_{256}$ the frequency of CLK when load is '1'. When this occurs, a flip-flop has failed to latch the voltage at its input node since the setup time or hold time of the flip-flop has not been met.

The layout of the test circuit is given in Figure 4.78 and has an area of 92 x 178 μm^2. The simulation results are shown in Figure 4.79 and Figure 4.80.

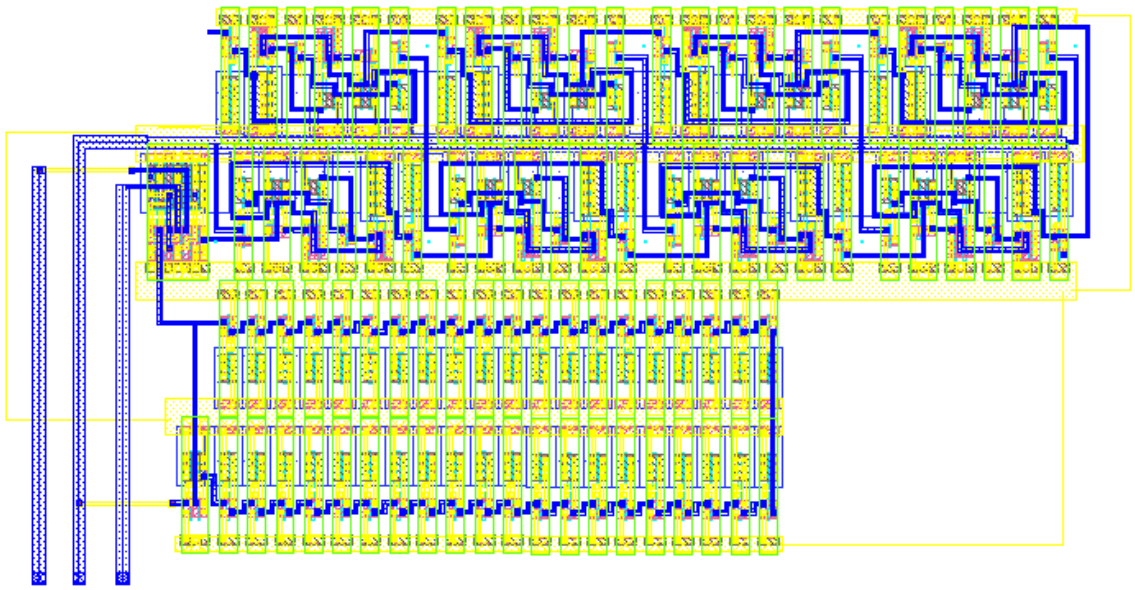


Figure 4.78 Layout of the test_out Generator

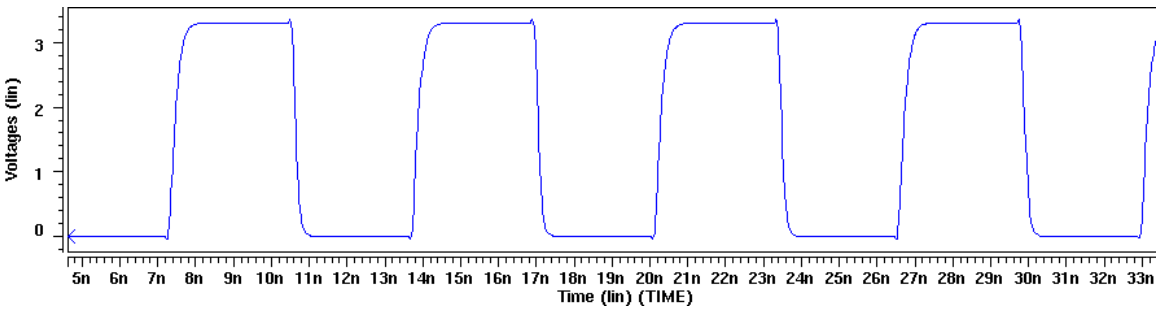


Figure 4.79 Simulation Results for the Ring Oscillator

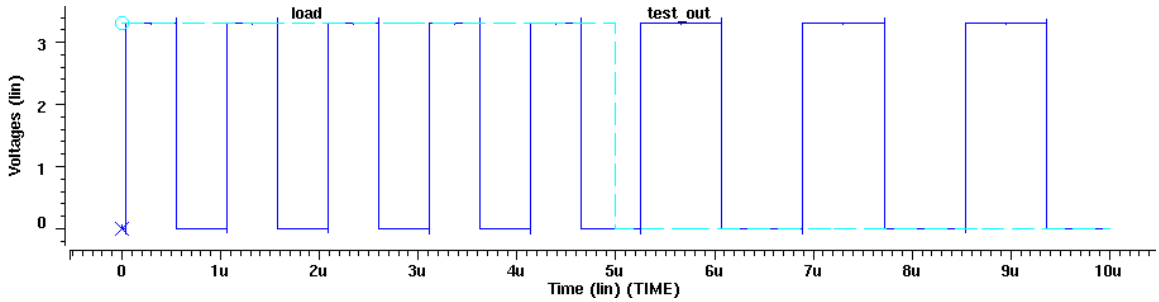


Figure 4.80 Simulation Results for the Counter

For the simulation results, the period of the 25% duty cycle CLK signal is 4 ns. Figure 4.79 shows the waveform generated by the ring oscillator, and Figure 4.80 shows the waveform generated by the 8-bit counter. The simulation results indicate the period of output of the ring oscillator is 6.447 ns and has a frequency of 155 MHz. Thus, the propagation delay of the minimum-size inverter is 0.1572 ns. Figure 4.80 shows the period of the test_out signal is 1.0240 µs and has a frequency of 977 kHz when load is high. The period of the test_out signal is 1.6459 µs, and the frequency of the test_out signal is 608 kHz when load is low. The frequency of 608 kHz corresponds to the frequency of the ring oscillator divided by 256, and the frequency of 977 kHz corresponds to the frequency of the clock signal divided by 256. Thus, the test circuit operates as expected.

In this chapter, we detailed the operation of our ADC and its implementation. Also, the plan for testing the test chip was given. In the next chapter we discuss the experimental results of our ADC.

Chapter 5

Experimental Results

5.1 Introduction

In the previous chapter, we described the implementation of our low-power, variable-resolution ADC based on the RSD algorithm. We laid out the ADC in a full-custom manner in the TSMC 0.35 μm, double-poly, triple-metal technology.

In this chapter, we present the simulation results for our ADC. We report the power dissipation for various resolutions, speed, and accuracy of our ADC.

All simulation results reported in this chapter were obtained using Avant! HSPICE with a clock frequency of 1.7 MHz and a singled-ended supply voltage of 3.3 V. For all simulation results, the input bias voltage Vbpi is 2.3 V, and the input bias voltage Vbi is 0.8 V.

5.2 Verification of Operation

We verified the correct operation of our ADC through HSPICE simulation. We give two simulation results to illustrate the operation of our ADC. We first give the simulation results for the maximum input current and then give the simulation results for the minimum input current.

The simulation results for the 90 μA maximum input current is shown in Figure 5.1. The input voltage of the ADC is 3.4515 V (refer to Figure 4.38).

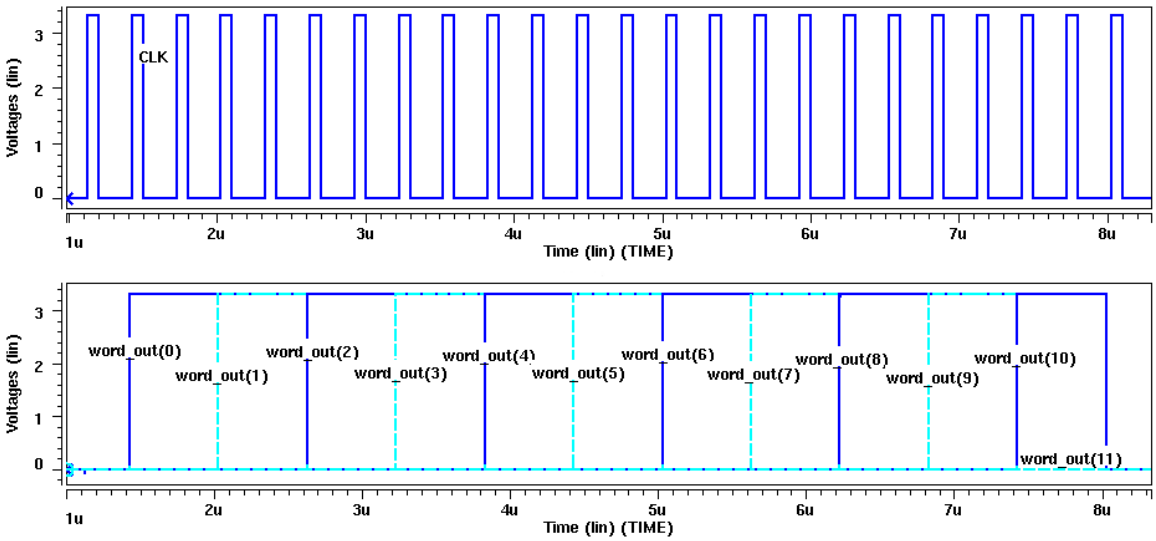


Figure 5.1 Output Word for the Maximum Input Current

The top waveform of Figure 5.1 is the system clock signal, and the bottom waveform is the two's complement output word produced by the RSD decoder. Before the output bits of the ADC are decoded, the flip-flops of the RSD decoder are reset. After the initial reset, all the flip-flops of the RSD decoder are set to '1' after 22 clock cycles with the exception of the flip-flop holding the MSB of the output word. Thus, the output word for a 90 µA input current is "0111 1111 1111". The RSD decoder is reset two clock cycles after the output word is completed. The ADC operates as expected for the maximum input current.

The simulation results for the minimum input of current 0 µA is shown in Figure 5.2. The input voltage of the ADC is 1.432 V.

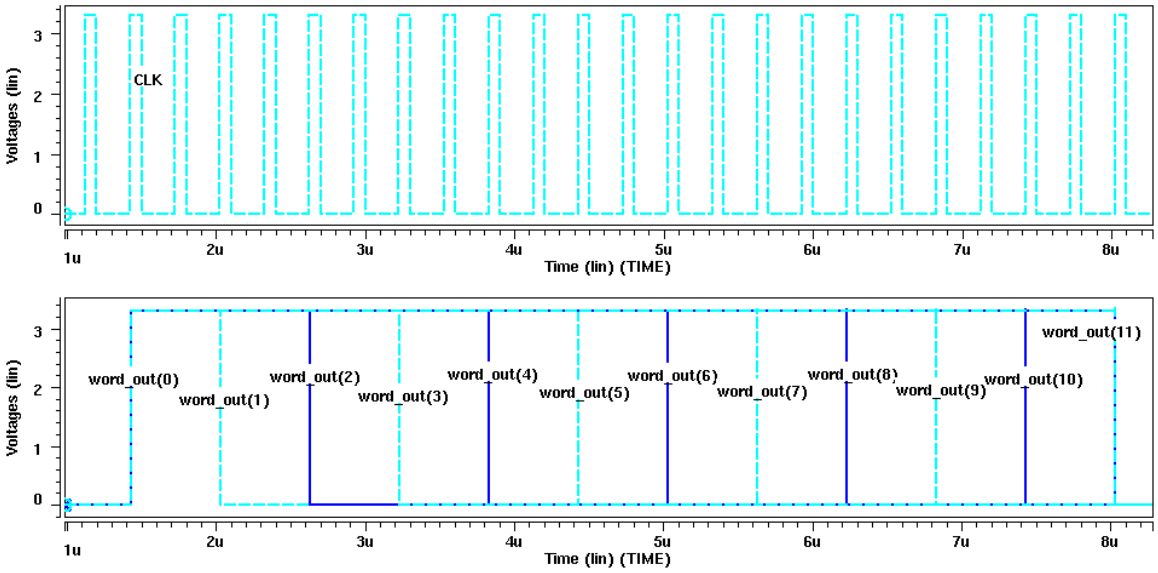


Figure 5.2 Output Word for the Minimum Input Current

The simulation results show that all the flip-flops of the RSD decoder contain the logic value '1' after the first output bit of the ADC is decoded. After 22 clock cycles, all the flip-flops of the RSD decoder are set to '0' with the exception of the flip-flop holding the MSB of the output word. Thus, the output word for a 0 µA input current is "1000 0000 0001" after 22 system clock cycles. The ADC operates as expected for the minimum input current.

5.3 Power Dissipation

The power dissipation of our ADC was measured for the six different resolutions of 2, 4, 6, 8, 10, and 12 bits. The input current was set to 90 µA during the measurement, which gives the maximum power dissipation for the given resolution. Also, a clock frequency of 1.7 MHz and a single-ended 3.3 V supply voltage were used for the measurement. The power measurements found through HSPICE simulation for the various resolutions are given in Figure 5.3. Figure 5.4 gives the percentile of each power measurement with respect to the maximum power dissipation of the ADC, which corresponds to a 12-bit resolution. Note that the power dissipation of the input/output

(I/O) pins of the chip have not been included in the power measurements presented with the exception of the I/O pin for the input voltage of the ADC.

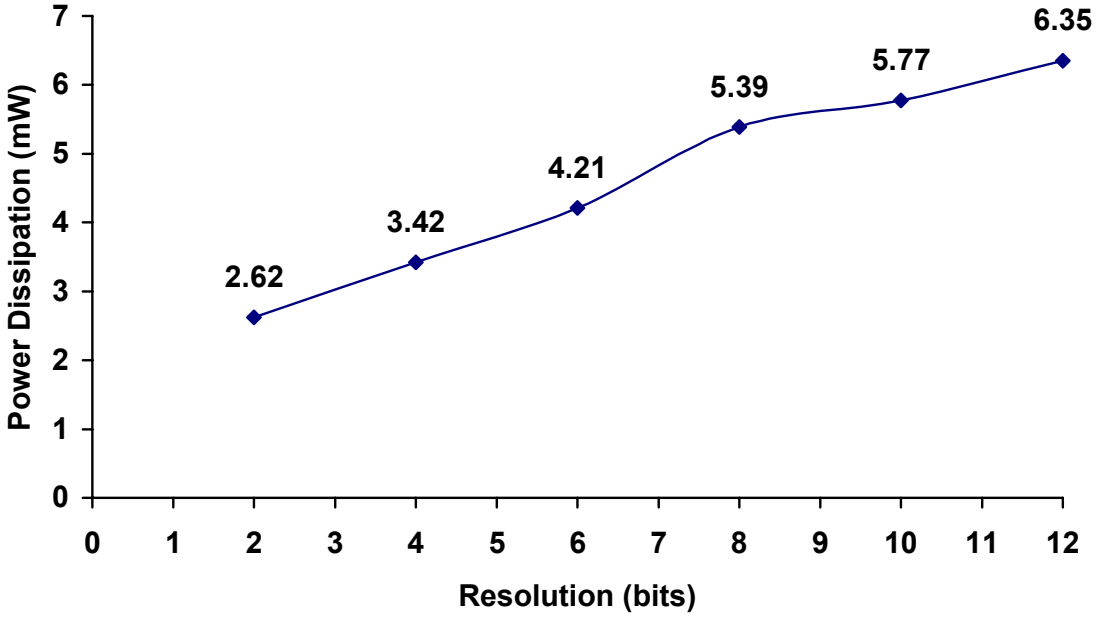


Figure 5.3 Maximum Power Dissipation versus Resolution

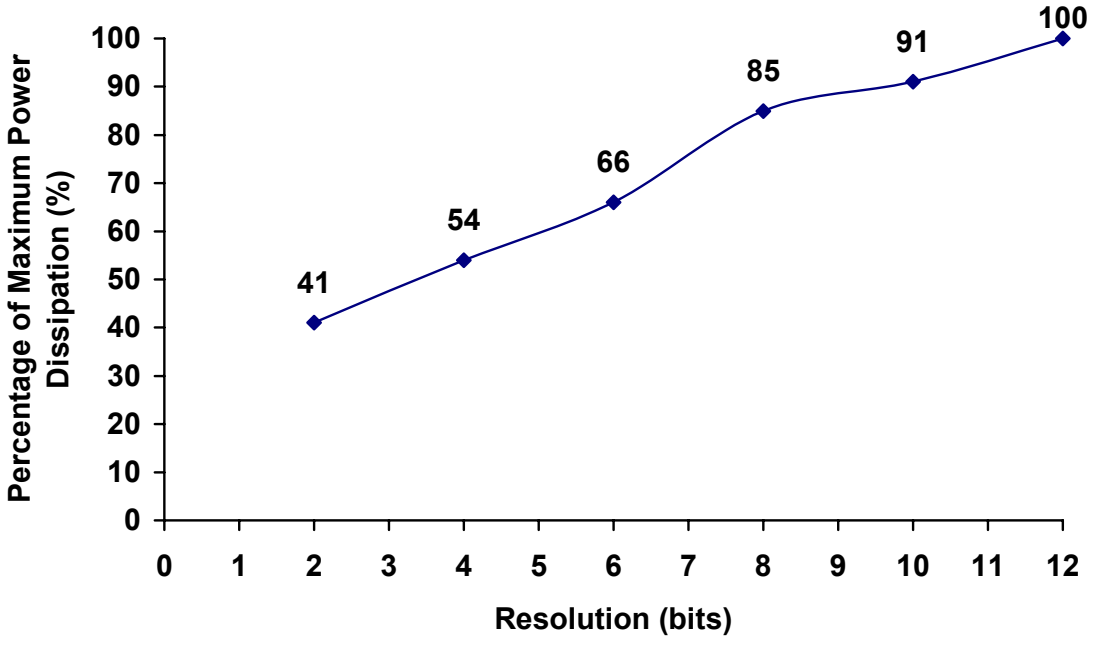


Figure 5.4 Percentage of the Maximum Power Dissipation versus Resolution

As shown in Figure 5.3, the maximum power dissipation for a 12-bit resolution is 6.35 mW, and the maximum power dissipation for a 2-bit resolution is 2.62 mW. The figures show that the power dissipation is approximately proportional to the resolution of the ADC. The trend is that when the resolution is decreased by two bits, the average power savings is 10 percent. Thus, our ADC is suitable for wireless communications applications where the resolution can be dynamically adjusted for the given communication channel condition.

The average power dissipation of the components for a 12-bit resolution measured over the period necessary to produce a 12-bit word is summarized in Table 5.1. Note that the power dissipation measured for the input circuit includes the I/O pad and the off-chip voltage with series resistance.

Table 5.1. Power Dissipation of the Components of the ADC

Block	Power Dissipation (mW)
Input Circuit	1.30
4 Voltage References	1.62
ADC Core	3.16
Digital Component	0.27
Total	6.35

The input circuit of the ADC contributes a significant amount of power dissipation. The major sources of power dissipation of the input circuit are the regulated-cascode current sources. The 200 μA NMOS regulated-cascode current source of Figure 4.16 dissipates 0.38 mW, and the 200 μA PMOS regulated-cascode current source of Figure 4.22 dissipates 0.45 mW. The op-amp of the input circuit (refer to Figure 4.42) dissipates 0.16 mW. The remainder of the power dissipation of the input circuit, which is approximately 0.3 mW, is due to the I/O pad of the input circuit and the off-chip voltage with series resistance.

The four voltage references used for the four comparators of the ADC also contribute a significant amount of power dissipation to the ADC. This power dissipation is solely due to the power dissipation of the four op-amps of the voltage reference

circuits. The power dissipation of the voltage reference circuits could possibly be reduced if the op-amps were further optimized with respect to power dissipation.

The major sources of power dissipation of the ADC core are the regulated-cascode current sources. At any given time during the conversion process, four 200 μA regulated-cascode current sources are sourcing current, which dissipate a total of 1.66 mW. These current sources are the bias currents of the current copiers. Also, during most of the conversion process (specifically, 11 bit cycles), a 45 μA bias current source is active. This current source is either the PMOS regulated-cascode current source I_{b1} or the NMOS regulated-cascode current source I_{b2} of Figure 4.1. The 45 μA PMOS regulated-cascode current source dissipates 0.21 mW, and the 45 μA NMOS regulated-cascode current source dissipates 0.19 mW. Furthermore, a reference current is subtracted from the residue current of the ADC every bit cycle for the maximum input current. Thus, an additional 45 μA regulated-cascode reference current source (I_{r1} or I_{r2} of Figure 4.1) is active during most of the conversion process (11 bit cycles) for the maximum input current. The power dissipation of each strobed, cross-coupled inverter comparator is 2.3 μW and is insignificant. The remainder of the power dissipation of the ADC core is due to the power dissipation required to source the 90 μA residue current.

The power dissipation of the digital portion of the ADC is fairly insignificant since it is implemented in fully complementary MOS and the clock frequency is relatively low.

5.4 Speed

The conversion time and the clock speed of our ADC are determined by the settling time of the current copiers and the current sources. The settling time required by the ADC was found to be 300 ns.

The maximum time required for the current copiers to settle within ½ I_{LSB} was found to be 100 ns, which is the required settling time when the current copiers store current. The settling time was measured as the time necessary for the current sourced by the memory transistor, T_m, of the current copier to settle within ½ I_{LSB} (refer to Figures 4.6 and 4.11). The settling time of the current copiers was found by using ideal current

sources for the current sources of Figure 4.1 and performing the operations outlined in Section 4.3 with the exception of the comparisons. The settling time of the current copiers was found to increase to 150 ns when the comparators of Figure 4.1 sample the gate voltage of the memory transistor 75 ns after the current copier begins to store current.

The time required for the regulated-cascode current sources to settle within ½ I_{LSB} was found to be 12 ns. The settling time was measured as the time required for the current sourced by the regulated-cascode current source to settle within ½ I_{LSB} after the switch at the output node is closed (refer to Figures 4.16 and 4.22). The settling time of the current source was determined by using the architecture of Figure 4.1 where ideal current sources were used for the bias current J of the NMOS and PMOS regulated-cascode current copiers. The operations outlined in Section 4.3 with the exception of the comparisons were then performed.

The settling time for the current copiers was measured as 300 ns when the complete ADC architecture of Figure 4.1 is employed and the operations described in Section 4.3 are performed. Since the clock speed of our ADC is determined by the settling time of the current copiers, the clock period of our ADC is 300 ns. As the ADC requires two clock cycles to produce one output bit, the bit rate is obtained as

$$bit\ rate = \frac{1}{2 * 300\ ns} = 1.7\ MHz\ .$$

Since no latency is required for our ADC between two consecutive words and 12 clock cycles are required to decode the output of the ADC, the word rate is obtained as

$$word\ rate = \frac{bit\ rate}{12} = 139\ kHz\ .$$

5.5 Accuracy

The HSPICE simulation time for one word is 11,370 seconds or 3.16 hours for the entire ADC system, and the simulation results require 0.5 GB of memory per word. Thus, it is prohibitive to obtain the transfer characteristic of our ADC, which would

require simulation of 2^{12} output words. Representative input samples were taken to judge the accuracy of our ADC.

The representative output words include the words corresponding to the maximum input current and the minimum input current. Note that the reference currents I_{r1} and I_{r2} of Figure 4.1 are employed every bit cycle when the maximum and minimum input currents are employed. Thus, the largest errors in the residue current should be present for these input currents. The accuracy was determined by observing the output bits generated by the ADC and the residue current stored and sourced by the current copiers. Also note that the input voltage of the ADC core is constant for these measurements. Thus, the inaccuracy of the input circuit is not included in these measurements.

The simulation results shown Figure 5.1 indicates the ADC correctly produces "0111 1111 1111" when the input current is the maximum (which is 90 μA). Figure 5.2 indicates the ADC correctly produces "1000 0000 0001" when the input current is the minimum (which is 0 μA). Thus, the output words of the ADC are accurate to twelve bits for these input currents.

The currents sourced by the current copiers during the conversion process for the minimum input current are shown in Figure 5.5.

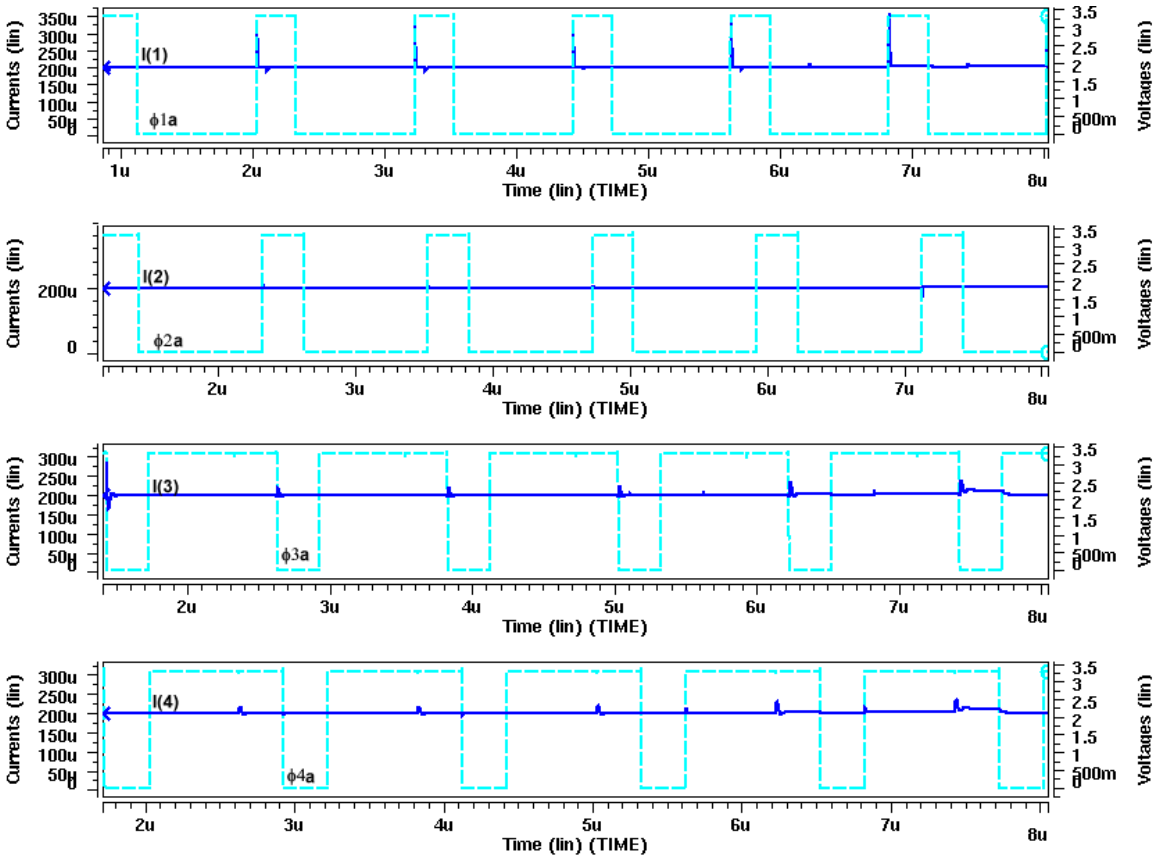


Figure 5.5 Currents Sourced by the Current Copiers of the ADC for the Minimum Input Current

The right vertical axes of the Figure 5.5 are voltage and the left vertical axes of Figure 5.5 are current. The horizontal axes are time. The topmost waveforms are the current sourced by the NMOS regulated-cascode current copier g_{m1} of the ADC architecture of Figure 4.1 and ϕ_{1a}, the control voltage of the gate switch of g_{m1}. The second set of waveforms from the top of the figure is the current sourced by the NMOS regulated-cascode current copier g_{m2} and ϕ_{2a}, the control voltage of the gate switch of g_{m2}. The third set of waveforms from the top of the figure is the current sourced by the PMOS regulated-cascode current copier g_{m3} and ϕ_{3a}, the control voltage of the gate switch of g_{m3}. Finally, the bottommost waveforms are the current sourced by the PMOS regulated-cascode current copier g_{m4} and ϕ_{4a}, the control voltage of the gate switch of g_{m4}. Note that the control voltages of the PMOS regulated-cascode current copiers are active low since the gate switches of the PMOS current copiers are P-type MOSFETs, and the

control voltages of the NMOS regulated-cascode current copiers are active high since the gate switches of the NMOS current copiers are N-type MOSFETs. When the control voltage of the gate switch of a current copier is active, the current copier is storing current. The signal current is the total current stored in a current copier less the 200 μA bias current J. One bit cycle corresponds to the current copiers g_{m1} and g_{m2} consecutively storing the signal current or the current copiers g_{m3} and g_{m4} consecutively storing the signal current. Figure 5.5 corresponds to 12 bit cycles of the ADC for the minimum input current.

Ideally, the residue current of the ADC remains 0 μA for an input current of 0 μA, regardless of the number of bit cycles since $\hat{I}_{res} = 2I_{res} + I_r - I_b = 2(0\ \mu A) + 45\ \mu A - 45\ \mu A = 0\ \mu A$ (refer to Section 4.3). Furthermore, the output bits PQ are ideally PQ = "00". Figure 5.5 shows the signal currents of the current copiers are close to 0 μA for 12 bit cycles. During the twelfth bit cycle, the signal current stored by each of the current copiers g_{m3} and g_{m4} is 12.52 μA. This current corresponds to PQ = "00" since the signal current is less than ¾ I_{ref} (33.75 μA). We could reasonably expect that the residue current of the thirteenth bit cycle is approximately $2I_{res} + I_r - I_b = 2*12.52\ \mu A + 45\ \mu A - 45\ \mu A = 25.04\ \mu A$, which also corresponds to PQ = "00". Thus, the ADC would accurately compute output bits for 13 bit cycles. Recall that an N-bit output word is produced in N-1 bit cycles for our ADC. *Thus, the simulation results for the minimum input current suggest the ADC is accurate to 14 bits.*

The simulation results for the maximum input current are shown in Figure 5.6.

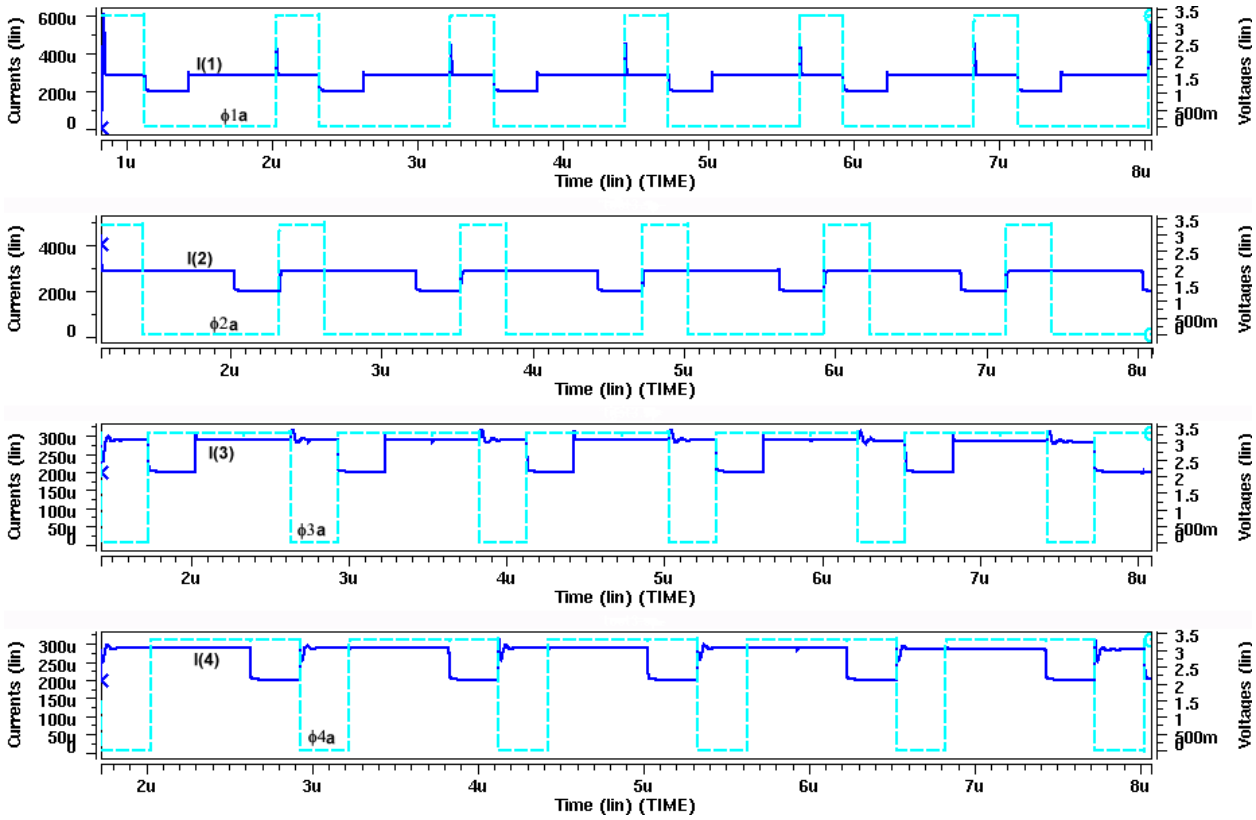


Figure 5.6 Currents Sourced by the Current Copiers of the ADC for the Maximum Input Current

Ideally, the residue current of the ADC remains 90 µA for an input current of 90 µA, regardless of the number of bit cycles since $\hat{I}_{res} = 2I_{res} - I_r - I_b = 2(90\ \mu A) - 45\ \mu A - 45\ \mu A = 90\ \mu A$. Furthermore, the output bits PQ are ideally PQ = "11". Figure 5.6 shows the signal currents stored by the current copiers are close to 90 µA for 12 bit cycles. During the twelfth bit cycle, the signal current stored by each of the current copiers g_{m3} and g_{m4} is 83.4 µA. This current corresponds to PQ = "11" since the current is greater than $^5/_4\ I_{ref}$ (56.25 µA). We could reasonably expect that the residue current of the thirteenth bit cycle is approximately $2I_{res} - I_r - I_b = 2*83.4\ \mu A - 45\ \mu A - 45\ \mu A = 76.8\ \mu A$ and the residue current of the fourteenth bit cycle is 63.6 µA, which both correspond to PQ = "11". Thus, the ADC would accurately compute the residue current for 14 bit cycles. *The simulation results for the maximum input current indicate the ADC is accurate to 15 bits*. Thus, the minimum effective number of bits for our ADC is 14 bits

for the representative input samples. The corresponding minimum signal-to-noise ratio (SNR) for the simulation results is approximately 84 dB (refer to Section 2.2).

The input voltage of the ADC core is constant for these measurements. Thus, the inaccuracy of the input circuit is not included. However, simulation results indicate that the input circuit is accurate to 14 bits if the frequency of the input voltage is less than 16.7 kHz. The error measured for this input frequency is given in Figure 5.7.

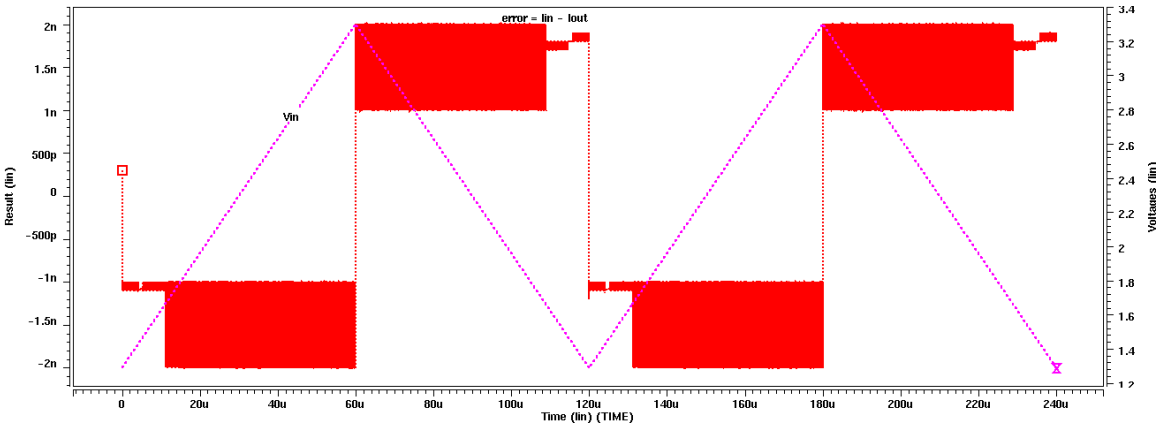


Figure 5.7 Error of the Input Circuit for 8.3 kHz

The difference between the input current (flowing through the Vin node in Figure 4.38) and the current sourced by the input circuit (flowing through the Vout node) was measured to find the error of the input circuit. The simulation results of Figure 5.7 indicate that the error of the input circuit is less than 2.75 nA, which corresponds to an error less than ½ I_{LSB} for 14 bits ($^1/_2$ 90 µA/2^{14}). Thus, if the maximum resolution of the ADC is increased to 14 bits, the maximum input frequency is 8.3 kHz.

In this chapter we discussed the simulation results for the ADC. The maximum power dissipation of the ADC for a 12-bit resolution is 6.35 mW, and the maximum power dissipation for a 2-bit resolution is 2.62 mW. The power dissipation is approximately proportional to the resolution of the ADC. The trend is that when the resolution is decreased by two bits, the average power savings is 10 percent. The maximum settling time of the current copiers of the ADC was found to be 300 ns. As a result, the bit rate is 1.7 MHz, and the word rate is 139 kHz. Simulation results for

representative input samples indicate the SNR of the ADC is 84 dB for input frequencies less than 8.3 kHz.

Chapter 6

Conclusion

6.1 Summary

Analog-to-digital converters (ADCs) are a major component in digital communications systems, where they are used to convert analog signals to the digital domain. Power dissipation is a major concern in portable applications, where minimizing power dissipation is a necessity. Furthermore, the power dissipation of an ADC in a communications application is often greater than necessary since the ADC meets the requirements for the worst-case channel condition, which rarely occurs. In this thesis, we investigated a low-power, variable-resolution ADC where the resolution can be dynamically adjusted according to the given channel condition.

Many different algorithms exist for analog-to-digital conversion. However, only a few are suitable for a low-power, variable-resolution approach. The chosen analog-to-digital conversion algorithm chosen for this research is the redundant signed-digit (RSD) cyclic algorithm. Variable resolution is easily implemented by limiting the number of iterations that the RSD cyclic ADC executes. Furthermore, the RSD cyclic algorithm has several advantages over other types of conversion algorithms, including insensitivity to loop and comparator offsets. Since the RSD cyclic algorithm is insensitive to offsets, simple, low-power comparators can be used.

The ADC proposed in this research is based on a switched-current technique. A switched-current technique is appropriate for digital processes since precision analog components are not required. The major component in switched-current architectures is the current copier, which stores current. The current copier used in the proposed ADC is

the regulated-cascode current copier. We chose to use this current copier since it has a high degree of accuracy, moderate circuit complexity, and low power dissipation.

Variable resolution is implemented through digital techniques. The finite-state machine (FSM) that controls the switches of the proposed ADC architecture applies the voltages necessary to open the switches of the ADC when the desired number of bits has been computed. When the desired number of bits has been computed, the ADC is disabled and dissipates little steady-state power. As a consequence, the power dissipation of our ADC is reduced significantly when a lower resolution is used.

Our ADC is implemented in a 0.35 μm technology with a single-ended 3.3 V power supply voltage with an active area of 1.26 mm^2. The maximum resolution of our ADC is 12 bits with a maximum power dissipation of 6.35 mW. The power dissipation decreases by an average of 10 percent when the resolution is lowered by two bits. Simulation results indicate our ADC achieves a bit rate of 1.7 MHz and has a SNR of 84 dB for input frequencies less than 8.3 kHz. Thus, our ADC is appropriate for wireless communications applications where low power dissipation is necessary.

6.2 Future Improvements

A couple of improvements can be made to our proposed ADC. One improvement is reduction of the error due to charge injection and consequently increasing the accuracy of the ADC. The major limitation on the precision of switched-current techniques is charge injection. When a switch is opened, the channel charge of the switch is injected into the storage capacitor of the current copier, creating an error in the stored current. Differential current copiers can be used to significantly reduce the error introduced by charge injection [27]. Thus, differential techniques would improve the accuracy of our ADC.

Another improvement is increasing the speed of our ADC through pipelining. Generally, the architecture of Figure 4.1 would be duplicated N-1 times for an N-bit resolution ADC in a pipelined implementation. The pipelined ADC would continuously produce a new output word every bit cycle. The feasibility of this approach has been proven by Macq, who implemented a 10-bit, pipelined, switched-current ADC based on

the RSD cyclic algorithm [17]. If pipelining were used in our ADC, the word rate of our ADC would be the bit rate. Thus, the word rate of our ADC would increase by a factor of the maximum resolution for a pipelined implementation, a twelve-fold increase in speed. However, the power dissipation also increases by the same order of magnitude. These possibilities are left to future research.

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