A LOW VOLTAGE CMOS CONSTANT CURRENT-VOLTAGE REFERENCE CIRCUIT

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ABSTRACT

The proposed CMOS current-voltage reference circuit consists of a traditional bandgap circuit based on the use of PMOS transistors in weak inversion. Its current is stabilized by an on-chip resistor with positive temperature coefficient. The voltage reference is produced by compensating the positive temperature coefficient of a resistor by the negative temperature coefficient of the diode connected PMOS transistor by driving the constant current of the current reference through them. The simulated temperature coefficients of the voltage and the current were less than 85 ppm/°C and 54 ppm/°C, respectively, in the worst-case simulation over the temperature range of -10°C to 70°C without trimming, and the supply-voltage coefficient of the voltage and current were 0.16% over the supply voltage range of 1.1 V to 2.2 V.

1. INTRODUCTION

A stable frequency-to-voltage converter needs both the constant current and the constant voltage to operate in a voltage reference locked oscillator circuit [1]. A stable voltage reference can be designed by using a conventional bandgap reference circuit [2] and a stable current reference is achieved by using a modified bandgap structure [3]. The disadvantages are that the size and the current consumption of the whole circuit increase.

The aim of this work was to develop a reference circuit that contains both the current and voltage references in a compact way. An idea was to generate the constant current by using the modified bandgap structure and then use this current to generate a constant voltage reference.

2. THE CURRENT-VOLTAGE REFERENCE CIRCUIT

The schematic diagram of the used current-voltage reference circuit is shown in figure 1. The circuit has two outputs V_{ref} and I_{ref}. The voltage V_{ref} is the generated voltage reference and the current I_{ref} is the mirrored, constant current reference. Both the current I_{Vref} and the I_{ref} can be trimmed by using a bias net to reduce the effect of the variation of the process parameters.

The current reference generation is based on the traditional bandgap circuit, except that here PNP bipolar transistors are substituted by diode connected PMOS transistors and the current reference is realized by compensating the positive temperature performance of the on-chip, N diffusion resistor R_1 and R_2 by the negative temperature dependence of the node n_1 and n_2 [3]. The voltage reference is generated by compensating the negative temperature coefficient of the diode connected PMOS transistor M3 by the positive temperature coefficient of the N diffusion resistor Re.

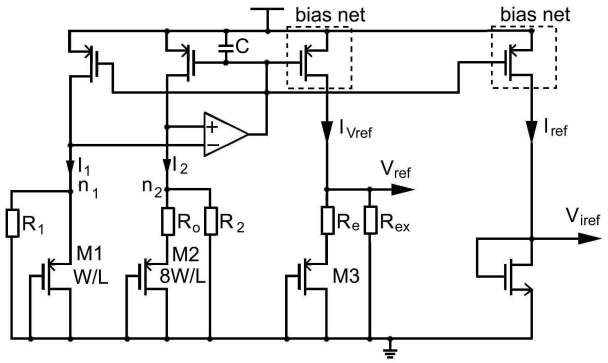

Figure 1. The schematic diagram of the current-voltage reference circuit.

PMOS transistors are in weak inversion, so they can be analyzed as PNP bipolar transistors in the first order analysis. The drain current I_D of the PMOS transistor can be expressed as [4]

$$I_D = \frac{W}{L} K \exp\left(\frac{V_{SG} - |V_{th}|}{n \cdot V_T}\right) \quad (1)$$

where W/L is the width to length ratio of the transistor, K is a process parameter, V_{SG} is the source to gate voltage, V_{th} is a threshold voltage of PMOS transistor, V_T equals to kT/q and n is approximately 1.5. If V_{SG} is solved from equation (1), V_{SG} can be expressed as

$$V_{SG} = \ln\left(\frac{I_D \cdot L}{KW}\right) \cdot nV_T + V_{th} \quad (2)$$

and now the ΔV_{SG} of the transistors of different W/L ratio can be expressed as $\Delta V_{SG} = nV_T\ln(N)$, where N is 8 in figure 1. The voltages of nodes 1 and 2 are kept on the same potential by an operational amplifier, so the currents through the equal resistors R_1 and R_2 are proportional to the V_{SG} of M1. Now we get the equation for the reference current.

$$I_1 = I_2 = \frac{n \cdot V_T \ln N}{R_0} + \frac{V_{SG}}{R_1} \tag{4}$$

In the first order analysis V_T can be expressed as

$$V_T = \frac{kT_0}{q}(1 + \alpha \cdot \Delta T) \tag{5}$$

where T_0 is the nominal temperature, and $\Delta T = T - T_0$. Also V_{SG} and R_0 can be expressed as

$$V_{SG} = V_{SG,T0}(1 - \beta \cdot \Delta T) \tag{6}$$

$$R_0 = R_{0,T0}(1 + \gamma \cdot \Delta T) \tag{7}$$

The ratio (r) of R_1 to R_0 can be chosen so that I_{ref} is stabilized. In this case the ratio should be satisfied as

$$r = \frac{qV_{SG,T0}}{kT_0 n \ln(N)} \cdot \frac{\beta + \gamma}{\alpha - \gamma} \tag{8}$$

and then the constant current is

$$I_1 = I_2 = \frac{1}{R_{0,To}} \cdot \left(n\frac{kT_0}{q}\ln(N) + \frac{V_{SG,T0}}{r} \right) \tag{9}$$

I_{ref} can now be generated to the required level of the application by choosing the size of the bias net transistor shown in figure 2.

The reference voltage V_{ref} can be expressed as

$$V_{ref} = \frac{R_{ex}}{R_e + R_{ex}} \cdot \left(I_{Vref} R_e + V_{SG} \right) \tag{10}$$

The mirrored current I_{Vref} is also constant, so if the voltage V_{ref} needs to be constant, too, the temperature drift of the V_{SG} of the transistor M3 has to be compensated for by the drift of R_e. This means that $I_{Vref}R_e + V_{SG}$ has to be constant as a function of temperature, so we can use (6) and (7) and write

$$V = I_{Vref} R_{eT0}(1 + \gamma \cdot \Delta T) + V_{SGT0}(1 - \beta \cdot \Delta T) \tag{11}$$

and by differentiating this we derive

$$\frac{\partial V}{\partial T} = \gamma R_{eT0} - \frac{V_{SGT0}}{I_{Vref}}\beta \tag{12}$$

$\partial V/\partial T$ is zero, so R_{eT0} can be expressed as

$$R_{eT0} = \frac{V_{SGT0}}{I_{Vref}} \cdot \frac{\beta}{\gamma} \tag{13}$$

The resistor R_{ex} is only used to choose the level of the reference voltage V_{ref} [2]. The temperature drift of the reference voltage is proportional to the absolute value of resistor R_{eT0}, but the process variation of the N diffusion resistor (±20%) is compensated for by the reference current variation, which is inversely proportional to the absolute value of the resistor R_1 and R_2.

The variation of process parameters in different chips is the main error source in a reference circuit. This is usually compensated by trimming resistors in reference circuits. Here trimming is made by using bias net circuits for both voltage generation to minimize a drift and to set an absolute value and the current generation to set an absolute value. Figure 2 shows the schematic diagram of the bias net circuit. The output of the operational amplifier is connected to the bias nets and the out nets are connected to the nodes V_{ref} and V_{Iref} shown in figure 1. The required current is chosen by a binary word ($B_0 - B_n$). The widths of the bias transistors are shown in table 1. W_V and W_I are the widths of the transistors in I_{ref} and V_{ref} generation, respectively. The absolute value of I_{ref} varies more than V_{ref} by the absolute value of the resistors in different chips, wherefore I_{ref} generation requires more transistors than V_{ref} generation.

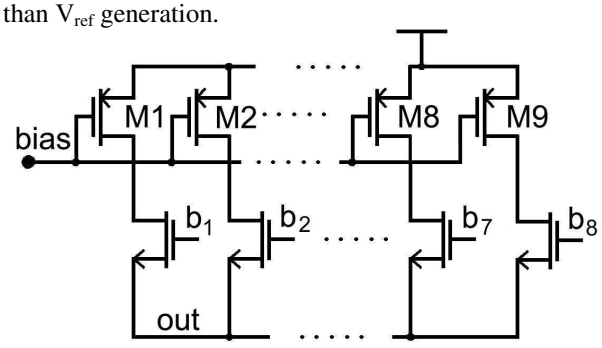

Figure 2. The schematic diagram of the bias net circuit.

Table 1. The sizes of the bias transistors in the bias net circuit.

	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}
W_V	0.5	1	1	1	1	5	5	10	-	-
W_I	0.5	1	1	1	1	5	10	20	30	40

3. SIMULATION RESULTS

The circuit was simulated in the 0.18 µm CMOS process by Spectre. The circuit was simulated at 9 different corner points, which were the combinations of maximum, typical and minimum value of resistors and slow, typical and fast MOS parameters. These 9 simulations were made in the temperature range of -10ºC to 70ºC and in the supply voltage range of 1 V to 2.2 V with and without trimming. The supply voltage was set to 1.8 V in the temperature performance simulations.

The temperature performance of the reference voltage at the different corner points without trimming is shown at the top of figure 4. Two worst-case parameter simulations are marked by a square and a triangle and the typical case parameter simulation by a rhombus. The temperature drifts were 6.6 ppm/ºC and 85 ppm/ºC in a typical and the worst-case parameter simulation, respectively, while the absolute variation was ±8.5%.

The temperature performance of the reference current at the different corner points without trimming is shown at the bottom of figure 4. The middle line is the current drift of typical case parameters. Other lines show the worst drifts at different corner points. The temperature drift of a typical case was 11 ppm/ºC and both of the worst-case drifts were less than 54 ppm/ºC and the absolute variation stayed within ±30%.

The temperature performance of the reference voltage and current at all different corner points with trimming the absolute value of the instants is shown from the top to the bottom in figure 5. The maximum temperature drifts of the reference voltage and current were 92 ppm/ºC and 53 ppm/ºC, respectively.

The supply voltage performance of the reference voltage and current at all different corner points with trimming the absolute value of the references is shown from the top to the bottom in figure 6. The maximum voltage and current variations were 0.35% and 0.43%, respectively, for a supply voltage of 1 to 2.2 V. The maximum variations were discovered in the simulations of the slow MOS process parameters and those results can be seen in figure 6, where the lines have nonlinear points for a supply voltage of 1 to 1.2 V. The reason for those nonlinear points is that load transistors enter the edge of the triode region in the operational amplifier. The simulations also showed that the maximum voltage and current variations were 0.13% and 0.16%, respectively, for a supply voltage of 1.1 to 2.2 V.

Temperature drift simulations were also made by using the supply voltage of 1 V, and then the maximum temperature drifts of the reference voltage and current were 94 ppm/ºC and 116 ppm/ºC, respectively. Using the supply voltage of 1.1 V maximum temperature drifts were the same as the drifts shown at the bottom in figure 5.

The voltage reference simulation also showed that if the absolute value of the voltage were not critical in an application such as a voltage reference locked oscillator circuit, the voltage reference could be trimmed so that the temperature drift is minimized. In that case the temperature drift of the voltage reference is less than 10 ppm/ºC at all different corner points.

The current consumption of the circuit is approximately 160 µA. In comparison with the design made of two separate reference circuits in a similar manner, this design needs only approximately 60% of the current and area.

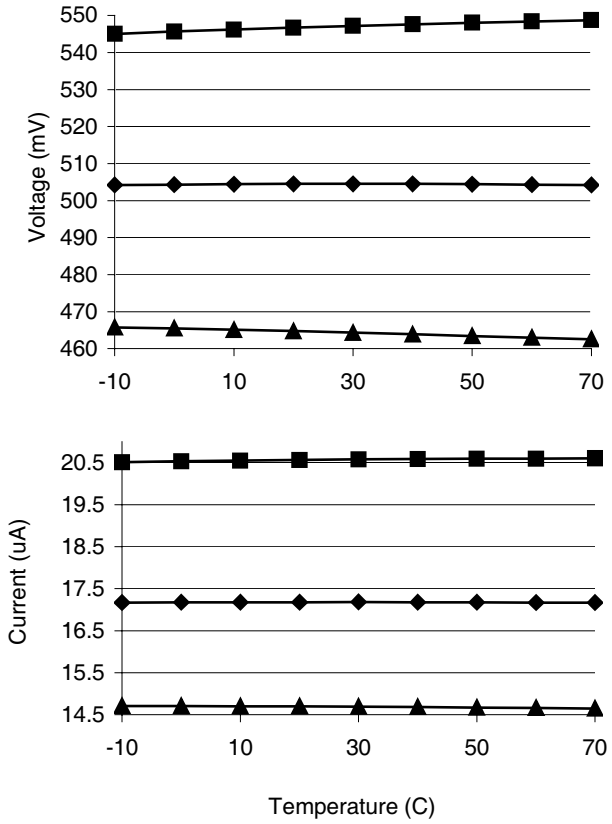

Figure 4. The temperature performance of the voltage and current references at the different corner points.

4. CONCLUSIONS

An integrated CMOS current-voltage reference circuit has been described. The current-voltage reference circuit has been simulated in the 0.18 µm CMOS process by Spectre. The current reference generation is based on diode connected PMOS transistors in weak inversion in the traditional bandgap circuit. The voltage reference is generated by using the constant reference current by compensating the negative temperature coefficient of the diode connected PMOS transistor by the positive temperature coefficient of the N diffusion resistor Re. This makes it possible to fabricate a reference circuit, where both the current and the voltage are generated by using

only one operational amplifier. This saves the current consumption and the used chip area of the circuit compared to the structure, where both the current and the voltage references are implemented by using conventional circuits.

The simulated worst-case temperature drifts of the voltage and current references were 92 ppm/ºC and 53 ppm/ºC with trimming and 85 ppm/ºC and 54 ppm/ºC without trimming, respectively, in the temperature range of -10ºC to 70ºC, and the simulated worst-case supply voltage drifts of the voltage and current references were 0.13% and 0.16%, respectively, for a supply voltage of 1.1 to 2.2 V. The current consumption and the area of the design were also reduced by 40% as compared to the structure, where both the current and the voltage references are implemented by using conventional circuits.

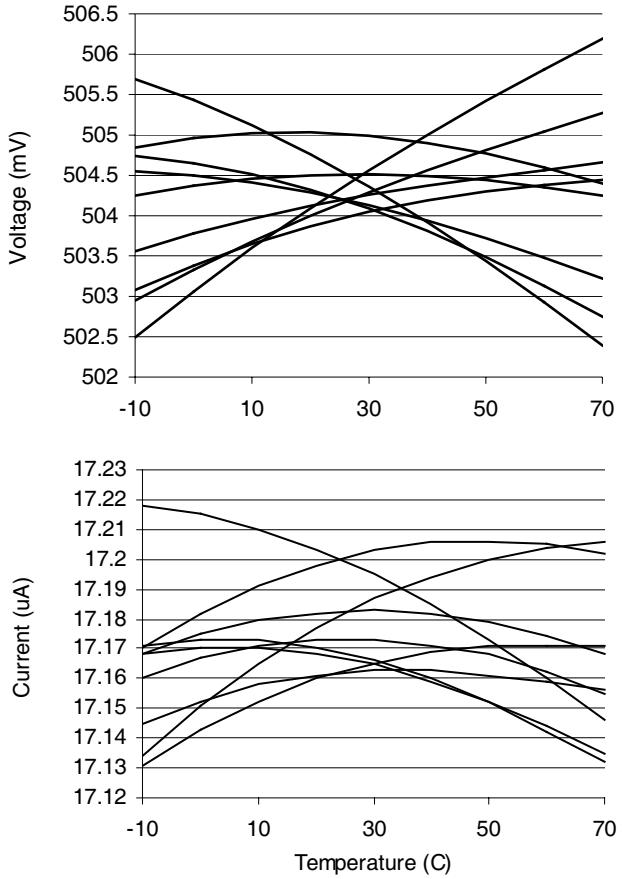

Figure 5. The temperature drifts of the trimmed voltage and current references at all different corner points.

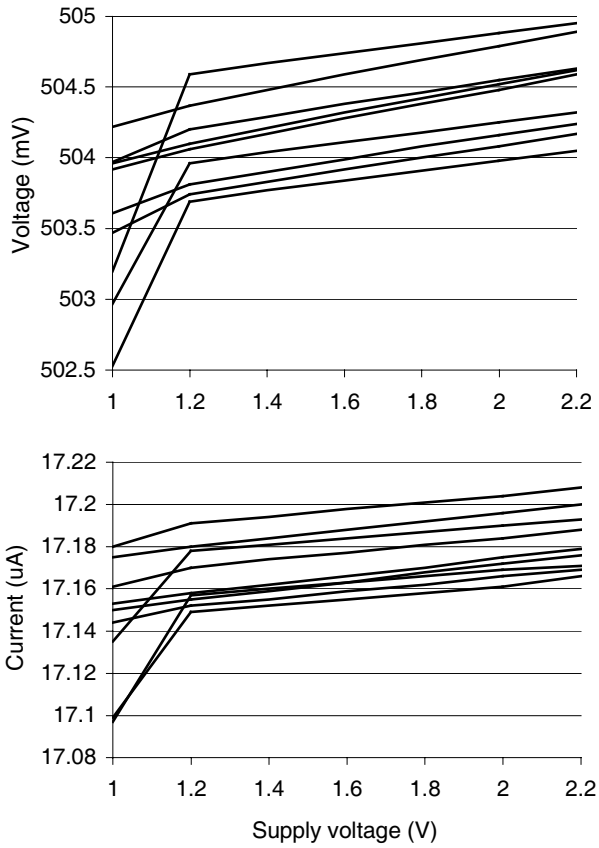

Figure 6. The supply voltage drifts of the voltage and current references at all different corner points.

5. REFERENCES

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