Low- voltage folded-switching mixers in 0.18 µm CMOS

A Low-Voltage Folded-Switching Mixer in 0.18-μm CMOS

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***Abstract*—Scaling of CMOS technologies has a great impact on analog design. The most severe consequence is the reduction of the voltage supply. In this paper, a low voltage, low power, ac-coupled folded-switching mixer with current-reuse is presented. The main advantages of the introduced mixer topology are: high voltage gain, moderate noise figure, moderate linearity, and operation at low supply voltages. Insight into the mixer operation is given by analyzing voltage gain, noise figure (NF), linearity (IIP3), and dc stability. The mixer is designed and implemented in 0.18-μm CMOS technology with metal–insulator–metal (MIM) capacitors as an option. The active chip area is 160 μm $\times$ 200 μm. At 2.4 GHz a single side band (SSB) noise figure of 13.9 dB, a voltage gain of 11.9 dB and an IIP3 of −3 dBm are measured at a supply voltage of 1 V and with a power consumption of only 3.2 mW. At a supply voltage of 1.8 V, an SSB noise figure of 12.9 dB, a voltage gain of 16 dB and an IIP3 of 1 dBm are measured at a power consumption of 8.1 mW.**

***Index Terms*—CMOS mixers, switching mixers, folded mixers, current-reuse, low voltage, low power.**

I. Introduction

FOR digital circuits, CMOS technology scaling yields an improvement in power consumption, operating speed, and number of transistors per unit area. While CMOS technology scaling is quite beneficial for digital circuits, this is not the case for RF analog circuits. The most severe consequence of technology scaling that affects the RF analog design is a reduction of the voltage supply. Insufficient voltage headroom causes that not all circuit topologies can satisfy the required specifications. Hence, research into low-voltage circuit topologies is important. This paper discusses a low-voltage ac-coupled folded-switching mixer with current-reuse. This mixer can operate at a supply voltage of 1 V and still offer good performance.

The performance of double-balanced switching mixers is normally sufficient for a majority of applications (typically noise figure (NF) of 10 dB, voltage gain of 10 dB and IIP3 of 1 dBm at power dissipation levels of 6 mW) [1]. In the double-balanced switching mixer (see Fig. 1) the transistors in the switching stage ($M3, M4, M5$, and $M6$) are stacked on top of the transistors that comprise the transconductor ($M1$ and $M2$). Also, the load resistor (R) is placed on top of the switching stage. This way of connecting the transconductor, the switching stage, and the load resistors is conflicting with operation at low supply voltages. All dc tail current flows through the transconductor, the switching stage and the load resistors. Therefore, at a low voltage supply (for example at $V_{\rm dd} = 1$ V) the voltage drops, across the load resistors, the switching transistors and the transistors in the transconductor become critical. In this particular case it is difficult to keep all the transistors to operate in their saturation region and this causes a significant drop in performance. Hence, it is of interest to find new mixer topologies that can handle successfully low supply voltages.

In terms of operation at low supply voltages, the goal is to reduce the voltage drops across the load resistors and the switching transistors. This can be done by designing a switching mixer in which only a part of the dc current from the transconductor flows through the switching stage and the load resistors. In this case the switching stage may be regarded as folded with respect to the transconductor. Therefore, we call this mixer folded-switching mixer. Apart from the dc current flow, the situation related to the flow of the ac current is quite opposite. In order to obtain the highest performance possible (voltage gain, noise figure) the total ac current from the transconductor must flow through the switching stage. So, the switching stage topology stays the same as in the double-balanced switching mixer and the topology of the transconductor has to be suitable for providing the desired flow of the ac and the dc current.

This paper is organized as follows. The transconductors suitable for application in the low-voltage folded-switching mixer are discussed in Section II. In Section III, the analysis and design related to the ac-coupled folded-switching mixer with current-reuse are presented. Insight into the mixer operation is given by discussing voltage gain, noise figure, linearity, and dc stability. The simulated and experimental results are reported in Section IV, while mixer benchmarking is discussed in Section V. The conclusions are presented in Section VI.

II. Transconductors for Folded-Switching Mixers

In the case of the double-balanced switching mixer (see Fig. 1), the single nMOS transistor is used as the transconductor. Fig. 2 shows three different transconductors suitable for application in the low-voltage folded-switching mixer. Actually, they represent improvement of the single nMOS transconductor with respect to operation at low supply voltages.

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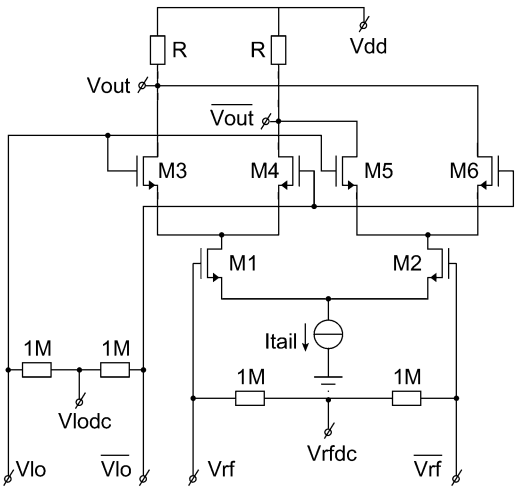

Fig. 1. Double-balanced switching mixer.

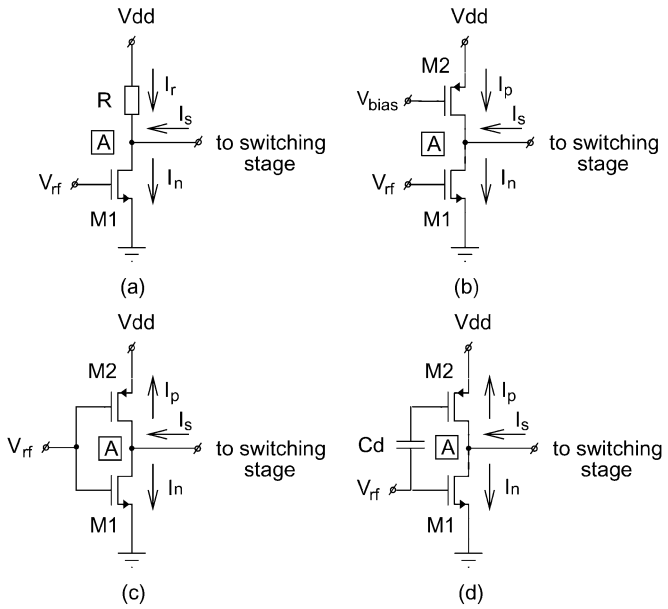

Fig. 2. Transconductors for folded-switching mixers.

The transconductor with resistive load is the most simple modification of the single nMOS transconductor [see Fig. 2(a)]. The ac current I_n, which is generated in the nMOS transistor, splits to the currents flowing through the switching stage (I_s) and through the resistor $R(I_r)$. The fact that a part of the ac current flows through the resistor R represents the drawback of this transconductor. In order to reduce I_r the value of the resistor R has to be increased. As a consequence care must be taken to keep the dc voltage at the node A sufficiently high in order to keep the transistor $M1$ saturated. At low supply voltages this problem is even more prominent.

The drawback of the transconductor with resistive load can be alleviated by using the transconductor with active load [see Fig. 2(b)]. By replacing the resistor R with the pMOS transistor the ac current through this transistor (I_p) is further reduced due to the high output impedance of the pMOS transistor. Instead of using pMOS transistor only to increase the impedance between the node A and $V_{\rm dd}$, it can be also used to amplify RF signals. In this way the leakage of the ac current toward the ac ground through the output impedance of the pMOS transistor can be ideally completely avoided. Hence, a CMOS inverter, which is used as the transconductor, is obtained [see Fig. 2(c)].

In the CMOS inverter, the RF signal amplification by the pMOS transistor is a result of current reuse principle [2]. This is an efficient way to have a high gain and a low noise figure with a low power. The ac current I_s is equal to the sum of the ac currents I_n and I_p. Based on that the total transconductance is equal to $g_{mn} + g_{mp}$, where g_{mn} is the transconductance of transistor M_1 and g_{mp} is the transconductance of transistor M_2. Before going further with a detailed analysis of the folded-switching mixer that uses the CMOS inverter as the transconductor, it is instructive to check the lowest supply voltage that can be applied. It is determined by the threshold voltages (V_t) and by the overdrive voltages of the transistors $M1$ and $M2$. The overdrive voltages of $M1$ $(V_{\rm ovn})$ and $M2$ $(V_{\rm ovp})$ can be calculated using

$$V_{\rm ovn} = V_{\rm rfdc} - V_t \tag{1}$$

$$V_{\rm ovp} = V_{\rm dd} - V_{\rm rfdc} - V_t. \tag{2}$$

$V_{\rm rfdc}$ is the biasing voltage applied at the gates of the transistors M_1 and M_2. Finally, the minimal supply voltage $(V_{\rm dd,min})$, at which this mixer can operate, is expressed as

$$V_{\rm dd,min} = V_{\rm ov1} + V_{\rm ov2} + 2V_t. \tag{3}$$

Typical value of V_t in 0.18-μm CMOS is in the range of 500 mV. From (3), it is clear that the minimum supply voltage $(V_{\rm dd,min})$ must be higher than 1 V. This is the disadvantage of the CMOS inverter, which is used as the transconductor in the low voltage folded-switching mixer.

In order to overcome the described limitation, the biasing for nMOS and pMOS transistors in the CMOS inverter have to be separated. In this way an ac-coupled complementary transconductor is obtained [see Fig. 2(d)]. If $V_{\rm rfdcn}$ is the biasing of $M1$ and $V_{\rm rfdcp}$ of $M2$, (3) becomes

$$V_{\rm dd,min} = V_{\rm ov1} + V_{\rm ov2} + 2V_t + V_{\rm rfdcp} - V_{\rm rfdcn}. \tag{4}$$

Choosing $V_{\rm rfdcn}$ to be greater than $V_{\rm rfdcp}, V_{\rm dd,min}$ can be reduced. Combining the ac-coupled complementary transconductor with the switching stage and the load resistors, the ac-coupled folded-switching mixer with current-reuse is obtained. It is presented in Fig. 3. The next section presents the analysis of this mixer.

III. AC-Coupled Folded-Switching Mixer With Current-Reuse

A. Gain and Noise Figure

Assuming that LO voltage is an ideal square wave, the voltage gain of the mixer in Fig. 3 can be approximated by

$$G = 20\log\left(\frac{2}{\pi}(g_{mn} + g_{mp})R\right). \tag{5}$$

g_{mn} is the transconductance of $M1$ and $M2, g_{mp}$ is the transconductance of $M3$ and $M4$ and R is the load resistor

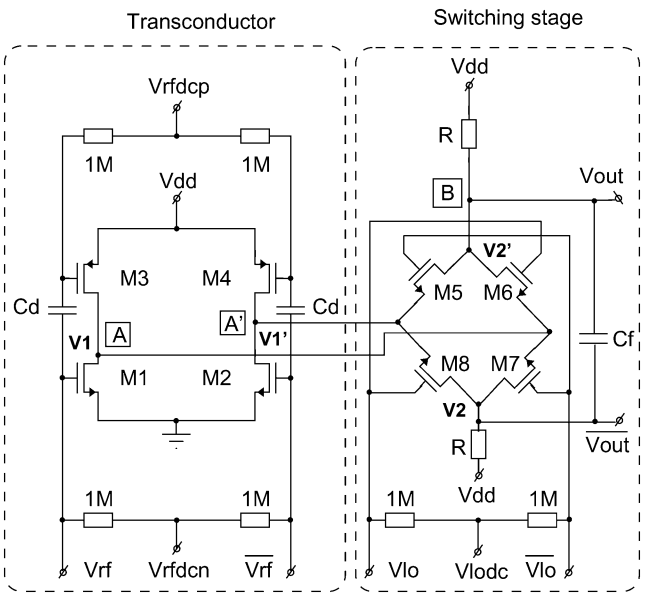

Fig. 3. AC-coupled folded-switching mixer with current-reuse.

(see Fig. 3). Since only a small part of the dc current from the transconductor flows through the switching stage, large load resistors can be used. Hence, the voltage gain is improved, but at the same time the switching transistors have to handle a large output voltage swing. Therefore, the dc voltage V_2 has to be kept sufficiently high and voltage V_1 sufficiently low. On the other hand, voltage V_1 should be sufficiently high in order to keep the transistors $M1$ and $M2$ saturated.

The NF of the ac-coupled folded-switching mixer with current-reuse, under the assumption that the LO voltage is an ideal square wave and taking into account the noise folding from the image frequency, can be approximated by

$$\mathrm{NF} = 10\log\left(2 + \frac{4(\gamma_n g_{mn} + \gamma_p g_{mp})}{R_s(g_{mn}+g_{mp})^2} + \frac{\pi^2}{2(g_{mn}+g_{mp})^2 R R_s}\right). \quad (6)$$

R_s is the source resistance and the coefficient γ_n is equal to $2/3$ for long channel transistors and need to be replaced with a larger value for submicron MOSFETs [3].

B. Linearity

The transfer function of the mixer $(V_{\mathrm{outdif}}/V_{\mathrm{rfdif}})$ is shown in Fig. 4. The switching transistors will be turned off by the high voltage swing at the nodes A and A' (see Fig. 3). In this case a high current pushed by the transistors $M3$ or $M4$ will cause a high voltage across the output impedance of the transistors $M1$ or $M2$ that will turn the switching transistors $M7$ and $M6$ or $M5$ and $M8$ off. The input voltage range between the points A and B is denoted with s (see Fig. 4). Nonlinearity in the mixer transfer function between the points A and B is caused by operation of the switching transistors in the linear region. In Fig. 4 the deviations are denoted with d. Linearity mainly depends on s. It can be improved by increasing s and reducing d. In the folded-switching mixer with current-reuse, s can be increased by decreasing the voltages $V1$ and $V1'$, and by reducing the

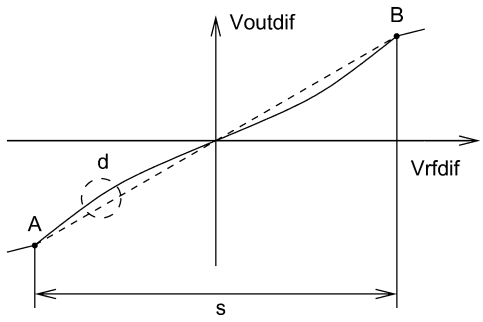

Fig. 4. Transfer function of the ac-coupled folded-switching mixer with current-reuse.

voltage swing at the nodes A and A' (see Fig. 3). The deviation (d) from a linear transfer function between the points A and B can be reduced by keeping the switching transistors far from the linear region.

C. DC Stability

In order to design a robust ac-coupled folded-switching mixer with current-reuse that can stand at least voltage supply variations of 10%, it is necessary to calculate the variations of voltage V_1 or V_1' as a function of the supply voltage variations ($\Delta V_{\mathrm{rfdcn}}$ and $\Delta V_{\mathrm{rfdcp}}$). This can be done by applying the large signal analysis and Kirchoff's law on the node A (see Fig. 3):

$$I_n = I_p + 2I_s. \quad (7)$$

I_n is the current through the transistor $M1$, I_p through $M3$ and I_s through $M6$ and $M7$. Current I_n can be expressed as

$$I_n = \frac{1}{2}\mu_n C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{gs}} - V_t)^2(1+\lambda V_1) \quad (8)$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W is the channel width, and L is the channel length, V_t is the threshold voltage, V_{gs} is the gate-source voltage and λ is channel-length modulation coefficient. Similar equations can be written for currents I_p and I_s. Substituting the expressions for I_n, I_p, and I_s in (7), an equation that contains V_1 to the third power is obtained that is difficult to solve it in an insightful closed form.

In order to overcome this difficulty, small signal analysis is applied assuming that the variations of voltages V_{rfdcn} and V_{rfdcp} are small. This analysis will give an estimation about the variations of voltage V_1. Substituting the small signal model for each transistor (parallel connection of transistor output impedance and ideal current source with value $g_m V_{\mathrm{in}}$, where g_m is the transconductance and V_{in} the small signal voltage at the gate) the variations of voltage $V1$ or $V1'$ can be calculated:

$$\Delta V1 = -\frac{g_{mp}\Delta V_{\mathrm{rfdcp}} + g_{mn}\Delta V_{\mathrm{rfdcn}}}{1/R_{\mathrm{op}} + 1/R_{\mathrm{on}} + 2g_{ms}}. \quad (9)$$

R_{op} and R_{on} are output impedances of transistors $M1$ and $M3$. g_{ms} is the transconductance of the switching transistors. In the denominator g_{ms} (in the design $g_{ms} = 2.5$ mS) dominates and reduces the variations of the voltage $V1$. Simulations are done taking into account process spread, supply voltage variations of 10% and temperature variations (-25 °C to 70 °C). Under

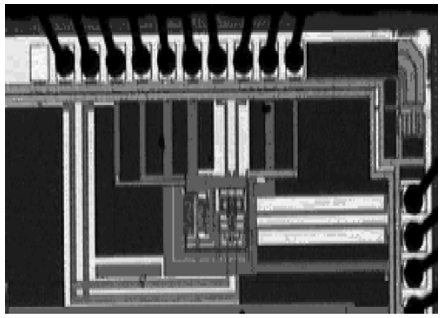

Fig. 5. Die microphotograph of the ac-coupled folded-switching mixer with current-reuse.

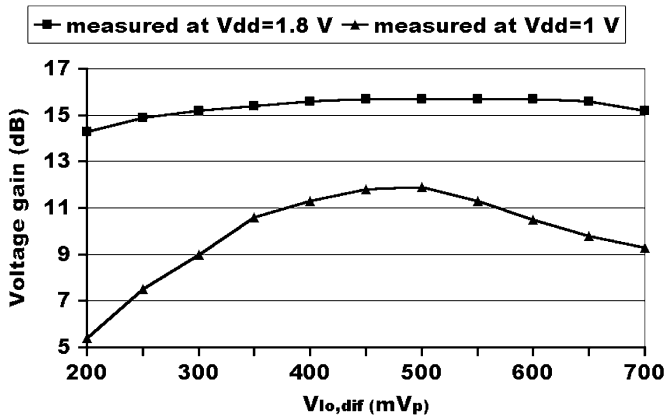

Fig. 6. Measured voltage gain versus LO voltage swing.

these conditions V_1 varies in the range from 232 to 450 mV and nominally $V_1 = 310$ mV. These variations do not deteriorate the circuit operation significantly and there is no need for common mode feedback, which is another advantage of the proposed mixer.

IV. Simulation and Experimental Results

Fig. 5 shows the die photograph of the realized ac-coupled folded-switching mixer with current-reuse. The active chip area is 160 μm $\times$ 200 μm. Total dissipation of the IC is 8.1 mW at a supply voltage $(V_{\rm dd})$ of 1.8 V and 3.2 mW at a supply voltage of 1 V.

Fig. 6 shows the measured mixer voltage gain (G) as a function of the differential LO voltage swing $(V_{\rm lo,dif})$. In Fig. 6 the numbers on the *x* axis denote the peak values of the applied differential LO voltage swing. The LO frequency is set to 2.4 GHz, while the output signal is measured at an intermediate frequency (IF) of 1 MHz. As it can be seen, the voltage gain reaches the highest value for $V_{\rm lo,dif} = 500$ mV$_{\rm p}$. For $V_{\rm lo,dif}$ lower than 500 mV$_{\rm p}$, the voltage gain is reduced because the switching transistors do not perform the current commutation well. For $V_{\rm lo,dif}$ higher than 500 mV$_{\rm p}$ the switching transistors partly operate in the linear region when they conduct. This also causes a gain reduction.

Measured and simulated voltage gain at supply voltages of 1 V and 1.8 V versus frequency are shown in Fig. 7. The difference between the measured and simulated results is mainly due to inter-connect parasitics.

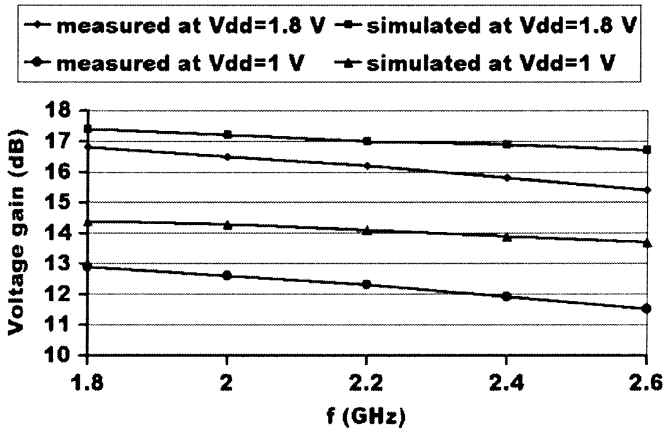

Fig. 7. Measured and simulated voltage gain versus frequency.

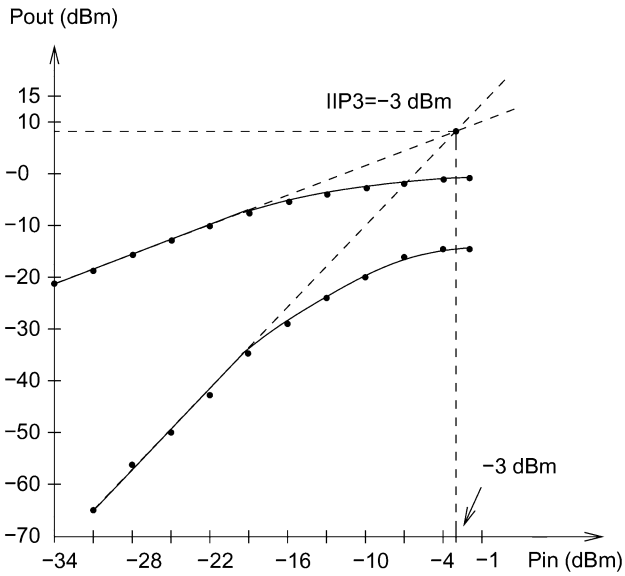

Fig. 8. Measured IIP3 at a supply voltage of 1 V.

The noise figure (NF) is measured and simulated at an IF of 1 MHz with a 50 Ω source resistance and 1 kΩ load resistance, and with a differential LO voltage swing of 500 mV$_{\rm p}$. For LO frequency of 2.4 GHz, a single side band (SSB) NF of 12.9 dB is measured at a supply voltage of 1.8 V and a SSB NF of 13.9 dB at a supply voltage of 1 V. The measured values for the NF corresponds very well to the simulated results: SSB NF $= 12$ dB at $V_{\rm dd} = 1.8$ V and SSB NF $= 13.4$ dB at $V_{\rm dd} = 1$ V.

Fig. 8 shows a measured IIP3 at a supply voltage of 1 V. The simulated IIP3 for the same supply voltage is -2.7 dBm. At $V_{\rm dd} = 1.8$ V, a measured and simulated IIP3 are 1 dBm and 0 dBm, respectively.

V. Mixer Benchmarking

In order to evaluate the performance of the ac-coupled folded-switching mixer with current-reuse, the performance of relevant CMOS mixers are given in Table I. It is important to mention that mixer performance given in the fifth row are extrapolated based on the measurement results presented in [7].

When comparing the measured performance of the ac-coupled folded-switching mixer with current-reuse with the performance

TABLE I
PERFORMANCE OF SOME CMOS MIXERS

Row	Ref.	freq. (GHz)	V_{dd} (V)	I (mA)	NF (dB)	G (dB)	IIP_3 (dBm)
1	[4]	0.9	0.9	5.2	13.5	2	3.5
2	[5]	1.9	1.8	4.8	10.2	0.5	-6
3	[6]	2.5	0.6	2.7	14.8	5.4	-2.8
4	[6]	2.5	0.8	3	15.9	5.7	4.3
5	[7]	2.4	1	6.6	14	11	4.1
6	this work	2.4	1.8	4.5	12.9	15.7	1
7	this work	2.4	1	3.2	13.9	11.9	-3

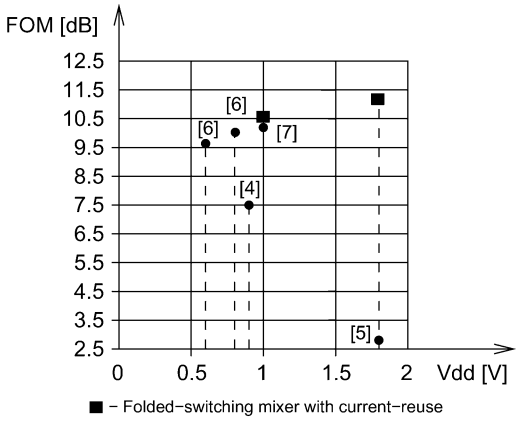

Fig. 9. Mixer benchmarking

of some CMOS mixers, given in Table I, the following advantages of the ac-coupled folded-switching mixer with current-reuse can be observed: high voltage gain, moderate noise figure combined with operation at low supply voltage. Comparing the measured value for the noise figure of the folded-switching mixer with current-reuse with the values for the noise figure of the CMOS mixers given in Table I it is important to take into account the fact that some referenced mixers are implemented in older CMOS technologies where the level of thermal and flicker noise was lower. Also some of them use very high intermediate frequency (IF) avoiding the contribution of the flicker noise. The disadvantage of the ac-coupled folded-switching mixer with current-reuse is bad power supply rejection ratio. Therefore, care must be taken to provide stable power supply.

The performance of the ac-coupled folded-switching mixer with current-reuse can also be expressed by a figure of merit (FOM). The FOM is defined in the following way:

$$\mathrm{FOM} = 10\log\left(\frac{10^{G/20}\cdot 10^{(\mathrm{IIP3}-10)/20}}{10^{\mathrm{NF}/10}\cdot P}\right). \qquad (10)$$

Voltage gain G and NF are expressed in dB and IIP3 in dBm. The FOM is based on the fact that the performance of the mixer is better if NF and power consumption (P) are as low as possible, while voltage gain (G) and IIP3 are as high as possible. The calculated FOM for the ac-coupled folded-switching mixer with current-reuse and for CMOS mixers from Table I is presented in Fig. 9. As it is evident from Fig. 9, the ac-coupled folded-switching mixer with current-reuse shows very good FOM compared to the CMOS mixers presented in Table I.

VI. CONCLUSION

A high-gain, low-voltage, low-power ac-coupled folded-switching mixer with current-reuse is presented. This mixer is designed and implemented in 0.18-μm CMOS technology. The main advantages of the proposed new mixer topology are high voltage gain (15.7 dB), moderate noise figure (12.9 dB), moderate linearity (IIP3 $=$ 1 dBm), operation at low supply voltages ($V_{\mathrm{dd}} = 1$ V), and simplicity since common-mode feedback is not necessary. Normalizing mixer performance with a figure of merit shows that the ac-coupled folded-switching mixer with current-reuse has excellent performance in comparison with other CMOS mixers.

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Since 2001, Dr. van Roermund has been one of the three organizers of the yearly Workshop on Advanced Analog Circuit Design (AACD). In 2004, he was awarded Simon Stevin Meester for his scientific and technological achievements.