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A Low-Voltage Low-Power Front-End for Wearable EEG Systems

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***Abstract*— A low-voltage and low-power front-end for miniaturized, wearable EEG systems is presented. The instrumentation amplifier, which removes the electrode drift and conditions the signal for a 10-bit A/D converter, combines a chopping strategy with quasi-FGMOS (QFG) transistors to minimize low frequency noise whilst enabling operation at 1 V supply. QFG devices are also key to the A/D converter operating at 1.2 V with 70dB of SNR and an oversampling ratio of 64. The whole system consumes less than 2uW at 1.2V.**

I. Introduction

Electroencephalography (EEG) has traditionally played a vital role in monitoring, diagnosis and treatment for certain clinical situations such as epilepsy, syncope and sleep disorders, and has relatively recently emerged as a powerful tool for neuroscientists to investigate cognitive states and enhance task-related performance of an operative through computer mediated assistance [1]. Ideally monitoring of cognitive states should be carried out using a sensor system which does not interfere with the user to avoid influencing the state of the user. In practice, long term monitoring is required (hours or days) and conventional EEG systems limit user mobility due to their bulky size. The main constraint for the weight reduction of current EEG systems is the battery size required for the long term operation of the constituent electronics. Reducing power consumption is thus the first step towards a truly miniaturized wearable EEG system. This is a challenging task due to the nature of scalp EEG signals. On one hand scalp EEG is very low in amplitude (2μV-500μV) and frequency (0.5 Hz-30Hz); on the other hand, scalp electrodes drift with time superimposing a low frequency signal in the order of tens of millivolts [2].

Two strategies can be followed to deal with this: a) eliminate the electrode drift following the signal acquisition; b) remove it in the front end. The main drawback of the first strategy is that the drift signal is much larger than the EEG signal necessitating a 20-bit analogue to digital converter. This is not trivial if the power is a constraint. The second strategy avoids this problem, but requires that the electrode drift is filtered without also affecting the band of interest.

This paper presents a very low power front end system suitable for wearable EEG systems. The front end consists of an instrumentation amplifier that filters out very low frequency signals and hence reduces the effect of the electrode drift, whilst amplifying the signals of interest by a factor of 100; and a 10-bit analogue-to-digital converter. The following sections explain how acceptable performance of these two blocks has been achieved despite challenging constraints on power consumption and supply voltage.

II. The Instrumentation Amplifier

The power, supply voltage and noise constraints combined with a signal dominated by electrode offset make the design of this amplifier particularly challenging. An rms input referred noise voltage of less than 2 μV is required to be able to sense the lowest EEG signal. The gain should be between 40 dB and 50 dB to achieve the required resolution with the ultra low power analogue-to-digital converter presented in the following section whilst ensuring that the amplifier does not saturate. The current drain should be no more than a few microamps at 1.2 V supply and the large DC offset must be rejected in order to achieve the required dynamic range.

The literature reveals that the chopper technique consistently achieves impressive noise performance [3] [4] and that low power operation is possible [4]. It was therefore decided to design a chopper amplifier for this application. The basic architecture is shown in figure 1. The frequency conversion process is performed by four switches at the input and output of the amplifier as shown in figure 1. The switches are driven by two antiphase non-overlapping clocks, Φ_1 and Φ_2, at the chop frequency, f_c.

Electrodes Drift: Rejection of the electrode dc offset before amplification is necessary to achieve the required dynamic range, which is severely limited by the low

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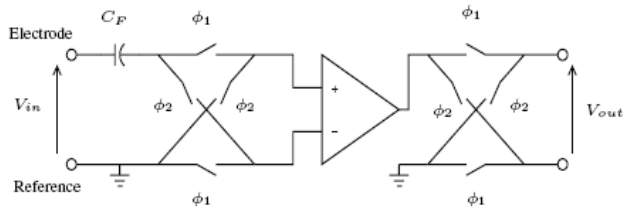

Figure 1. Chopper amplifier with preceding DC rejection filter

voltage supply. To minimize the required capacitance for a high pass corner frequency of below 0.5 Hz a very large resistance (R_F>10^{10} Ω for C_F≤40 pF) is needed. This high pass filtering must take place before the signal is upconverted since precisely designing a corner frequency between f_c and f_c+0.5 Hz would be extremely challenging. To minimize flicker noise no active devices are used before frequency upconversion. The input chopper switches combined with the input capacitance of the differential amplifier emulate a resistor, R_F. The equivalent circuit is shown in figure 2. C_F and the effective resistance, R_F, form a high pass filter. $C_{in,1}$ and $C_{in,2}$ represent the input capacitances of the differential amplifier. The node at which voltage V_F is generated, is biased by the body-source diode of the NMOS input switches. Assuming $C_{in,1}$=$C_{in,2}$=C_{in} the equivalent filter resistance, R_F, is given by:

$$R_F = \frac{T_C}{2 \cdot C_{in}}$$

A high R_F can be achieved by decreasing the chop frequency and decreasing the size of the differential amplifier input transistors, M_1 and M_2 (see figure 3).

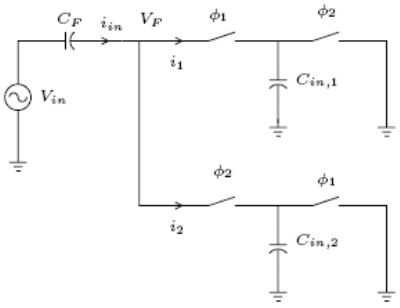

Figure 2. Equivalent high pass filter

Differential Amplifier: The differential amplifier has been designed in two stages as shown in figure 3. To minimise noise in this circuit there is little option but to increase the drain current in the first stage. The noise will be predominantly thermal due to the frequency upconversion process and the transconductance in weak inversion (biasing region for the transistors) can only be improved through increased drain current. Unlike strong inversion operation, this results in the ratio of device sizes being unimportant. The differential output of the first stage is high pass filtered, to control the input common mode of the second stage and to reject offset voltage due to mismatch or process variation, by using QFG transistors at the input of the second stage (M_5 and M_6). The output is also high pass filtered before downconversion. The filtering is done using the diode connected 4 μm by 4 μm PMOS devices, M_{R1}, M_{R2} and M_{R3}, which form an extremely high incremental resistance (>10^{11}) as described in [7], in conjunction with capacitors C_1, C_2 and C_3. C_1 and C_2 (10 pF) and C_3 (1 pF). C_1 and C_2 are set to the higher value of 10 pF to reduce the capacitive division with the input capacitances of the next stage.

Sizing transistors M_1, M_2, M_3 and M_4 is a delicate balance between minimizing noise, maintaining a high R_F and ensuring that g_{m1} is not significantly less than gm3 since the gain of this first stage is g_{m1}/g_{m3}. Transistors M_3 and M_4 are diode-connected to allow M_1 and M_2 to be minimum length. Transistors M_5, M_6, M_7, M_8 and M_{10} form a second stage differential amplifier which provides the gain. Here the transistors can be much larger than those of the first stage to ensure that mismatch and process variation has little effect.

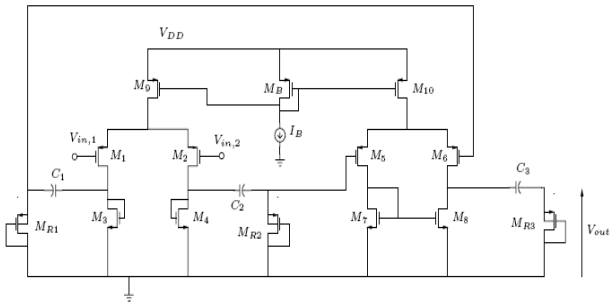

Figure 3. Differential amplifier.

III. The Sigma-Delta Converter

The converter was implemented using a ΣΔ modulator. The sigma-delta modulator basically consists of a filter, a quantizer, and a feedback DAC, and its operation has been thoroughly analyzed in the literature. A second-order architecture has been selected and its block diagram is illustrated in figure 4.

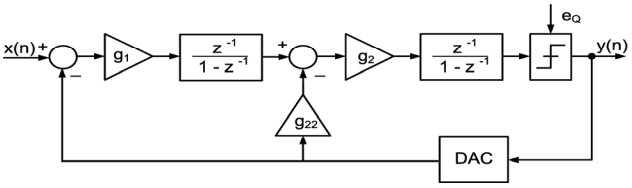

Figure 4. 2nd order ΣΔ modulator block diagram.

This topology was proposed in [6] and presents a lower dynamic range requirement for the integrators' output than the conventional second-order design. Other advantages of this scheme are its relative simplicity (with few operational amplifiers to contribute to the power dissipation) and it's highly insensitive to component mismatches. The converter must exhibit a dynamic range (DR) higher than 65 dB to fulfill the 10-bit accuracy with an oversampling ratio of OSR=64. As the Nyquist frequency is 50 Hz, the sampling frequency is f_s=3.2 kHz.

The integrators' coefficients were appropriately chosen (g_1=0.25, g_{22}=0.5, g_2=0.5), in order to approach the signal range required at the output of the two integrators to the quantizer output range (Δ). This task is even more important in low voltage designs. System simulations have demonstrated an extremely low sensitivity of the modulator with respect to integrator coefficient variations owing to the single-loop architecture. A tolerance for mismatch between capacitors about 20 percent does not affect to the modulator performance.

A: Some Design Considerations

Integrators: Input and feedback gains of the first integrator have the same value. This enables to share the same capacitor for input and feedback sampling, reducing the kT/C noise. Fully differential switched-capacitor integrators were used. For the first integrator a correlated double-sampling strategy was adopted at the input of the integrator to reduce the effect of flicker noise.

Analog switches: A serious problem in switched-capacitor circuits operating at very low voltages is that not enough overdrive voltage can be provided to the gates of transistors acting as switches, strongly limiting signal swings. Several techniques have been proposed to overcome this issue: multi-threshold processes, switched-opamp technique and voltage multiplication in the clock signals. This last technique has been widely used in the past. As an alternative, QFG transistors [7] can be efficiently employed to get rail-to-rail analog switching with more power efficiency than in conventional voltage multiplication, and without affecting the speed of the circuit. Figure 5 shows the analog switch employed [8]. Two complementary QFG transistors, M_{passN} and M_{passP} are connected in series. The gate of M_{passN} is weakly tied to V_{DD} through a large nonlinear resistor implemented by transistor $M_{Rlarge1}$. It is also coupled to the clock signal through a small valued capacitor C_1, so that the clock signal is transferred to the quasi-floating gate. This capacitor performs a level shift of approximately V_{DD} (due to the nonlinear behavior of $M_{Rlarge1}$ the level shift is not of $V_{DD}/2$ as can be found in [10]), which allows switching under very low voltage restrictions. The rail-to-rail operation is achieved thanks to transistor M_{passP}.

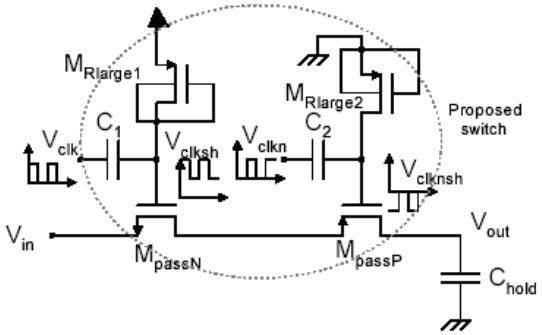

Figure 5. Rail-to rail QFG switch.

Capacitor sizes: SpectreS simulations have been performed to estimate the amplifier's input noise. To evaluate the impact of sampling noise on the base-band modulator input, the equations obtained in [9] have been used. According to the noise study, sampling capacitor of the first integrator greater than 35fF is required. However, to provide a safety's margin, a sampling capacitor of 100fF is used.

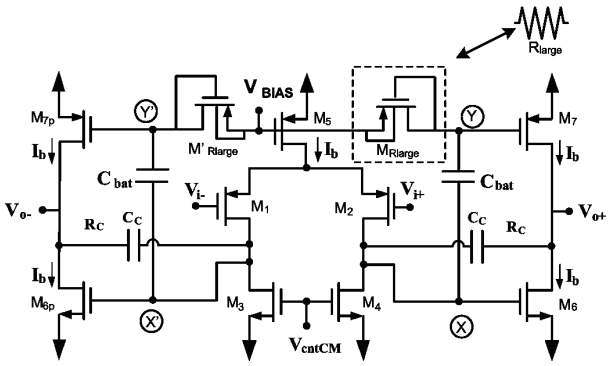

Figure 6. Fully Differential Class AB Opamp.

Operational amplifiers: At low supply voltages the dynamic range is reduced and makes unpractical the use of cascode transistors for high-gain stages. In this context, two stage op-amps are the natural choice since they have rail-to-rail output swing and can drive both resistive and capacitive loads. In order to achieve the settling-time requirement with high slew-rate and very low power consumption, the two stage class AB amplifier, illustrated in detail in Figure 6, has been used [11]. The main novelty of this scheme is that the output stage includes a large resistive element implemented using a minimum size diode connected PMOS transistor M_{Rlarge} and a small valued capacitor C_{bat}. This circuit is able to set the DC operating point of the output stage and, at the same time, during dynamic operation, given that capacitor C_{bat} can not discharge/charge rapidly through M_{Rlarge} it acts as a floating battery and transfers the voltage variations at node X to node Y. This provides class AB (push pull) operation to the output stage.

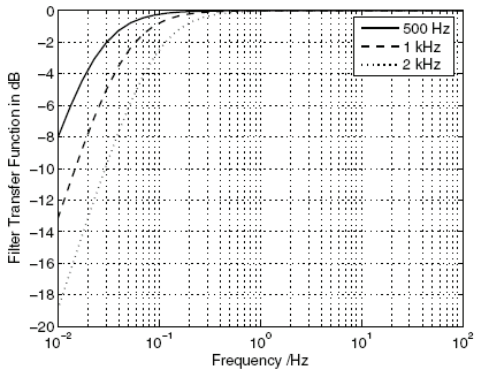

Figure 7. Input filter transfer function for different values of f_c.

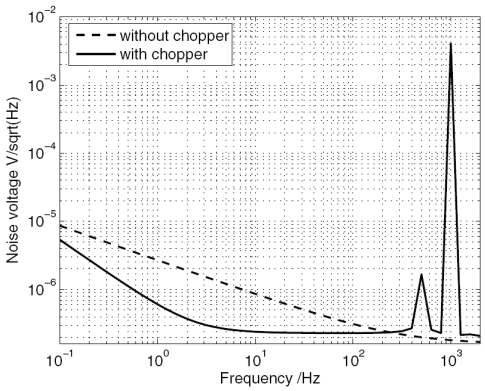

Figure 8. Noise voltage comparison for f_c = 500 Hz.

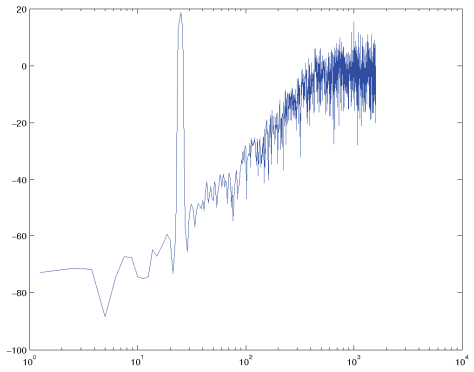

Figure 9. Post-layout simulated output spectrum (2Vpp input signal).

IV. Simulation Results

The circuit was simulated using SPECTRE RF. The performance of the chopper input high pass filter is illustrated in figure 7. The input referred noise voltage, integrated from 0.5 Hz to 30 Hz, of 5.54uV rms is reduced to only 1.5 uV rms by upconverting low frequency flicker noise as shown in figure 8. The chopper amplifier achieves a gain of 44 dB, and consumes 1.7 uW for 1.2V, although it operates down to 1V. The summary of performance for the amplifier in Figure 6 is shown in Table I.

Supply voltage	1.2 V
DC gain	90 dB
Unity gain bandwidth	30 kHz
Bias current	3 nA
Slew-rate	10k V/ms

Table I. Summary of the op-amp performance.

Figure 9 shows the post-layout simulated output spectrum of the complete modulator, featuring 67 dB of SNR. The total power consumption of the ΣΔ modulator is 55 nW.

V. Conclusions And Discussion

Front end circuits suitable for wearable EEG systems have been developed. This work has demonstrated how low power, low voltage design techniques can be profitably exploited in order to improve performance in a biomedical system. A new design technique based on the use of QFG transistors has been exploited in order to accomplish the requirements of this application with very low power consumption. The combined power consumption of the chopper amplifier and the ADC is less than 2uW at 1.2V.

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