A Low Voltage Switched-Capacitor Current Reference Circuit with low dependence on Process, Voltage and Temperature

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Abstract

A low voltage switched-capacitor circuit that generates an almost constant reference current across process, voltage and temperature (PVT) is proposed. The reference voltage is generated by a low voltage band-gap circuit. The output reference current is obtained by applying the generated reference voltage to a low voltage V – I converter. The resistor in the proposed V – I converter is further replaced by a switched capacitor resistor. Due to less variation in the capacitor value across PVT's and high accuracy in integrated voltage reference, the output reference current remains fairly constant. The circuit has been designed in 0.13u CMOS process at 1.5V supply voltage. The simulation results show that the output reference current is quite insensitive to PVT and varies linearly with clock frequency and capacitor value of the switched capacitor resistor.

1. Introduction

Low power design has been a topic of interest of researchers and designers that has compelled the industry to produce circuit designs with very low supply voltage. This paper presents the design of a low voltage current reference circuit that can be operated at supply voltage as low as 1V. The use of low voltage band-gap reference circuit along with a low voltage V-I converter makes it possible to operate the current reference circuit at such low supply voltage. Further, the resistor used in V-I converter has been realized by switched-capacitor (SC) circuit technique. Due to low variation in SC equivalent resistor values coupled with high accuracy in band-gap reference voltage, the generated reference current has very low dependence on PVT thus making it suitable for use in analog and mixed signal circuits which require constant current reference.

2. Circuit Description

Fig.1 shows the schematic of a conventional Vref/R current reference circuit in which a simple V–I converter is used to convert the band-gap reference voltage (Vbg) into a reference current. The minimum supply voltage required to operate this circuit is Vbg + Vds (M1) + Vds (M2) which may be difficult to achieve at lower supply voltages (below 2V). Fig.2 shows the modified V–I converter circuit. In this circuit, there are only two elements in the series, resistor R and transistor M3. Due to virtual short of op-amp, Vbg will appear across R. Therefore the minimum supply voltage required to operate this circuit will be Vbg + Vds (M3).

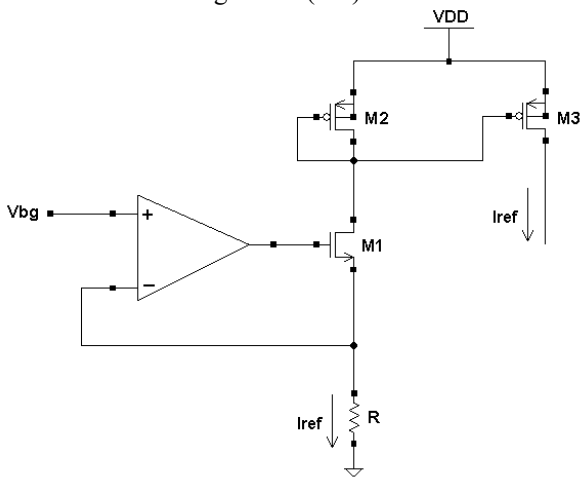

Figure 1. A conventional V-I converter

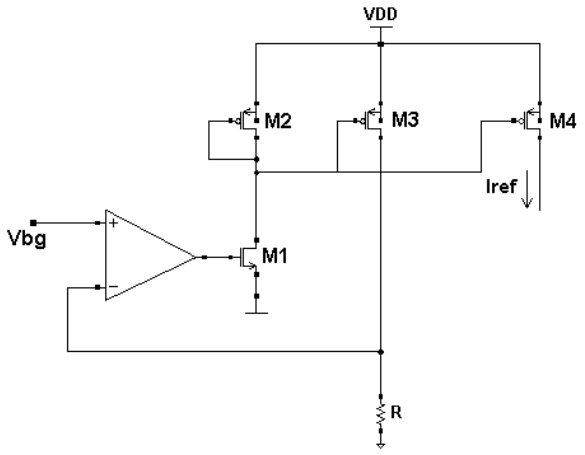

Figure2. A Low Voltage V-I converter

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The reference voltage has been generated by a low voltage band-gap circuit shown in fig.3.

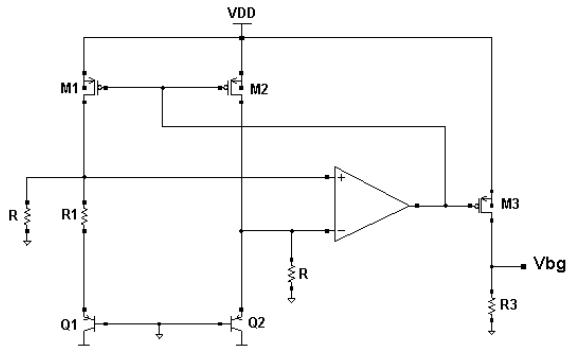

Figure 3. A Low Voltage Band-gap Reference Circuit

The band-gap voltage generated by conventional band-gap [1-2] circuits comes at about 1.2V thus they cannot be used in low voltage current reference. The band-gap circuit proposed in [3] can generate reference voltage less than 1.2V. The expression for band-gap voltage is given by

$$V_{bg} = I.R_3 = \frac{R_3}{R} V_{be2} + \frac{R_3}{R_1} V_T \ln(m) \qquad .....(1)$$

As is clear from eq. (1), the output voltage depends upon the ratio of resistors R3 and R and can be scaled down for low voltage operation.

Fig.4 shows the schematic of the proposed current reference circuit. CLK1 and CLK2 are two non-overlapping clocks that are generated using the circuit shown in Fig.5 to drive the switches M7, M10 and M8, M9 respectively in the SC resistors. Ca and Cb are two equal value capacitors used to construct the SC resistors. When CLK1 is high and CLK2 is low, capacitor Ca is charged to Vbg and capacitor Cb is discharged to VSS. Similarly, when CLK1 is low and CLK2 is high, Ca is discharged to VSS and Cb is charged to Vbg. Thus, a switching current flows in M5 whose average value is given by

$$I_{ref} = 2.V_{bg}.C_a.F_{ref} \qquad .....(2)$$

Where Fref is the clock frequency and total SC resistance is given *by 1/(2.Fref.Ca)*.

By taking two SC resistors in parallel, the switching current will flow in both clock cycles CLK1 and CLK2. Due to this, the frequency of the ripple generated will be twice the frequency of Fref. This ripple voltage can be filtered out more effectively by a low pass filter with lower values of R and C (higher 3dB cutoff) resulting in Iref with very low ripples. However, effective resistance of the two SC resistors in parallel will become half and therefore a factor of 2 comes in equation (2). A low pass filter composed of capacitor C3 and resistor R5 has been inserted between the gates of transistors M5 and M11 that effectively reduces the ripple in Iref to very low value.

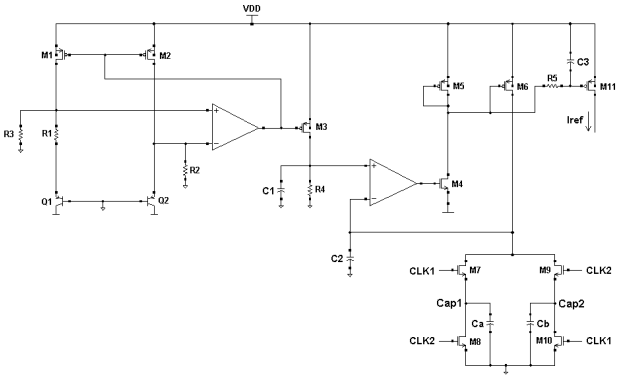

Figure 4. The proposed Low Voltage Constant Current Reference Circuit

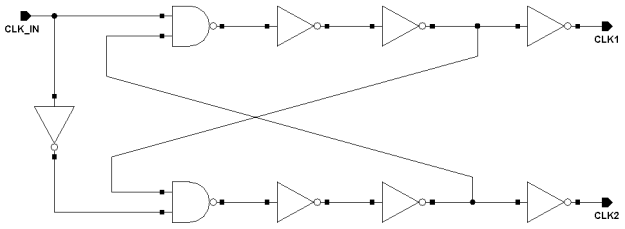

Figure 5. A non-overlapping clock generator

4. Simulation Results

Fig. 6-9 show the results of the proposed circuit simulated for various operating conditions. The circuit was designed for typical value of Vbg = 750mV, output current of 15uA with Ca = Cb = 1pF and Fref = 10MHz.

Fig. 6 shows the transient simulation result of the current reference circuit. The steady state current (Iref) is approx. 16uA. The difference between the expected and simulated results is due to the effect of parasitic capacitances that come in parallel to Ca and Cb. This increases the effective value of capacitance to be charged or discharged which decrease the effective SC resistor value. Due to this, the reference current increases.

Fig.7 shows the variation of output reference current (Iref) with temperature. Results show the maximum deviation of 0.6% from the typical value with –40 to 120 Deg.C temperature sweep.

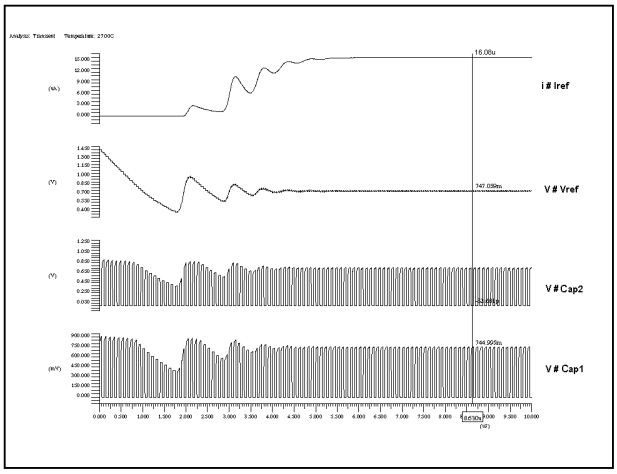

Figure 6. Waveforms showing transient response of the proposed circuit

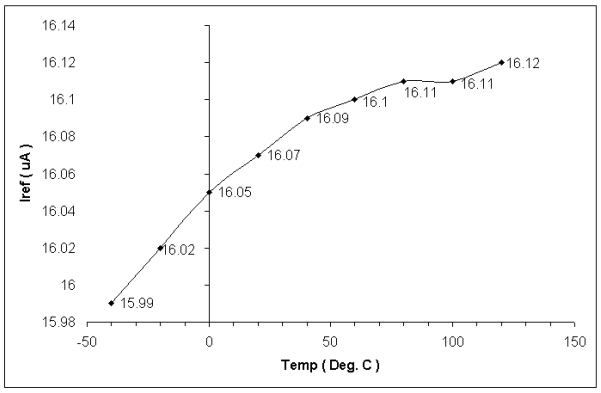

Figure 7. Simulation waveform showing variation of reference current (Iref) w.r.t. Temp.

Fig.8 shows the behavior of circuit with clock frequency and the output current is almost linear with the frequency sweep of 10MHz to 50MHz.

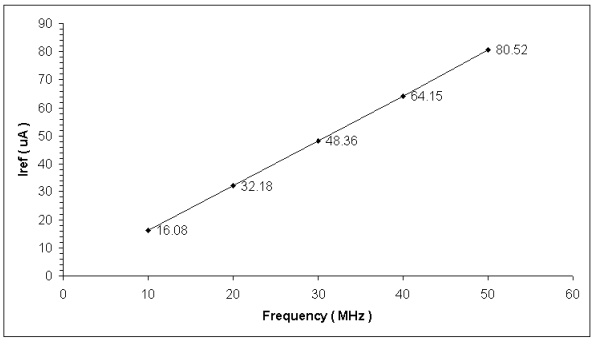

Figure 8. Simulation waveform showing variation of reference current (Iref) w.r.t. Freq

Fig.9 shows the variation of reference current with change in capacitors Ca and Cb values from 0.5pF to 5pF. It is seen from Fig.9 that there is some non-linearity in the variation of Iref with capacitances Ca and Cb, this is due the effect of parasitic capacitances coming in parallel with Ca and Cb. The total value of capacitance is the sum of the value of Ca and parasitic capacitance. The parasitic capacitance remains almost constant and does not scale up in the fashion as Ca and Cb are scaled up. Therefore, Iref does not increase linearly with increase in Ca and Cb. It is concluded from the waveform of Fig.9 that the reference current is approaching to its actual value as the capacitors Ca and Cb are increased. This is due to the lesser effect of parasitic capacitances at higher values of Ca and Cb.

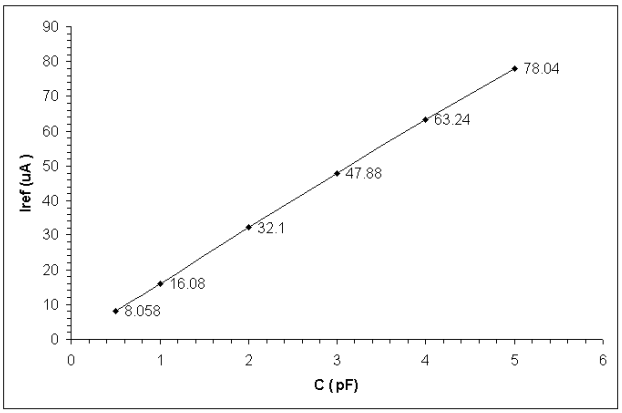

Figure 9. Simulation waveform showing variation of reference current (Iref) w.r.t. cap.

5. References

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