A Magnetic-Less DC–DC Converter for Dual-Voltage Automotive Systems

Fang Zheng Peng, *Senior Member, IEEE,* Fan Zhang, and Zhaoming Qian, *Senior Member, IEEE*

***Abstract*—The automotive industry is moving toward 42 V to meet more electrical needs. Several dual-voltage (42 and 14 V) architectures have been proposed for the transition and accommodation of 14-V loads. A dc–dc converter that connects the 42 and 14 V is one key device in any dual-voltage architecture. This paper presents a compact, efficient, magnetic-less bidirectional dc–dc converter for dual-voltage (42/14 V) automotive systems. The dc–dc converter is based on the generalized multilevel converter topology having the ability to balance battery voltages, emit zero or low electromagnetic interference, and have low cost by using low-voltage MOSFETs. The main circuit of the dc–dc converter is analyzed and its control scheme is presented in the paper. A self-powered gate drive circuit is developed for the dc–dc converter to reduce costs, signal connections, and circuit complexity. A prototype has been built and experimental results are presented.**

***Index Terms*—DC–DC converter, dual-voltage automotive system, multilevel converter, 42-V automotive system.**

I. Introduction

IN ORDER TO meet more electrical needs, the automotive industry is moving toward 42 V. Several dual-voltage (42 and 14 V) architectures have been considered for the transition and accommodation of 14-V loads. Figs. 1 and 2 show the two most popular architectures: dual- and single-battery 42/14-V systems. A dc–dc converter that connects the 42 and 14 V is indispensable in either dual-voltage architecture. An integrated starter generator (ISG), or integrated starter alternator (ISA) is used to generate 42 V.

Fig. 3 shows a traditional bidirectional dc–dc converter using relatively high-voltage and low-current MOSFETs, where each MOSFET has to sustain 42 V continuously. For this configuration, MOSFETs with a voltage rating of at least 150 V should be used considering load dump transients. For reference, a 14-V alternator's voltage can be as high as 50 V at load dump transients. Therefore, one may have to parallel several MOSFETs to reach current ratings required. Fig. 4 shows a traditional bidirectional dc–dc converter using relatively low-voltage and high-current MOSFETs, where each MOSFET has to sustain only 14 V continuous. In this case,

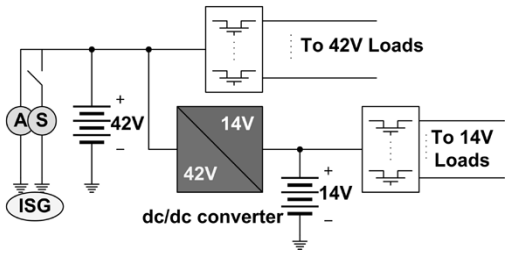

Fig. 1. Dual-battery 42/14-V system architecture.

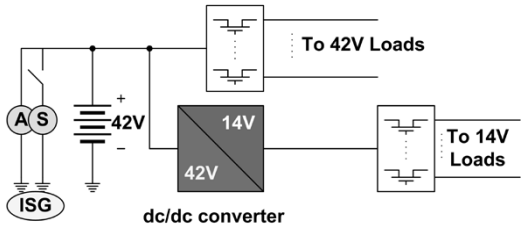

Fig. 2. Single-battery 42/14-V system architecture.

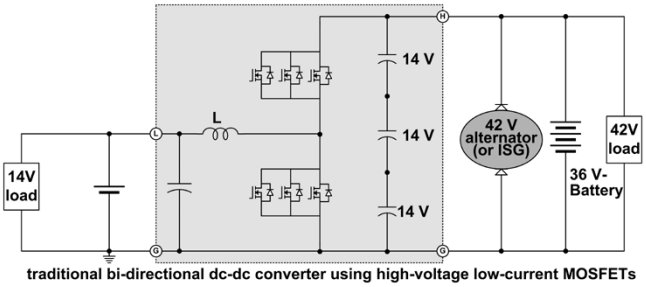

Fig. 3. Traditional bidirectional dc–dc converter using high-voltage low-current MOSFETs, where each MOSFET has to sustain 42 V.

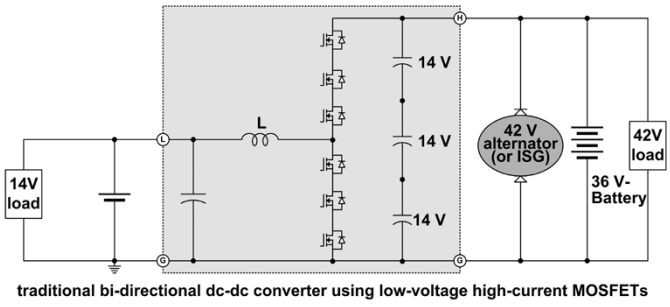

Fig. 4. Traditional bidirectional dc–dc converter using low-voltage high-current MOSFETs, where each MOSFET has to sustain only 14 V.

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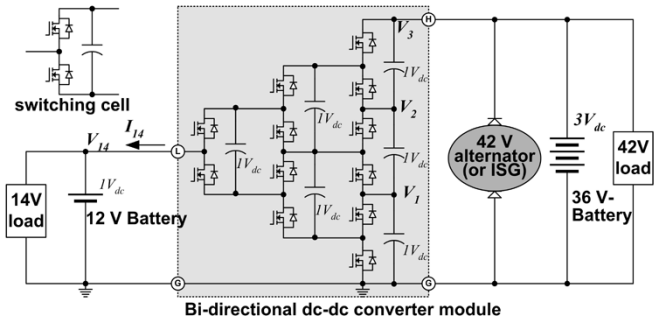


Fig. 5. Proposed four-level bidirectional dc–dc converter using low-voltage MOSFETs, where each MOSFET only sustains 14 V.

three low-voltage MOSFETs are put in series to reach the high voltage of 42 V. In either configuration, an *LC* filter is needed on the low voltage side. The inductor is the most lossy and bulkiest component in the converter. The magnetic component also has been the stumbling block to converters' circuit integration. In order to reduce the size and weight of the inductor, the MOSFET devices have to be switched at a very high frequency, typically tens to hundreds of kilohertz. However, this increases switching power loss and thermal management. Semiconductor heat dissipation also limits the switching frequency of the converter, and a low switching frequency results in increased size and weight of the magnetic components, further increasing converter size and weight. Therefore, it is sought to develop a simple cost-effective topology to reduce dc–dc converter size and weight and improve efficiency. This paper presents a novel dc–dc converter to achieve these goals.

II. Main Circuit and Operating Principle

Fig. 5 shows the proposed four-level bidirectional dc–dc converter using relatively low-voltage high-current MOSFETs, where each MOSFET only sustains 14 V. The converter is composed of six switching cells forming three switching poles. The converter does not use any magnetic components and operate at a fixed duty ratio and frequency with no pulsewidth modulation (PWM). The four-level dc–dc converter operates like a voltage multiplier. Each capacitor's voltage is kept close to 1 V_{dc}, which is one third of the high-side voltage. The converter has three switching states that generate an output voltage of 1 V_{dc} on the low-voltage side.

Figs. 6–8 show the three respective switching states, where the circled devices are gated on. These three redundant switching states keep all voltages balanced. In Fig. 6, capacitors C1, C3, and C6 are charge-equalized and connected to the 12-V battery (or 14-V loads), thus, we have $V_{14} = V_{C1} = V_{C3} = V_{C6}$ and $V_{C2} = V_{C5}$. Similarly, we have $V_{14} = V_{C3} = V_{C6}$ and $V_{C1} = V_{C2} = V_{C5}$ in Fig. 7 and $V_{14} = V_{C6}$, $V_{C1} = V_{C3} = V_{C5}$, and $V_{C2} = V_{C4}$ in Fig. 8. After one cycle of these three states, all capacitors and output voltage on the 12-V battery side are kept balanced and charged to the one-third of the 36-V battery. Any adjacent two switches of each switch pole are complementary to each other. Therefore, if any switch's state is determined or known then

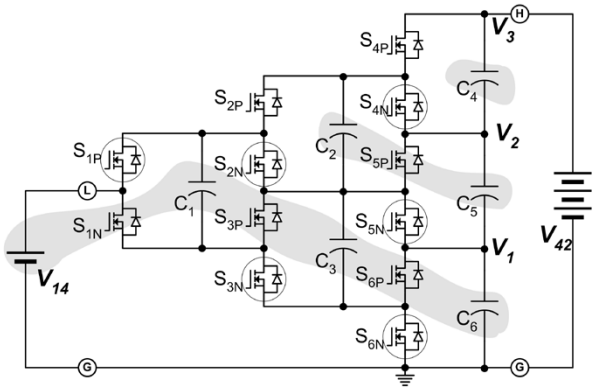


Fig. 6. Switching state I: $(S_{1P}, S_{2P}, S_{4P}) = (1, 0, 0)$ to produce 1 V_{dc}.

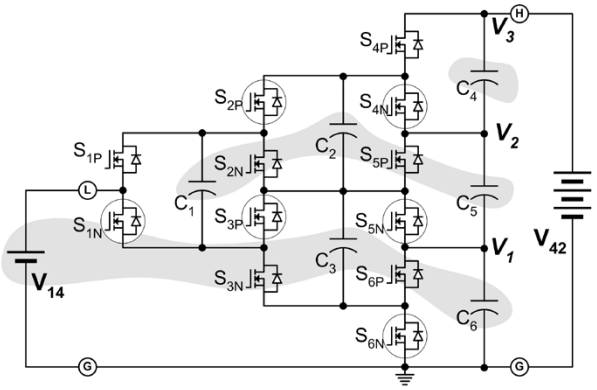


Fig. 7. Switching state II: $(S_{1P}, S_{2P}, S_{4P}) = (0, 1, 0)$ to produce 1 V_{dc}.

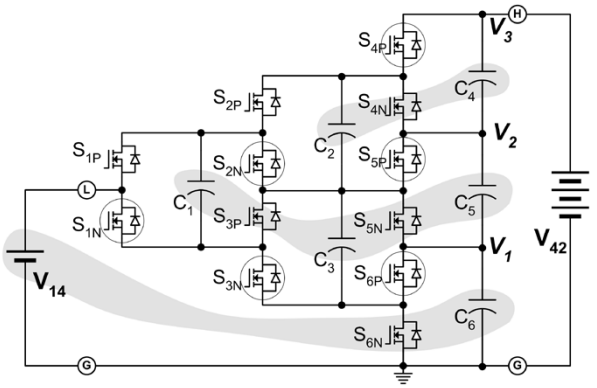


Fig. 8. Switching state III: $(S_{1P}, S_{2P}, S_{4P}) = (0, 0, 1)$ to produce 1 V_{dc}.

the rest switches of the pole are automatically determined. In Fig. 6–8, only the top switch of each pole (S_{1P}, S_{2P}, S_{4P}) is used to describe switching states. Fig. 9 shows the gating sequence.

The dc–dc converter behaves like an ideal voltage multiplier or voltage divider interfacing the 14-V and 42-V buses as shown in Fig. 10. That is, the bidirectional converter module steps down the 36-V battery (or 42-V load) into an equivalent 12-V battery (or 14-V load) when viewed from the low-voltage side

$$V_{14} = \frac{1}{3} V_{42} \tag{1}$$

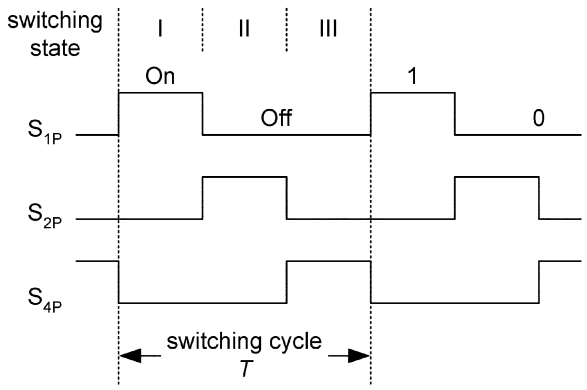


Fig. 9. Switching sequence of the converter.

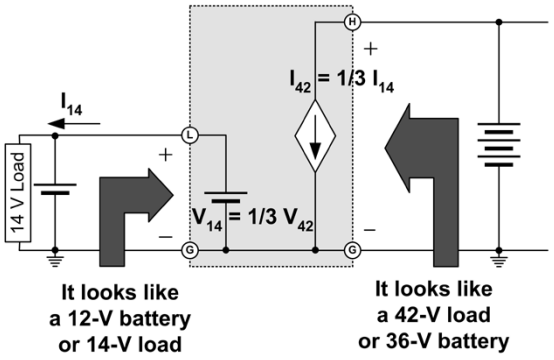


Fig. 10. Equivalent circuits as seen from either side.

and steps up the 14-V load (or 12-V battery) into an equivalent 42-V load (or 36-V battery) when viewed from the high-voltage side

$$V_{42} = 3V_{14}. \tag{2}$$

In other words, for a single 36-V battery system, the converter behaves like a 12-V battery to the 14-V load or a 42-V load to the 36-V battery. Equations (1) and (2) indicate that the voltage ratio of the low- and high-voltage sides is locked to a factor of 3. This integer multiplication/division relationship between the 14- and 42-V sides is desirable in most cases because the battery status is passed onto the other side and it is consistent with the traditional 14-V load requirements.

For noninteger multiplication/division or independent voltage regulation, switching frequency control or a PWM operation with minimal inductor can be used.

III. Self-Powered Gate Drive and Control Circuit

As described above, the four-level dc–dc converter has six switching cells. Each cell only sustains 14 V, which makes it easy to implement a simple gate drive and control circuit. The dc–dc converter developed is a self-contained module, where each switching cell is driven by a self-powered gate drive circuit. An oscillator circuit is used to generate gate sequence signals. Fig. 11 shows a brief sketch of the circuit, where a high- and low-side gate driver based on charge pump is used to drive each switching cell. The oscillator circuit is based on the converter

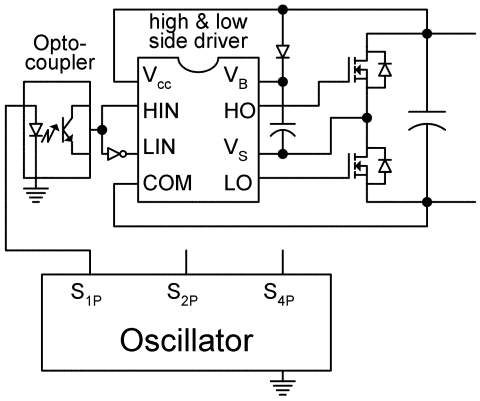


Fig. 11. Self-powered gate drive and control.

ground and each cell is level-shifted or opto-isolated through an optocoupler. The power is directly from each cell's dc capacitor voltage, which is 14 V. The circuit is designed operable for a voltage range of 8–16 V covering the traditional 12-V battery operating range. This self-powered gate drive reduces circuit complexity and cost tremendously. For the subject power (1 kW) and voltage (42 V) levels, gate drive circuits (about U.S. \$2∼\$3 per switching cell) and their power supply with isolation (U.S. \$3–\$6 per switching cell) cost much more than the main MOSFET device itself (about U.S. \$2∼\$3 per 30 V/2.8 mΩ MOSFET). This four-level dc–dc converter structure makes the self-powered gate drive possible and, thus, reduces cost greatly.

IV. Analysis of Power Loss and Efficiency

The traditional dc–dc converter's power loss can be divided into four major parts: switching loss, conduction loss, gate drive loss, and magnetic component (or inductor) loss. Since the new converter has no magnetic parts, magnetic component loss does not exist. Switching and gate drive losses are very small, compared with those of the traditional converter because the switching frequency (1–10 kHz) used is one to two orders lower. However, capacitor loss exists in the new converter. As discussed above, the capacitors' charge/voltage is balanced through rotating the three redundant switching states and connecting capacitors to parallel. Therefore, energy loss occurs at each switching-over instant when different capacitors with different voltages are connected together in parallel for charge balancing. This capacitor loss is analyzed in the Appendix. The total capacitor loss and voltages in the worst case are expressed as follows:

$$P_{\mathrm{Cap-loss}} = 0.218\frac{I_L^2}{C \cdot f} \tag{3}$$

$$V_{C4} = V_3 - V_2 = V_0 + 0.147\Delta \tag{4}$$

$$V_{C5} = V_2 - V_1 = V_0 + 0.076\Delta \tag{5}$$

$$V_{14} = V_{C6} = V_1 = V_0 - 0.223\Delta \tag{6}$$

$$\Delta = \frac{I_L}{C \cdot f} \tag{7}$$

where I_L is the load current, C is the capacitance, f is the switching frequency, and $V_0 = V_{42}/3$. The power loss and voltage unbalance Δ are inversely proportional to the capacitance and switching frequency. By increasing capacitance and

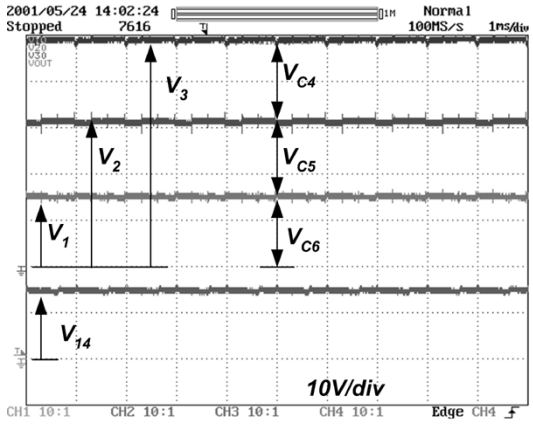


Fig. 12. Voltage waveforms ($V_{\rm batt} = \sim 110\%$ and $f_{\rm sw} = 1$ kHz). $V_{C4} = 17$ V, $V_{C5} = 15.45$ V, and $V_{C6} = 14.5$ V.

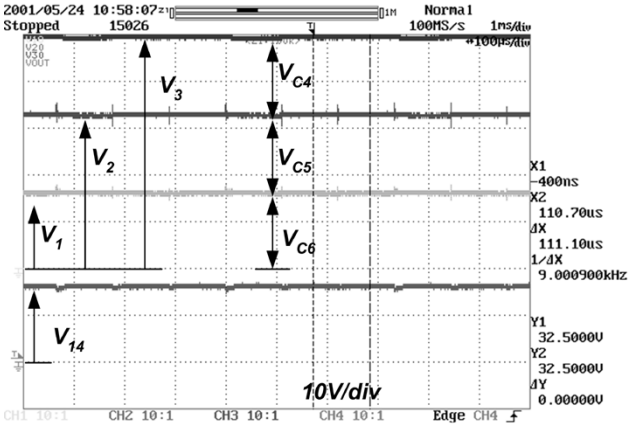


Fig. 13. Voltage waveforms ($V_{\rm batt} = \sim 110\%$ and $f_{\rm sw} = 3$ kHz). $V_{C4} = 16$ V, $V_{C5} = 15.7$ V, and $V_{C6} = 15.45$ V.

switching frequency, efficiency and voltage balance can be improved. For example, considering that the load current $I_L = 50$ A, the capacitance $C = 4700\ \mu$F, switching frequency $f = 10$ kHz, and the input voltage $V_{42} = 42$ V, we have

$$P_{\rm Cap-loss} = 0.218\frac{I_L^2}{C \cdot f} = 11.596\ {\rm W},$$

which is about 1.66% of the output power, $(14\ {\rm V}) \cdot (50\ {\rm A}) = 700$ W, and the capacitor voltages are

$$\Delta = \frac{I_L}{C \cdot f} = 1.064\ {\rm V},$$
$$V_{C4} = V_3 - V_2 = V_0 + 0.147\Delta = 14.156\ {\rm V},$$
$$V_{C5} = V_2 - V_1 = V_0 + 0.076\Delta = 14.081{\rm V}$$
$$V_{C6} = V_1 = V_0 - 0.223\Delta = 13.763\ {\rm V}.$$

As can be seen from the above calculation, with enough capacitance and switching frequency, the capacitor loss and voltage unbalance are relatively small even in the worst case. In real applications, the capacitor loss and voltage unbalance will be smaller for single battery systems because of larger output capacitance and even much smaller for dual battery systems. The detailed analysis is given in Appendix.

In addition, it should be noted that independent voltage control /regulation can be implemented by controlling switching

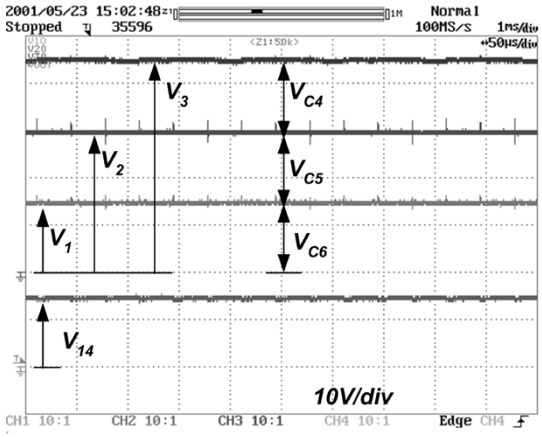


Fig. 14. Voltage waveforms ($V_{\rm batt} = \sim 100\%$ and $f_{\rm sw} = 10$ kHz). $V_{C4} = 14.8$ V, $V_{C5} = 14.5$ V, and $V_{C6} = 14.3$ V.

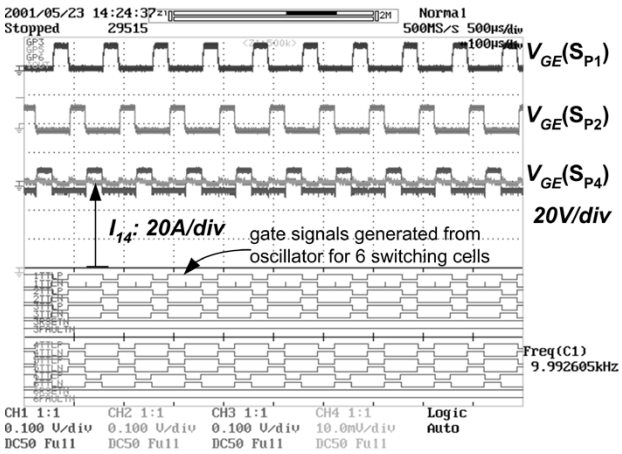


Fig. 15. Gate voltage and signals ($V_{\rm batt} = 48\%$ and $f_{\rm sw} = 10$ kHz).

frequency, because the output voltage V_{14} is related to the switching frequency as indicated in (6).

V. Experimental Results

Figs. 12–16 show experimental results with capacitance $C = 4,700\ \mu$F and power flow from the 42-V to 14-V side. Figs. 12–14 show voltage waveforms at three different switching frequencies: 1, 3, and 10 kHz. With 1-kHz switching, Fig. 12 shows that the voltage unbalance is appreciable: $V_{C6} < V_{C5} < V_{C4}$, which is consistant with the analytical conclusions expressed in (4)–(6). While increasing the switching frequency to 10 kHz, the voltage unbalance becomes insignificant. Fig. 15 shows gate voltages and signals that were generated by the self-powered gate drive and control circuit. Fig. 16 shows high efficiency over a wide load range at full (100%) battery voltage. The efficiency was measured by a Yokogawa power meter with power flow from the high voltage to low voltage at difference battery voltage levels. Since both the input and output voltage and current are dc, the measurement error should be less than 0.3% according to the power meter specifications. The experimental results clearly demonstrated voltage balance, voltage ripple reduction,

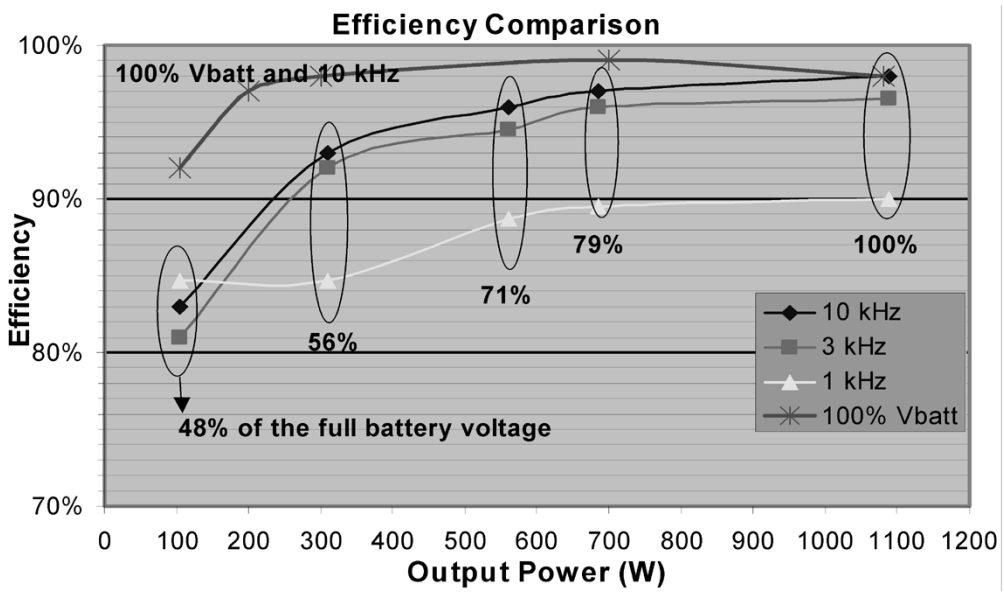


Fig. 16. Measured efficiency. A 12-V battery is considered fully charged at 14.2 V (or 100%) and empty at 8 V (56%), while a 36-V battery is full at 42.6 V (or 100%) and empty at 24 V (or 56%). The operating range is 8∼16 V for 14-V loads and 24∼48 V for 42-V loads. The efficiency measurement was performed further down to 7 V (∼48%) and 21 (∼48%) V for 14- and 42-V loads, respectively.

and efficiency improvement when the switching frequency is increased, which is consistant with the analysis.

VI. Conclusions

This paper has presented a compact, efficient, magnetic-less bidirectional dc–dc converter for dual voltage (42/14 V) automotive systems. The dc–dc converter is based on the generalized multilevel converter topology having ability to balance battery voltages, emit zero or low electromagnetic interference (EMI), and have low cost by using low-voltage MOSFETs.

The multilevel configuration makes it possible to utilize low voltage MOSFETs, which have extremely low on-resistance and are low cost because of large production volume for switching power supplies used in communication and computer industries. A self-powered gate drive and control circuit has been developed. Advantages of the dc–dc converter include: 1) no magnetic components; 2) compact size and light weight; 3) easy manufacturing (possible to build a whole converter system on package, or IC power module); 4) high efficiency (>98%); and 5) low EMI emission. A prototype using six cell modules was built and tested. Experimental results demonstrated that the new dc–dc converter has high efficiency, good voltage regulation, and low EMI.

In addition, it has been analyzed that independent voltage control/regulation can be implemented by changing switching frequency. This technique can be used when the fixed input–output relation (i.e., the output voltage is always 1/3 of the input voltage) is not desirable (e.g., one battery is overdrained or overcharged) and voltage regulation is needed.

Appendix

Analysis of Capacitor Loss and Voltage Unbalance

According to the control scheme used, the capacitors' charge /or voltage is balanced through rotating the three redundant switching states every $T/3$ as shown in Fig. 9 and connecting capacitors to parallel. Power loss occurs when capacitors with different voltage are connected together to parallel. To determine the power loss and voltage unbalance of the capacitors, we need to consider each of the three redundant states and their transitions.

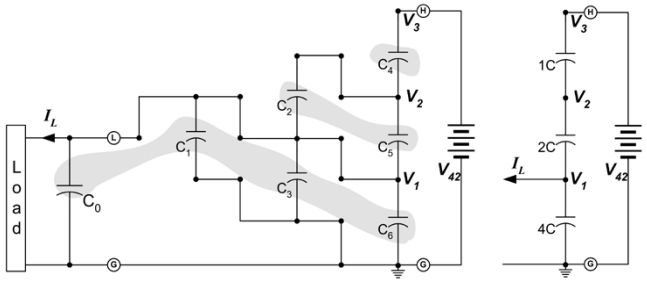


Fig. 17. Equivalent circuit of Fig. 6 (i.e., State I).

A. Switching State I: Fig. 6, $(\mathbf{S_{1P}}, \mathbf{S_{2P}}, \mathbf{S_{4P}}) = (\mathbf{1}, \mathbf{0}, \mathbf{0})$

At the beginning of State I, assume that

$$V_{C4} = V_3 - V_2 = V_0 + \Delta_3 \tag{8}$$

$$V_{C2} = V_{C5} = V_2 - V_1 = V_0 + \Delta_2 \tag{9}$$

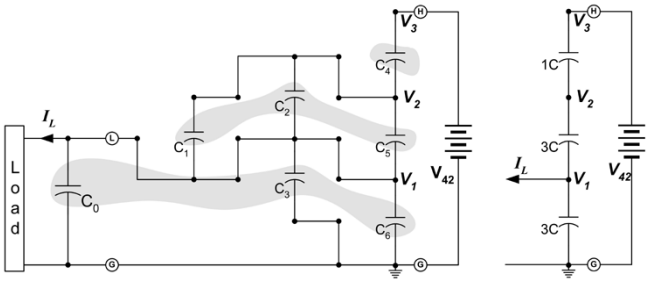
$$V_{C0} = V_{C1} = V_{C3} = V_{C6} = V_1 = V_0 + \Delta_1 \tag{10}$$

where

$$V_0 = \frac{1}{3} V_{42} \tag{11}$$

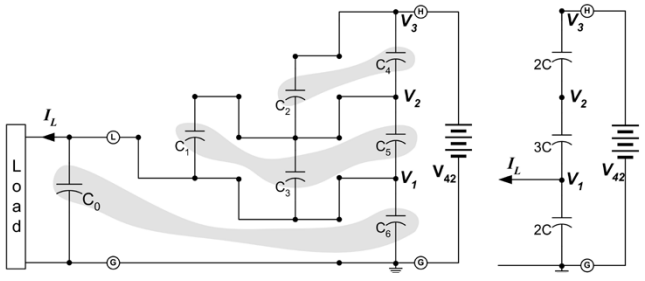
$$\Delta_1 + \Delta_2 + \Delta_3 = 0. \tag{12}$$

The equivalent circuit of State I is shown in Fig. 17(a), which can be further reduced to Fig. 17(b). Note that the on-resistance of MOSFETs has no effect on the capacitor balancing and power loss rather than the initial charge /discharge current [1], thus using short circuit to represent conducting MOSFETs in Fig. 17. For simplicity, assume all capacitors including the output capacitor C_0 in the converter have the same capacitance C. This is the



(a) (b)

Fig. 18. Equivalent circuit of Fig. 7 (i.e., State II).



(a) (b)

Fig. 19. Equivalent circuit of Fig. 8 (i.e., State III).

worst case for power loss and voltage unbalance of the converter. For a dual-battery system, C_0 is the 12-V battery that has equivalently large capacitance. For a single-battery system, 14-V loads normally have input capacitors that augment the total output capacitance C_0. The load current I_L charges the upper capacitors and discharges the lower capacitors as shown in Fig. 17(b). This state lasts $T/3$ as shown in Fig. 9. At the end of State I (after $T/3$), the voltages become

$$V_{C4} = V_3 - V_2 = V_0 + \Delta_3 + \frac{1}{21}\Delta \tag{13}$$

$$V_{C2} = V_{C5} = V_2 - V_1 = V_0 + \Delta_2 + \frac{1}{42}\Delta \tag{14}$$

$$V_{C0} = V_{C1} = V_{C3} = V_{C6} = V_1 = V_0 + \Delta_1 - \frac{1}{14}\Delta \tag{15}$$

where

$$\Delta = \frac{I_L \cdot T}{C}. \tag{16}$$

B. At the Transition From State I to State II

Now consider the transition from State I to State II. Fig. 18 shows the equivalent circuits of State II (Fig. 7).

Before State II (i.e., at the end of State I), the capacitors' voltages are expressed in (13)–(15), which are the initial values before the switching over transition. After switching over to State II, the capacitors settle down to the following voltages, which can be calculated from (13)–(15) and Fig. 18:

$$\begin{aligned} V_{C4} &= V_3 - V_2 \\ &= V_0 - \frac{1}{5}\Delta_1 + \frac{1}{5}\Delta_2 + \Delta_3 + \frac{1}{15}\Delta \end{aligned} \tag{17}$$

$$\begin{aligned} V_{C1} &= V_{C2} = V_{C5} = V_2 - V_1 \\ &= V_0 + \frac{4}{15}\Delta_1 + \frac{11}{15}\Delta_2 + \frac{1}{630}\Delta \end{aligned} \tag{18}$$

$$\begin{aligned} V_{C0} &= V_{C3} = V_{C6} = V_1 \\ &= V_0 + \frac{14}{15}\Delta_1 + \frac{1}{15}\Delta_2 - \frac{41}{630}\Delta. \end{aligned} \tag{19}$$

C. At the End of State II

At the beginning of State II, the voltages are expressed in (17)–(19). Using the similar analysis described in State I, the voltages at the end of State II become

$$\begin{aligned} V_{C4} &= V_3 - V_2 \\ &= V_0 - 0.2\Delta_1 + 0.2\Delta_2 + \Delta_3 + 0.1333\Delta \end{aligned} \tag{20}$$

$$\begin{aligned} V_{C1} &= V_{C2} = V_{C5} = V_2 - V_1 \\ &= V_0 + 0.2666\Delta_1 + 0.7333\Delta_2 + 0.0206\Delta \end{aligned} \tag{21}$$

$$\begin{aligned} V_{C0} &= V_{C3} = V_{C6} = V_1 \\ &= V_0 + 0.9333\Delta_1 + 0.0667\Delta_2 - 0.1539\Delta. \end{aligned} \tag{22}$$

D. At the Transition From State II to State III

Now consider the transition from State II to State III. Fig. 19 shows the equivalent circuits of State III (Fig. 8). Before State III (i.e., at the end of State II), the capacitors' voltages are expressed in (20)–(22), which are the initial values before this switching over transition. After switching over to State III, the capacitors settle down to the following new voltages:

$$\begin{aligned} V_{C2} &= V_{C4} = V_3 - V_2 \\ &= V_0 - 0.1376\Delta_1 + 0.45\Delta_2 + 0.6875\Delta_3 + 0.12\Delta \end{aligned} \tag{23}$$

$$\begin{aligned} V_{C1} &= V_{C3} = V_{C5} = V_2 - V_1 \\ &= V_0 + 0.3751\Delta_1 + 0.5\Delta_2 + 0.125\Delta_3 - 0.009\Delta \end{aligned} \tag{24}$$

$$\begin{aligned} V_{C0} &= V_{C6} = V_1 \\ &= V_0 + 0.7624\Delta_1 + 0.05\Delta_2 + 0.1875\Delta_3 - 0.111\Delta. \end{aligned} \tag{25}$$

E. At the End of State III

At the beginning of State III, the voltages are expressed in (23)–(25). Similarly, after $T/3$ at the end of State III the voltages become

$$\begin{aligned} V_{C2} &= V_{C4} = V_3 - V_2 \\ &= V_0 - 0.1376\Delta_1 + 0.45\Delta_2 + 0.6875\Delta_3 + 0.1825\Delta \end{aligned} \tag{26}$$

$$\begin{aligned} V_{C1} &= V_{C3} = V_{C5} = V_2 - V_1 \\ &= V_0 + 0.3751\Delta_1 + 0.5\Delta_2 + 0.125\Delta_3 - 0.0327\Delta \end{aligned} \tag{27}$$

$$\begin{aligned} V_{C0} &= V_{C6} = V_1 \\ &= V_0 + 0.7624\Delta_1 + 0.05\Delta_2 + 0.1875\Delta_3 - 0.2152\Delta. \end{aligned} \tag{28}$$

F. At the Transition From State III to State I

Now consider the transition from State III back to State I. The equivalent circuits of State I have been shown in Fig. 17. Before State I (i.e., at the end of State III), the capacitors' voltages are expressed in (26)–(28), which are the initial values before the switching over transition. After switching over to State I, the capacitors settle down to new voltages as follows:

$$\begin{aligned} V_{C4} &= V_3 - V_2 \\ &= V_0 - 0.12\Delta_1 + 0.3357\Delta_2 + 0.5446\Delta_3 \\ &\quad + 0.0682\Delta \end{aligned} \tag{29}$$

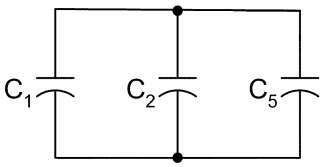


Fig. 20. Parallel connection resulting from State I to II switchover.

$$V_{C0} = V_{C2} = V_{C5} = V_2 - V_1 = V_0 + 0.2474\Delta_1 + 0.4178\Delta_2 + 0.3348\Delta_3 + 0.05\Delta \quad (30)$$

$$V_{C0} = V_{C1} = V_{C3} = V_{C6} = V_1 = V_0 + 0.6331\Delta_1 + 0.2464\Delta_2 + 0.120\,55\Delta_3 - 0.12\Delta. \quad (31)$$

G. Solution of the Voltages

After one cycle, the voltages come back to the beginning of State I. Therefore, (29)–(31) should equal (8)–(10), respectively. From (8)–(12) and (29)–(31), we get the following equations:

$$V_0 + \Delta_3 = V_0 + 0.12\Delta_1 + 0.3357\Delta_2 + 0.5446\Delta_3 + 0.0682\Delta \quad (32)$$

$$V_0 + \Delta_2 = V_0 + 0.2474\Delta_1 + 0.4178\Delta_2 + 0.3348\Delta_3 + 0.05\Delta \quad (33)$$

$$\Delta_1 + \Delta_2 + \Delta_3 = 0. \quad (34)$$

Solving the above three equations, we have

$$\Delta_1 = -0.223\Delta, \quad (35)$$

$$\Delta_2 = 0.076\Delta \quad (36)$$

$$\Delta_3 = 0.147\Delta. \quad (37)$$

Therefore, the voltages are

$$V_3 - V_2 = V_0 + 0.147\Delta, \quad (38)$$

$$V_2 - V_1 = V_0 + 0.076\Delta, \quad (39)$$

$$V_1 = V_0 - 0.223\Delta. \quad (40)$$

H. Power Loss Calculation

When connecting together capacitors with different voltages power loss always occurs. There are the following five instances per switching cycle.

1) C1–C2–C5 Connection From State I to State II (Fig. 20): Before the switching-over transition of State I to State II, capacitors C1, C2, and C5's voltages are expressed in (14) and (15). After the switching over, they settle down to a new voltage and become (18). In this case, C1 has a different voltage from C2 and C5 before the connection. The energy loss at this connection is $(1/3)C{\delta_i}^2$, where δ_i is the voltage difference between the two initial voltages. The voltage difference between (14) and (15) is

$$\delta_i = 0.394\Delta. \quad (41)$$

Therefore, the energy loss at this switching-over transition is

$$E_i = \frac{1}{3}C\delta_i^2 = 0.052C\Delta^2. \quad (42)$$

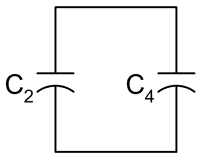


Fig. 21. Parallel connection resulting from State II to III switchover.

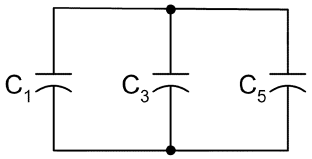


Fig. 22. Another parallel connection resulting from State II to III switchover.

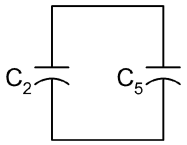


Fig. 23. Parallel connection resulting from State III to I switchover.

2) C2–C4 Connection From State II to State III (Fig. 21): Before this switching-over transition, capacitors C2 and C4's voltages are expressed in (20) and (21). After the switching over, they become (23). The energy loss in this case—two capacitors with two different voltages connected together is $(1/4)C{\delta_{ii}}^2$, where δ_{ii} is the voltage difference between the two initial voltages. The voltage difference between (20) and (21) is

$$\delta_{ii} = 0.3233\Delta. \quad (43)$$

Therefore, the energy loss is

$$E_{ii} = \frac{1}{4}C\delta_{ii}^2 = 0.026C\Delta^2. \quad (44)$$

3) C1–C3–C5 Connection From State II to State III (Fig. 22): Before the switching-over transition, capacitors C1, C3, and C5's voltages are expressed in (21) and (22). After the switching over, their voltages become (24). Similarly, the voltage difference between (21) and (22) is

$$\delta_{iii} = 0.3734\Delta. \quad (45)$$

Therefore, the energy loss is

$$E_{iii} = \frac{1}{3}C\delta_{iii}^2 = 0.047C\Delta^2. \quad (46)$$

4) C2–C5 Connection From State III to State I (Fig. 23): Before the switching-over transition, capacitors C2 and C5's voltages are expressed in (26) and (27). After the switching over, they become (30). The voltage difference between (26) and (27) is

$$\delta_{iv} = 0.343\Delta. \quad (47)$$

Therefore, the energy loss is

$$E_{iv} = \frac{1}{4}C\delta_{iv}^2 = 0.029C\Delta^2. \quad (48)$$

5) C0–C1–C3–C6 Connection From State III to State I (Fig. 24): Before the switching-over transition, capacitors C0, C1, C3, and C6's voltages are expressed in (27) and (28). After

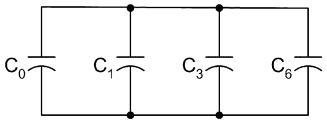


Fig. 24. Another parallel connection resulting from State III to I switchover.

the switching over, they become (31). The voltage difference between (27) and (28) is

$$\delta_v = 0.359\Delta. \tag{49}$$

Therefore, the energy loss is

$$E_v = \frac{1}{2}C\delta_v^2 = 0.064C\Delta^2. \tag{50}$$

The total loss over one cycle is

$$E = \sum_{j=i}^{v} E_j = 0.218C\Delta^2 \tag{51}$$

and the power loss for a switching frequency of f is

$$P_{\text{Cap-loss}} = E \cdot f = 0.218\frac{I_L^2}{C \cdot f}. \tag{52}$$

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