A Majority-Logic Device Using an Irreversible Single-Electron Box

Takahide Oya, Tetsuya Asai, Takashi Fukui, and Yoshihito Amemiya

***Abstract*—We describe a majority-logic gate device suitable for use in developing single-electron integrated circuits. The device consists of a capacitor array for input summation and an irreversible single-electron box for threshold operation. It accepts three binary inputs and produces a corresponding output, a complementary majority-logic output, by using the change in its tunneling threshold caused by the input signals; it produces a logical 1 output if two or three of the inputs are logical 0 and a logical 0 output if two or three of the inputs are logical 1. We combined several of these gate devices to form subsystems, a shift register and a full adder, and confirmed their operation by computer simulation. The gate device is simple in structure and powerful in terms of implementing digital functions with a small number of devices. These superior features will enable the device to contribute to the development of single-electron integrated circuits.**

***Index Terms*—Adder, circuit, gate, majority logic, single electron.**

I. Introduction

A PROMISING area of research in nanoelectronics is the development of integrated circuits on the basis of single-electron circuit technology. For this purpose, we propose a functional single-electron logic device that has a simple and concise structure. The device is a majority-logic gate consisting of an irreversible single-electron box with a double or multiple tunneling junction.

The single-electron circuit is an electronic circuit designed to manipulate electronic functions by controlling the transport of individual electrons (for a detailed explanation, see Gravert and Devoret [1]). It has been receiving increasing attention because it can be used to produce large-scale ICs (LSIs) that combine huge scales of integration with ultralow levels of power dissipation. To move closer to this goal, we must develop digital devices that can perform complex and large-scale logic operations efficiently through the use of single electrons. In this paper, we propose one such device—a single-electron logic gate based on the concept of majority logic—and demonstrate its operation by computer simulation.

Majority logic is a way of implementing digital operations in a manner different from that of Boolean logic. Instead of using Boolean logic operators (AND, OR, and their complements), majority logic represents and manipulates digital functions on the basis of *majority decision*. The logic process of majority logic is much more sophisticated than that of Boolean logic; consequently, majority logic is more powerful for implementing a given digital function with a smaller number of logic gates (Amarel *et al.* [2] and Meo [3] have given details).

The prospects for the practical application of majority logic wholly depend on the feasibility of a logic device suitable for majority logic. In the late 1950s, several computer systems based on a majority-logic architecture were developed and constructed for practical use by using a nonlinear-reactance device called the *parametron*, a majority logic device that makes use of the phenomenon of parametric phase-locked oscillation. After these developments, however, majority logic had to leave the stage because the transistor gate circuit—a Boolean logic device by nature—came to be the dominant device in digital electronics. However, majority logic can be expected to make a comeback with the development of nanotechnology and quantum devices. This is so because quantum devices fabricated using nanotechnology provide functional properties that can be well used for implementing majority-logic operations. The leading examples are the quantum-flux parametron, which is composed of Josephson junction circuits [4], the quantum cellular automaton consisting of quantum dot arrays [5] and, in the area of single-electron circuits, the majority-logic gate based on Tucker's single-electron inverter [6].

To develop a single-electron majority logic device that is simpler and more suitable for LSI applications, we previously developed [7] a majority-logic gate consisting of a balanced pair of single-electron boxes. In this paper, we propose a more simplified majority-logic gate device. It has a very concise structure with only one single-electron box.

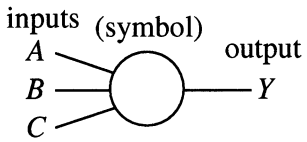
The first of the following sections (Section II) is an outline of the unit function required for majority logic. The next section (Section III) describes a logic-gate device that implements this unit function. The device consists of a simple single-electron circuit, i.e., an irreversible single-electron box with a double or multiple tunneling junction. Its majority-logic operation uses the change in the tunneling threshold caused by the input signals. Section IV describes the design of two sample subsystems, a shift register, and a full adder that combine several gate devices. The simulated operation of these subsystems is also described. Section V estimates the effects of undesirable factors that produce errors in the gate operation. Section VI concludes with the design for actual gate devices and the schematics for fabrication.

Manuscript received June 15, 2002; revised September 18, 2002. This paper is based on a presentation at the IEEE Silicon Nanoelectronics Workshop of 2002.

T. Oya, T. Asai, and Y. Amemiya are with the Department of Electrical Engineering, Hokkaido University, Sapporo 060-8628, Japan (e-mail: ooya@sapiens-ei.eng.hokudai.ac.jp).

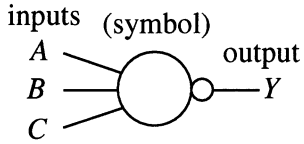
T. Fukui is with the Research Center for Integrated Quantum Electronics, Hokkaido University, Sapporo 060-8628, Japan.

Digital Object Identifier 10.1109/TNANO.2003.808507



inputs A	B	C	output Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(a)



inputs A	B	C	output Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(b)

Fig. 1. Three-input majority gates. (a) Majority-logic gate. (b) Complementary majority-logic gate.

II. Unit Function of Majority Logic

The unit function of majority logic is to determine the output state by means of the majority vote of input states. The logic element, a majority gate, has an odd number of binary inputs and a binary output. It produces an output of one if the majority of the inputs is one, and produces an output of zero if the majority is zero. The function of a three-input gate is shown in Fig. 1(a) together with the logic symbol of the gate. When, for instance, the three inputs are 0, 1, and 1, the output is 1 (fourth row in the table); when the inputs are 1, 0, and 0, the output is 0 (fifth row in the table). (For further details on majority logic, see [2] and [3].) Any digital function can be implemented using a combination of majority gates and inverters. A majority gate can have five or more inputs, but three-input gates suffice for the construction of any logic system.

Fig. 1(b) gives the *complement* of the three-input majority function. The gate device we will describe in the next section produces this complementary function [in contrast, our previous device in [7] produced the ordinary majority function of Fig. 1(a)]. Any digital function can be implemented using only the gates of the complementary majority function (using inverters jointly makes the logic system design more concise). In the following sections, we discuss only the complementary majority-function gate, so we call it simply a "majority gate." We use the logic symbol given in Fig. 1(b).

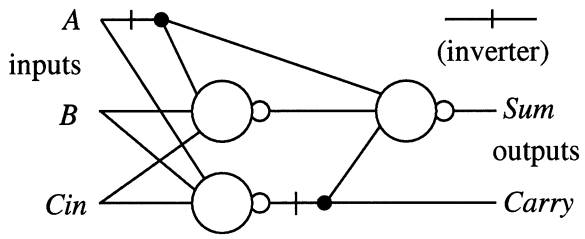


Fig. 2. Full adder consisting of majority gates.

Majority logic provides a concise implementation for most functions encountered in logic design applications. As an example, the implementation of a full adder is illustrated in Fig. 2 in which an inverter is represented by a segment on a connection branch (according to the conventional flow-diagram description of majority logic). A full adder is composed of only three gates with two inverters. In contrast, a Boolean-based implementation requires a larger circuit with seven or eight gate elements (about 25–30 MOSFETs).

III. Logic-Gate Device

A. Double-Junction Single-Electron Box

The main component of the majority gate device we are proposing is the irreversible single-electron box consisting of a double or multiple tunneling junction (the irreversible box is sometimes called a single-electron trap). An irreversible single-electron box with a double junction is illustrated in Fig. 3(a). It consists of two identical tunneling junctions Cj connected in series, a bias capacitor CL, and a bias voltage Vd. It has an island node 1 at which excess electrons are stored ("excess electrons" means electrons that are not canceled by the background positive ions in the node material). At the low temperatures at which the Coulomb-blockade effect occurs, the number n of excess electrons takes a value such that the electrostatic energy in the circuit (including the bias voltage source) is locally minimized. The value of n is 0 at $Vd = 0$ and it changes with Vd because of electron tunneling between node 1 and the ground through junctions Cj via intermediate node 2. In this circuit, as described in [1], n is a hysteretic staircase function of Vd, as shown in Fig. 3(b); n changes from 0 to 1 when Vd is increased above threshold $V2$ $[=e(1 + CL/Cj)/(2CL)$; e is the elementary charge] and returns from 1 to 0 when Vd is decreased below threshold $V1$ $[=e(1 - CL/Cj)/(2CL)]$. Owing to this discrete changes in n, the voltage at node 1 is a hysteretic sawtooth function of Vd, as shown in Fig. 3(c).

A similar hysteretic function can be obtained using a multijunction box—an irreversible single-electron box that has three or more tunneling junctions connected in series. A multijunction box can therefore also be used to construct the majority gate. In an N junction trap, the thresholds are given by $V2 = e(1+(N-1)CL/Cj)/(2CL)$ and $V1 = e(1-(N-1)CL/Cj)/(2CL)$.

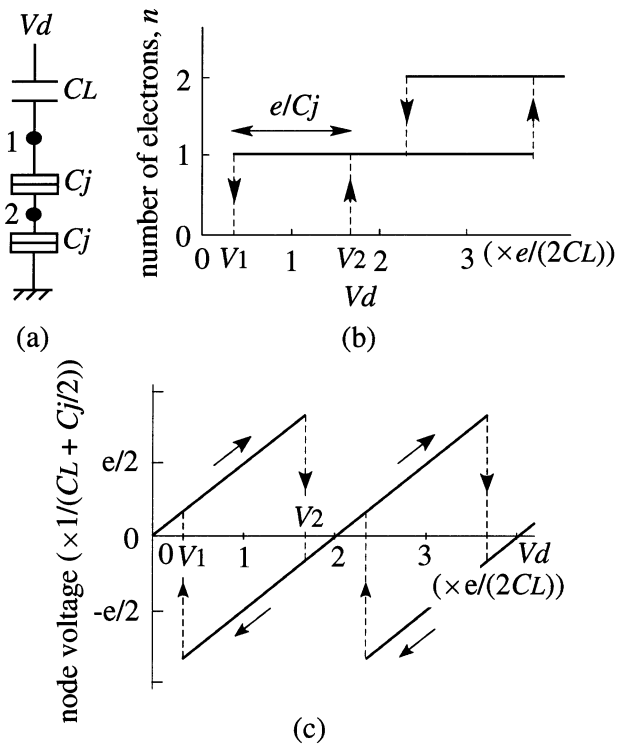


Fig. 3. Irreversible single-electron box. (a) Circuit configuration with a double tunneling junctions. (b) Static number n of excess electrons on node 1 as a function of bias voltage Vd. (c) Voltage at node 1 as a function of Vd.

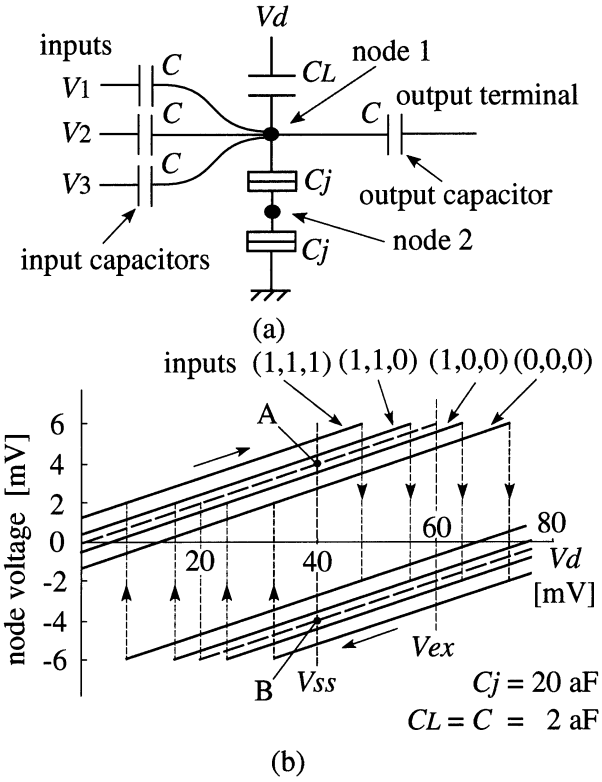


Fig. 4. Majority-gate device. Simulated (a) circuit configuration and (b) voltage at node 1 as a hysteretic function of Vd with four sets of inputs as parameters. The dashed lines show the node voltage at inputs $V1 = V2 = V3 = 0$ V.

B. Constructing a Majority-Gate Device

We used the double-junction box to construct the majority-gate device illustrated in Fig. 4(a); the figure shows a three-input configuration. The majority gate consists of a double-junction box (CL and two junctions Cj), three input capacitors C, and an output capacitor C (the input and output capacitors are set at equal capacitance). Three input voltages, $V1$, $V2$, and $V3$, are applied to node 1 through the input capacitors. The input capacitors form a voltage-summing network and produce the mean of their inputs on node 1. The double-junction box then produces the complementary majority-logic output on the same node, as illustrated later, and the output is sent to a succeeding gate through the output terminal. Binary logic values 1 and 0 are represented by a positive voltage and a negative voltage of equal amplitude.

The majority gate works as followings. We first ground the output terminal and apply the input voltages and then increase bias voltage Vd to an appropriate excitation value, Vex. The voltage at node 1 reaches a positive value determined by Vex and input voltages $V1$, $V2$, and $V3$. If the node voltage exceeds a threshold, an electron will tunnel from the ground to node 1 via intermediate node 2; consequently, the node voltage will turn negative. In contrast, if the node voltage does not reach the threshold, it will remain positive. We then retrieve the node voltage as an output. For successful majority-logic operation, we set excitation voltage Vex to $e(1+(CL+4C)/Cj)/(2CL)$, so that the electron tunneling will take place only if two or three inputs are a logical 1 (or only if the mean of three input voltages is positive). After exciting the gate, we decrease bias Vd to a holding voltage, $e/(2CL)$, ground the input terminals (or set $V1, V2$, and $V3$ to 0 V), and then observe the voltage at node 1, the output voltage. The output voltage (therefore, input voltage for a succeeding gate) is $-e/(2CL+8C+Cj)$, or logical 0, if two or three inputs are 1 (electron tunneling takes place), and it is $e/(2CL+8C+Cj)$, or logical 1, if two or three inputs are 0 (no electron tunneling takes place).

We tested the gate operation by computer simulation. Fig. 4(b) shows the result for a sample set of parameters, $CL = 2$ aF, $Cj = 20$ aF, $C = 2$ aF, and zero temperature. (We used a modified Monte Carlo simulation method. Kuwamura *et al.* [8] have given details of this method. Also see [7, Appendix].) We represented a logical 1 by a voltage of 4 mV and a logical 0 by -4 mV. The figure shows the voltage at node 1 as a function of Vd with a set of three inputs as a parameter set (the output terminal is grounded). In the figure, for example, "inputs (1, 1, 0)" means that two inputs are set to 4 mV (logical 1) and one input is set to -4 mV (logical 0). With increasing Vd, the node potential increases to a maximum, then drops to a negative because of electron tunneling. The threshold value of Vd, at which the electron tunneling takes place, depends on the sum of the inputs; in this example, the threshold is 56 mV for inputs (1, 1, 0) and 64 mV for inputs (1, 0, 0). To operate the device as a majority gate, we increased Vd to an excitation value of 60 mV (indicated by Vex in the figure). The logic output, or the voltage at node 1, was retrieved through the output terminal. To do this retrieving, we decreased bias Vd to a holding value of 40 mV (indicated by Vss), grounded the

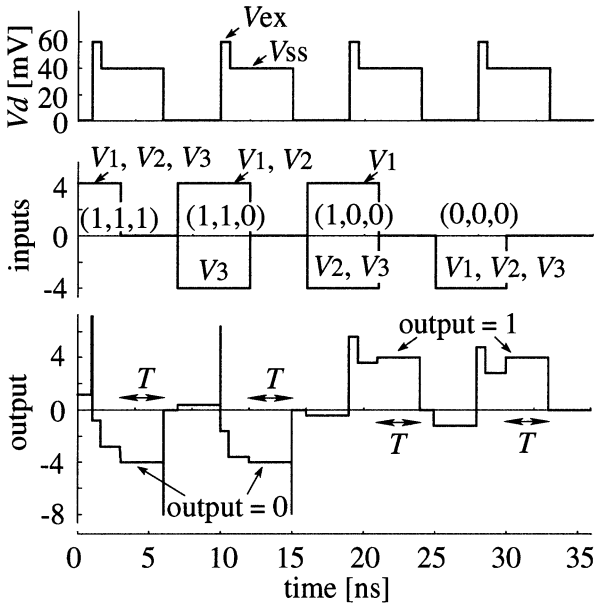


Fig. 5. Simulated majority-logic operation of the gate device.

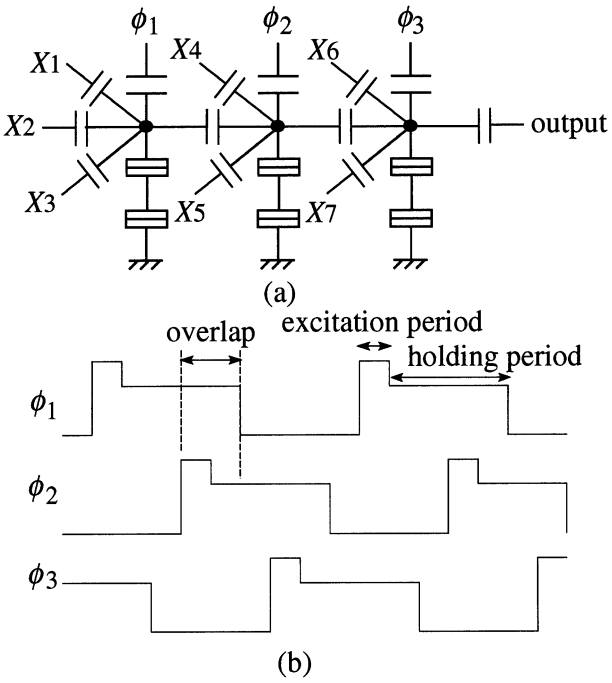


Fig. 6. Gating with a three-phase clock. (a) Configuration of interstage coupling ($X1$ to $X7$ denote inputs from other gates). (b) The three-phase two-step clock pulses used to excite gates.

three input terminals, and checked the voltage of node 1. The node voltage was 4 mV (quiescent point A on the dashed line) when the output was 1 and -4 mV (quiescent point B) when the output was 0.

We simulated the majority logic operation for all input combinations. Fig. 5 shows the results for $CL = 2$ aF, $Cj = 20$ aF, $C = 2$ aF, tunneling junction conductance $= 5$ μS, and zero temperature. The bias voltage Vd is the two-step clock pulse shown in the upper plot in the figure; first, Vd is set to an excitation voltage Vex of 60 mV and then it is set to a holding voltage Vss of 40 mV. Three inputs ($V1$, $V2$, $V3$) are applied synchronously with the bias clock. They are the rectangular pulses (4 mV for logical 1 and of -4 mV for logical 0) in the middle plot in Fig. 5. In the figure, the four sets of inputs (1, 1, 1), (1, 1, 0), (1, 0, 0), and (0, 0, 0) were applied in sequence. Depending on the majority of the inputs, the voltage at node 1 changes from 0 to positive (1-valued) or negative (0-valued) (bottom plot in Fig. 5). With the output is 0, the output voltage initially goes high for an instant with the rise in Vd and then turns negative as electron tunneling takes place. The output established in each clock cycle is maintained after the input pulses are turned off, until Vd returns to zero (duration T in the bottom plot).

IV. Using Majority Gate to Design Subsystems

A. Interstage Coupling

Any logic function can be implemented by combining identical gates into a cascade configuration, with the output capacitor of one gate acting as the input capacitor of the following gate. An example is illustrated in Fig. 6(a). The majority gate proposed here is bilateral, so we control the signal-flow direction by gating with a three-phase clock (which is analogous to an Esaki-diode pair circuit and a quantum-flux-parametron circuit). We divide the gate circuits into three groups, and excite each group in turn by one phase of the three clock signals, $\phi 1$ to $\phi 3$, as shown in Fig. 6(b). For instance, in Fig. 6(a), the leftmost gate (and every fourth gate thereafter) belongs to the first group and is excited by the $\phi 1$-phase clock; the middle gate (and every fourth gate thereafter) belongs to the second group and is exited by the $\phi 2$-phase clock; the rightmost gate (and every fourth gate thereafter) belongs to the third group and is excited by the $\phi 3$-phase clock. The phases of the three clock signals overlap so that the output of a stage will be established while the preceding stage is maintaining its output during its holding period; signals are thus transmitted from one gate to the next. For successful interstage coupling, the duration of the overlap has to be longer than the excitation period, as shown in Fig. 6(b). The signal-flow direction is determined by the relative timing of the three phases; in Fig. 6(a), it is rightward.

B. Shift Register

A shift register can be constructed by connecting a number of gates to form a chain, with two inputs of each gate grounded. A sample configuration with six gates (1 through 6) is shown in Fig. 7(a). The code ($\phi 1$ through $\phi 3$) above each gate indicates the clock phase with which the gate is driven [the clocks have the timings shown in Fig. 7(b)]. Each gate acts as a simple inverter because two of its input terminals are grounded and, therefore, its output is determined by the polarity of the third input. Signals travel through the shift register from the input terminal to the output terminal, repeating 1–0 logical inversion.

A simulated result for signal transmission along the shift register is illustrated in Fig. 7(b); the device parameters are as given in Section III-B. The input applied to gate 1 was the sequence "100 100 100…" with clock $\phi 3$. After a delay of two clock periods, the sequence "100 100 100…" appeared at the output of gate 6. Five cycles of this sequence of operations are shown in the figure.

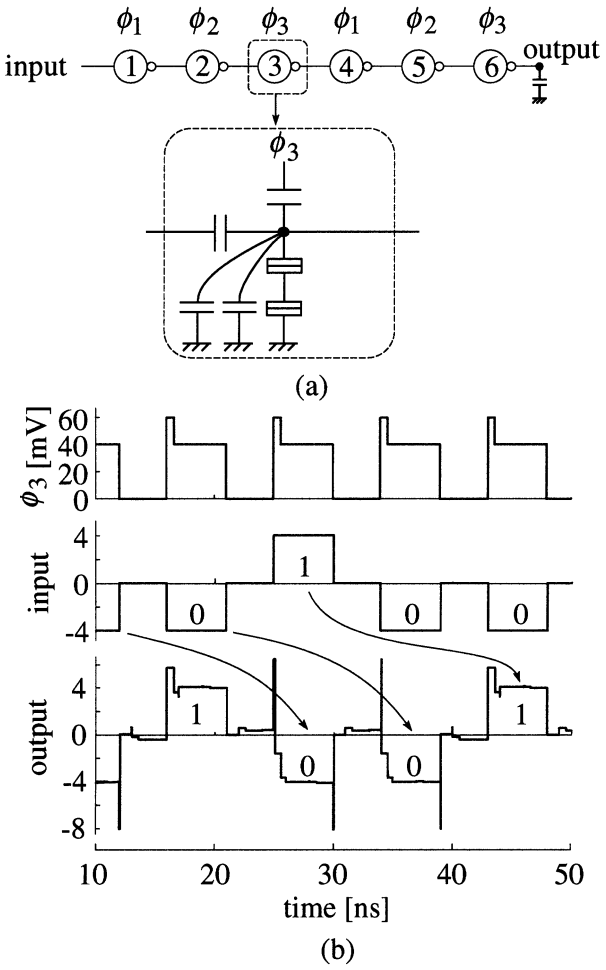


Fig. 7. Shift register. (a) Circuit configuration. (b) Simulated output waveform. Waveforms of $\phi 3$-clock signal and the input are also shown. Clocks $\phi 1$ and $\phi 2$ are not shown.

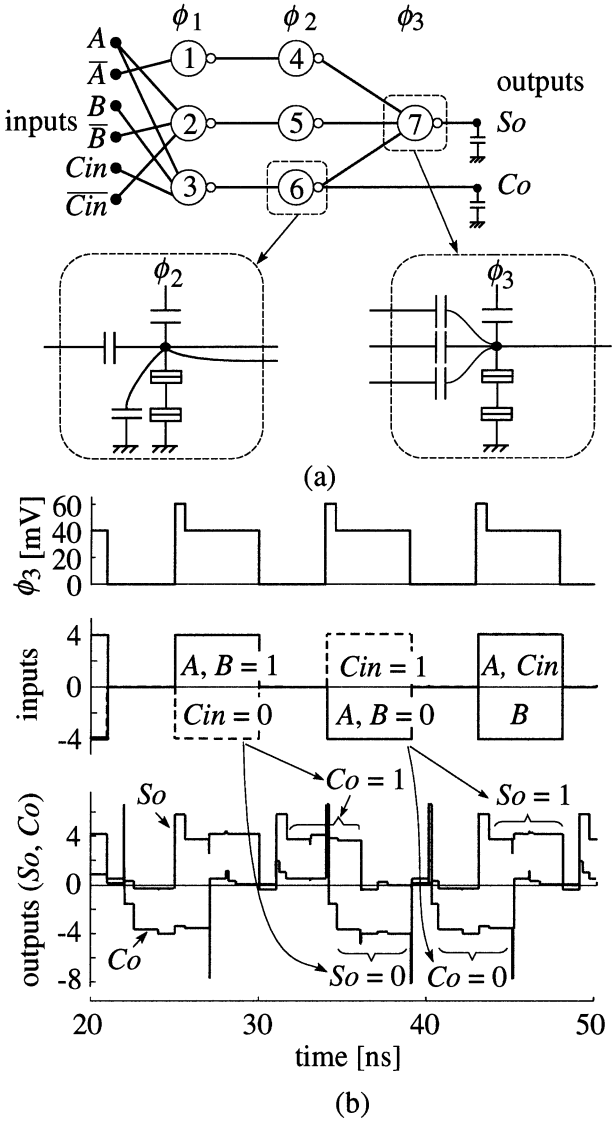


Fig. 8. Full adder. (a) Circuit configuration. (b) Simulated output waveforms of carry Co and sum So, waveforms of $\phi 3$-clock and the inputs. Clocks $\phi 1$ and $\phi 2$ are not shown.

C. Full Adder

Fig. 8(a) illustrates an implementation of the full adder shown in Fig. 2. The adder accepts three inputs, augend A, addend B, and carry input Cin (and their complements $\bar{A}$, $\bar{B}$, and $\bar{Cin}$); it then produces the corresponding carry output Co and sum output So. The core of the adder consists of majority gates 2, 3, and 7. The other gates (1, 4, and 5) acts as a delay buffer; they have the same configuration as in Fig. 7(a) and transfer the signal from the preceding stage to the following stage with the correct clock timing. Gate 6 is a fan-out buffer that transmits signals from the following stage to the succeeding two stages. The inputs are taken in while clock $\phi 3$ is in the excitation period. Carry output Co is produced when $\phi 2$ goes high and is retrieved by gate 7, while $\phi 2$ is in the holding period. Sum output So is produced when $\phi 3$ goes high again. The delays between the inputs and the carry output is two-thirds of a clock period and that between the inputs and the sum output is one clock period.

We simulated the add operation and confirmed correct operation for all input combinations. Three clock cycles of the simulated output waveforms of carry Co and sum So are shown in Fig. 8(b); the device parameters are as given in Section III-B. Two sets of inputs $(A, B, Cin) = (1, 1, 0)$ and (0, 0, 1) were sequentially entered, and the correct outputs $(Co, So) = (1, 0)$ and (0, 1) were produced in response. Multibit adders can be constructed by combining the full adders into a cascade configuration.

V. Error Factors in Gate Operation

In a majority gate circuit, one logic operation will succeed if the gate determines its 1–0 output correctly during the excitation period and maintains the output during the holding period. There are several factors, however, that will produce operation errors: signal noise, waiting time for electron tunneling, thermally induced tunneling, and cotunneling. The effects of these undesirable factors on gate operation are estimated in the following sections.

A. Noise Margin

The majority gate produces its output according to the polarity of the sum of three input voltages. Each input is the output of a preceding gate and its voltage without noise is given by

$e/(2CL+8C+Cj)$ for a logical 1 and $-e/(2CL+8C+Cj)$ for a logical 0, as described in Section III-B. The gate output will therefore be affected if the magnitude of the total noise on the three inputs exceeds $e/(2CL+8C+Cj)$. Noise margin, or the magnitude of the allowable noise voltage on each input, is therefore given by $(e/3)/(2CL+8C+Cj)$. The set of parameters used in Section III, for example, gives a noise margin of 1.3 mV.

B. Operation Delay Due to the Waiting Time for Tunneling

The gate determines its output state in the excitation period according to given inputs, using its hysteretic function shown in Fig. 4(b). This process has a delay due to the waiting time for electron tunneling. The delay occurs when the gate produces a logical-0 output in response to the excitation pulse (Vex in Fig. 5) under a set of inputs, (1, 1, 0) or (1, 1, 1). When the excitation pulse is applied, an electron tunnels after a waiting time from the ground to node 1 through the junctions [see Fig. 4(a)] to make the gate output logical-0. Because the waiting time for the tunneling shows a probabilistic fluctuation, the tunneling might occur after a very short wait or it might not occur for a long time. To operate the gate without errors, the excitation period has to be set long enough to make certain that the tunneling occurs within the excitation period. This requirement limits the maximum clock frequency of the gate operation.

The probability $\varepsilon 1$ of "stochastic" errors, or the probability that the tunneling does *not* occur during the excitation period, is given by

$$\varepsilon 1 = \exp(-t1/\tau 1)$$

where $t1$ is the duration of the excitation period, and $\tau 1$ is the mean waiting time given by $\tau 1 = 1/\Gamma 1$ ($\Gamma 1$ is the tunneling rate). A small error probability of 10^{-10}, for example, requires an excitation period of $23t1$ duration.

The tunneling from the ground to node 1 through the junctions consists of two sequential step: a tunneling from the ground to intermediate node 2, and a tunneling from node 2 to node 1 [see Fig. 4(a)]. The first step has a smaller tunneling rate and therefore a longer waiting time, so it limits the minimum length of the excitation period required. Its tunneling rate can be calculated from the change of energy in the tunneling event and is given by

$$\Gamma 1 = CG/(2CL+8C+Cj)^2$$

where G is tunneling junction conductance, and input set (1, 1, 0) and zero temperature are assumed [input set (1, 1, 1) gives a larger tunneling rate and is not a limiting process]. The set of circuit parameters in Section III, for example, gives a tunneling rate of 6.3×10^9 s^{-1} and, therefore, a mean waiting time of 160 ps. This result shows that an excitation period of 3.7 ns is required for a 10^{-10} error probability. The duration of one logic cycle is several times longer than this excitation period, so it cannot be reduced to less than 15–20 ns.

Scaling down the circuit capacitances and increasing the tunnel conductance make higher speed operation possible, but it will be difficult to attain a higher speed than that of CMOS devices. On the other hand, our gate devices will provide the possibility of producing LSIs with a huge integration scale of 10^{9-10} gates/cm^2; this will enable fabrication of novel LSIs with far more advanced functions than those of CMOS integrated circuits.

C. Operation Error Caused by Thermally Induced Tunneling

After determining its output state in the excitation period, the gate has to maintain the state without fail during the holding period. The output state may be inverted unexpectedly, however, because of thermally activated tunneling events through the junctions; therefore, a thermally induced error may occur in the holding period.

This situation is similar to that of the single-electron-box memory described by Averin and Likharev [9], so we estimated the gate error by using their results on a memory device. (The tunneling-rate equations in the following are also from Averin and Likharev.) The rate of the thermal inversion events is

$$\Gamma 2 = (1/2)(G/CL)\exp\left(-e^2/(6CLkBT)\right)$$

where kB is Boltzmann constant and T is temperature. Probability $\varepsilon 2$ of thermal error during holding period $t2$ is given by $\varepsilon 2 = \Gamma 2 t2$. The circuit parameters used in Section III and a 1-ns holding duration give a small probability of thermal errors less than 10^{-10} if the gate is operated below 5.1 K. The gate can operate without errors at higher temperatures if the capacitances in the gate are decreased.

D. Operation Error Caused by Cotunneling

The second source of errors in the holding period is the cotunneling phenomenon, i.e., an undesirable coherent tunneling of electrons through the two junctions in the gate. This is again similar to that of a memory device. Averin and Likharev has given the characteristic value of the cotunneling rate

$$\Gamma 3 = (1/6)(G/Cj)\left(hG/\left(4e^2\pi^2\right)\right)$$

where h is Planck constant. Probability $\varepsilon 3$ of the cotunneling error during holding period $t2$ is given by $\varepsilon 3 = \Gamma 3 t2$. The circuit parameters used above gives an error probability of 1.4×10^{-1}.

This error probability is somewhat large and, therefore, undesirable for most applications. A way of reducing the cotunneling error is to make the gate device with many tunneling junctions connected in series instead of with two junctions. The same gate operations as shown in Fig. 4(b) can be obtained if N junctions are obtained and the capacitance parameters is set to $Cj = CL(N-1)$. Under these conditions, the characteristic value of the cotunneling rate is given by

$$\Gamma 4 = (1/2)(G/Cj)(hG/(4e^2\pi^2))^{N-1}(N/2)^{2N} \cdot((2N-1)!)^{-1}((N-1)!)^{-2}$$

instead of by $\Gamma 3$. Using $N = 5$ gives a sufficiently small error probability of 10^{-13}.

VI. Toward Actual Gate Devices

The unit element of our majority device is a double, or, for reducing cotunneling errors, a multijunction single-electron

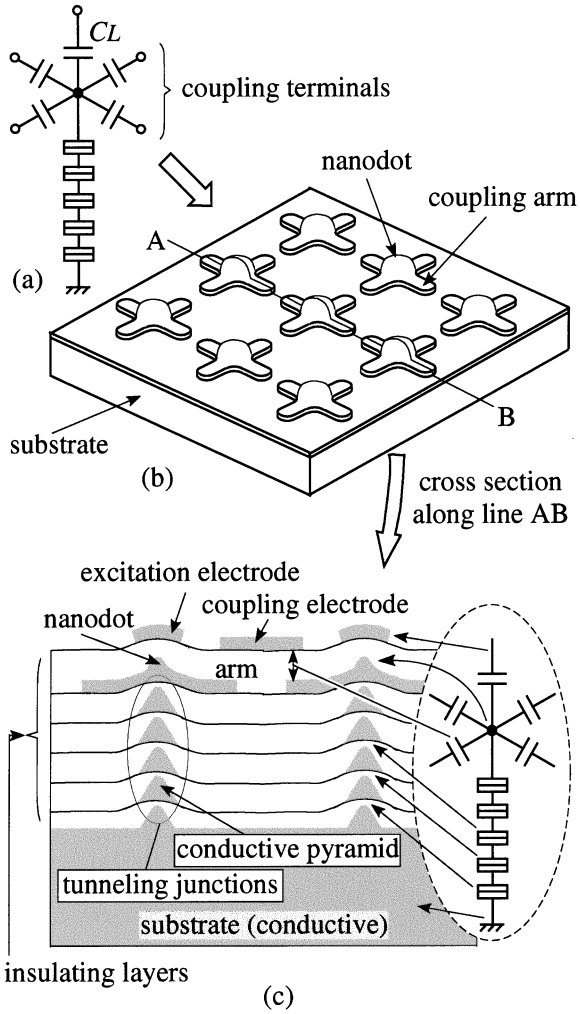


Fig. 9. Schematic of an actual gate device. (a) Unit element of the gate—an irreversible single-electron box with four coupling terminals. (b) Arrayed nanodots with their coupling arms. (c) Cross section of nanodots with their arms and five tunneling junctions.

box with four terminals for capacitive coupling: Fig. 9(a) shows an element consisting of a five-junction trap. Joining several of such elements produces majority-logic integrated circuits, so our next task is to fabricate many identical elements on a substrate. Fig. 9(b) and (c) shows the three-dimensional and cross-sectional schematics of the device structure. Each element consists of a conductive nanodot with four coupling arms [Fig. 9(b)]; series-connected five junctions run between the nanodot and a conductive substrate beneath the nanodot [Fig. 9(c)]; all of the nanodots are covered with an insulating layer [Fig. 9(c)]. The bias capacitor, through which the gates are excited, can be made by forming an excitation electrode over each nanodot. Capacitive coupling between two elements can be achieved by forming a coupling electrode over the arms of the two elements. We can thus fabricate various majority circuits simply by designing appropriate patterns of electrodes.

The key point in this majority-circuit construction is to form the arrangement of nanodots with their coupling arms and tunneling junctions. We previously proposed and demonstrated a process technology that can be used to fabricate the structure for the circuit [7]. This technology uses self-organized crystal growth by selective-area metalorganic vapor-phase epitaxy (SA-MOVPE) and it can be used to fabricate GaAs nanodots with arms and tunneling junctions on a GaAs substrate by making use of the dependence of the crystal growth rate in SA-MOVPE on crystal orientation (for detailed explanations, see [7] and [10]). This technology can automatically make the multijunction structure simply by repeating the growth of a n-type GaAs layer and an insulating AlGaAs layer; the nanodot with four arms can be formed also automatically in a self-organizing manner. Using such a process, we have succeeded in forming GaAs nanodots with the arms in a form of a two-dimensional arrangement (with a pitch of 400 nm, corresponding to 8×10^8 gates/cm^2) on a substrate, though our technology is as yet imperfect and we have yet to fabricate a complete device. We are now developing an improved process technology to form GaAs nanodots with arms and multilayered junctions arranged regularly with a pitch of 100 nm or less (corresponding to 10^{10} gates/cm^2). With the improved process technology, we will be able to implement the majority-gate device described here and proceed to develop majority-logic LSIs.

REFERENCES

[1] H. Gravert and M. H. Devoret, *Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures*. New York: Plenum, 1992.
[2] S. Amarel, G. Cooke, and R. O. Winder, "Majority gate network," *IEEE Trans. Electron. Comput.*, vol. EC-13, pp. 4–13, 1964.
[3] A. R. Meo, "Majority gate networks," *IEEE Trans. Electron. Comput.*, vol. EC-15, pp. 606–618, 1966.
[4] K. F. Loe and E. Goto, "Analysis of flux input and output Josephson pair device," *IEEE Trans. Magn.*, vol. MAG-21, pp. 884–887, 1985.
[5] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum cellular automata," *Nanotechnol.*, vol. 4, pp. 49–57, 1993.
[6] H. Iwamura, M. Akazawa, and Y. Amemiya, "Single-electron majority logic circuits," *IEICE Trans. Electron.*, vol. E81-C, pp. 42–48, 1998.
[7] T. Oya, T. Asai, T. Fukui, and Y. Amemiya, "A majority-logic nanodevice using a balanced pair of single-electron boxes," *J. Nanosci. Nanotechnol.*, vol. 2, no. 3/4, pp. 333–342, 2002.
[8] N. Kuwamura, K. Taniguchi, and C. Hamakawa, "Simulation of single-electron logic circuits," *IEICE Trans. Electron.*, vol. J77-C-II, pp. 221–228, 1994.
[9] D. V. Averin and K. K. Likharev, "Possible applications of the single charge tunneling," in *Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures*. New York: Plenum, 1992, ch. 9.
[10] K. Kumakura, J. Motohisa, and T. Fukui, "Formation and characterization of coupled quantum dots (CQD's) by selective area metalorganic vapor phase epitaxy," *J. Cryst. Growth*, vol. 170, pp. 700–704, 1997.

Takahide Oya received the B.E. degree in electrical engineering from Hokkaido University, Sapporo, Japan, in 2002.

He is currently working toward the M.E. and Dr. Eng. degrees in the Department of Electrical Engineering, Hokkaido University. His current research interests are intelligent devices using single-electron circuits.

Tetsuya Asai received the B.E. and M.E. degrees in electrical engineering from Tokai University, Kanagawa, Japan, in 1993 and 1996, respectively, and the Dr. Eng. degree in electrical and electronic engineering from Toyohashi University of Technology, Aichi, Japan, in 1999.

He is now an Associate Professor with the Department of Electrical Engineering, Hokkaido University, Sapporo, Japan. His current research interests include sensory information processing in neural networks as well as design and applications of neuromorphic VLSIs and the reaction-diffusion chip.

Takashi Fukui received the B.S. and M.S. degrees in applied physics and the Dr. Eng. degree in electronic engineering from Hokkaido University, Sapporo, Japan, in 1973, 1975, and 1983, respectively.

From 1975 to 1991, he was with NTT Basic Research Laboratory, Musashino, Tokyo. In 1991, he joined, as a Professor, the Research Center for Integrated Quantum Electronics, Hokkaido University. His research interest includes the crystal growth of III–V compound semiconductor materials for quantum nanostructures such as quantum dots, quantum-wires, and superlattices, and the development of functional devices using such nanostructures.

Yoshihito Amemiya received the B.E., M.E., and Dr. Eng. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1970, 1972, and 1975, respectively.

From 1975 to 1993, he was with NTT LSI Laboratory, Atsugi, Japan. Since 1993, he has been a Professor with the Department of Electrical Engineering, Hokkaido University, Sapporo, Japan. His research interests are in the field of electronic circuits, LSI circuits, functional devices based on nonlinear analog computation, logic systems using single-electron circuits, and information-processing devices using quantum-effect nanostructures.